Derivation and Comparative Analysis of Multi-Cell Isolated Front End and Isolated Back End SSTs

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Agenda

Introduction

S³T (IFE) Derivation and Operating Principle

IFE vs. IBE Conclusions

Appendix: Other S³T Configurations

References
Introduction
Motivation: SSTs as MV AC to LV DC Power Interfaces

- Emerging Low-Voltage DC Applications Could Benefit From Direct Connection to Medium-Voltage
  - Datacenters with Internal 400V DC Distribution
  - Larger PV Plants
  - Fuel Cell or Battery Storage
  - UPS
  - ...

MVAC ↔ LVDC Solid-State Transformers

Key Requirements:
- Galvanic Isolation and Voltage Scaling
- Unity Power Factor
- High Efficiency
- Low Complexity

Isolated PFC Functionality
Partitioning of Isolated AC//DC PFC Functionality

- **Required Functionality**
  - **F**: Folding of the AC Voltage Into a |AC| Voltage
  - **CS**: Input Current Shaping
  - **I**: Galvanic Isolation & Voltage Scaling
  - **VR**: Output Voltage Regulation

- **Isolated PFC Functionality Partitioning Variants:**
  - **Isolated Back End (IBE)** → Broadly Analyzed and Employed in SSTs
  - **Isolated Front End (IFE)** → Less Common, Interesting Alternative
  - **Fully Integrated**
IBE and IFE Origins

Isolated Back End

- Steiner, 1996 → Traction Applications
- Primary Side Active Rectification
- ISOP System Structure

- Soft-Switched Isolation Stage (HC-DCM Series Resonant Conv.)

Isolated Front End

- Weiss, 1985 (!) → Traction Applications
- Hard-Switched Isolation Stage

- Han et al., 2014 → Ext. to Resonant & Modular Concept

[Steiner1998], [Steiner2000] [Weiss1985], [Han2014]
IBE and IFE Status

Isolated Back End

- **Fully Functional Traction SST** by ABB (Dujic, Zhao, et al.), ca. 2011-2014
- **Soft-Switched Isolation Stage** (HC-DCM Series Resonant Conv.)

Isolated Front End

- ETH, 2015, in the Scope of
- All-SiC, Full ZVS Realization
- Simplified Input Stage
- Further Configurations: 3-Ph., AC/AC, etc. → Cf. Later!
- **Soft-Switched Isolation Stage** (HC-DCM Series Resonant Conv.)

ETH / [Kolar2016]
**Autonomous Isolation Stage: HC-DCM-SRC Review**

- **Isolation Stage: No Control Required!**
  - → Minimize Complexity
  - → Autonomous Isolation Stage

- **Enter HC-DCM SRC:**
  (Half-Cycle Discontinuous-Conduction-Mode Series-Resonant Converter)

  - Source Side Actively Switched
  - Each Switching Action Excites Resonant Tank → **Current Amplitude Depends on Ex. Volt. Step**

- **Automatically Tight Coupling of DC (or LF) Voltages!**
  \[ V_{out} \approx V_{in} \quad (\text{Small Deviation Due to Losses}) \]

- **Isolation Stages**

- **Control Stages**

**Further Reading:** [McMurray1971], [Huber2015] (!)
IBE Example System

MV Side Control Stage
- (Cascaded) AC/DC Boost (ARU)
  - Approx. Const. MV DC Volt.
  - Total Blocking Volt. Ca. 1.2 x \( v_{g,Pk} \)
  - Complexity (MV Side Meas. & Contr.)
  - Hard Switching

Transform Cur. Envelope \( \propto \sin^2(t) \)
- DC Buffer Caps.
IFE Example System: The Swiss SST ($S^3T$)

LV Side Control Stage
- (Interleaved) |AC|-DC Boost Conv.

$S^3T$ Specifications
- 25kW
- 6.6kV AC (line-line)
- 5 Cascaded Cells
- 400V DC
- All-SiC
S$^3$T Derivation and Operating Principle
**Topology Derivation (1): aIFE Insertion**

Non-Isolated, Unidirectional Boost PFC

Extension by an Autonomous Isolation Front End (aIFE)

- **Note:** $C_1$ and $C_2$ are NOT DC Buffer Capacitors!
  - → Commutation/Resonant Capacitors
Topology Derivation (2): Direct AC Input

- Bidirectional Switches on Primary Side
  → SRC Switching And Folding of the Grid Voltage

- Note: $C_{r1}$, $C_{r2}$, and $C_{r3}$ are Resonant/Commutation Cap.
Operating Principle of the Swiss SST (1)

Note: 
\[ L_F = 0 \]
\[ R_F = 0 \]

- HC-DCM SRC αIFE Acts as AC-|AC| Converter

\[ V_{T,mv} \]
Operating Principle of the Swiss SST (2)

Note:
\[ L_F = 0 \]
\[ R_F = 0 \]

No Energy Storage in \( a\)IFE

→ Boost Stage Input Characteristics Are Translated to the Grid

\[ \bar{p}_{\text{Boost}}(t) \text{ Defined by Boost Control} \]
Dynamic Behavior and Modeling

- aIFE Terminal Behavior Can Be Modeled By Passive Equivalent Circuit

  ![Equivalent Circuit Diagram]

- Transfer Function From Boost Current to Grid Current, $G_i$
  - aIFE Translates Boost Stage Current to the Grid w/o Distortion or Delays
  - Resonance Between Grid/Filter Impedance and Input Capacitance Requires Damping

  ![Transfer Function Graph]

Unity Gain For Low Frequencies!

1 Background Reading: [Huber2015]
Input-Series Output-Parallel (ISOP) Configuration

- Cascaded aIFEs, Single (Interleaved) Boost Stage
- No MV Control or Meas. Required!

Interleaving of aIFE Switching

See Appendix For Other Configurations!
**ISOP: Balancing & Load Sharing**

- **aIFE Tightly Couples Its Terminal Voltages**
  - All Cells Share Common LV Bus Voltage

→ **MV Side Voltage Sharing is Ensured!**

**Example:**
- Add. Load (10% nominal) On MV Side of One Cell

→ **Redistribution of Power Transfer**

→ **Voltage Sharing Ensured**

- **Also Simulated w/o Problems for Primary Resonant Capacitance Tolerances (20%)**
**aIFE ZVS Considerations (1)**

- Magnetizing Current is Used for Load-Independent ZVS (LLC Operation)
  - Transf. Volt. Envelope $\propto \sin(t)$
  - Magn. Current Amplitude $\propto \sin(t)$
  - Nonlinear Parasitic FET $C_{oss}$

$\rightarrow$ ZVS Not Ensured Over Entire Grid Period!
**aIFE ZVS Considerations (2)**

- **Optimize Magn. Ind. Value and Interlock Time for Min. Losses**
  - Partial ZVS Losses Are Very Small (Calc. for 1700V SiC FET)
  - ZVS Not Ensured Over Entire Grid Period!

- **Full-ZVS Still Desirable for EMI Noise Limitation**
  - Higher Losses With Adapted Magn. Ind. & Const. Dead Time
  - Variable Interlock Time
  
  \[
  t_d^* = \frac{1}{\omega_0} \left[ \pi - \arctan \left( \frac{Z_0 i_M}{V_{Cr1}} \right) - \arccos \left( \frac{V_{Cr2} + q \overline{v}_{g,c}}{\sqrt{i_M^2 Z_0^2 + V_{Cr1}^2}} \right) \right]
  \]

  - Potentially Compromises Interleaving – Analyses Ongoing!

**Control Stage ZVS**

- **Known Concepts from Literature (TCM, Clamp Switch, etc.)**
Control & Modulation With LV Meas. Only

- Sinusoidal Grid Current
- Unity Power Factor (0.99+)
- Output Voltage Regulation
- Grid. Volt. Polarity Est. for MV Side
- ZVS Modulation
IBE and IFE
Comparison & Conclusion
**IFE Example System: The Swiss SST (S³T)**

Back Side
- (Interleaved) |AC|-DC Boost

- MV “DC” Volt. $\propto \sin(t)$
- Lower Total MV Block. Volt.
- Low MV Side Complexity and Smaller Floating Assembly
- Full ZVS Possible

- Transf. Cur. Envelope $\propto \sin(t)$
  - Larger SiC Area, More Copper
  - Less Core Mat.
Comparative Evaluation of IBE and IFE Concept

Key Differences

- **Control Stage (Boost) Location**
  - IBE: MV Side
  - IFE: LV Side

- **Transf. Volt. Envelope**
  - IBE: $\propto \sin(t)$
  - IFE: $1.44 \cdot \bar{I}_T$

IFE ($S^3T$) Features...

- Low MV Side Complexity
  - (No Contr., Meas., Smaller Mech. Assem., etc.)
- Lower Total MV Blocking Voltage
  - (5 Instead of 6 Casc. Cells for 6.6kV)
- No DC Buffering Per Cell (3-ph)
- Possibly Full ZVS of Contr. Stage
- Limitation To $\cos \varphi \approx 1$ (Bidirectional)
- Higher SRC LV Side Cur. (Lower Volt.)

- Higher Copper Usage
- Higher SiC Area Usage
- Lower Transf. Core Mat. Usage

Ca. 2...3x (!)
(Preliminary) Conclusions

- **Isolated Back End Main Advantage:**
  Lower RMS Currents → Lower Semic. Area

- **Isolated Front End Main Advantage:**
  Lower MV Side Complexity

- **IFE Concept ($S^3T$) Has Potential for SST Appl. with Lower Power Ratings**
  → Higher Contrib. of Meas. And Control Electronics To Costs

- **Comparative Evaluation is Work in Progress:**
  - Grid Filter Requirements
  - Control Stage Sw. Losses
  - Full Multi-Objective Optimization
  - ...

**S^3T Research Status**

- Analyzed
- To Be Analyzed (!)
Thank You!

Further Reading: [Kolar2016]; Upcoming: [Huber2016a], [Huber2016b]
Appendix:
Other $S^3T$ Configurations
Other Input-Series Output-Parallel Configurations

- Cascaded αIFEs, Single (Interleaved) Boost Stage:

- One Boost Stage Per Converter Cell
  - Control for Equal Input Impedance
  - Ensures MV Side Voltage Balancing

- Common Folding Stage
  - Passive or Active Grid Freq.
  - Rectifier
Three-Phase System Configuration

- **Combination of Three Phase Stacks**
  (Example Realized With One Boost Stage Per Cell)

- **Benefit: In Theory No Need for Intermediate Energy Buffers in the Cells**
Scott-Transformer Configuration

- **Magnetic Scott Transformer**
  - Three-Phase AC Input
  - Two 90° Phase-Shifted AC Outputs
  - Symmetric Grid Currents If Outputs Equally Loaded

- **S³T Scott Transformer**
  - Three-Phase AC Input
  - Two Isolated DC Outputs
    → Series Connection for ±190V DC Distr.
  - Symmetric Grid Currents If Outputs Equally Loaded (!)
**Direct AC/AC Operation**

Symmetric AC-AC aIFEs in ISOP Conf.

- Optional Voltage Control with LV AC Chopper

**Note: Back To The Roots!**

- Simulation with RL-Load

**WILLIAM McMURRAY 1971 (!)**  
[McMurray1971]
References
References: A-Z


