Impact of Magnetics on Power Electronics Converter Performance

State-of-the-Art and Future Prospects

J. W. Kolar et al.

Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
www.pes.ee.ethz.ch
Impact of Magnetics on Power Electronics Converter Performance

State-of-the-Art and Future Prospects


Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
www.pes.ee.ethz.ch
Outline

► Performance Trends
► Design Space / Performance Space
► Performance Characteristics of Key Components
► Feasible Performance Space / Pareto Front
► Losses Due to Local Stresses in Ferrite Surfaces
► The Ideal Switch is NOT Enough!
► Challenges in MV/MF Power Conversion
► Future Prospects
Introduction

Converter Performance Indicators
Design Space / Performance Space
Power Electronics Converter Performance Indicators

- Power Density \([\text{kW/dm}^3]\)
- Power per Unit Weight \([\text{kW/kg}]\)
- Relative Costs \([\text{kW/\$}]\)
- Relative Losses \([\text{\%}]\)
- Failure Rate \([\text{h}^{-1}]\)

Environmental Impact...
\([\frac{\text{kg}_{\text{Fe}}}{\text{kW}}]\)
\([\frac{\text{kg}_{\text{Cu}}}{\text{kW}}]\)
\([\frac{\text{kg}_{\text{Al}}}{\text{kW}}]\)
\([\frac{\text{cm}^2}{\text{Si/kW}}}]\)

State-of-the-Art

Future

Costs

Time-to-Market
Performance Limits (1)

- Example of Highly-Compact 1-Φ PFC Rectifier
- Two Interleaved 1.6kW Systems

\[ P_o = 3.2kW \]
\[ U_N = 230V \pm 10\% \]
\[ U_0 = 400V \]

\[ f_p = 450kHz \pm 50kHz \]

\[ \eta = 95.8\% @ \rho = 5.5 \text{ kW/dm}^3 \]

- High Power Density @ Low Efficiency
- Trade-Off Between Power Density and Efficiency
Performance Limits (2)

- Example of Highly-Efficient 1-Φ PFC Rectifier
- Two Interleaved 1.6kW Systems

\[
\begin{align*}
P_\varnothing &= 3.2kW  \\
U_N &= 230V\pm10\%  \\
U_0 &= 365V  \\
\eta &= 99.2\% \quad @ \quad \rho = 1.1 \text{ kW/dm}^3
\end{align*}
\]

\[f_p = 33kHz \pm 3kHz\]

\[\Rightarrow \text{High Efficiency \, @ \, Low Power Density}\]

\[\Rightarrow \text{Trade-Off Between Power Density and Efficiency}\]
Abstraction of Power Converter Design

Performance Space
- Efficiency
- Power Density
- Costs
- Reliability
- etc.

Design Space
- System
  - Phase-Shift DC/DC Conv.
  - Resonant DC/DC Conv.
  - DC Link AC/AC Conv.
  - Matrix AC/AC Conv.
  - etc.

- Components
  - Power Semiconductor
  - Interconnections
  - Inductors, Transf.
  - Capacitors
  - Control Circuit
  - etc.

- Materials
  - Semiconductor Mat.
  - Conductor Mat.
  - Magnetic Mat.
  - Dielectric Mat.
  - etc.

Mapping of “Design Space” into “Performance Space”
Derivation of $\eta-\rho$-Performance Limit of Converter Systems

Component $\eta-\rho$-Characteristics
Converter $\eta-\rho$-Pareto Front
Derivation of the $\eta$-$\rho$-Performance Limit

- Example of DC/AC Converter System

- Key Components
  - Storage Capacitor
  - Semiconductors & Heatsink
  - Output Inductor
  - Auxiliary Supply

$\Rightarrow$ Construct $\eta$-$\rho$-Characteristics of Key Components
$\Rightarrow$ Determine Feasible System Performance Space
**η-ρ-Characteristic of Energy Storage**

- **Electrolytic Capacitors**
- **Losses (ESR) Neglected**

\[ \gamma_C = \frac{1}{2} \frac{C U_{DC}^2}{V_C} \]

\[ \alpha_{\Delta u_C} = \frac{\hat{u}_C}{U_{DC}} = \frac{i_c}{U_{DC}} \frac{x_C}{P_o} = \frac{P_o}{1} \frac{1}{2 \omega_N C} \]

\[ \rho_C = \frac{P_o}{V_C} = \frac{4 \omega_N \alpha_{\Delta u_C} \gamma_C}{\beta_C} = \frac{\beta_C \gamma_C}{\rho_C} = \text{const.} \]

\[ \rightarrow \text{Energy Storage Defines a Converter Limit } \rho_{max} \leq \rho_C \]
**Remark - Active Power Pulsation Buffer**

- Large Voltage Fluctuation *Foil or Ceramic Capacitor*
- Buck-Type (Lower Voltage Levels) or Boost-Type DC/DC Interface Converter

→ **Significantly Lower Overall Volume Compared to Electrolytic Capacitor** BUT **Lower Efficiency**
\[ P_H = (1 - \eta_H) P_I = (1 - \eta_H) \frac{P_O}{\eta_H} \]

\[ P_H = \frac{\Delta T_{s-a}}{R_{th}} = \Delta T_{s-a} G_{th} = \Delta T_{s-a} \frac{CSPI \cdot V_H}{g_{th}} \]

\[ \frac{(1 - \eta_H)}{\eta_H} P_O = \frac{\alpha_H}{\Delta T_{s-a}} CSPI \cdot V_H \]

\[ \eta_H = \frac{P_O}{V_H} = \frac{\eta_H}{(1 - \eta_H)} \]

- Heatsink Defines a Converter Limit \( \rho \leq \rho_H \)

\[ CSPI = \frac{G_{th}}{V_H} \left[ \frac{W}{dm^3K} \right] \]
**Remark - Selection of Semiconductor Chip Area**

- Optimize Chip for Minimum Sw. and Conduction Losses
- Loss Minimum Dependent on Sw. Frequency
- Influence of Power Semiconductor FOM

\[
P_H = I_{H,rms}^2 R_{DS(on)} + \frac{1}{2} C_{eq} U_{DC}^2 f_P = I_{H,rms}^2 \frac{R_{DS(on)}^*}{A_{Si}} + \frac{1}{2} C_{eq}^* A_{Si} U_{DC}^2 f_P
\]

\[
\frac{dP_H}{dA_{Si}} = 0 \quad \rightarrow \quad A_{Si,\text{opt}}, \quad P_{H,\text{min}}
\]

\[
P_{H,\text{min}} = \sqrt{2} I_{H,rms} U_{DC} \sqrt{f_P} FOM^{\frac{1}{2}} \propto P_O \sqrt{f_P}
\]

\[
\Delta \eta_{H,\text{min}} \propto \sqrt{f_P}
\]

- Larger Losses for Higher Sw. Frequency
- Large \( A_{Si} / \) Low Cond. Losses only for ZVS
- Extreme Efficiency Only for Low Sw. Frequ.

\[
R_{DS(on)}^* = \frac{R_{DS(on)}}{A_{Si}}
\]

\[
C_{eq} = C_{eq}^* A_{Si}
\]

\[
FOM = R_{DS(on)}^* C_{eq}^*
\]
**η-ρ-Characteristic of Auxiliary Supply**

- Power Consumption of Control, Fans etc. Independent of Output Power
- Power Density Relates Volume of Aux. Supply to Total (!) Output Power

\[
\Delta \eta_{\text{aux}} = \frac{P_{\text{aux}}}{P_O} \\
\rho_{\text{aux}} = \frac{P_O}{V_{\text{aux}}}
\]

→ Auxiliary Power Defines Efficiency Limit
\( \eta - \rho \)-Characteristic of Storage+Heatsink+Auxiliary

- Overall Power Density Lower than Lowest Individual Power Density
- Total Efficiency Lower than Lowest Individual Efficiency

\[
V = V_C + V_H + V_{\text{aux}} \quad | \quad \rho_i = \frac{P_i}{V_i} \\
\rho^{-1} = \rho_C^{-1} + \rho_H^{-1} + \rho_{\text{aux}}^{-1}
\]

\[
P_i = P_O + \sum_i P_i = \frac{P_O}{\eta} \quad \rightarrow \quad \eta = \frac{1}{1 + \left(1 + \frac{i}{P_O}\right)}
\]

- Example of Heat Sink + Storage (No Losses)

\[
\rho_C = \beta_C \gamma_C \\
\rho_H = \Delta T_{s-a} \cdot \text{CSPI} \cdot \frac{\eta_H}{(1 - \eta_H)} \\
\rho_{CH} = \frac{\beta_C \gamma_C}{1 + \left(1 - \eta_H\right) \beta_C \gamma_C \alpha_H^{-1}}
\]

\( \eta - \rho \) Characteristic w/o Magnetics
\( \rightarrow \) Higher Sw. Frequ. Leads to Larger Volume
\[ \eta - \rho - \text{Characteristic of Inductor (1)} \]

- Inductor Flux Swing Defined by DC Voltage & Sw. Frequ. (& Mod. Index)

\[ \Delta \Phi = \frac{U_{DC}}{NA_F} \frac{T_p}{f_p A_F} \propto \frac{1}{A_F} \propto \frac{1}{l^2} \]

\[ P_E \propto f_p \Delta \hat{B}^\beta V_E \propto \left( \frac{1}{l^4} \right) l^3 \propto \frac{1}{l} \]

\[ P_W = I_{rms}^2 R_W \propto \frac{l}{\kappa A_W} \propto \frac{l}{l^2} \propto \frac{1}{l} \]

- 

**\( \alpha = 1 \)**

\[ P_L \propto U_{DC} I_{rms} \]

\[ \propto \frac{U_{DC}}{\sqrt{f_p V_L}} \]

\[ \propto l \]

\( \rightarrow \) Losses are Decreasing with Increasing Linear Dimensions & Sw. Frequency
- Loss-Opt. of Single-Airgap N87 Core Inductor
- Consideration of HF Winding and Core Losses
- Thermal Limit Acc. To Natural Convection
- Assumption: Given Magnetic Core

→ Higher Sw. Freq. – Lower Min. Ind. Losses – Overall Loss Red. Limited by Semicond. Sw. Losses
η-ρ-Characteristic of Inductor (3)

- Overall Power Density Lower than Lowest Individual Power Density
- Total Efficiency Lower than Individual Efficiency

\[ P_L \propto \frac{U_{DC}I_{\text{rms}}}{\sqrt{f_P V_L^3}} \propto \frac{P_O}{\sqrt{f_P V_L^3}} \quad \left( = k_{L,\text{max}} V_L^2 \right) \]

\[ P_L = (1 - \eta_L) P_I = (1 - \eta_L) \frac{P_O}{\eta_I} \]

\[ \rho_L = \frac{P_O}{V_L} \propto P_O f_P^3 \frac{(1 - \eta_L)^3}{\eta_L^3} \]

- Natural Convection

\[ \rho_{L,\text{max}} \propto \sqrt{f_P} \]

→ η-ρ Characteristic of Inductors
→ Higher Sw. Freq. Leads to Lower Vol.
→ Allowed Losses Defined by Cooling

\[ \frac{P_L}{P_O} = \frac{1 - \eta_L}{\eta_L} \propto \frac{1}{\sqrt{f_P V_L^3}} \]
**Remark - Natural Conv. Thermal Limit (1)**

- Example of Highly-Compact 3-Φ PFC Rectifier
- Nat. Conv. Cooling of Inductors and EMI Filter
- Semiconductors Mounted on Cold Plate

\[ P_p = 10 \text{ kW} \]
\[ U_N = 230V_{AC} \pm 10\% \]
\[ f_N = 50\text{Hz} \text{ or } 360\ldots800\text{Hz} \]
\[ U_o = 800V_{DC} \]
\[ f_p = 250\text{kHz} \]

\[ \rho = 10 \text{ kW/dm}^3 \quad @ \quad \eta = 96.2\% \]

- Systems with \( f_p = 72/250/500/1000\text{kHz} \)
- Factor 10 in \( f_p \) - Factor 2 in Power Density
Remark - Natural Conv. Thermal Limit (2)

- Example of Highly-Compact 3-Φ PFC Rectifier
- Nat. Conv. Cooling of Inductors and EMI Filter
- Semiconductors Mounted on Cold Plate

\[ P_o = 10 \text{ kW} \]
\[ U_N = 230V_{AC\pm10}\% \]
\[ f_N = 50\text{Hz or } 360 \ldots 800\text{Hz} \]
\[ U_O = 800V_{DC} \]
\[ f_P = 250kHz \]

\[ \rho = 10 \text{ kW/dm}^3 \] @ \[ \eta = 96.2\% \]

- Systems with \[ f_P = 72/250/500/1000kHz \]
- Factor 10 in \[ f_P \] - Factor 2 in Power Density
Remark – Natural Conv. Thermal Limit (3)

- Consideration of Different Shape Factors
- Constant Power to be Processed

Planar Structure Facilitate High Power Density
Cube Shape Shows Low Surface Area @ Given Volume
Nat. Conv. Requires Min. Thickness of Boundary Layer (>5mm) which is often Not Considered
\( \eta - \rho \)-Characteristic of Inductor (4)

- Natural Convection Heat Transfer Seriously Limits Allowed Inductor Losses
- Higher Power Density Through Explicit Inductor Heatsink

\[ P_L = \frac{(1-\eta_L)}{\eta_L} P_O \leq k_{L,\text{max}} V_I^2 = k_{L,\text{max}} \left( \frac{P_O}{\rho_L} \right)^{\frac{2}{3}} \]

\[ \rho_{L,\text{max}} = k_{L,\text{max}}^\frac{2}{3} \left( \frac{\eta_L}{1-\eta_L} \right)^{\frac{3}{2}} P_O^{-\frac{1}{2}} \]

\[ \rho_{L,\text{max}} \propto \sqrt{f_p} \]

- Explicit Heatsink

\[ \rho_{LH,\text{max}} \approx \frac{1}{2} \rho_{H,\text{max}}(\eta_L) \]

\( \rightarrow \) Heat Transfer Coefficients \( k_L \) and \( \alpha_L \) Dependent on Max. Surface Temp. / Heatsink Temp.

\( \rightarrow \) Water Cooling Facilitates Extreme (Local) Power Densities
Remark – Example for Explicit Heatsink for Magn. Component

- Phase-Shift Full-Bridge Isolated DC/DC Converter with Current-Doubler Rectifier
- Heat Transfer Component (HTC) & Heatsink for Transformer Cooling
- Magn. Integration of Current-Doubler Inductors

\[ P_D = 5kW \]
\[ U_{in} = 400V \]
\[ U_0 = 48...56V \text{ (300mV}_{pp} \) \]
\[ T_a = 45^\circ C \]

\[ f_P = 120kHz \]

\[ 9 \text{ kW/dm}^3 (148\text{ W/in}^3) @ 94.5\% \]
Remark – Example for Explicit Heatsink for Magn. Component

- Phase-Shift Full-Bridge Isolated DC/DC Converter with Current-Doubler Rectifier
- Heat Transfer Component (HTC) & Heatsink for Transformer Cooling
- Magn. Integration of Current-Doubler Inductors

\( P_D = 5\text{ kW} \)
\( U_{in} = 400\text{V} \)
\( U_0 = 48\ldots56\text{V} \ (300\text{mV}_{pp}) \)
\( T_a = 45\degree\text{C} \)

\( f_p = 120\text{kHz} \)

\[ 9\text{ kW/dm}^3 \ (148\text{W/in}^3) \ @ \ 94.5\% \]
Remark – Dependency of Efficiency on Load Condition

- Assumption of Purely Ohmic Losses
- Quadratic Dependency of Losses on Output Power

\[ \eta_L = \frac{P_O}{P_L + P_O} = \frac{1}{1 + \frac{P_L}{P_O}} \approx 1 - \frac{P_L}{P_O} \]

\[ P_L = R_W I_{rms}^2 = k_2 P_O^2 \rightarrow \eta \approx 1 - k_2 P_O \]

- Quadratic Reduction of Losses with Output Power
- High Part Load Efficiency Despite Low Rated Load Efficiency (Thermal Limit @ Rated Load)
Overall Converter $\eta$-$\rho$-Characteristics

- **Low Semiconductor Sw. Losses**

- **High Semiconductor Sw. Losses**

$\Rightarrow$ Low Sw. Losses / High Sw. Frequ. / Small Heatsink / Small Ind. / High Total Power Density

$\Rightarrow$ High Sw. Losses / Low Sw. Frequ. / Large Heatsink / Large Ind. / Low Total Power Density
Overall Converter $\eta$-$\rho$-Characteristics – Summary

- Inductor Takes Significant Influence on Efficiency/Power Density Characteristic
- Converters with Inductor → Very Low Losses Only for Very Low Power Density
- Conv. with No Inductor → Very High Power Density @ Low Losses
- Inductor Defines Power Density Limit of Ultra-Efficient Converter Systems!

$\rightarrow$ Eff./Power Density Characteristic Strongly Dependent on Converter Type!
$\rightarrow$ Variable Speed Drive Inverters – No Inductor (Built into AC Machine) – Very High Power Density
Reduction of Inductor Requirement

→ Parallel Interleaving
→ Series Interleaving
**Inductor Volt-Seconds / Size**

- Inductor Volt-Seconds are Determining the Local Flux Density Ampl.
- Output Inductor has to be Considered Part of the EMI Filter

- Multi-Level Converters Allow to Decrease Volt-Seconds by Factor of $N^2$
- Calculation of Equivalent Noise Voltage @ Sw. Frequency (2nd Bridge Leg w. Fund. Frequ.)

$$\Delta \hat{B} \propto \frac{T_p U_{DC}}{A_E} \propto \frac{U_{DC}}{f_p A_E}$$

$$U_{f_p, eq, rms}^2 = U_{AC, rms}^2 - U_{O, rms}^2$$

$$U_{f_p, eq, rms} = \sqrt{M \left( \frac{2}{\pi} - \frac{M}{2} \right) U_{DC}}$$

→ EMI Filter Design Can be Based on Equiv. Noise Voltage
Reduction of Inductor Volt-Seconds / Size

- Multi-Level Characteristic through Series-Interleaving
- Multi-Level Characteristic through Parallel Interleaving

\[ \Delta B \propto \frac{T_p U_{DC}}{N} \]

Identical Spectral Properties for Both Concepts
- Series Interleaving Avoids Coupling Inductor of Parallel Interleaving!
**Multi-Level Converter Approach**

- Multi-Level PWM Output Voltage – Minimizes Ind. Volume
- Flying Cap. Conv. – No Splitting of DC Inp. Voltage Required
- Low-Voltage GaN or Si Power Semiconductors

**FIG. 1**

Full-Bridge Topology or DC/AC Buck-Type + Unfolder

**FIG. 4**

Example of 5-Level Flying Capacitor Converter

- 5 Output Voltage Levels
- 320 kHz Single-Cell Sw. Frequency
- 12µF Flying Capacitors
- Improved Phase-Shift PWM

→ Very Small Output Inductor
→ Voltage Balancing Challenging in certain Operating Conditions
Higher Switching Frequency Increases Required Attenuation
Higher Switching Frequ. Increases Required Att. → Only Option $f_P > 500\text{kHz}$
Transformers

Optimal Operating Frequency
Example of MF/MV Transformer
Transformer Operation Frequency Limit

- Dependency of Volume and Weight on Frequency
  - Higher Frequency Results in Smaller Transformer Size only Up to Certain Limit (Prox. Eff.)
  - Defined Frequencies for Min. Vol. or Min. Weight – Dep. On Strand Diam. & Wdg Width

Source: Philips

- 100Vx1A 1.1 Transformers, 3F3, 30°C Temp. Rise
Future Direct MV Supply of 400V DC Distribution of Datacenters

- Reduces Losses & Footprint / Improves Reliability & Power Quality
- Unidirectional Multi-Cell Solid-State Transformer (SST)
- AC/DC and DC/DC Stage per Cell, Cells in Input Series / Output Parallel Arrangement

---

Conventional US 480V\textsubscript{AC} Distribution

- Facility-Level 400 V\textsubscript{DC} Distribution

→ Unidirectional SST / Direct 6.6kV AC → 400V DC Conversion
Example of a 166kW/20kHz SST DC/DC Converter Cell

- Half-Cycle DCM Series Resonant DC-DC Converter
- Medium-Voltage Side 2kV
- Low-Voltage Side 400V
**MF Transformer Design**

- **DoF** – Electric (# of Turns & Op. Frequ.) / Geometric / Material (Core & Wdg) Parameters
- Cooling / Therm. Mod. of Key Importance / Anisotr. Behavior of Litz Wire / Mag. Tape
- **20kHz Operation** Defined by IGBT Sw. Losses / Fixed Geometry

→ **Region I:** Sat. Limited / Min. Loss @ \( P_c/P_w = 2/\beta \) (\( R_{ac}/R_{dc} = \beta/\alpha \)) / Region III: Prox. Loss Domin.
→ Heat Conducting Plates between Cores and on Wdg. Surface / Top/Bottom H2O-Cooled Cold Plates
**MF Transformer Prototype**

- **Power Rating**: 166 kW
- **Efficiency**: 99.5%
- **Power Density**: 44 kW/dm³

- Nanocrystalline Cores with 0.1mm Airgaps between Parallel Cores for Equal Flux Partitioning

- Litz Wire (10 Bundles, 950 x 71μm Each) with CM Chokes for Equal Current Partitioning
Calculation of Converter $\eta$-$\rho$-Performance Limits

Google Little Box Challenge
Ultra-Efficient 3-Φ PFC Rectifier
LiTTLE BOX CHALLENGE

- Design / Build the 2kW 1-Φ Solar Inverter with the Highest Power Density in the World
- Power Density > 3kW/dm³ (50W/in³)
- Efficiency > 95%
- Case Temp. < 60°C
- EMI FCC Part 15 B

Push the Forefront of New Technologies in R&D of High Power Density Inverters

\[ S_o \leq 2 \text{kVA} \]
\[ \cos \Phi_o \leq +0.7 \ldots -0.7 \]
\[ f_o = 60 \text{ Hz} \]
Selected Converter Topology

- Interleaving of 2 Bridge Legs per Phase
- Active DC-Side Buck-Type Power Pulsation Buffer
- 2-Stage EMI AC Output Filter

→ ZVS of All Bridge Legs @ Turn-On/Turn-Off in Whole Operating Range (4D-TCM-Interleaving)
→ Heatsinks Connected to DC Bus / Shield to Prevent Cap. Coupling to Grounded Enclosure
ZVS of Output Stage / TCM Operation

- TCM Operation for Resonant Voltage Transition @ Turn-On/Turn-Off

- Requires Only Measurement of Current Zero Crossings, i = 0
- Variable Switching Frequency Lowers EMI
Evaluation of Power Semiconductors

- Comparison of Soft-Switching Performance of ~60mΩ, 600V/650V/900V GaN, SiC, Si MOSFETs
- Measurement of Energy Loss per Switch and Switching Period

- GaN MOSFETs Feature Best Soft-Switching Performance
- Similar Soft-Switching Performance Achieved with Si and SiC
- Almost No Voltage-Dependency of Soft-Switching Losses for Si-MOSFET
High Frequency Inductors (1)

- Multi-Airgap Inductor with Multi-Layer Foil Winding Arrangement Minim. Prox. Effect
- Very High Filling Factor / Low High Frequency Losses
- Magnetically Shielded Construction Minimizing EMI
- Intellectual Property of F. Zajc / Fraza

- $L = 10.5\mu H$
- $2 \times 8$ Turns
- $24 \times 80\mu m$ Airgaps
- Core Material DMR 51 / Hengdian
- $0.61mm$ Thick Stacked Plates
- $20 \mu m$ Copper Foil / 4 in Parallel
- $7 \mu m$ Kapton Layer Isolation
- $20m\Omega$ Winding Resistance / $Q \approx 600$
- Terminals in No-Leakage Flux Area

→ Dimensions - $14.5 \times 14.5 \times 22mm^3$
High Frequency Inductors (2)

- High Resonance Frequency → Inductive Behavior up to High Frequencies
- Extremely Low AC-Resistance → Low Conduction Losses up to High Frequencies
- High Quality Factor

Shielding Eliminates HF Current through the Ferrite → Avoids High Core Losses
Shielding Increases the Parasitic Capacitance
High Frequency Inductors (3)

- Cutting of Ferrite Introduces Mech. Stress
- Significant Increase of the Loss Factor
- Reduction by Polishing / Etching (5 μm)

\* Knowles (1975!)

→ Comparison of Temp. Increase of a Bulk and a Sliced Sample @ 70mT / 800kHz
Multi-Airgap Inductor Core Loss Measurements (1)

- Investigated Materials - DMR51, N87, N59
- 30 µm PET Foil with Double Sided Adhesive Between the Plates
- Varying Number $N$ of Air Gaps Assembled from Thin Ferrite Plates
- Number of Air Gaps:
  - Solid $N=6$
  - $N=20$

$\Rightarrow$ Sinusoidal Excitation with Frequencies in the Range of 250 kHz ... 1MHz
Multi-Airgap Inductor Core Loss Measurements (2)

- Magnetic Circuit Designed to Concentrate Flux-Density in Sample
- Homogeneous Flux-Density in Sample
- Stray Field in Vicinity of Excitation Winding is Negligible
- Primary Winding: 12 Turns with 270 x 71µm Litz Wire
- Aux. and Sense Winding: 12 Turns with 75 x 50 µm Litz Wire

Stationary Flux Density Distribution with $B = 150$ mT in the Sample Area
Multi-Airgap Inductor Core Loss Measurements (3)

- Losses in Sample – Increasing Temperature
- Excitation with 100 mT @ 750 kHz
- Start @ $T=35^\circ C$
- Excitation Time = 90 s

Solid, $\Delta T=27.7^\circ C$

$N=20$, $\Delta T=73.5^\circ C$
Multi-Airgap Inductor Core Loss Measurements (4)

- Total Core Loss in Sample with Varying Air Gaps and Test Fixture
- Excitation @ 500 kHz

\[ \text{Losses Increase Linearly with the Number } N \text{ of Introduced Air Gaps} \]

\( \rightarrow \text{Conclusion: Surface Layers Deteriorated by Machining of Ferrite} \)
Analysis of Ferrite Surface Condition

- Untreated Samples - Cut with Diamond Saw from Sintered Ferrite Rod
- Etched Samples - 100 µm Etching of Cut Plates with Hydrochloric (HCl) Acid
- Electron Microscopy - 45° Angle and 200 µm Resolution
- Focused Ion Beam - FIB Preparation for 5 µm Resolution Electron Microscopy
Comparison - *Untreated* Samples

- **DMR 51**
- **N 59**
- **N 87**
Comparison - *Etched Samples*

- DMR 51
- N 59
- N 87
DMR 51 Untreated – FIB Preparation (1)
DMR 51 ETCHED – FIB Preparation (2)
Multi-Airgap Inductor Core Loss Approximation (1)

\[ \begin{align*}
DMR51 & \quad k_0 = 1.24e - 7 & \quad k_s = 0.238 \\
& \quad \alpha = 2.25 & \quad \alpha_s = 1.09 \\
& \quad \beta = 3.16 & \quad \beta_s = 2.63 \\
N59 & \quad k_0 = 0.496 & \quad k_s = 0.0025 \\
& \quad \alpha = 1.09 & \quad \alpha_s = 1.46 \\
& \quad \beta = 2.56 & \quad \beta_s = 2.58 \\
N87 & \quad k_0 = 9.02e - 9 & \quad k_s = 2.2091 \\
& \quad \alpha = 2.32 & \quad \alpha_s = 1.04 \\
& \quad \beta = 1.90 & \quad \beta_s = 3.19
\end{align*} \]

- Comp. of Coefficients – DMR51, N59, N87

\[ P_V = k_0 f^{\alpha} \hat{B}^{\beta} \left( \frac{A_s}{A_c} \right)^{\alpha_s} + k_s f^{\alpha_s} \hat{B}^{\beta_s} \cdot N \cdot A_s \]
Multi-Airgap Inductor Core Loss Approximation (2)

- Total Core Loss in Sample with Varying Air Gaps and Test Fixture
- Excitation @ 500 kHz

\[ P_{\text{loss}}(N) = k_0 f^\alpha \hat{B}^\beta \left( V_C \left( \frac{A_S}{A_C} \right)^\beta + V_S \right) + k_S f^{\alpha_S} \hat{B}^{\beta_S} \cdot N \cdot A_S \]

Sufficiently Accurate
Little-Box 1.0 Prototype

- **Performance**
  - 8.2 kW/dm³
  - 96.3% Efficiency @ 2kW
  - $T_c=58^\circ C @ 2kW$

- **Design Details**
  - 600V IFX Normally-Off GaN GIT
  - Antiparallel SiC Schottky Diodes
  - Multi-Airgap Ind. w. Multi-Layer Foil Wdg
  - Triangular Curr. Mode ZVS Operation
  - CeraLink Power Pulsation Buffer

→ Analysis of Potential Performance Improvement for “Ideal Switches”
Little-Box 1.0 Prototype

■ Performance
- 8.2 kW/dm³
- 96.3% Efficiency @ 2kW
- $T_c=58°C$ @ 2kW

■ Design Details
- 600V IFX Normally-Off GaN GIT
- Antiparallel SiC Schottky Diodes
- Multi-Airgap Ind. w. Multi-Layer Foil Wdg
- Triangular Curr. Mode ZVS Operation
- CeraLink Power Pulsation Buffer

★ 135 W/in³

→ Analysis of Potential Performance Improvement for “Ideal Switches”
Little Box 1.0 @ Ideal Switches (TCM)

- Multi-Objective Optimization of Little-Box 1.0 (X6S Power Pulsation Buffer)
- Step-by-Step Idealization of the Power Transistors
- Ideal Switches: $k_c = 0$ (Zero Cond. Losses); $k_s = 0$ (Zero Sw. Losses)

⇒ Analysis of Improvement of Efficiency @ Given Power Density & Maximum Power Density
⇒ The Ideal Switch is NOT Enough (!)
\[ \rho = 6 \text{kW/dm}^3 \]
\[ \eta \approx 99.35\% \]
\[ L = 50 \mu\text{H} \]
\[ f_s = 500\text{kHz or 900kHz} \]

→ **L & \( f_s \)** are Independent Degrees of Freedom
→ **Large Design Space Diversity** (Mutual Compensation of HF and LF Loss Contributions)
High-Efficiency 3-Φ Buck-Type PFC Rectifier
3-Φ Integrated Active Filter (IAF) Rectifier

- Injection of 3rd Harmonic Ensures Sinusoidal Input
- Six-Pulse Output of Uncontrolled Rectifier Stage
- Buck-Type Output Stage Generates DC Output from Six-Pulse Rectifier Output
- Three Devices in the Main Conduction Path

\[ U_{in} = 400V_{AC} \]
\[ U_{O} = 400V_{DC} \]
\[ P_{O} = 8kW \]
\[ f_{P} = 27kHz \]
3-Φ IAF Rectifier Multi-Objective Optimization

- Life Cycle Costs: (i) Initial Costs & (ii) Electricity Costs of Converter Losses

\[ \eta \approx 99\% \text{ for Min. LCC} \]

\[ \rightarrow \text{10 Years of 24/7 Operation Demands} \]
3-Φ IAF Rectifier Demonstrator

- Efficiency $\eta > 99\%$ @ 60% Rated Load
- Mains Current $THD_r \approx 2\%$ @ Rated Load
- Power Density $\rho \approx 4\text{ kW/dm}^3$

⇒ SiC Power MOSFETs & Diodes
Future Prospects of Power Electronics

MV / MF Power Electronics

Standard / Integrated Solutions

Smart Microgrids, DC Distribution

System Applications

100 kW

Micro Power Electronics

Microelectronics Technology, Power Supply on Chip

Future Extension of Power Electronics Application Area
Future Prospects of Magnetics

- Side Conditions
  - Magnetics are Basic Functional Elements (Filtering of Sw. Frequ. Power, Transformers)
  - Non-Ideal Material Properties (Wdg. & Core) Result in Finite Magnetics Volume (Scaling Laws)
  - Manufacturing Limits Performance (Strand & Tape Thickness etc.) @ Limited Costs

- Option #1: Improve Modeling / Optimize Design
  - Core Loss Modeling / Measurement Techniques (Cores and Complete Ind. / Transformer)
  - Multi-Obj. Optimiz. Considering Full System
  - Design for Manufacturing

- Option #2: Improve Material Properties / Manufacturing
  - Integrated Cooling
  - PCB-Based Magnetics with High Filling Factor (e.g. VICOR)
  - Advanced Locally Adapted Litz Wire / Low-$\mu$ Material (Distributed Gap) / Low HF-Loss Material

- Option #3: Minimize Requirement
  - Multi-Level Converters
  - Magnetic Integration
  - Hybrid (Cap./Ind.) Converters

Magnetics/Passives-Centric Power Electronics Research Approach!
Thank You!