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Roadmap Power Electronics 2025

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Summary of 1st Roadmap Team Meeting

- Magnetic Components are the Highest Cost Factor in Power Supplies
- EMI and Semiconductor Oscillations are #1 Risk for Time to Market
- Robustness is Often More Important than Reliability
- Modularity Made it Never Into the Market
- External Manufacturing Results in Too High Costs
- Only 6-8 Weeks Development Time Requires Finished Building Blocks
- Need for Fast Simulation Models
- Digital Control Issues (Safety Requirements / Redundancy)
- Efficiency is also a Political Issue / Depends on Standardization
- Efficiency is not a Selling Argument (only for Last Person in Supply Chain)
- Ranking: Costs / Reliability / Ease of Manufacturing / Robustness

Some Challenges / Limitations Identified
Summary of 2nd Roadmap Meeting

... see Summary presented by Th. Harder
Summary of 3rd Roadmap Team Meeting

- 2025 Performance Target Values
- Evaluation of Current Research Level Technologies
- Enabling Technologies
- Technology / Research Gaps

... see Following Summary
Discussion @ 3rd Meeting
Key Performance Indices which Must be Considerably Improved until 2025

- Costs
- Power Density
- Efficiency
- Reliability / Robustness
- Time-to-Market

Environmental Impact...

$[\text{kg}_{Fe}/\text{kW}]$
$[\text{kg}_{Cu}/\text{kW}]$
$[\text{kg}_{Al}/\text{kW}]$
$[\text{cm}^2_{Si}/\text{kW}]$

State-of-the-Art

Performances are Mutually Coupled
Main Components / Concepts / Processes
Determining the Performance Limits

η-ρ-Pareto Limit

- Switching Circuit
- Transformers
- Filter Components
- EMI Filter Components
- Interconnections
- Heatsink
- Sensors
- Control Circuit
- Package
- Manufacturing

Ideal η-ρ-Limit

η-ρ-Limit for 80% Construction Volume Utilization

f_s = 20 kHz

Output Diode + MOSFETs & Inductors

Output Capacitor

Heat sink

Heat sink & Output Cap.

η-ρ-Limit

50 kHz

100 kHz

500 kHz

Power Density [kW/dm^3]

Efficiency [%]
Roadmap Approach

Step #1 ➔ Define 2025 Performance Targets
   ... Considering Past Trend Lines

Step #2 ➔ Current Research Level Technologies
         ➔ High Switching Frequency
         ➔ High Operating Temperature
   ... Considered for Each Component in Order to Check for Potential Improvements of a Selected Performance Index

Step #3 ➔ “Enabling Technologies”
   ... Selected Subset of “Current Research Level Technologies” which Potentially Enable a Considerable Performance Improvement

Step #4 ➔ “Technology / Research Gaps”
   ... Technologies Crucial for Reaching the 2025 Performance Target but Currently Not Considered in Research
Roadmap Approach

Application of a *Selection of Current Research-Level Technologies* = *Enabling Technologies*
* WBG Power Semicond.
* Adv. Packaging
* etc.

State-of-the-Art
* Power Semicond.
* Topologies
* Modulation
* Materials
* etc.

2015

20XX

2025

Technology Space / Design Space

Performance Space

2025 Performance Target Determined from Extrapolation of Performance Trends in 1990...2015

Technology/Research Gaps
General Remark

- Pragmatic Approach
- Only Already Known Research Concepts are Considered
- No Speculations on Unknown Disruptive Concepts (e.g. Nanomaterials)
- Identified Barriers are Indicating Future Research Needs
- Trivial Requirements (e.g. Higher Energy Density of Caps) are not Listed
Power Density - Expected Impr. until 2025 – Factor 2 ... 5 (10)

Filter Components (→ Minimize Volume)

→ Increase Switching Frequency

Challenges: * Higher Switching Losses
* Higher HF Losses of Passives / Thermal Management
* Increased EMI Noise (for Hard Switching)

Enablers: * Low Switching Loss WBG Semiconductors
* Adv. Inductor Concepts (e.g. Distributed Gaps)
* Adv. Packaging – Min. Parasitics (Gate & Power)
* ZVS / Resonant Converter Concepts
* High Clock Frequency Digital Control

Barriers: * Mag. Materials (Permeability /Losses at HF)
* Conductor Types / Winding Arrangements
* Thermal Management
* Adv. Design Tools (Layout, Magnetics)
* Adv. Measurem. Tools Integrated with Simulation
* Engineering Experience

Detour: * Interleaving for Frequency Multiplication

Remark: * Only Basic Converter Topologies are of Interest

→ „Enablers“ are Taken from the List of „Current Research Technologies“
→ „Barriers“ are Indicating „Technology Gaps“
→ Increase Operating Temp.

**Challenges:**
* Reliability of Interconnection Technologies
* Higher Losses

**Enablers:**
* High Temperature Passive Components
* Interconnection Technologies for Higher Temp.
* WBG Semiconductors

**Barriers:**
* Requirement to Enable all Used Components and Technologies for High Temp.

**Remark:**
* Especially Effective for High Temp. Environment

→ Change from CCM to DCM

**Challenges:**
* Higher Conduction Losses
* Higher Filtering Effort

**Enablers:**
* Low On-Resistance Power Switches (CoolMOS, WBG)
* Advanced Digital Control
* Interleaving for Red. of Filter Effort

**Barriers:**
* New Circuit Topologies / Modulation Schemes
* Magnetic Materials (High Flux Swing, High Freq.)
* Conductor Types / Winding Arrangements

**Remark:**
* Only Basic Conv. Topologies with Modified Control / Min. Auxiliary Circuits are of Interest

→ etc., etc.

→ Change from CCM to DCM
- **EMI Filter (→ Minimize Volume)**

  → **Increase Switching Freq. Beyond 500kHz**

  | Challenges:  | .... |
  | Enablers:    | .... |
  | Barriers:    | .... |
  | Remark:      | .... |

  → etc., etc.

- **Heat Sink (→ Minimize Volume)**

- **Interconnection / Packaging (→ Minimize Volume)**

- **etc.**
Efficiency

- Expected Loss Reduction until 2025 – Factor 2 ... 3

- Evaluation of Contributions to Loss Reduction of the Main Components Employing Current Research Level Technologies
  - Switching Circuit and Gate Drive
  - Transformers
  - Filter Components
  - EMI Filter Components
  - Heatsink
  - Interconnections
  - Sensors
  - Control Circuit

- Utilized Current Research Concepts
  - Enabling Technologies

- Required Additional New Technologies
  - Technology Gaps
Costs

- Expected Reduction until 2025 – Factor ... 2

- Evaluation of Contributions to Loss Reduction of the Main Components Employing Current Research Level Technologies
  - Switching Circuit and Gate Drive
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  - Sensors
  - Control Circuit

- Utilized Current Research Concepts
  - Enabling Technologies

- Required Additional New Technologies
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Examples of Enabling Technologies
Enabling Technologies (1)

→ Wide Bandgap Semiconductors
  * Low Switching Losses
  * Low Conduction Losses

→ Next Generation (LV) Si Semiconductors
  * Low Conduction Losses

- Wide Bandgap Semiconductors
- Next Generation (LV) Si Semiconductors
- **Enabling Technologies (2)**

- **Wide Bandgap Semiconductors**
  - Low Switching Losses
  - Low Conduction Losses

- **Next Generation (LV) Si Semiconductors**
  - Low Conduction Losses

- 600V GaN Switching Behavior
- Main Challenges in Packaging (!)
Enabling Technologies (3)

→ Adv. Packaging of Power Semicond (Chip Scale etc.)
  * Low Power Path Parasitics
  * Low Gate Drive Parasitics
  * Low Coupling of Power and Gate Drive Path
  * Low Thermal Resistance
  * 3D Interconnection
  * PCB Embedding (incl. Therm. Management)
  * Minimizing DM and CM EMI (Integr. Switch. Cell)

Ultra Low Inductance Package

DC/DC Converter with Embedded Chip
# Enabling Technologies (4)

- Heterogeneous Integration
  - Switching Cell in a Package
  - Drivers with Integrated Power Supply
  - DC/DC Converter in a Package
### Enabling Technologies (5)

#### Heterogeneous Integration

<table>
<thead>
<tr>
<th>Competitor A</th>
<th>PI3101</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1 in² and 34 W/in²</td>
<td>0.57 in² and 105 W/in²</td>
</tr>
<tr>
<td>72 Watts</td>
<td>60 Watts</td>
</tr>
</tbody>
</table>

**Vicor**

#### System in Package (SiP) Approach
- **Enabling Technologies (6)**

  → **Heterogeneous Integration**

  ![Information Processors Are Sawn Out of Scalable Wafers](image1)

- **System in Package (SiP) Approach**

  ![ChiP Power Components Are Sawn Out of Scalable Magnetic Panels](image2)
**Enabling Technologies (7)**

→ **Heterogeneous Integration**

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**12V PowerStage in Embedded Die System-in-Package**

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**Challenges to Higher Density 12Vin POL solutions**

1. FET Switching Losses  
   Sarda GaAs FET

2. High current inductors are large  
   Multiphase (lower I/phase)

3. Parasitic Impedances  
   Integrated Power Stage

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► **Presented @ APEC 2015**
Enabling Technologies (8)

Heterogeneous Integration

HIPS Module

Available technology to enable compact multi-chip HIPS module: Embedded Die in Substrate

Two motivations:
1. Performance (minimize parasitics for multi-MHz operation)
2. PowerStage package size

- Monolithic Quad GaAs die
- 2-phase CMOS driver
- Chip caps
- Boot caps
- AC-coupled gate caps
- Schottky diodes (for diode emulation)

Integrates performance-critical components

Presented @ APEC 2015
Enabling Technologies (9)

Heterogeneous Integration

HIPS Approach
- Embed Active components
  - Quad GaAs FET die
  - CMOS 2-phase driver
- Integrate performance-critical components
  - Driver & FET
  - Cbyp, Boot caps, gate caps, Schottky's

Gen2 HIPS Performance
- Power Train Density
- Examines Gen2 performance in 1-5MHz range
- Can push to higher Fsw also

Presented @ APEC 2015
Enabling Technologies (10)

→ Adv. Inductor Concepts
  * Magnetic Integration (CM/DM)
  * Multi-Gapped Magnetic Cores
  * Constant Flux Density Magnetic Cores
  * Integrated Cooling
  * Parasitic Capacitance Cancellation
  * 3D Interconnection

→ Adv. Capacitor Concepts
  * Low Parasitic Ind. 3D Interconnection
  * Integrated Cooling / High Current Concepts

→ Adv. Component Interconnection Concepts
  * Low DC and HF Loss Interconnection
  * Integrated Concepts (Cooling, Sensing)

→ Adv. Cooling Concepts
  * Heat Spreading Concepts
  * Two-Side Cooling
  * Two Phase Cooling
  * Integr. Concepts (El. and Thermal Interconn.)

→ Adv. Low Frequency Energy Buffer Concepts
  * Replace Electrolytic Cap. by Conv. And High Δv Cap.
Enabling Technologies (11)

Advanced Inductor Concepts

- Layered Foils as Alternative to Litz Wire
- New Winding Geometries
- Quasi-Distributed Airgap
- etc.

Source: Ch. Sullivan / Dartmouth
Enabling Technologies (12)

- **Digital Control (Moores Law)**
  * High Calc. Capability / Monitoring / Adv. Control
  * High Clock Rates / High Sampling Frequ.

- **Change from CCM to DCM Operation**
  * DCM Inductors Store Less Energy / Lower Vol.
  * Facilitates ZVS / Res. Transition Operation
  * Workaround for Slow Passives Improvement
  * i=0 Instead of Cont. Current Sensor

- **Advanced Modulation**
  * Noise Shaping Variable Switching Frequency

- **Active ZVS / Resonant Operation**
  * Low Switching Losses
  * Low EMI / No Free Ringing

- **Interleaving / Multi-Cell / Multi-Level Converters**
  * Increase of Effective Switching Frequency
  * Cancellation (DM-CM Transfer) instead of Filtering

- **Advanced Control**
  * Trajectory-Based Control
  * Predictive Control
Enabling Technologies (13)

→ Bringing Together Advanced Circuit Concepts / Semiconductors / Packaging

* World Smartest Laptop Charger

* World Smallest Laptop Charger
Enabling Technologies (14)

→ Bringing Together Advanced Circuit Concepts / Semiconductors / Packaging

* World Smallest Laptop Charger
Enabling Technologies (15)

→ Predictive Control and Optimal Trajectory Control

Consider Individual Switching Instants vs. Average over Numerous Switching Cycles
Examples of Technology Barriers
■ **Technology Barriers**

► **Example: Serious Limitation of Operating Frequency by HF Losses**

— Core Losses (incr. @ High Freq. & High Operating Temp.)
— Temp. Dependent Lifetime of the Core
— Skin-Effect Losses
— Proximity Effect Losses

\[
F_s = r / \sqrt{N}
\]

Source: Prof. Albach, 2011

■ Adm. Flux Density for given Loss Density

■ Skin-Factor \( F_s \) for Litz Wires with \( N \) Strands
Technology Barriers

- >50 MHz Switches
- Multi-Domain/Objective Design / Models
- Design for (3D)Manufacturing
- Manufact. of 3D-Integrated Planar Structures
- Built-In Measurement Devices
- Merging of Simulation & Measurement
- Full Integration / Limited Flexibility
- etc.

- < 500 kHz Magnetics
- High Parasitics of Packages
- Single Domain Design Tools / Models
- Conventional Voltage / Current Probes
- Discrete Components / Max. Flexibility
- Technological Limits of Universities
- etc.

- Chicken & Egg Problem of New Technologies / Identification of Killer Applications
Example of Advanced Power Electronics Design Platform

Source: GECKO Simulations

Input
Topology | Device Models | Control Circuit | 3D-Geometry | Materials

- GeckoEMC
  3D-Electromagn. Parasitics Extraction
  Reduced Order Impedance Matrix

- GeckoCIRCUITS
  Fast Circuit Simulator

- GeckoHEAT
  3D-Thermal FEM Solver
  Thermal Impedance Matrix

- Modeling & Design
  - Circuit Simulation
  - Thermal Simulation
  - EM Simulation

Post Processing
Design Metrics Calculation
Summary
Summary (1)

- WBG Semiconductor Technology
- Microelectronics (Moore’s Law)

Enabling an up to Factor of 10 Performance Improvement
Summary (2)

- Considerable Future Extension of Power Electronics Application Area
  
  * Smart Homes / DC Distribution
  * Zero Energy Buildings
  * Wireless Power Transfer
  * Personal Digital Assistants
  * Automated Manufacturing / Robotics
  * EV Charging
  * etc.

- Bridge to Power Systems
- Establish (Closer) University / Industry (Technology) Partnerships
- Establish Cost Models, Consider Reliability as Performance

- MEGA Power Electronics
  (Medium Voltage, Medium Frequency)

- Micro Power Electronics
  (Microelectronics Technology Based, Power Supply on Chip)

- "Largely" Standard Solutions

- Smart Homes / DC Distribution
- Zero Energy Buildings
- Wireless Power Transfer
- Personal Digital Assistants
- Automated Manufacturing / Robotics
- EV Charging
- etc.
Thank you!