Multi-Objective Optimization of Power Electronics Converter Systems

Johann W. Kolar
Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
www.pes.ee.ethz.ch
Outline

► Introduction
► Multi-Objective Optimization Approach
► Optimization Application Examples
► Summary

Acknowledgement
D. Bortis
R. Bosshard
R. Burkart
F. Krismer
Introduction

Power Electronics Performance Trends
Power Converter Design Challenge
Power Electronics Converters Performance Trends

Performance Indices

- Power Density \([\text{kW/dm}^3]\)
- Power per Unit Weight \([\text{kW/kg}]\)
- Relative Costs \([\text{kW/\$}]\)
- Relative Losses \([\%]\)
- Failure Rate \([\text{h}^{-1}]\)

Environmental Impact...

\[
\frac{\text{kg}_{\text{Fe}}}{\text{kW}}, \frac{\text{kg}_{\text{Cu}}}{\text{kW}}, \frac{\text{kg}_{\text{Al}}}{\text{kW}}, \frac{\text{cm}^2_{\text{Si}}}{\text{kW}}
\]

State-of-the-Art

Future

Time-to-Market

Costs

Losses

Weight

Volume

Failure Rate
Performance Improvements (1)

- **Power Density**
  - **Telecom Power Supply Modules:** Typ. Factor 2 over 10 Years
Performance Improvements (2)

Inefficiency (Losses)... $1 - \eta$

- Efficiency
  - PV Inverters: Typ. Loss Red. of Typ. Factor 2 over 5...10 Years
Multi-Objective Design Challenge (1)

- Performances are Approaching Physical Limits (e.g. Efficiency)
- Counteracting Effects of Key Design Parameters
- Mutual Coupling of Performance Indices - Trade-Offs

→ Large Number of Degrees of Freedom / Multi-Dimensional Design Space
→ Full Utilization of Design Space only Guaranteed by Multi-Objective Optimization
Multi-Objective Design Challenge (2)

- Performances are Approaching Physical Limits (e.g. Efficiency)
- Counteracting Effects of Key Design Parameters
- Mutual Coupling of Performance Indices - Trade-Offs

→ Large Number of Degrees of Freedom / Multi-Dimensional Design Space
→ Full Utilization of Design Space only Guaranteed by Multi-Objective Optimization
Multi-Objective Design Challenge (3)

- Specific Performance Profiles / Trade-Offs Dependent on Application

- Functional Performance Profiles
  - Cost, Size, Reliability, Efficiency

  - Domestic Applications
  - Industry Applications
  - Information & Communication Industry
  - Laboratory Applications
  - Aerospace Applications
Visualization of Multiple Performances

- Spider Charts, etc.
- Chernoff-Faces ;-) 

Multi-Objective Optimization

Abstraction of Converter Design
Design Space / Performance Space
Pareto Front
Sensitivities / Trade-Offs
Abstraction of Power Converter Design

Performance Space

- Efficiency
- Power Density
- Costs
- Reliability
- etc.

Design Space

- System
  - Phase-Shift DC/DC Conv.
  - Resonant DC/DC Conv.
  - DC Link AC/AC Conv.
  - Matrix AC/AC Conv.
  - etc.

- Components
  - Power Semiconductor
  - Interconnections
  - Inductors, Transf.
  - Capacitors
  - Control Circuit
  - etc.

- Materials
  - Semiconductor Mat.
  - Conductor Mat.
  - Magnetic Mat.
  - Dielectric Mat.
  - etc.

→ Mapping of “Design Space” into System “Performance Space”
Mathematical Modeling of the Converter Design

Specifications $V_i, V_o, P_o, \Delta V_o, \text{CISPR 11/22 A,B}$

Converter Topology Modulation Scheme

Electric Power Circuit Model

Specifications $V_i, V_o, P_o, \Delta V_o, \text{CISPR 11/22 A,B}$

Converter Topology Modulation Scheme

Mathematical Modeling of the Converter Design

Multi-Objective Optimization – Best Utilization of All Degrees of Freedom
**Multi-Objective Optimization (1)**

- Ensures Optimal Mapping of the “Design Space” into the “Performance Space”
- Identifies Absolute Performance Limits → Pareto Front / Surface

→ Clarifies Sensitivity $\Delta \tilde{p} / \Delta \tilde{k}$ to Improvements of Technologies
→ Trade-off Analysis
Multi-Objective Optimization (2)

- Design Space Diversity
- Equal Performance for Largely Different Sets of Design Parameters

→ E.g. Mutual Compensation of Volume and Loss Contributions (e.g. Cond. & Sw. Losses)
→ Allows Optimization for Further Performance Index (e.g. Costs)
**Converter Performance Evaluation Based on $\eta$-$\rho$-$\sigma$-Pareto Surface**

- Definition of a Power Electronics "Technology Node" $\rightarrow (\eta^*, \rho^*, \sigma^*, f_p^*)$
- Maximum $\sigma$ [kW/\$], Related Efficiency & Power Density

→ Specifying Only a Single Performance Index is of No Value (!)
→ Achievable Perform. Depends on Conv. Type / Specs (e.g. Volt. Range) / Side Cond. (e.g. Cooling)
Multi-Objective Optimization
Application Examples

Comparative Converter Evaluation
Impact of Technology Progress
Design Space Diversity
Comparative Converter Evaluation
Wide Input Voltage Range
Isolated DC/DC Converter

Structure of “Smart Home” DC Microgrid

- Universal Isolated DC/DC Converter
  - Bidirectional Power Flow
  - Galvanic Isolation
  - Wide Voltage Range
  - High Partial Load Efficiency

Universal DC/DC Converter

- Advantages
  - Reduced System Complexity
  - Lower Overall Development Costs
  - Economies of Scale

\[ P_r = 5 \text{ kW} @ \eta_{\text{max}} > 98\% \]

\[ I_{\text{dc1,max}} = 22 \text{ A} \]

\[ V_{\text{dc1}} = [100, 700] \text{ V} \]

\[ V_{\text{dc2}} = 750 \text{ V} \]

DC Loads

DC Bus
Comparative Evaluation of Converter Topologies

- Conv. 3-Level Dual Active Bridge (3L-DAB)

- Advanced 5-Level Dual Active Bridge (5L-DAB)
Optimization Results - Pareto Surfaces

- 3-Level Dual Active Bridge
- 5-Level Dual Active Bridge

Switching Frequency $f_{sw}$ (kHz)

50 75 100 125 150 175 200 225

Average Efficiency $\eta_{avg}$ (%)

Power Density $\rho_{box}$ (kW/dm$^3$)

1 2 3 4 5 6

Watts per Euro $\sigma_P$ (W/€)

5 10 15 20

3L $\eta_{avg} - \rho_{box}$ PF

5L $\eta_{avg} - \sigma_P$ PF

5L $\sigma_P - \rho_{box}$ PF

$\sigma_P$ (W/€) $\rho_{box}$ (kW/dm$^3$)
Impact of Technology Progress & Design Space Diversity
**LiTTLE BOX CHALLENGE**

- Design / Build the 2kW 1-Φ Solar Inverter with the Highest Power Density in the World
- Power Density > 3kW/dm³ (50W/in³)
- Efficiency > 95%
- Case Temp. < 60°C
- EMI FCC Part 15 B

→ Push the Forefront of New Technologies in R&D of High Power Density Inverters
**Selected Converter Topology**

- Interleaving of 2 Bridge Legs per Phase
- Active DC-Side Buck-Type Power Pulsation Buffer
- 2-Stage EMI AC Output Filter

→ ZVS of All Bridge Legs @ Turn-On/Turn-Off in Whole Operating Range (4D-TCM-Interleaving)
→ Heatsinks Connected to DC Bus / Shield to Prevent Cap. Coupling to Grounded Enclosure
Little-Box 1.0 Prototype

- **Performance**
  - 8.2 kW/dm³
  - 96.3% Efficiency @ 2kW
  - $T_c=58^\circ C$ @ 2kW

- **Design Details**
  - 600V IFX Normally-Off GaN GIT
  - Antiparallel SiC Schottky Diodes
  - Multi-Airgap Ind. w. Multi-Layer Foil Wdg
  - Triangular Curr. Mode ZVS Operation
  - CeraLink Power Pulsation Buffer

→ Analysis of Potential Performance Improvement for Ideal Switches
Little Box 1.0 @ Ideal Switches (TCM)

- Multi-Objective Optimization of Little-Box 1.0 (X6S Power Pulsation Buffer)
- Step-by-Step Idealization of the Power Transistors
- Ideal Switches: $k_c = 0$ (Zero Cond. Losses); $k_s = 0$ (Zero Sw. Losses)

→ Analysis of Improvement of Efficiency @ Given Power Density & Maximum Power Density
→ The Ideal Switch is NOT Enough (!)
Little Box 1.0 @ Ideal Switches (PWM)

- **L** & **f<sub>S</sub>** are Independent Degrees of Freedom
- Large Design Space Diversity (Mutual Compensation of HF and LF Loss Contributions)

\[ \rho = 6 \text{ kW/dm}^3 \]
\[ \eta \approx 99.35\% \]
\[ L = 50 \text{ uH} \]
\[ f_S = 500 \text{ kHz or } 900 \text{ kHz} \]
Summary

Future Developments/Design Process
Future Research Topics
Power Electronics 2.0
Appendix
Future Developments

- **Megatrends** - Renewable Energy / Energy Saving / E-Mobility / “SMART” XXX
- **Power Electronics** will massively spread in applications

![Diagram showing technology push and market pull]

- **Technology Push**
  - WBG Semiconductors
  - Digital Control
  - Adv. Design & Packaging

- **Market Pull**
  - Standardized
  - 3-D Integrated
  - Reliable
  - Cost Optimized
  - Plug & Play
  - Environmentally Friendly

- More Application Specific Solutions
- Mature Technology - Cost Optimization @ Given Performance Level
- Design / Optimize / Verify (in Simulation) - Cheaper / Faster / Better
Future Design Process

- Main Challenges: Modeling (EMI, etc.) & Implementation in Industry

- Reduces Time-to-Market - Cheaper / Faster / Better
- Allows to Understand Mutual Dependencies of Performances / Sensitivities (!)
- Simulate What Cannot Any More be Measured (High Integration Level)
Power Electronics Technology S-Curve

“Passives”
+ $\eta$-$\rho$-$\sigma$-Design
+ Adv. Packaging
+ Systems

- Super-Junct. Techn. / WBG
- Digital Power
  Modeling & Simulation

- Power MOSFETs/IGBTs
- Microelectronics
  Circuit Topologies
  Modulation Concepts
  Control Concepts

SCRs / Diodes
Solid-State Devices

Performance

Emerging
Established
Mature

Effort / Time

2015
2025

Paradigm Shift

ETH Zürich

Power Electronics Workshop 2016
Summary

- **Advantages**
  - Design / Optimize / Verify - All in Simulation
  - Provide a Fully Virtual Design for Fully Automated Manufacturing
  - Reduce Design Period from Weeks to Hours (Factor >100)
  - Directly Build Systems from Optimiz. Results (3D Printing etc.)
  - Pre-Analyze Improvement by New Technologies (“Research Efficiency”)
  - Optimize over Extreme Span (Semicond. Doping to Conv. Mission Profile)
  - Free Adjustment of Optimization Criteria (Design on Demand)

- **Research Topics**
  - Reduced Order Models / Model Accuracy
  - Opt. Combination of Analytical & FEM Models
  - Partitioning of Optimiz. (Local/Global Variables & Optimiz. etc.)
  - Selection of Abstraction Level / Timescale /
  - Translation of Geometries into Model Parameters (e.g. EMI)
  - Consideration of Geometric Limitations (Design for Manufact.)
  - New Models for Highly Integr. Converters (Strong EM & Therm. Coupl.)
  - Convergence of Simulations & Measurements (Autom. Param. Adj.)
  - Visualization of Optim. Results / Interfaces (Programming & Results)

- **Challenges**
  - Introduction in Industry (and Academia ;-))
  - Company-Wide Updates / Maintenance
  - Integration in “Virtual Prototyping” Environment

- **Limitations**
  - Simulation Extends the Knowledge Space ... But,...
  - Cannot Create Fundamentally New Concepts (!)
Future Paradigm Shift
Power Electronics 2.0

- Design Considering Converters as “Integrated Circuits” (PEBBs)
- Extend Analysis to Converter Clusters / Power Supply Chains / etc.

- “Converter” → “Systems” (Microgrid) or “Hybrid Systems” (Automation / Aircraft)
- “Time” → “Integral over Time”
- “Power” → “Energy”

\[ p(t) \rightarrow \int_{0}^{t} p(t) \, dt \]

- Power Conversion → Energy Management / Distribution
- Converter Analysis → System Analysis (incl. Interactions Conv. / Conv. or Load or Mains)
- Converter Stability → System Stability (Autonom. Cntrl of Distributed Converters)
- Cap. Filtering → Energy Storage & Demand Side Management
- Costs / Efficiency → Life Cycle Costs / Mission Efficiency / Supply Chain Efficiency
- etc.
New Power Electronics Systems Performance Figures/Trends

- Power Density [kW/m²]
- Environm. Impact [kWs/kW]
- TCO [$/kW]
- Mission Efficiency [%]
- Failure Rate [h⁻¹]
Thank You!
Appendix #1

Determination of the $\eta$-$\rho$-Pareto Front
Determination of the $\eta$-$\rho$-Pareto Front (1)

- Comp.-Level Degrees of Freedom of the Design
  - Core Geometry / Material
  - Single / Multiple Airgaps
  - Solid / Litz Wire, Foils
  - Winding Topology
  - Natural / Forced Conv. Cooling
  - Hard-/Soft-Switching
  - Si / SiC
  - etc.
  - etc.
  - etc.

- System-Level Degrees of Freedom
  - Circuit Topology
  - Modulation Scheme
  - etc.
  - etc.
  - etc.

- Only $\eta$-$\rho$-Pareto Front Allows Comprehensive Comparison of Converter Concepts (!)
Determination of the $\eta$-$\rho$-Pareto Front (1)

- Specific Design $\rightarrow$ Only $f_p$ as Variable Design Parameter
- Only the Consideration of All Possible Designs / Degrees of Freedom Clarifies the Absolute $\eta$-$\rho$-Performance Limit

$\star$ $f_p = 100\text{kHz}$
Appendix #2

Performance & Life-Cycle-Costs of SiC vs. Si
Multi-Objective $\eta - \rho - \sigma$-Comparison of Si vs. SiC

- Three-Phase PV Inverter System
  - Single-Input/Single-MPP-Tracker Multi-String PV Converter
  - DC/DC Boost Converter for Wide MPP Voltage Range
  - Output EMI Filter
  - Typical Residential Application

$P_t = 10\, \text{kW}$

$V_{m_{pp}} = [400, 800] \, \text{V}$

$\hat{V}_g = (325 \pm 10\%) \, \text{V}$

- Exploit Excellent Hard- AND Soft-Switching Capabilities of SiC
- Find Useful Switching Frequency and Current Ripple Ranges
- Find Appropriate Core Material
Topologies - Converter Stages

- **Si IGBT 2L-PWM Inverter**

- **SiC MOSFET 2L-PWM Inverter**

- **SiC MOSFET Interleaved 2L-TCM Inverter**
Optimization Results - Pareto Surfaces

- No Pareto-Optimal Designs for $f_{sw,\text{min}} > 60$ kHz
- No METGLAS Amorphous Iron Designs
- Pareto-Optimal Designs for Entire Considered $f_{sw}$ Range
- No METGLAS Amorphous Iron Designs
- Pareto-Optimal Designs for Entire Considered $f_{sw}$ Range
- METGLAS Amorphous Iron and Ferrite Designs
Optimization Results – Investigations Along Pareto Surfaces

- Comparison of the Inverter Concepts
  - 2L-TCM
  - 2L-PWM
  - 3L-PWM

→ Semiconductor Losses Clearly Dominating (35...70%)
Extension to Life-Cycle Cost (LCC) Analysis

- **Performance Space Analysis**
  - 3 Performance Measures: $\eta$, $\rho$, $\sigma$
  - Reveals Absolute Performance Limits / Trade-Offs Between Performances

- **LCC Analysis**
  - Post-Processing of Pareto-Optimal Designs
  - Determination of Min.-LCC Design
  - Arbitrary Cost Function Possible

→ Which is the Best Solution Weighting $\eta$, $\rho$, $\sigma$, e.g. in Form of Life-Cycle Costs (LCC)?
→ How Much Better is the Best Design?
→ Optimal Switching Frequency?
**Post-Processing**

- **LCC – Analysis**

  - Best System – 2L-PWM SiC Converter @ 44kHz & 50% Ripple
    - 22% Lower LCC than 3L-PWM
    - 5% Lower LCC than 2L-TCM
    - Simplest Design
    - Probably Highest Reliability
    - Lower Vol. (Housing) Not Yet Considered!

  → Application of SiC Justified on “System Level”