Power Electronic Systems Laboratory

ETH zürich

FCCee CPES

Cryogenic Power Electronic Supply for Cryo-Cooled HTS Magnet Systems

J. Huber, D. Zhang, M. Akbas, E. Bürgisser, D. Cao, J. W. Kolar

Power Electronic Systems Laboratory
ETH Zürich

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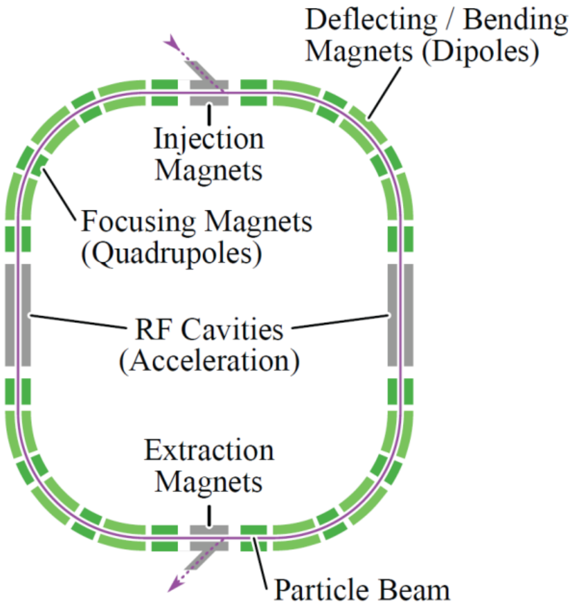
CHART
Swiss Accelerator Research and Technology

Motivation

- LHC electricity consumption: 750 GWh/a (equiv. of 150’000 Swiss households)
- LHC employs room-temp. magnets (conduction losses) and 1.9-K magnets (cryocooler power)
- FCC circumference 100 km vs. 27 km of LHC / Energy efficiency is one FCC design objective



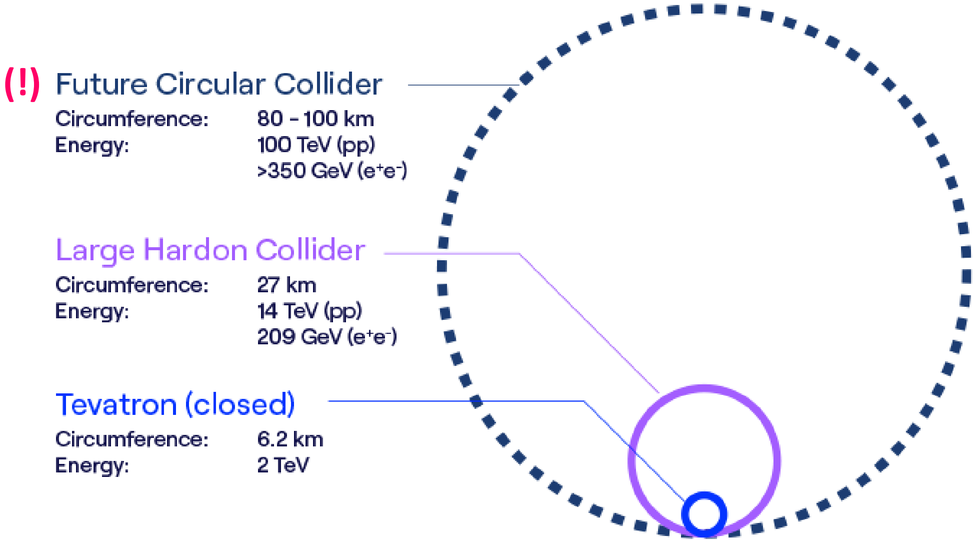
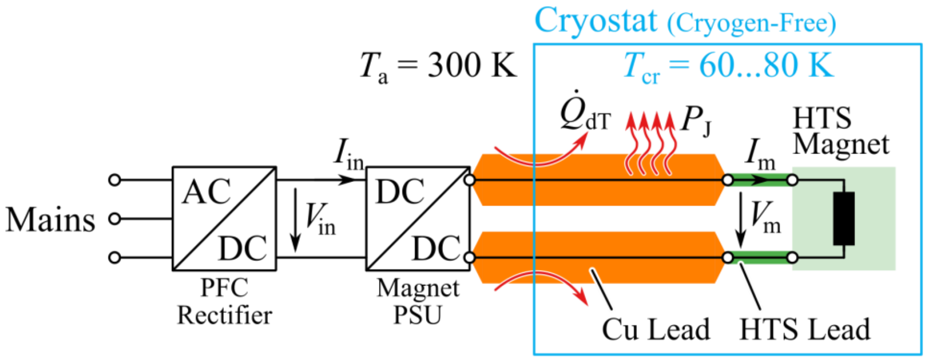


Image: CERN / fcc.web.cern.ch/overview

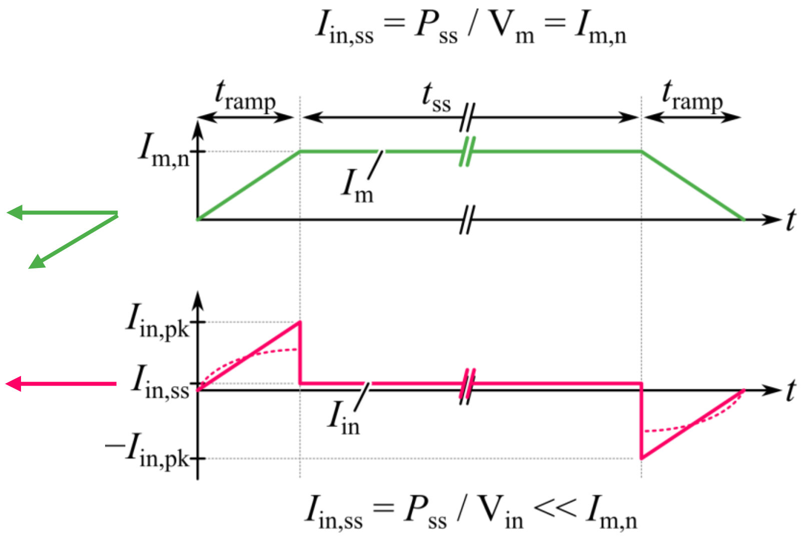
- High-temperature superconducting (HTS) magnets at about 40 K → FCCee HTS4: 250-A HTS Magnet

Concept

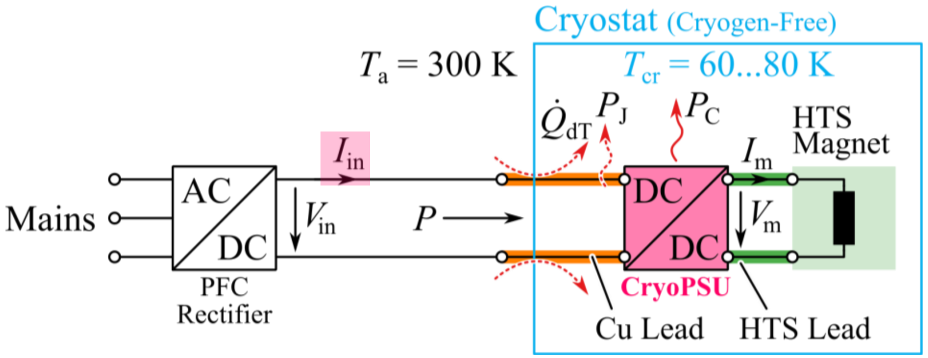
■ Conventional: Power supply unit (PSU) at room-temperature



- **Minimum leak-in losses: 21 W** (250 A, 300 K to 60 K, opt. *L*/*A* leads)



■ CryoPSU: DC-DC stage *inside* of the cryostat / $V_{in} >> V_m$



- **Target total losses: 5…6 W (!)** (Leak-in plus converter losses)

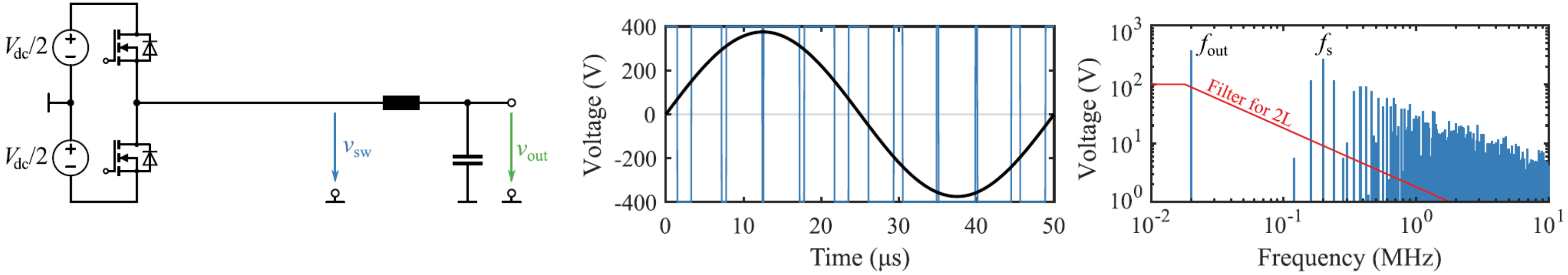
- Extracting 1 W of losses requires about 20 W of cryocooler power (60 K to 300 K) [1] → Ultra-low losses!

[1] S. Büttner and M. März, "Profitability of low-temperature power electronics and potential applications," *Cryogenics*, vol. 121, p. 103392, Jan. 2022.

“Power Electronics in a Nutshell”

■ **Transistor half-bridge switching stage + output filter:**

- Switch-mode operation: Transistor *on* OR *off* => Low losses / Switching-frequency harmonics (noise)



■ **Interleaving instead of hard paralleling: Reduce conduction losses / Increase filter cutoff frequency**

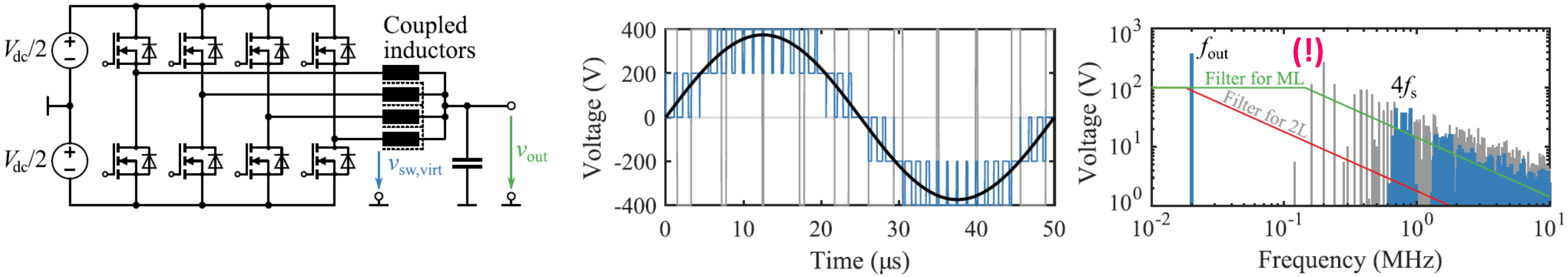
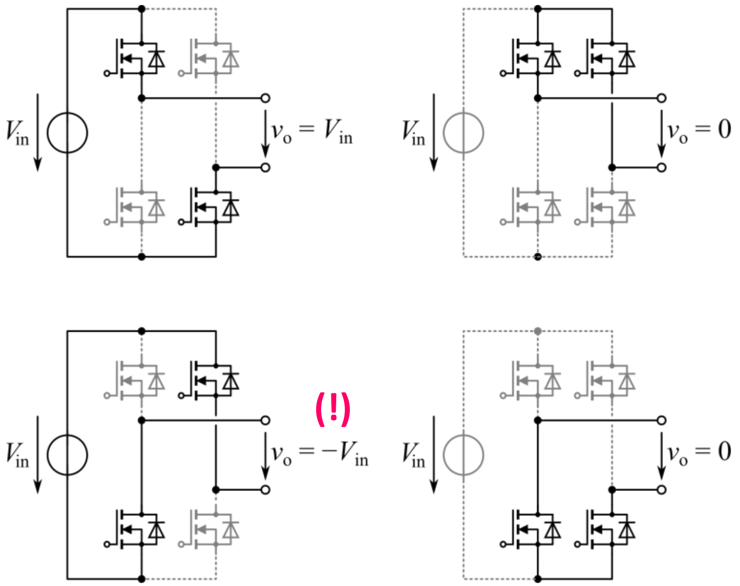
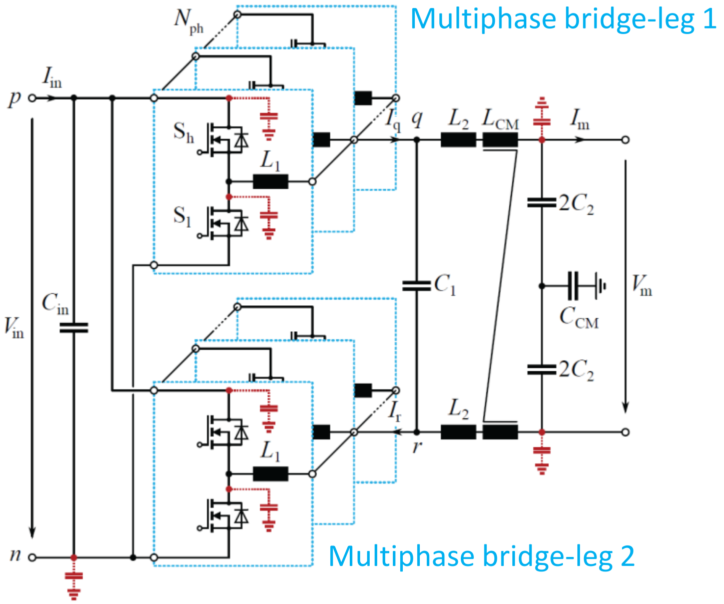


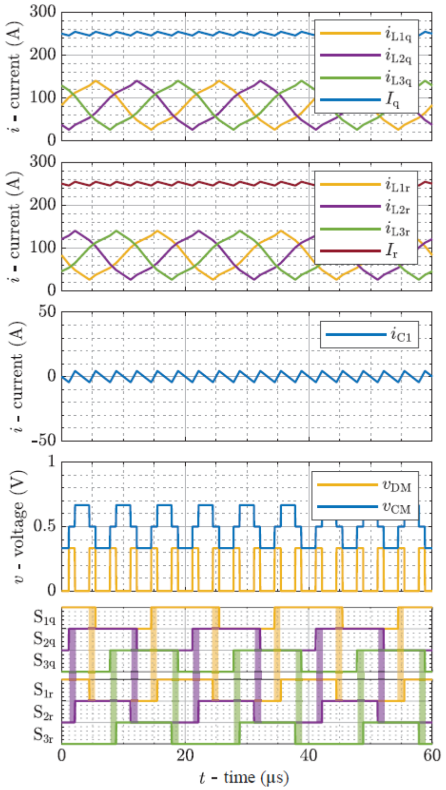
Figure from J. Böhler, J. Huber, et al., “Ultra-High-Bandwidth Power Amplifiers: A Technology Overview and Future Prospects,” *IEEE Access,* vol. 10, pp. 54613–54633, 2022.

Converter Topology

- **Full-bridge with multiphase bridge legs (current sharing / interleaving) / EMI filter (strict CERN EMI limits)**

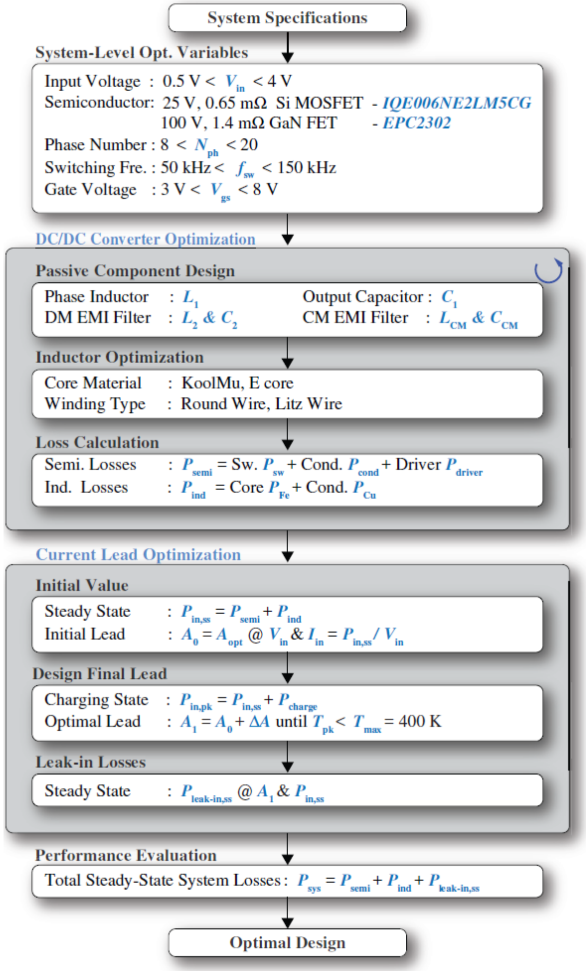






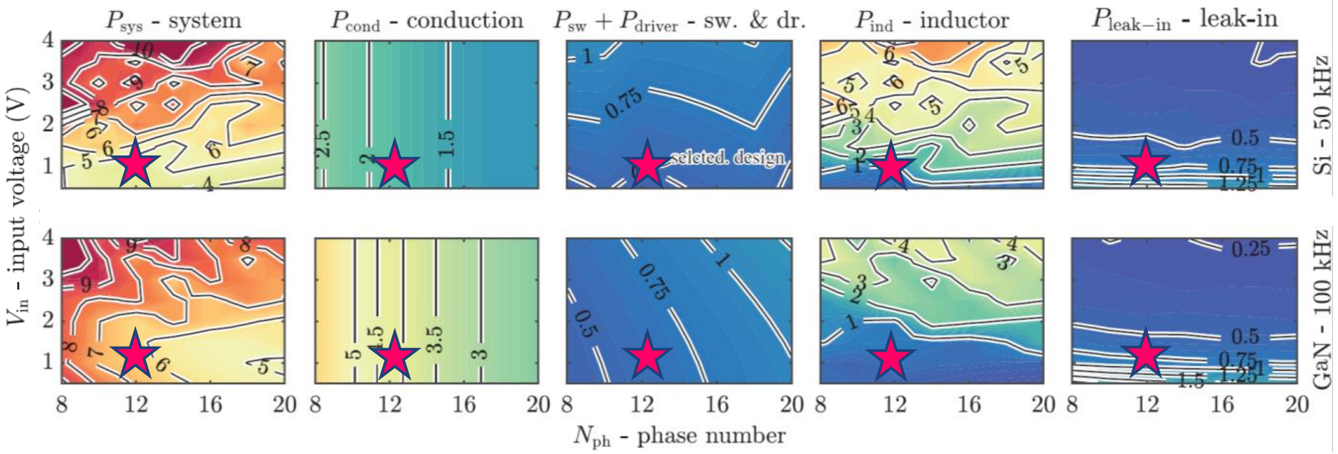
- **Key degrees of freedom with preliminary values**
  - V_{in} ≈ 1…2 V — galvanic isolation required; *not* in cryostat
  - N_{phase} ≈ 8…12 — per bridge leg
  - f_{sw} ≈ 50….100 kHz — per bridge leg

Optimization Framework



- **Specifications** (250 A, 60 K, 500 mH, 1000 s ramp-up, …)
- **Constraints** (EMI Limits from CERN, …)
- **Degrees of freedom** (switching frequency, # phases, transistors, gate volt., …)

- **Loss models for key components** (transistors, inductors, current leads, …)



25-V Silicon Transistors

100-V GaN Transistors

- 25-V silicon transistors: Lowest on-state resistance per package but low-temp. behavior (carrier freezeout) to be verified!

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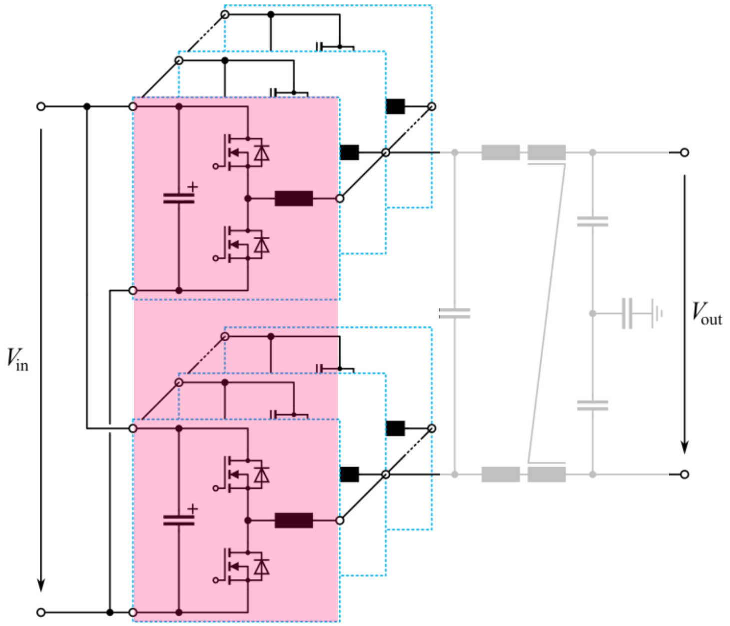
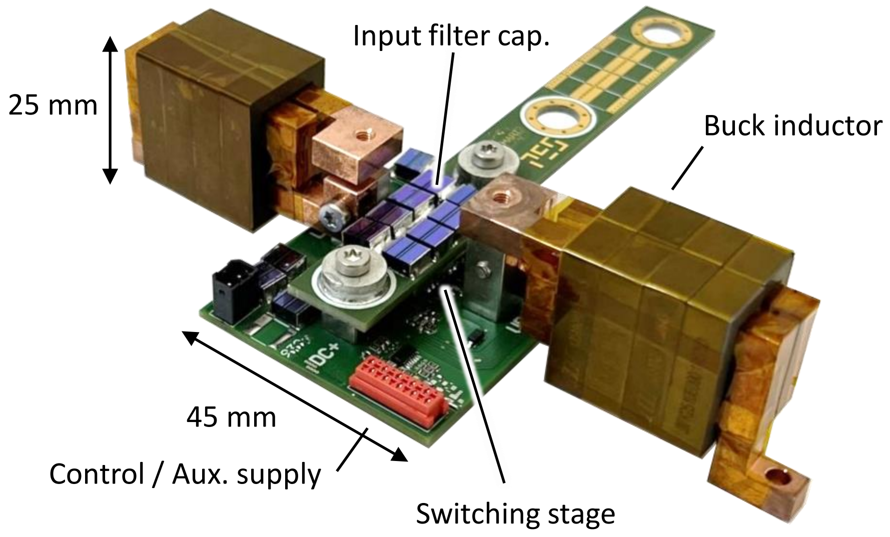
Further reading: D. Cao, D. Zhang, J. W. Kolar, and J. Huber, "Conceptualization of a cryogenic 250-A power supply for high-temperature-superconducting (HTS) magnets of future particle accelerators," in *Proc. 11th Int. Conf. Power Electron. (ICPE – ECCE Asia)*, Jeju, Korea, May 2023, pp. 688–696.

Silicon-Based Phase Module Demonstrator (1)

- **250 A using 12 Phases with 21 A current each / Phase module sufficient as PoC for loss targets (!)**

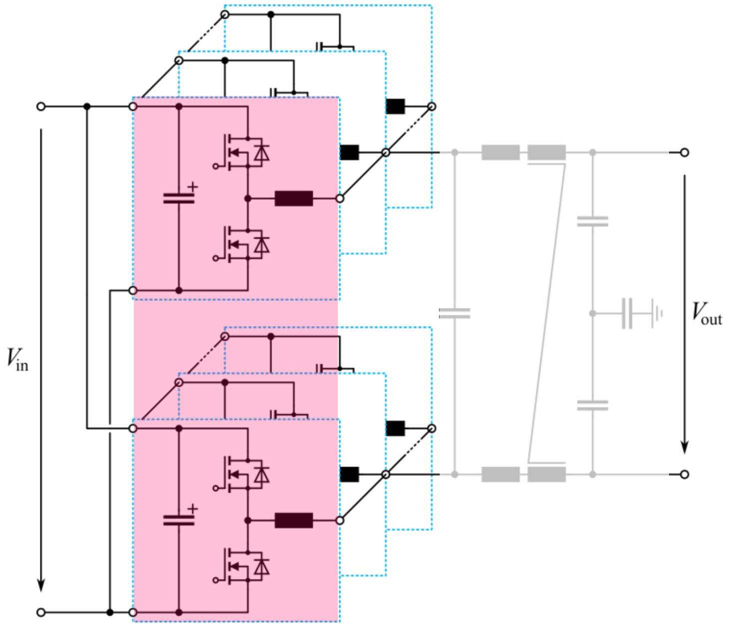


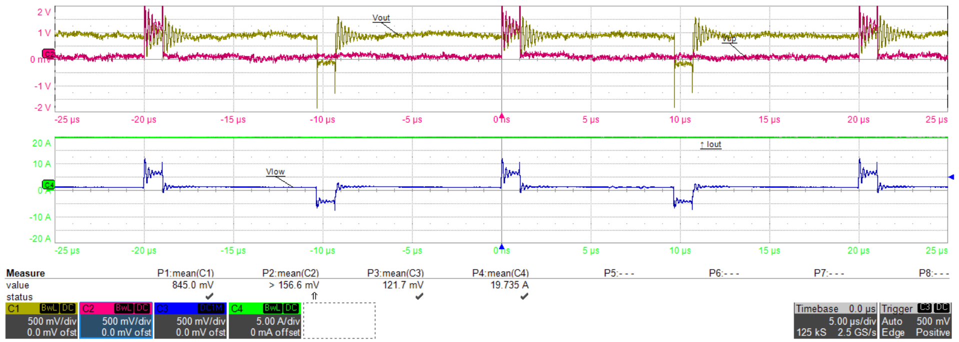


- **Transistor full bridge + Phase inductors / 1 V dc input, 21 A output current / 25-V Si MOSFETs (IQE006NE2LM5)**

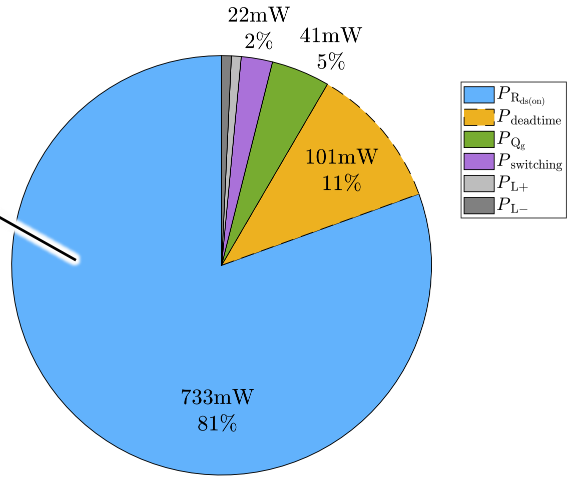
Silicon-Based Phase Module Demonstrator (2)

- **Testing in LN$_2$ @ 77 K / 1 V dc input, 21 A output current / 50 kHz switching frequency**





(!) Transistor conduction losses

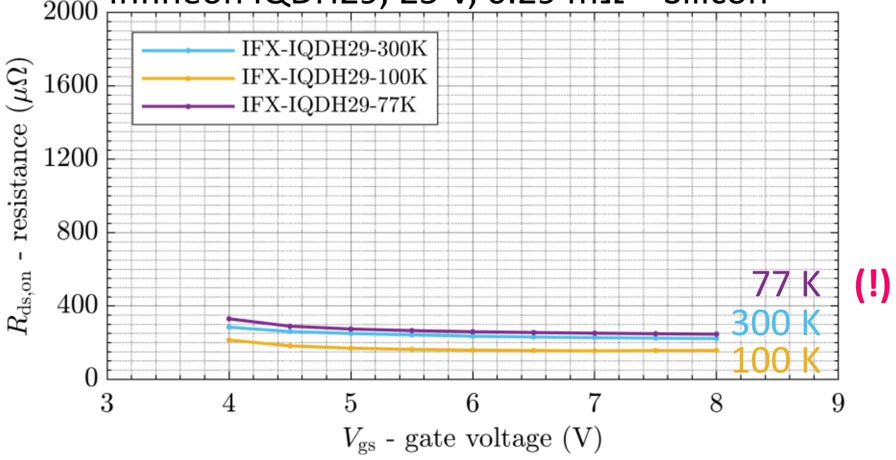


- **Calculated losses: 920 mW**
- **Measured losses: 945 ± 12 mW**

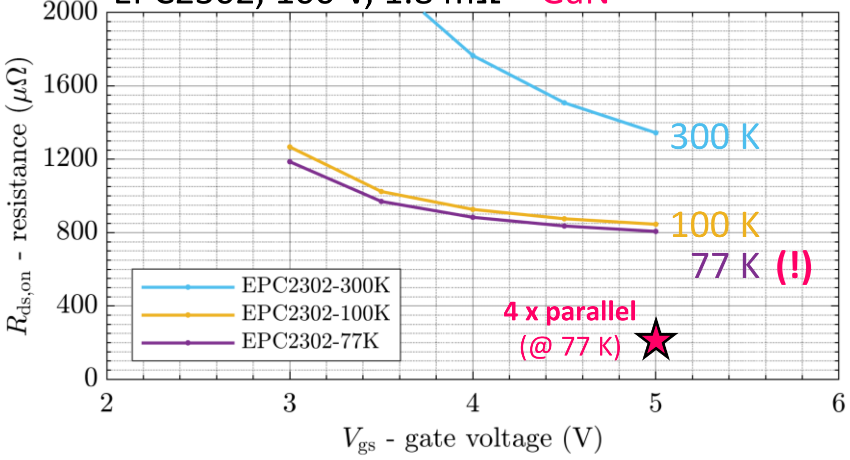
GaN-Based Phase Module Demonstrator (1)

- **Low-voltage silicon transistors: Lowest on-state resistance per package / Carrier freezeout < 100 K**

Infineon IQDH29, 25 V, 0.29 mΩ – Silicon



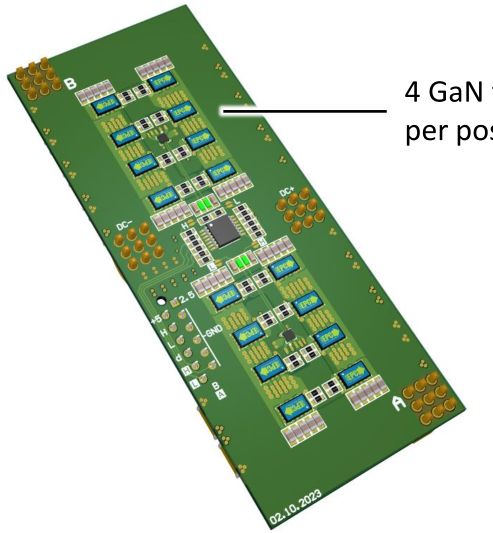
EPC2302, 100 V, 1.8 mΩ – GaN

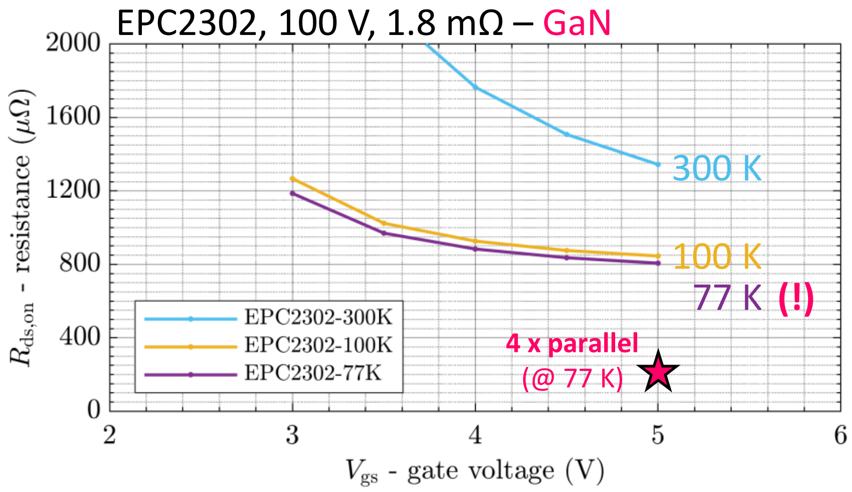


- **Alternative: Paralleling of 4 GaN transistors per position**

GaN-Based Phase Module Demonstrator (2)

- **Low-voltage silicon transistors: Lowest on-state resistance per package / Carrier freezeout < 100 K**



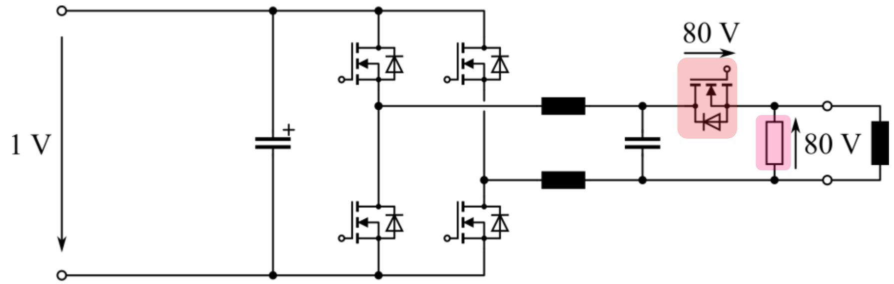


- **Alternative: Paralleling of 4 GaN transistors per position**
- **Expected total power-stage losses of about 4 W (w/o control electronics) vs. 5…6 W overall target**
  - Experimental verification in October

Remark: Integration of Quench Protection

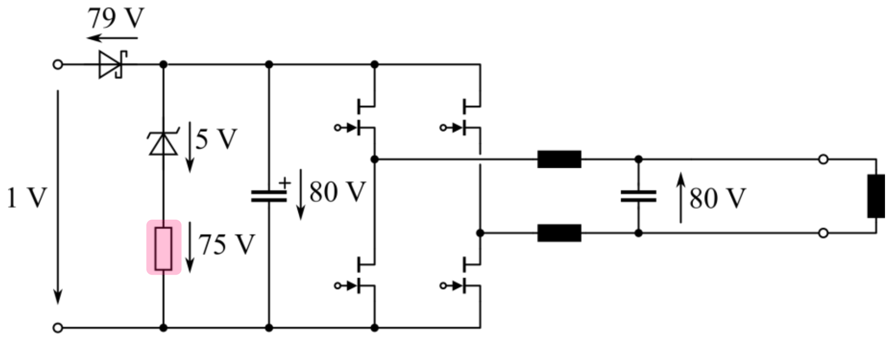
- Quench protection: Fast extraction of magnet energy requires min. 80 V / Decoupling of 25-V power stage!

25-V Si Power Stage



- Series 250-A disconnect switch
- + x W losses in normal operation

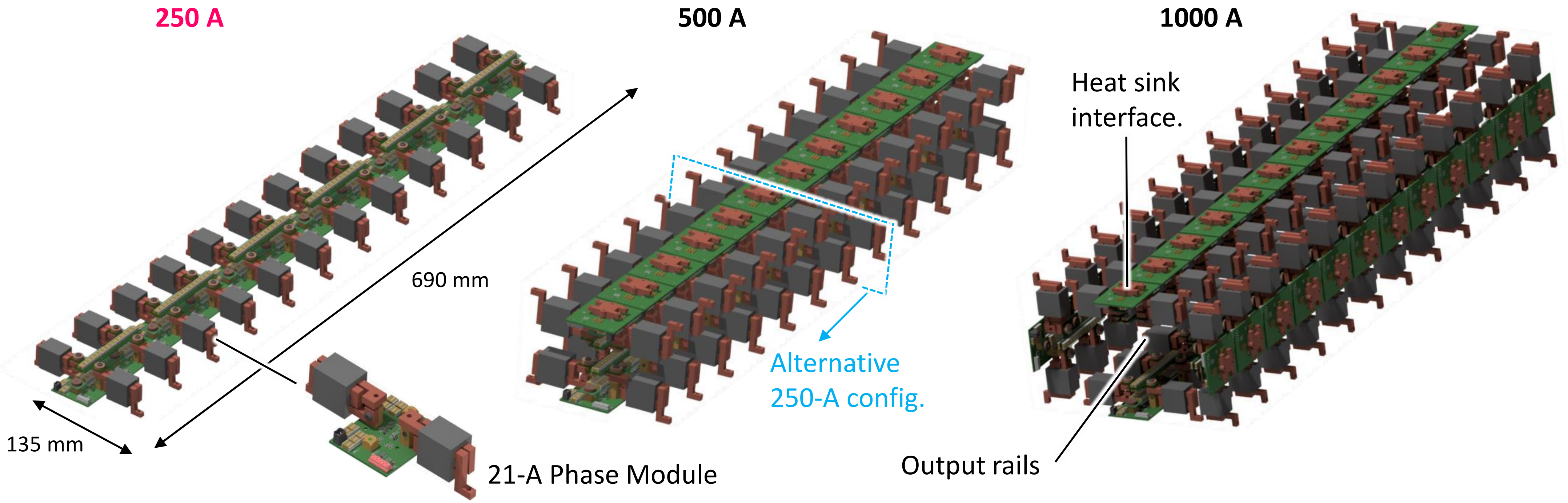
100-V GaN Power Stage



- Dump resistor parallel to dc input
- + 0 W losses in normal operation
- Dump resistor *outside* of cryostat possible

Outlook

- Demonstration of feasibility (5…6 W loss target) with GaN-based phase module
- Demonstration of low-temperature control platform / Control of phase current sharing
- Demonstrator with 3+ phase modules / In-vacuum tests @ PSI



- Modularity facilitates scalability and reliability through redundancy

Thank you!