New single-stage bidirectional three-phase ac-dc solid-state transformer

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High-power applications with low-voltage (LV) dc loads, for example, fast charging stations for electric vehicles (EVs), are typically supplied from the medium-voltage (MV) grid. Aiming for low volume, MVac-LVdc solid-state transformers (SSTs) that provide galvanic separation with medium-frequency transformers (MFTs) are thus considered, which are conventionally realized as two-stage systems that consist of an ac-dc power-factor-correction (PFC) rectifier and an isolated dc-dc converter. This letter extends a new single-stage isolated bidirectional PFC rectifier concept to MV levels, resulting in an SST that performs MVac-LVdc conversion in a single converter stage and, unlike many modular SST concepts, employs only a single MFT. The SST's primary side operates modular-multilevel-converter (MMC) bridge legs, whose input voltages contain large ac components, in the quasi-two-level mode to minimize the cell capacitors. The secondary side employs a standard LV three-phase rectifier, and a dual-active-bridge-(DAB)-like modulation strategy allows power flow regulation and ensures sinusoidal grid currents. The concept is explained and validated using detailed circuit simulations of an exemplary 1-MW system operating between a 10-kV three-phase grid and an 800-V dc output. The component stresses are evaluated, and an efficiency of 98.1% and a power density of up to 0.6 kW/dm^3 are estimated.

Introduction: Low-voltage dc (LVdc) applications with high power demand in the megawatt range are typically supplied from the medium-voltage (MV) three-phase mains. Conventionally, a low-frequency, that is, grid-frequency transformer (LFT) provides galvanic separation and steps down the MVac voltage to low-voltage ac (LVac) levels like 400 or 690 V. The subsequent power-factor-correction (PFC) rectifier is then not exposed to MV, but, on the other hand, the LFT's relatively large volume might limit the overall power density. To enable more compact system realizations and/or to provide extended functionality [1], MVac-LVdc solid-state transformers (SSTs) employing medium-frequency transformers (MFTs) instead of LFTs are considered for applications like EV charging [2–11], electrolyzers [12], and future datacenters [13–15].

Historically, the limited blocking voltage of power semiconductors naturally led to multi-cell converter structures, where several isolated ac–dc converter cells are configured in an input-series, output-parallel (ISOP) structure [16, 17]. However, then each cell contains an MFT that must provide the full isolation voltage rating and hence requires, for example, large bushings. The availability of high-voltage (HV) SiC transistors with blocking voltages of 10 kV extends the applicability of well-known isolated power supply topologies to at least lower MV levels, but whereas then only a single MFT is needed, still typically two power conversion stages (PFC rectifier and isolated dc–dc converter) are used [18]. Alternatively, single-stage MVac-LVdc SST topologies with an MV-side modular multilevel converter (MMC) that directly converts an LF ac three-phase voltage system to a single-phase MF voltage applied to the primary side of a single MFT have been proposed in the 2000s [19] and are currently considered again [6]. The converter cells of the MMC ac–ac front-end, however, require large capacitors to buffer the inherent LF power fluctuations. Another recently presented single-stage MVac-LVdc SST topology [20] is limited to unidirectional power flow but interestingly extends a known single-stage PFC rectifier topology to MV input by replacing a standard *two-transistor* half-bridge with a *two-arm* MMC structure that operates in the quasi-two-level (Q2L) mode.

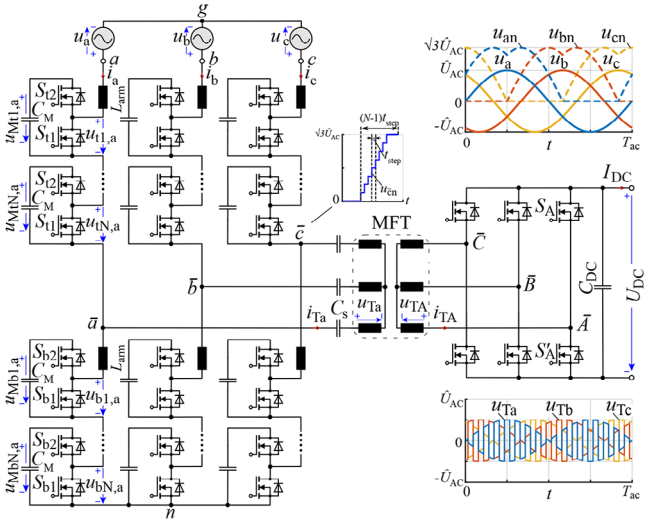

Fig. 1 *Main power circuit of the proposed single-stage medium-voltage ac (MVac) to low-voltage dc (LVdc) solid-state transformer (SST), which is an extension of [37] to MVac input using quasi-two-level (Q2L) modular multilevel converter (MMC) bridge legs, each with N series-connected half-bridge cells in the top and the bottom arm, respectively. The corresponding main converter waveforms within one grid period $T_{AC} = 1/f_{AC}$ are indicated, that is, the grid voltages u_a, u_b, u_c (with amplitude $\hat{U}_{AC} = \sqrt{2/3}U_{LL}$), the converter input voltages u_{an}, u_{bn}, u_{cn} referred to the primary-side converter star point n, and the primary-side medium frequency transformer (MFT) voltages u_{Ta}, u_{Tb}, u_{Tc}. Note that, alternatively, the arms could be realized with N/2 full-bridge cells*

The Q2L operating mode has initially been proposed for diode-clamped converters [21, 22] and then also been applied to flying-capacitor bridge legs [23–26] and to MMC bridge legs [27–33] (note that a similar concept is known as "integrated capacitor-blocked transistor cells" [34–36]). Essentially, Q2L operation employs the available intermediate voltage levels of the multilevel converter structure only very briefly during the transitions between a high and a low output voltage level; for example, the output node is connected to either of the Q2L-MMC bridge leg's two input terminals for most of the time; see also Figure 1. Whereas this forgoes the improved harmonic performance otherwise achieved by multilevel converters, the energy storage elements needed for providing the intermediate voltage levels, that is, the cell capacitors in the case of Q2L MMC bridge legs, can be reduced, and the du/dt of the staggered transitions of the quasi-two-level output voltage waveform is advantageously still limited.

Using such Q2L MMC bridge legs, this letter extends a recently published single-stage bidirectional isolated three-phase buck-boost PFC rectifier concept for LVac to LVdc conversion [37], which employs standard half-bridge transistor arrangements on the ac-side and on the dc-side, to MVac input. Figure 1 shows the thus proposed SST topology, which advantageously features single-stage ac–dc power conversion, supports bidirectional power flow, minimizes the stored energy in the MMC bridge legs, and requires only a single MFT.

Basic operating principle: The proposed topology shown in Figure 1 comprises three Q2L MMC bridge legs, each with N series-connected half-bridge cells in the top and the bottom arms. With the considered Q2L modulation [27–33] all cells of the top arm are either bypassed (main switch $S_{t1} = 1$, auxiliary switch $S_{t2} = 0$) or inserted (main switch $S_{t1} = 0$, auxiliary switch $S_{t2} = 1$) during most part of the switching period T_s, while the cells of the bottom arm are switched complementarily, that is, the switch node $\bar{a}$ is connected to either the grid terminal a or to the converter star point n. The switching states of an arm's individual cells only differ during the short (i.e., $(N-1) \times t_{step} \ll T_s$) staggered switching transitions. Because the cell capacitors C_M are thus not subject to an LF energy buffering requirement (as in conventionally operated MMCs such as [6, 19]), small capacitances C_M are sufficient to maintain cell voltage balancing.

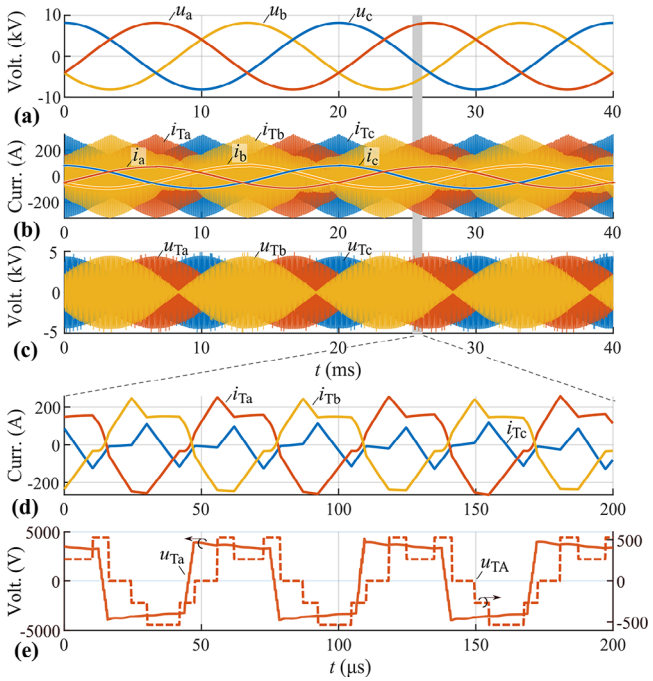

Fig. 2 *Exemplary simulation waveforms of the proposed SST from Figure 1 operating at nominal conditions (see Table 1): (a) Grid voltages (u_a, u_b, u_c); (b) LF components of the grid currents (i_a, i_b, i_c) and transformer primary-side currents (i_{Ta}, i_{Tb}, i_{Tc}); (c) transformer primary-side voltages (u_{Ta}, u_{Tb}, u_{Tc}); (d) transformer currents (zoomed, i_{Ta}, i_{Tb}, i_{Tc}); (e) primary-side and secondary-side transformer voltages of phase* a *(zoomed, u_{Ta}, u_{TA})*

Further, the MVac front-end's Q2L output voltage waveforms are essentially identical to those of an LVac-LVdc system using two-transistor bridge legs (i.e., half bridges) [37]; hence, the same operating and modulation concepts are applicable and are therefore only briefly outlined here. The ac front-end converts the LF grid voltages u_a, u_b, u_c into MF amplitude-modulated differential-mode (DM) transformer voltages u_{Ta}, u_{Tb}, u_{Tc} (with peak amplitudes of up to $\pm 1/2\,\hat{U}_{AC}$, see Figure 1) by synchronously switching the three arms of the ac-side Q2L-MMC front-end with a constant 50% pulse-width modulation (PWM) duty cycle; note that series capacitors C_s are necessary to block the LF components of the resulting switch-node voltages. The common-mode (CM) offset voltage between the converter star point n and the grid star point g does not impact the generated (DM) transformer voltages [37] and is, therefore, a degree of freedom to ensure strictly positive arm voltages u_{an}, u_{bn}, u_{cn} (required as the top S_t and bottom arm switches S_b have unipolar voltage blocking capability only, that is, the arm voltages cannot be negative). Here, a suitable CM voltage offset results from clamping the input terminal of the phase with the instantaneously lowest grid voltage to the converter star point n during 120° intervals of the grid period T_{AC}, which is achieved by simultaneously bypassing all cells of both the top and the bottom arm (i.e., $S_{t1} = S_{b1} = 1$) of the respective phase. This results in a discontinuous PWM (DPWM) operation where the maximum arm blocking voltage $\hat{u}_{an}$ is limited to the MV grid line-to-line voltage amplitude (see Figure 1).

Figure 2a–e show simulated key waveforms that further illustrate the operating principle. The secondary-side rectifier is operated as in [37] and realizes sinusoidal grid currents i_a, i_b, i_c (Figure 2b), in phase with the grid voltages u_a, u_b, u_c, using the space-vector PWM (SVPWM) from [38]. The power flow from the grid P is then regulated by the PWM carrier phase-shift $\varphi \in [-\pi/2, \pi/2]$ between the primary-side Q2L MMC front-end and the secondary-side rectifier, similar to a dual-active-bridge (DAB) converter. The relationship can be approximated as

$$P(\varphi) \approx \frac{6}{\pi^4} \frac{\hat{U}_{AC} U'_{DC}}{f_s L_s} \sin(\varphi) \sin\left(\frac{\sqrt{3}\pi}{4} \frac{\hat{U}_{AC}}{U'_{DC}}\right), \tag{1}$$

with the switching frequency f_s, the transformer leakage inductance L_s, and $U'_{DC} = k_{MFT} U_{DC}$ representing the DC output voltage referred to the primary side. Note that the phase shift between primary-side voltage and secondary-side voltage is clearly visible in Figure 2d,e, where the transformer currents and voltages (phase a only) are shown over a few switching periods.

Table 1. Exemplary specifications

Description	Symbol	Value
Grid voltage (line-to-line rms)	U_{LL}	10 kV
Grid frequency	f_{AC}	50 Hz
Nominal power	P_N	1 MW
DC output voltage	U_{DC}	800 V

Table 2. Key system parameters

Description	Symbol	Value
Switching frequency	f_s	16 kHz
MFT turns ratio (primary: secondary)	k_{MFT}	12:1
MFT leakage inductance (primary side)	L_s	162 μH
LF blocking series capacitance	C_s	6 μF
Number of cells per top/bottom arm	N	7
MMC cell capacitance	C_M	1 μF
MMC cell nominal peak voltage	$\hat{u}_M$	2 kV
Effective top/bottom arm inductance	L_{arm}	3.5 μH
Prim. side power transistors	S_{tx}, S_{bx}	3.3 kV SiC
Sec. side power transistors	S_X, S'_X	1.2 kV SiC

Design aspects: The design of the proposed SST is exemplified for the specifications from Tables 1 and 2. First, the MFT turn ratio $k_{MFT} = 12$ is selected to match the primary-side-referred output voltage $U'_{DC} = 9.6$ kV to the primary-side transformer voltages (see Figures 1 and 2e). Considering a switching frequency of $f_s = 16$ kHz (at the boundary of the audible range) and targeting a nominal PWM phase-shift angle of $\varphi_N = \pi/4$, (1) can be solved for the required transformer leakage inductance as $L_s = 162$ μH (note that also an explicit series inductor could be placed in case the MFT's leakage inductance is too small). The series (LF-blocking) capacitor C_s is sized such that its impedance is about an order of magnitude smaller than the impedance of the leakage inductance L_s at the switching frequency and $C_s = 6$ μF is selected here.

As highlighted in Figure 1, the employed DPWM of the ac front-end results in a maximum arm voltage $\hat{u}_{an} = \sqrt{3}\hat{U}_{ac} = 14.1$ kV which is equally shared by the N series connected cells of the top and bottom arm, respectively (i.e. the time-varying capacitor voltage of an exemplary cell is $u_{Mt1,a} = u_{an}(t)/N$, see Figure 1). For a realization with 3.3 kV SiC MOSFETs (alternatively, 3.3 kV Si IGBTs could be employed), $N = 7$ cells per arm are required to limit the maximum cell voltage (nominal operation) to $\hat{u}_{Mt1,a} = 2$ kV, which ensures a sufficient (30%) blocking voltage margin even for a cell voltage deviation of +10%. With the Q2L operation of the ac front-end, the converter cells' capacitors are only subject to a notable current flow during the brief staggered switching transitions (but not during the majority of the switching period where the switch node $\bar{a}$ is either connected to the phase terminal a or to the star point n). Thus, the required cell capacitance can be calculated according to [26], using a peak-to-peak voltage ripple criterion $\Delta U_{C,pp}$, as

$$C_M = \frac{I_{Ta,sw,max}(N-1)t_{step}}{\Delta U_{C,pp}}, \tag{2}$$

where $I_{Ta,sw,max} = 120$, A is the maximum transformer current switched by the primary-side Q2L MMC bridge legs (obtained from circuit simulations). Employing SiC MOSFETs allows for a low step time (i.e. the time each intermediate voltage level appears during the staggered switching transition, see Figure 1) of $t_{step} = 500$ ns (several μs would be required in the case of IGBTs due to the slower switching speeds and hence longer interlock delay times [27, 30]). Further,

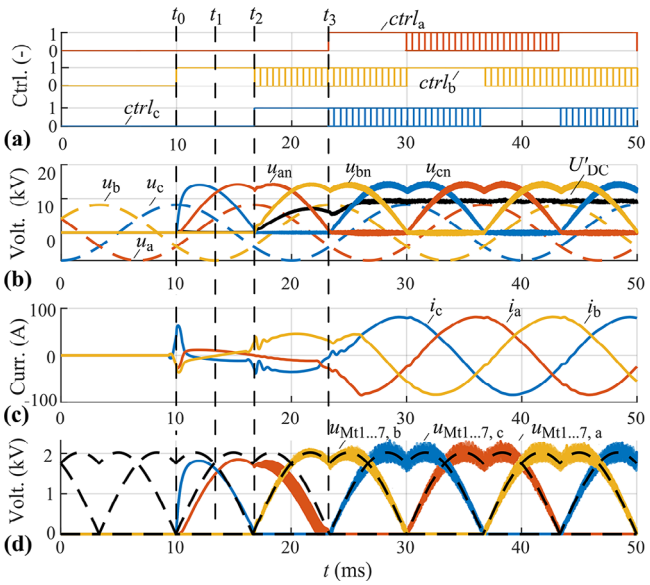

Fig. 3 *Simulated converter waveforms during the proposed start-up sequence, which ensures limited blocking voltage stress for the converter cells' transistors: (a) Control signals for the quasi-two-level (Q2L) modular multilevel converter (MMC) bridge legs, where 0 indicates all cells of both arms are inserted, 1 indicates the discontinuous pulse-width modulation (DPWM) clamping interval (i.e., all cells of both arms are bypassed), and toggling between 0 and 1 indicates normal 50%-duty PWM operation of the corresponding bridge leg; (b) grid voltages u_a, u_b, u_c, converter input voltages u_{an}, u_{bn}, u_{cn} and primary-side-referred dc output voltage U'_{DC}; (c) low-frequency (LF) components of the grid currents i_a, i_b, i_c; (d) top arm cell capacitor voltages $u_{Mt1,a} \dots u_{Mt7,a}$, $u_{Mt1,b} \dots u_{Mt7,b}$, $u_{Mt1,c} \dots u_{Mt7,c}$ with the corresponding cell voltage reference values $u_{an}(t)/N$, $u_{bn}(t)/N$, $u_{cn}(t)/N$ highlighted with a dashed line. Note that the startup simulation considers a simplified LC grid filter with a capacitance of 1.1 μF and an inductance of 11 mH per phase*

considering a permissible maximum peak-to-peak capacitor voltage variation of $\Delta U_{C,pp} = 400$ V (20% of the nominal peak cell voltage $\hat{u}_{Mt1,a}$), a small cell capacitance of about $C_M = 1$ μF results. Note that high capacitance values (like in a non-Q2L MMC) would result in significant reactive currents at the grid input because of the arm voltages' LF ac components.

The arm inductors L_{arm} limit currents between the cell capacitors during switching transitions, but they must be small to allow for a quick commutation of the load current [31]. Each converter cell can be assumed to contribute about 0.5 μH of parasitic series inductance [27], such that the arm inductors are not realized as discrete components but result from the sum of the $N = 7$ parasitic cell inductances as $L_{arm} = 3.5$ μH. The arm inductors and the cell capacitors form a resonant circuit with a resonance frequency of $f_r = 1/(2\pi\sqrt{2L_{arm} \cdot C_M/N}) = 159$ kHz (independent of the switching state), which is excited by each switching action. The resonance is only lightly damped, as efficiency requirements demand low series resistance and power density requirements demand low cell capacitances [31]. Thus, to avoid excessive ringing (resulting in increased transistor currents), an R_dC_d-damping branch ($R_d = 3.2$ Ω and $C_d = 1$ μF following [39]) is connected in parallel to each cell capacitor C_M.

Cell voltage balancing and system startup: Several methods have been proposed to balance the cell voltages in Q2L MMC systems, where typically the cell voltage references are constant [27–33]; in contrast, here the cell voltage references contain large LF ac components (see Figure 1a). Nevertheless, the standard Q2L balancing method based on sorting the switching actions of an arm's cells depending on the cell voltages and the sign of the switch-node current [27–29, 33] is applicable.

Figure 3 illustrates the proposed startup procedure, which ensures that the transistor blocking voltages stay below the rated values. Before converter startup, all cells of all arms are inserted with all cell capacitors C_M discharged. At $t = t_0$, the ac terminals are connected to the MV grid via 75 Ω pre-charge resistors to limit the inrush currents. Advantageously, $t = t_0$ is aligned with the start of the DPWM clamping interval of one phase, here phase b which becomes the phase with the most negative voltage at $t = t_0$; thus, all its cells are bypassed (with $S_{t1,b} = S_{b1,b} = 1$) to clamp the converter star point n to the grid terminal b. Note that the cell voltage sharing in the arms of phases a and c is not controlled and established passively (i.e. defined by the cell impedances). However, as all cells of both arms of each bridge leg are inserted simultaneously (in contrast to normal Q2L operation), the blocking voltage margin increases by more than a factor of two compared to normal operation. At $t = t_1$, the pre-charge resistors are bypassed. Subsequently, phase c and phase a start the DPWM operation at the beginning of the next clamping interval (when the corresponding phase voltage becomes the most negative one) at $t = t_2$ and $t = t_3$, respectively. Note further that the output dc voltage U_{DC} already begins to increase at $t = t_2$ when the first phase (phase b) releases clamping and starts 50% PWM duty cycle operation, as the primary-side transformer voltage pulses are rectified by the secondary-side MOSFET body diodes. At $t = t_3$, that is, once all phases operate with DPWM, the SVM of the secondary-side rectifier is enabled, and the output voltage U_{DC} and/or power transfer P can be regulated by the PWM carrier phase shift φ according to (1).

Component stresses and performance estimation: A rough estimate of key component stresses and of the converter's efficiency using state-of-the-art SiC power devices is performed based on a detailed circuit simulation (PLECS) for the considered specifications with $P = P_N = 1$ MW, see also Figure 2. At this nominal operating point, the primary-side RMS transformer current is $I_{Ta} = 136$ A (the stresses in the other two phases are identical), that is, about twice the grid rms current of $I_{ac} = 59$ A because the DM transformer voltage is only half of the grid phase voltage, see Figure 1 and [37]. The converter cells' main switch (S_{t1} and S_{b1}) RMS currents are identical and equal to 99 A, whereas the Q2L operation results in a much lower current stress of 8 A for the auxiliary switches S_{t2} and S_{b2}. Due to the lower voltage levels, the rms current stresses of the secondary-side rectifier's transistors are higher, and simulation results give $I_{SA} = 930$ A and $I_{S'A} = 1340$ A for the high-side and low-side transistors, respectively; paralleling of individual power modules is thus necessary, or, alternatively, paralleling of several rectifier units could be considered.

The transistor conduction losses are modeled based on temperature-dependent loss models provided by the manufacturers, assuming a heat sink temperature of 70 °C. The hard-switching losses are provided by these models as well, and the soft-switching losses are approximated as 10% of the hard-switching losses [40]. In the Q2L MMC front-end's converter cells, four parallel-connected G2R50MT33K 3.3-kV SiC MOSFETs are considered for the realization of the main S_{t1} switch whereas a single G2R50MT33K device suffices for the auxiliary switch S_{t2} (note that there are no 3.3-kV devices with smaller chip areas available). The switched currents of the cells of the top and bottom arms are not identical [37], but due to most transitions being soft-switched [37], the sum of conduction and switching losses of the main transistors in the top and bottom arms is almost the same, that is, $P_{St1,a} = P_{Sb1,a} \approx 172$ W. The auxiliary switch losses are, as expected, much lower, that is, $P_{St2,a} = 9$ W and $P_{Sb2,a} = 4$ W. The RC damping branches connected in parallel to each cell's capacitor dissipate 29 W per cell. Hence, the total losses of the three Q2L MMC bridge legs (including the losses in the damping branches) sum up to roughly 8.7 kW or about 0.9% of the nominal power P_N. Given the much higher current levels, four parallel CAB760M12HM3 1.2-kV power modules are considered for the rectifier switches S_A and S'_A, resulting in simulated losses of $P_{SA} = 520$ W and $P_{S'A} = 1052$ W, respectively, as the rectifier switches are also soft-switched throughout most of the mains period [37]. The total rectifier semiconductor losses sum up to roughly 4.7 kW or about 0.5% of the nominal power P_N. Assuming a typical MFT realization with 0.5% losses (5 kW) [41, 42], the estimated overall system efficiency is ≈98.1%. This is a competitive value for state-of-the-art MVac-LVdc SSTs [15], leaving some headroom for losses of the grid-side input filter.

Similarly, the proposed SST's volumetric power density can be estimated based on the main components. First, assuming forced air cooling, the heat sink volume can be estimated with a cooling system performance index [43] of CSPI = 10 W/(K dm^3); with the total

semiconductor losses calculated above, a maximum heat sink temperature of 70 °C, and an ambient temperature of 45 °C, we find about 50 dm^3. The volume of the MFT is estimated at 285 dm^3 by conservatively assuming a power density of 3.5 kW/dm^3 based on built prototypes reported in the literature [44]. The cell capacitors can, for example, be realized using 1 μF, 2-kV WIMA MKP1U041007J film capacitors, and the series capacitors from two 3 μF, 2.9-kV (rms) AIC E51.R11-302R20/H in parallel (due to the high rms current), resulting in a total volume of about 13 dm^3; the series capacitors contribute about 50%. Interestingly, the peak energy stored in the cell capacitors $C_M + C_d$ of the Q2L MMC front-end and in the series capacitors C_s can be calculated as

$$W_C = 3\left(\frac{1}{2}C_s\left(\frac{\hat{U}_{AC}}{2}\right)^2 + 2N \cdot \frac{1}{2}(C_M + C_d)\left(\frac{\hat{u}_{an}}{N}\right)^2\right), \quad (3)$$

resulting in $W_C = 321\,\mathrm{J}$ ($w_C = W_C/P_N = 321\,J/MW$), which compared to conventional MMCs with typical values of at least $w_C = 10$ kJ/MW [45, 46] is ≈30 times lower. Finally, considering a volume overhead factor of 5 to 10 to account for isolation distances, mechanical assembly structures, grid filter, and housing [15], we estimate a total converter power density of about $\rho \approx 0.3$ kW/dm^3 to $\rho \approx 0.6$ kW/dm^3, which is in the same range as comparable MVac-LVdc conversion solutions [15]. Whereas the above estimates of efficiency and power density are promising, finally, only a fully rated prototype system facilitates a direct quantitative comparison against alternative solutions. However, the proposed single-stage SST topology has a clear conceptual advantage compared to fully modular SSTs because it employs only a single MFT that must provide the large isolation distances for withstanding lightning impulse tests required by standards like IEC 62477-2 [47].

Conclusion: This letter presents a single-stage three-phase MVac-LVdc solid-state transformer (SST) concept with only a single medium-frequency transformer (MFT) and thus simplified isolation coordination, low stored energy in the modular-multilevel-converter-(MMC)-type front-end, and bidirectional power flow capability. Using MMC-type bridge legs operated in the quasi two-level (Q2L) mode with time-varying input voltages (grid voltages with a dc offset) on the MFT's MV side, a standard three-phase rectifier on the secondary side, and a dual-active-bridge-(DAB)-like modulation technique, bidirectional power flow regulation and sinusoidal grid currents are achieved. Detailed circuit simulations of an exemplary 1-MW system reveal the key component stresses and facilitate estimates of efficiency (98.1%) and power density (up to 0.6 kW/dm^3), which are both competitive with other MVac-LVdc SST concepts. Future research should address a detailed quantitative comparative evaluation against other single-stage and two-stage MVac-LVdc SST concepts and, ultimately, a full-scale hardware realization of the proposed system.

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References

1 Liserre, M., et al.: Unlocking the hidden capacity of the electrical grid through smart transformer and smart transmission. *Proc. IEEE* **111**(4), 421–437 (2023). doi:https://doi.org/10.1109/JPROC.2022.3157162
2 Srdic, S., Lukic, S.: Toward extreme fast charging: Challenges and opportunities in directly connecting to medium-voltage line. *IEEE Electrific. Mag.* **7**(1), 22–31 (2019). doi:https://doi.org/10.1109/MELE.2018.2889547
3 Ahmad, A., et al.: An overview on medium voltage grid integration of ultra-fast charging stations: Current status and future trends. *IEEE Open J. Ind. Electron. Soc.* **3**, 420–447 (2022). doi:https://doi.org/10.1109/OJIES.2022.3179743
4 Zhu, C.: High-efficiency, medium-voltage input, solid-state, transformer-based 400-kW/1000-V/400-A extreme fast charger for electric vehicles. Paper presented at the DOE Vehicle Technologies Office Annual Merit Review about Electrification, US Department of Energy, Washington, DC, 29 June 2021. doi:https://tinyurl.com/4nnjbm7u
5 Nakatsu, K., et al.: Development of smart power management for achieving carbon neutrality by 2050: Energy ecosystems for widespread EV adoption. *Hitachi Rev.* **71**(1), 51–57 (2022)
6 Pouresmaeil, K., et al.: Single-phase bidirectional ZVZCS AC-DC converter for MV-connected ultra-fast chargers. In: PCIM Europe 2022; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, pp. 1–7. IEEE, Piscataway, NJ (2022)
7 Feng, H., et al.: Design and implementation of DC-transformer using 10 kV SiC MOSFET for medium-voltage extreme fast charger. In: Proceedings of 2022 IEEE Energy Conversion Congress and Exposition (ECCE USA), pp. 1–5. IEEE, Piscataway, NJ (2022)
8 Tahir, Y., et al.: A state-of-the-art review on topologies and control techniques of solid-state transformers for electric vehicle extreme fast charging. *IET Power Electron.* **14**(9), 1560–1576 (2021). doi:https://doi.org/10.1049/pel2.12141
9 Franzese, P., et al.: Fast DC charging infrastructures for electric vehicles: Overview of technologies, standards, and challenges. *IEEE Trans. Transp. Electrific.* **9**(3), 3780–3800 (2023). doi:https://doi.org/10.1109/TTE.2023.3239224
10 Valedsaravi, S., El Aroudi, A., Martínez-Salamero, L.: Review of solid-state transformer applications on electric vehicle DC ultra-fast charging station. *Energies* **15**(15) 5602 (2022). doi:https://doi.org/10.3390/en15155602
11 Zand, M., et al.: Energy management strategy for solid-state transformer-based solar charging station for electric vehicles in smart grids. *IET Renewable Power Gener.* **14**(18), 3843–3852 (2020). doi:https://doi.org/10.1049/iet-rpg.2020.0399
12 Unruh, R., et al.: 1-MW full-bridge MMC for high-current low-voltage (100 V–400 V) DC-applications. In: Proceedings of PCIM Europe Digital Days 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, pp. 1–8. IEEE, Piscataway, NJ (2020)
13 Krein, P.T.: Data center challenges and their power electronics. *CPSS Trans. Power Electron. Appl.* **2**(1), 39–46 (2017). doi:https://doi.org/10.24295/CPSSTPEA.2017.00005
14 Rothmund, D., et al.: 99.1% efficient 10 kV SiC-based medium-voltage ZVS bidirectional single-phase PFC AC/DC stage. *IEEE Trans. Emerging Sel. Top. Power Electron.* **7**(2), 779–797 (2019). doi:https://doi.org/10.1109/JESTPE.2018.2886140
15 Huber, J., et al.: Comparative evaluation of MVAC-LVDC SST and hybrid transformer concepts for future datacenters. In: Proceedings of 2022 International Power Electronics Conference (IPEC-Himeji 2022-ECCE Asia), pp. 2027–2034. IEEE, Piscataway, NJ (2022)
16 Huber, J.E., Kolar, J.W.: Solid-state transformers: On the origins and evolution of key concepts. *IEEE Ind. Electron. Mag.* **10**(3), 19–28 (2016). doi:https://doi.org/10.1109/MIE.2016.2588878
17 Zhao, C., et al.: Power electronic traction transformer—Medium voltage prototype. *IEEE Trans. Ind. Electron.* **61**(7), 3257–3268 (2014). doi:https://doi.org/10.1109/TIE.2013.2278960
18 Anurag, A., et al.: A three-phase active-front-end converter system enabled by 10-kV SiC MOSFETs aimed at a solid-state transformer application. *IEEE Trans. Power Electron.* **37**(5), 5606–5624 (2022). doi:https://doi.org/10.1109/TPEL.2021.3131262

19 Glinka, M., Marquardt, R.: A new AC/AC multilevel converter family. *IEEE Trans. Ind. Electron.* **52**(3), 662–669 (2005). doi:https://doi.org/10.1109/TIE.2005.843973

20 Zhang, C., et al.: A single-stage three-phase isolated AC-DC converter for medium voltage solid state transformer applications. In: Proceedings of 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 1503–1509. IEEE, Piscataway, NJ (2023)

21 Adam, G.P., et al.: Capacitor balance issues of the diode-clamped multilevel inverter operated in a quasi two-state mode. *IEEE Trans. Ind. Electron.* **55**(8), 3088–3099 (2008). doi:https://doi.org/10.1109/TIE.2008.922607

22 Adam, G.P., et al.: Quasi-two-level and three-level operation of a diode-clamped multilevel inverter using space vector modulation. *IET Power Electron.* **5**(5), 542–551 (2012). doi:https://doi.org/10.1049/iet-pel.2011.0229

23 Schweizer, M., Soeiro, T.B.: Heatsink-less quasi 3-level flying capacitor inverter based on low voltage SMD MOSFETs. In: Proceedings of 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe), pp. P1–P.10. IEEE, Piscataway, NJ (2017)

24 Czyz, P., et al.: Load-independent voltage balancing of multi-level flying capacitor converters in quasi-2-level operation. *Electronics* **10**(19), 2414 (2021). doi:https://doi.org/10.3390/electronics10192414

25 Kopacz, R., et al.: Medium voltage flying capacitor DC–DC converter with high-frequency TCM-Q2L control. *IEEE Trans. Power Electron.* **37**(4), 4233–4248 (2022). doi:https://doi.org/10.1109/TPEL.2021.3122329

26 Mersche, S.C., Schwendemann, R., Hiller, M.: Validation of the quasi-two-level operation for a flying capacitor converter in medium-voltage applications. *Energies* **16**(6), 2797 (2023). doi:https://doi.org/10.3390/en16062797

27 Gowaid, I.A., et al.: Quasi two-level operation of modular multilevel converter for use in a high-power DC transformer with DC fault isolation capability. *IEEE Trans. Power Electron.* **30**(1), 108–123 (2015). doi:https://doi.org/10.1109/TPEL.2014.2306453

28 Gowaid, I.A., et al.: Analysis and design of a modular multilevel converter with trapezoidal modulation for medium and high voltage DC-DC transformers. *IEEE Trans. Power Electron.* **30**(10), 5439–5457 (2015). doi:https://doi.org/10.1109/TPEL.2014.2377719

29 Mertens, A., Kucka, J.: Quasi two-level PWM operation of an MMC phase leg with reduced module capacitance. *IEEE Trans. Power Electron.* **31**(10), 6765–6769 (2016). doi:https://doi.org/10.1109/TPEL.2016.2537372

30 Milovanovic, S., Dujic, D.: Comprehensive analysis and design of a quasi two-level converter leg. *CPSS Trans. Power Electron. Appl.* **4**(3), 181–196 (2019). doi:https://doi.org/10.24295/CPSSTPEA.2019.00018

31 Kucka, J., Mertens, A.: Designing a passively damped quasi-two-level-operated modular multilevel converter for drive applications. *IEEE Access* **8**, 80218–80232 (2020). doi:https://doi.org/10.1109/ACCESS.2020.2990888

32 Kucka, J., et al.: Quasi-two-level PWM-operated modular multilevel converter with nonlinear branch inductors. *IEEE Trans. Power Electron.* **36**(7), 7600–7611 (2021). doi:https://doi.org/10.1109/TPEL.2020.3042635

33 Wang, R., et al.: Quasi-two-level (Q2L) half bridge cascaded (HBC) super switch (SS) concept for medium voltage applications. In: Proceedings of 2022 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 1–6. IEEE, Piscataway, NJ (2022)

34 Aeloiza, E., Canales, F., Burgos, R.: Power converter having integrated capacitor-blocked transistor cells. US Patent 9,525,348B1, 20 Dec 2016

35 Yu, J., Burgos , R.: Capacitor voltage control in medium-voltage converters based on integrated capacitor-blocked transistor (ICBT) cells. In: Proceedings of 2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL), pp. 1–6. IEEE, Piscataway, NJ (2022)

36 Mocevic, S., et al.: Design of a 10 kV SiC MOSFET-based high-density, high-efficiency, modular medium-voltage power converter. *iEnergy* **1**(1) 100–113 (2022). doi:https://doi.org/10.23919/IEN.2022.0001

37 Menzi, D., et al.: Novel bidirectional single-stage isolated three-phase buck-boost PFC rectifier system. In: Proceedings of 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 1936–1944. IEEE, Piscataway, NJ (2023)

38 Baranwal, R., et al.: A dual-active-bridge-based single-phase AC to DC power electronic transformer with advanced features. *IEEE Trans. Power Electron.* **33**(1), 313–331 (2018). doi:https://doi.org/10.1109/TPEL.2017.2669148

39 Erickson, R.W.: Optimal single resistor damping of input filters. In: Proceedings of Fourteenth Annual Applied Power Electronics Conference and Exposition (APEC), pp. 1073–1079. IEEE, Piscataway, NJ (1999)

40 Haider, M., et al.: Novel ZVS S-TCM modulation of three-phase AC/DC converters. *IEEE Open J. Power Electron.* **1**, 529–543 (2020). doi:https://doi.org/10.1109/OJPEL.2020.3040036

41 Czyz, P., et al.: Analysis of the performance limits of 166 kW/7 kV air- and magnetic-core medium-voltage medium-frequency transformers for 1:1-DCX applications. *IEEE Trans. Emerging Top. Comput. Intell.* **10**(3), 2989–3012 (2022). doi:https://doi.org/10.1109/JESTPE.2021.3123793

42 Guo, Z., et al.: A novel high insulation 100 kW medium frequency transformer. *IEEE Trans. Power Electron.* **38**(1), 112–117 (2023). doi:https://doi.org/10.1109/TPEL.2022.3205646

43 Drofenik, U., Laimer, G., Kolar, J.: Theoretical converter power density limits for forced convection cooling. In: Proceedings of the International Conference Power Electronics, Intelligent Motion, Power Quality, pp. 608–619. ZM Communications GmbH, San Diego, CA (2005)

44 Djekanovic, N., Dujic, D.: Design optimization of a MW-level medium frequency transformer. In: Proceedings of PCIM Europe 2022; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, pp. 1–10. IEEE, Piscataway, NJ (2022)

45 Merlin, M.M.C., Green, T.C.: Cell capacitor sizing in multilevel converters: Cases of the modular multilevel converter and alternate arm converter. *IET Power Electron.* **8**(3), 350–360 (2015). doi:https://doi.org/10.1049/iet-pel.2014.0328

46 Zygmanowski, M., Grzesik, B., Nalepa, R.: Capacitance and inductance selection of the modular multilevel converter. In: Proceedings of 15th European Conference on Power Electronics and Applications (EPE), pp. 1–10. IEEE, Piscataway, NJ (2013)

47 IEC 62477-2:2018: Safety requirements for power electronic converter systems and equipment - Part 2: Power electronic converters from 1 000 V AC or 1 500 V DC up to 36 kV AC or 54 kV DC.