Comparative Evaluation of Gate Driver and LC-Filter Based dv/dt-Limitation for SiC-Based Motor-Integrated Variable Speed Drive Inverters

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ABSTRACT

Compared to state-of-the-art IGBTs, SiC power semiconductors allow to achieve ever higher system efficiencies and higher power densities in next-generation Variable Speed Drives (VSDs), thanks to their smaller relative chip size, ohmic on-state characteristic and lower specific switching losses resulting in a smaller switching-stage footprint and lower heat sink as well as DC-link capacitor volumes. However, the high slew rate of the switching transitions, an inherent consequence of the low switching losses, represents a major challenge and potentially results in lifetime degrading unequal voltage distribution across the motor windings and bearing currents. This work analytically and experimentally compares different means for dv/dt-limitation, namely, a conventional passive LC-dv/dt-filter and a Gate Driver (GD)-based approach based on increased GD resistances in combination with explicit Miller capacitors, at the example of a 10 kW industrial motor-integrated VSD. For a state-of-the-art dv/dt-limitation of up to 6 V/ns the LC-filter shows lower losses compared to the GD-based limitation. The latter, however, has a higher part-load efficiency and/or lower losses compared to the (roughly) load independent losses in the LC-filter resulting from the dissipation of the energy stored in the filter capacitor within each switching cycle, beneficial for light loads, e.g., < 40 % of rated output power. Next-generation motors with reinforced insulation allow a dv/dt-limitation of up to 15 V/ns. In this case, the GD-based limitation shows lower losses in the whole operating range, since they directly scale with the now smaller overlap of voltage and current resulting from the faster switching transitions. Considering a state-of-the-art motor, finally, a hardware demonstrator of a three-phase VSD employing an LC-filter to limit the dv/dt to 5.6 V/ns is realized, which achieves a full inverter stage power density of 30 kW/dm$^3$ (497 W/in$^3$) and an inverter efficiency of > 99 %.

INDEX TERMS

Gate drivers, permanent magnet motors, pulse width modulation converters, silicon carbide, transmission lines, variable speed drives.

I. INTRODUCTION

Between 40 % and 50 % of the global energy consumption is attributed to electric motor-driven systems [2], [3], primarily in industrial applications, which motivates an investigation of improvements in energy conversion efficiency, in particular of three-phase VSD inverter systems. In the multi-kW range, state-of-the-art inverters are typically composed of Si IGBTs with antiparallel freewheeling diodes and are operated at switching frequencies in the range of several kHz to several tens of kHz [4], [5]. SiC MOSFETs are offering an interesting alternative for next-generation VSDs, since they contain internal diodes, hence omitting the need of dedicated external freewheeling diodes, and in contrast to IGBT power devices they do not exhibit a constant forward voltage drop in the on-state, hence offering significantly reduced conduction losses, which is of particular advantage for part-load operation that
often contributes a major share in typical mission profiles of electric motors [6]. Thanks to their high switching speed (high \(dv/dt\) and high \(di/dt\)) and the significantly lower reverse recovery charge of the internal freewheeling diodes, for the same conduction losses, SiC power semiconductors have a significantly smaller chip area and therefore, lower switching losses [7]. For a given loss budget they can thus be operated at a higher switching frequency up to hundred kHz or more [8], which reduces the required capacitance / size of the DC-link capacitor and increases power density. A minimized functional volume, i.e., a high power density, is particularly important for ever-more popular Integrated Motor Drives (IMDs) where the VSD is placed inside the machine housing and thus must be realized as compact as possible due to space restrictions [9]. A further advantage of IMDs is the absence of long motor cables, which on the one hand are expensive and heavy and on the other hand already for relatively low voltage transition rates of the switched PWM output voltage lead to transmission line effects, e.g., voltage reflections and ringing [10] that increase the insulation stress due to overvoltage at the machine terminals.

A higher switching frequency and accompanying lower volume, however, increases the loss density of the inverter system. Given that typical electric motors have efficiencies in the range of \(90 – 95\%\), a required inverter efficiency of typically \(> 99\%\) for IMDs is dictated by the thermal design in order to safely dissipate the losses, more than by the overall system efficiency, which is clearly dominated by the motor.

The high switching speed (in particular the high \(dv/dt\)) of \(20 \ldots \geq 50\ V/nS\) occurring in SiC MOSFETs imposes various challenges, for example, said transmission line effects typically occurring in state-of-the-art IGBT VSDs with long motor cables can now also occur in IMDs, i.e., even without motor cables [11], [12]. These effects mainly result in an uneven voltage distribution (coil-to-coil and turn-to-turn) within the machine winding, which can drastically reduce the lifetime of the insulation, e.g., due to partial discharge and/or accelerated insulation aging [9], [13]. Moreover, the Common Mode (CM) voltage components with a high \(dv/dt\) lead to high bearing currents that reduce the bearing lifetime [14]. While a full sinewave filter would address the aforementioned challenges and thanks to the increased switching frequency in next-generation SiC-based VSDs may be more attractive to implement, it would still significantly impair the inverter power density and would also be a major cost driver. Therefore, it is desired to only implement the absolutely minimum necessary filtering, i.e., to only limit the fast \(dv/dt\) voltage transients applied to the motor (a Permanent Magnet Synchronous Motor (PMSM) in the case at hand), e.g., by means of a single-stage \(LC-dv/dt\)-filter [15], [16], as shown in Fig. 1. Considering according standards [17], [18], the \(dv/dt\)-values (voltage slew rate; measured between \(10\%\) and \(90\%\) of \(V_{DC}\) and vice versa) of industrial inverter systems are typically limited to \(3 \ldots 6\ V/nS\) in order to restrain the aforementioned detrimental effects. However, next-generation electric machines with reinforced motor insulation are projected to withstand considerably higher \(dv/dt\)-ratings of \(10 \ldots 15\ V/nS\). Various \(dv/dt\)-limiting/filtering concepts, i.e., active, passive and hybrid approaches, are reported in literature and have been reviewed in [1]. It should be noted that there are also concepts to directly mitigate the overvoltage at the machine terminal and/or the unequal voltage distribution across the winding coils inside the machine by means of small auxiliary circuits in parallel to the first few turns (“smart coils”) [19]. These solutions, however, need careful tuning for each specific machine and require additional active components (switches) with driving circuitry.

This article focuses on the two most promising \(dv/dt\)-limitation concepts on the VSD side, namely a passive \(LC-dv/dt\)-filter employing a single stage \(LC\)-filter with diode-clamped damping network (DRC damping) [20], [21] as well as a GD-based \(dv/dt\)-limiting concept featuring a Miller feedback capacitor in combination with increased GD resistances [22], [23] for the exemplary case of a 10kW three-phase IMD employing SiC power semiconductors with the specifications listed in Table 1. It answers the question, which concept is better suited in terms of efficiency and power density for two distinct maximum \(dv/dt\)-values of \(5\ V/nS\) for state-of-the-art motors and \(12\ V/nS\) for future motors and different load scenarios (full-load or part-load operation) by

![SiC Variable Speed Drive](Image)

**TABLE 1. Specifications of the Three-Phase IMD Inverter System**

<table>
<thead>
<tr>
<th>Description</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max. Mech. Output Power</td>
<td>(P_{M,\text{max}})</td>
<td>10 kW</td>
</tr>
<tr>
<td>Nom. Mech. Output Power</td>
<td>(P_{M,\text{nom}})</td>
<td>8 kW</td>
</tr>
<tr>
<td>Rated Mechanical Speed</td>
<td>(n_M)</td>
<td>4000 rpm</td>
</tr>
<tr>
<td>Rated Inv. Output Frequency</td>
<td>(f_E)</td>
<td>333 Hz</td>
</tr>
<tr>
<td>DC-Link Voltage</td>
<td>(V_{DC})</td>
<td>800 V</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>(f_{sw})</td>
<td>16 kHz</td>
</tr>
<tr>
<td>Voltage Slew Rate Limit</td>
<td>(dv/dt)</td>
<td>5 V/nS or 12 V/nS</td>
</tr>
</tbody>
</table>
theoretical and experimental validation. The switching frequency of \( f_{sw} = 16 \text{kHz} \) is just above the audible range and is selected to minimize the switching losses and to facilitate direct comparison to state-of-the-art VSDs implemented with IGBTs.

Section II explains the two considered \( dv/dt \)-limiting concepts before Section III introduces the accompanying trade-offs in terms of losses and functional volume. Section IV then analytically compares the two concepts for different \( dv/dt \)-values and load conditions and derives a boundary to select the better-suited concept depending on the operating conditions. The calculations are experimentally verified for both investigated concepts and a three-phase VSD inverter system realization suitable for motor integration is presented. Finally, Section V concludes the article.

II. \( dv/dt \)-LIMITING CONCEPTS
A. LC-FILTER BASED \( dv/dt \)-FILTER
Passive \( LC-dv/dt \)-filters are composed of a filter inductor \( L_f \) and a filter capacitor \( C_f \), whereas the latter is advantageous referred to the DC-link rails in order to filter CM and Differential Mode (DM) voltage components simultaneously (cf. Fig. 2(a)). The resulting phase modular nature facilitates integration, e.g., into power modules. General filter design goals are to limit the \( dv/dt \) to a certain maximum value and at the same time to limit the inductor current swing \( \Delta i_L \) and output voltage overshoot \( \Delta v_{u*n} \) below given boundaries. In this regard, filter damping is essential to avoid overshoot and excessive ringing of the voltage applied to the motor. In the simplest case of a series \( LCR \)-filter, damping is implemented with a resistor \( R_f \) in series with \( C_f \) (cf. Fig. 1) [24], [25], such that the oscillatory transition excited by each switching pulse quickly decays to the steady state, i.e., \( v_{u*n} = V_{DC} \) and \( i_{u*n} = i_u \). The drawback of this approach is the dependency of the resultant voltage rise time not only on the filter resonance frequency \( \omega_0 = 1/\sqrt{L_f C_f} \) but also on the selected quality factor \( Q = R_f/Z_t \) (characteristic filter impedance \( Z_t = \sqrt{L_f/C_f} \)) that also defines the overshoot and is therefore difficult to calculate [1]. Diode-clamped damping networks (DRC damping) [20], [21] as shown in Fig. 2(a) advantageously decouple the \( dv/dt \) and the damping. The desired \( dv/dt \) defines the voltage transition rise time \( t_{R0} \) and fall time \( t_{F0} \) (10% to 90% of \( V_{DC} \) and vice versa) with

\[
t_{R0} = t_{F0} = \frac{0.8 \cdot V_{DC}}{dv/dt} \tag{1}
\]

and thanks to the disconnected damping network for \( 0 < v_{u*n} < V_{DC} \) is solely defined by the resonance formed with \( L_f \) and \( C_f \) (cf. characteristic waveforms in Fig. 2(b)), i.e.,

\[
v_{u*n}(t) = V_{DC} \cdot (1 - \cos(\omega_0 t)) \tag{2}
\]

Therefrom, the rise time

\[
t_{R0} = t_{|v_{u*n}(t)=0.9V_{DC}} - t_{|v_{u*n}(t)=0.1V_{DC}} \tag{3}
\]

results and finally, the \( dv/dt \) can be analytically described as

\[
dv/dt = \frac{0.8 \cdot V_{DC}}{(\arccos(0.1) - \arccos(0.9))/\omega_0} = 0.8 \cdot V_{DC} \cdot \frac{\omega_0}{\Omega_2} \tag{4}
\]

FIGURE 2. Investigated \( dv/dt \)-limiting concepts [1] for phase \( u \) from Fig. 1. (a) \( LC-dv/dt \)-filter with diode-clamped damping network (DRC damping) to limit the inductor peak current and voltage overshoot in phase \( u \). (b) Characteristic waveforms of the \( LC-dv/dt \)-filter, with the unfiltered switch-node voltage \( v_{u*n} \) (dashed), the filtered output voltage \( v_{u*n} \) (blue) and the inductor current \( i_{u*n} \) (red) for two cases, with and without additional damping capacitors \( C_p \) and \( C_n \) which help to further reduce the voltage overshoot. (c) GD-based \( dv/dt \)-limiting with a Miller feedback capacitor \( C_M \) and GD resistor \( R_G \) (in the actual realization, different \( R_G \) values are used for the turn-on and the turn-off switching transition). (d) Zoomed idealized (straight line approximation) view of the voltage \( v_{u*n} \) across the low-side transistor (blue) and its corresponding channel current \( i_{u*n} \) (red) for a negative instantaneous phase current \( i_u \) (indicates the physical current direction) during one switching period \( T_{sw} = 1/T_{fu} = 62.5 \mu s \), indicating the “kink” current, which leads to a slew-rate limited turn-off transition (during \( T_{L} \)). The limited voltage transients of the turn-on and turn-off transitions (during \( T_{0} \) and \( T_{0u} \), both equal 160 ns for a \( dv/dt = 5 \text{V/ns} \) and \( V_{DC} = 800 \text{V} \) are highlighted.
with $\Omega := \arccos(0.1) - \arccos(0.9) \approx 1.02$. It therefore only depends on $L_t$ and $C_t$, which have to be selected accordingly. Considering that the filter is loaded with the motor (i.e., its input impedance in case of an IMD) or even with the motor cable + motor, the filter characteristic becomes load-dependent. It is very difficult to generalize such a setup due to the large variety of different motors and cables. In the case at hand we focus on an IMD (no motor cable) for the PMSM 1F77084 from Siemens [26], which is a typical example for an industrial 10 kW drive system with specifications as listed in Table 1. In order to be largely independent of the machine loading, the filter output impedance $Z_{\alpha,f}$ must be smaller than the machine input impedance in the frequency range of interest for the considered $du/dt$, i.e., around the filter resonance frequency $f_0 = \omega_0/(2\pi)$ [1]. In a typical modulation scheme, only one bridge-leg is switched at a time, which leads to the same voltage step applied to the machine regardless of the switching state changes, i.e., always one phase is switched from 0 V to $V_{DC}$ (or vice versa), while the other two terminals are assumed to be clamped to the negative (or positive) DC-link rail and in addition, considering the worst-case of a direct connection of the negative DC-link rail with PE, i.e., a shorted $C_\gamma$ (cf. Fig. 1), also to PE. Therefore, the machine impedance seen between, e.g., terminal u and shorted terminals v, w, and PE (case) ($Z_{U-VWPE}$) has to be evaluated and impedance measurements reveal that in the relevant frequency range the PMSM behaves like a capacitance of around 300 pF (cf. Appendix). Thus, in order to ensure $Z_{\alpha,f} < Z_{U-VWPE}$ with the worst-case assumption that $Z_{\alpha,f}$ is solely defined by $C_t$, $C_t \geq 1 \text{nF}$ is selected (three times larger value). While the semiconductor losses remain unaffected by placing an LC-$du/dt$-filter (they still switch with a very high $du/dt$ in the range of $20...50 \text{ V/ns}$), the filter capacitor $C_t$ needs to be charged and discharged once every switching period. This translates into an energy loss $E_C = 2 \cdot \frac{1}{2} C_t V_{DC}^2$, independent of the switched current, which is dissipated mainly in the resistors of the damping network. It is thus advisable to select the minimum possible $C_t$ to minimize the filter losses. For a given $C_t$ the filter inductance $L_t$ directly follows from the desired $du/dt$ using (4), e.g., a $du/dt$ of 5 V/ns and 12 V/ns requires $L_t = 14 \text{ mH}$ and $L_t = 2.4 \text{ mH}$, respectively, for $C_t = 1 \text{nF}$ and $V_{DC} = 800 \text{ V}$. The filter losses are dissipated in the damping resistors $R_p$ and $R_n$ (cf. Fig. 2(a)), which are selected to achieve critical damping ($Q = 0.5$). The additional capacitors $C_p$ and $C_n$ in parallel to the respective damping resistors do not influence the filter losses but reduce the voltage overshoot $\Delta v_{tr,n}$ at the cost of a prolonged discharging time, as indicated with the dim curves in the characteristic waveforms of Fig. 2(b). The filter inductors must be designed for a peak current $i_{L,pk} = i_a + \Delta i_{L,a}$, with the phase current amplitude $i_a$ and the inductor current swing $\Delta i_{L,a} = V_{DC}/Z_t$ to charge $C_t$. Fig. 3(a) exemplary shows the required components to implement one slew-rate limited bridge-leg of the three-phase VSD with a $du/dt$-limitation of 5 V/ns realized by means of a passive LC-filter employing DRC damping.

B. GATE DRIVER BASED $du/dt$-LIMITATION

The apparent drawback of a passive $du/dt$-limiting filter is the additional volume and cost of the filtering elements (though, they are considerably smaller compared to a full sinewave filter). Alternatively, the $du/dt$ of the voltage applied to the machine can be limited directly via the GD voltage, which only requires very small passive elements and therefore, has a negligible contribution to the component volume, as depicted in Fig. 3(b). Different realizations either limit the gate time constant, e.g., by using different gate resistance values [27], [28], [29] or by implementing closed-loop gate control [30], [31]. An alternative implementation not only modifies the gate time constant but also artificially increases the gate-to-drain capacitance $C_{GD}$ of the MOSFET with an external so-called Miller capacitance $C_{GD}$ between drain and gate (in the range of few pF, hence very small) as shown in Fig. 2(c), to inherently slow down the $du/dt$ transient and thereby potentially gains advantages in terms of losses. A detailed analysis of the resulting MOSFET turn-on and turn-off transitions is carried out in [23] and reveals that both are equally slowed down by the combination of gate resistance $R_G$ and $C_M$. This is indicated in Fig. 2(d), which shows a zoomed view of one switching period $T_{sw}$ during the fundamental frequency period $T_E = 1/f_E$ where the momentary phase current $i_a$ (and thus switched current) is negative ($i_a$ in Fig. 2(c) indicates the physical current direction).

The slowed down voltage transitions lead to a voltage-current overlap and hence to increased switching losses. The additional overlap losses in the (ideally lossless) turn-off transition (during $t_{ro}$ for a negative switched current of the low-side transistor $T_n$) have been comprehensively discussed in [22] and are attributed to the voltage-current overlap resulting from a residual current in the channel of $T_n$ while its $C_{GD}$, $C_M$ and the drain-to-source capacitance $C_{DS}$ are charged (and the high-side transistor $T_h$’s $C_{DS}$, $C_{GD}$ and $C_M$ are discharged). Assuming for simplicity no external Miller capacitor ($C_M = 0 \text{ pF}$) and a certain switched current $i_a$, the resonant Zero Voltage Switching (ZVS) transition would charge $C_{GD}$ of $T_n$ with a current $i_{C_{GD}}$ determined by the current divider $C_{GD}/(C_{DS} + C_{GD})$ (and similarly charge
\( C_{DS} \) of \( T_L \) with a current determined by \( C_{DS}/(C_{DS} + C_{GD}) \), which together with a current discharging the gate-to-source capacitance \( C_{GS} \) equals the total gate current \( i_G \). The latter is limited to \( i_{G,max} = (v_{th} + |V_{GD,n}|)/R_{G,off} \) by the GD as a function of the MOSFET threshold voltage \( v_{th} \), the negative GD voltage \( V_{GD,n} \) and the turn-off gate resistance \( R_{G,off} \) (composed of the externally placed resistance and a GD-internal part representing the limited current drive capability). For switched currents above a certain limit \( i_k \) (the so-called “kink” current [22]) and considering only the capacitive current divider, \( i_{G,max} \) would need to exceed \( i_{G,max} \), which is not possible. Therefore, a certain residual current \( (i_k - i_k) \) continues to flow in the MOSFET channel, causing said overlap losses. As derived in [22], the limit \( i_k \) is defined as the switched current \( i_k = i_k \) that is entirely split between \( C_{GD} \) and \( C_{CM} \) in parallel of \( T_L \) and the parallel combination of \( C_{GS} \) of \( T_L \), \( C_{GS} \) of \( T_H \) and \( C_{GD} \) and \( C_{CM} \) of \( T_H \) (current divider) and where \( i_{G,off} = i_{G,max} \), i.e.,

\[
i_k = \frac{v_{th} + |V_{GD,n}|}{R_{G,off}} \cdot 2 \cdot \left(1 + \frac{C_{dQ,DS}}{C_{dQ,GS} + C_{CM}}\right), \tag{5}
\]

assuming a very high MOSFET transconductance \( g_m \). To account for the non-linear capacitances \( C_{DS} \) and \( C_{GD} \) with changing voltage, \( C_{dQ,DS} \) and \( C_{dQ,GS} \) denote the charge-equivalent linear capacitances for a voltage change between 10% and 90% of \( V_{DC} \) (or between 90% and 10% of \( V_{DC} \)), i.e., the voltage range \( \Delta v = 0.8 \cdot V_{DC} \) in which the \( dv/dt \) is evaluated. The factor of two in (5) accounts for the charging/discharging of \( C_{DS} \), \( C_{GD} \) and \( C_{CM} \) of the high-side and low-side transistors during the ZVS transition. \( i_k = [6.3 \text{ A}, 18.2 \text{ A}] \) result for the utilized component values and the two considered \( dv/dt \)-limiting values of 5 V/ns and 12 V/ns, respectively (cf. Table 2), which accounts for \( \sim 24 \% \) and \( \sim 70 \% \) of the phase current amplitude at full output power (cf. (11)). Therefore, it is important to consider the effect of \( i_k \) on the resulting semiconductor losses as it is done in Section III-C.

From \( i_k \) follows now directly the desired reduced turn-off voltage transition rate (straight-line approximation)

\[
dv{dr}_{off} = \frac{i_k}{2 \cdot (C_{dQ,DS} + C_{dQ,GS} + C_{CM}) + C_{par}}, \tag{6}
\]
as further derived in [22] and again using the charge-equivalent capacitances. Moreover, \( C_{par} \) includes various parasitic capacitances, e.g., from the PCB layout or the heat sink. Combining (5) and (6) and neglecting \( C_{par} \), the simplified expression

\[
dv{dr}_{off} = \frac{v_{th} + |V_{GD,n}|}{R_{G,off} \cdot (C_{dQ,GS} + C_{CM})} \tag{7}
\]
results. Equation (7) clearly illustrates that for a given GD supply voltage, the \( dv/dr \) is defined by the product of GD resistance and (total) Miller capacitance and therefore, multiple combinations result in the same \( dv/dr \). Note that (5) to (7) assume \( C_{M} \) and \( C_{GD} \) connected in parallel, i.e., the internal gate resistance of the power semiconductor is assumed zero. Furthermore, it has to be noted that the \( dv/dr \) in (7) slightly increases for switched currents \( i_k > i_k \), since the gate-to-source voltage during the voltage transition equals the Miller-plateau voltage \( v_m = v_{th} + (i_k - i_k)/g_m \) (MOSFET transconductance \( g_m \)), slightly raising the maximum possible gate current and thus accelerating the charging of \( C_{GD} \) and \( C_{CM} \). Given the typically very high \( g_m \) of power MOSFETs (\( g_m \approx 53 \text{ S} \) for the device used here, C3M0016120K, cf. Table 2) this effect is not significant.

The turn-on transition of \( T_L \) (during \( t_p \) in Fig. 2(d)), again assuming a negative phase current and thus a negative switched current \( i_k \), is a Hard Switching (HSW) transition, which causes overlap losses, because after turn-off of the high-side switch \( T_H \), \( i_k \) commutes in its freewheeling diode, i.e., \( V_{DC} \) remains across the low-side transistor \( T_L \), and only after an enforced dead time \( i_k \) commutes to the channel of \( T_L \) (turn-on of \( T_L \)). With increasing gate resistance and/or Miller capacitance the maximum current to charge \( C_{GD} \) (and \( C_{CM} \)) of \( T_H \) and to discharge \( C_{GD} \) (and \( C_{CM} \)) of \( T_L \) is limited by the GD resulting in increased overlap losses due to the desired slowed down turn-on voltage transition

\[
dv{dr}_{on} = \frac{V_{GD,on} - v_{th}}{R_{G,on} \cdot (C_{dQ,GS} + C_{CM})}, \tag{8}
\]
with the positive GD drive supply voltage \( V_{GD,p} \) and the turn-on gate resistance \( R_{G,on} \).

Resulting from (7) and (8), a certain \( dv/dr \) can be achieved with different combinations of \( R_{G,on} \) and \( R_{G,off} \) and \( C_{M} \), for example a slow rate limit of 10 V/ns could be achieved with \( C_{M} = 50 \text{ pF}, R_{G,on} = 9.5 \Omega \) and \( R_{G,off} = 11.0 \Omega \) or with \( C_{M} = 0 \text{ pF} \) (only the device-internal \( C_{GD} \) is effective), \( R_{G,on} = 30.1 \Omega \) and \( R_{G,off} = 24.3 \Omega \) [23]. Measurements in [23] show, however, that the losses do not significantly change for different combinations, thus in the interest of simplicity, \( C_{M} = 0 \text{ pF} \) can be chosen and the \( dv/dr \) is set entirely with the GD resistance. Actual \( dv/dr \) in Table 2. Note that changing the gate resistance directly changes the gate time constant \( \tau_{GS,on} = R_{G,on} \cdot C_{GS} \) \( (\tau_{GS,off} = R_{G,off} \cdot C_{GS}) \), which influences the time for the gate-to-source voltage to rise from the threshold voltage \( v_{th} \) to the Miller-plateau voltage \( v_m = v_{th} + i_k/g_m \) during the turn-on transition (and vice versa fall from the Miller plateau to \( v_{th} \) during the turn-off transition) and therefore leads to a finite current slew rate \( dv/dr \) (indicated in Fig. 2(d)). Calculations with the utilized device parameters (cf. Table 2) verify that the current rise and fall times are still more than one order of magnitude faster compared to the voltage transition times \( t_{R0} \) and \( t_{R0} \) and are hence neglected.

### III. LOSS AND VOLUME CALCULATION

Both presented \( dv/dr \)-limiting concepts cause additional losses, either due to capacitor charging/discharging (filter capacitor \( C_f \) of the LC-\( dv/dr \)-filter) or overlap losses (GD-based limitation), and further contribute a certain volume, e.g., of
additional passive elements and of the required heat sink to dissipate the additional losses. Since the goal is to select the best-suited dv/dr-limiting approach based on loss and volume considerations, approximative quantitative loss and volume models are derived in the following. It is important to discriminate the additional losses/volumes caused by dv/dr-limiting concepts from losses that are inherently present, including the capacitive losses occurring due to charging/discharging of the parasitic machine capacitances. These losses act as loss offset and in a first approximation are assumed to not change if the voltage slew rate is limited by either of the concepts.

A. INVERTER OUTPUT POWER

At rated mechanical rotational speed $n_M = 4000$ rpm ($\omega_M = 2\pi \cdot n_M/60 = 2\pi \cdot 67$ Hz) and with the voltage constant $k_V = \frac{V_{\text{nom}}}{n_M} = 83$ mV/rpm and $p = 5$ pole pairs [26], the induced motor winding (phase) voltage has an amplitude $\hat{v}_{\text{ind}}$ and an electrical angular frequency $\omega_E$

\[
\hat{v}_{\text{ind}} = \sqrt{\frac{2}{3}} \cdot k_V \cdot n_M = 270 \text{ V},
\]

in accordance with [1]. The resulting maximum phase current amplitude at full power ($P_{\text{M, max}} = 10$ kW), i.e., at full torque of $T_{\text{M, max}} = 23.8$ Nm, is

\[
\hat{i}_{u, \text{ max}} = \sqrt{\frac{2}{3}} \cdot \frac{T_{\text{M, max}}}{k_T} = 25.9 \text{ A}
\]

with the machine torque constant $k_T = \frac{T_{\text{M, max}}}{\frac{2}{3} \cdot \frac{V_{\text{nom}}}{P_{\text{M, max}}}} = 1.3$ Nm/A [26]. Typical mission profiles of industrial drive systems are largely containing part-load operation, e.g., a reduced nominal torque of $T_{\text{nom}} = 0.8 \cdot T_{\text{M, max}} = 19$ Nm ($i_{u, \text{ nom}} = 20.7$ A) at nominal rotational speed, which justifies investigation of the optimally suited dv/dr-limiting concept for such a part-load case. Unsurprisingly, combining (9) with (11) results in the maximum mechanical output power of $P_{\text{M, max}} = 10$ kW and when using $T_{\text{nom}}$ instead of $T_{\text{M, max}}$, in $P_{\text{nom}} = 8$ kW. The output power of each inverter phase can be expressed with

\[
P_u = \frac{1}{\sqrt{2}} \cdot M \cdot \frac{V_{\text{DC}}}{2} \cdot \cos(\varphi) \cdot \frac{\hat{i}_u}{\sqrt{2}} = \frac{1}{4} \cdot M \cdot V_{\text{DC}} \cdot \cos(\varphi) \cdot \hat{i}_u,
\]

where $M \cdot V_{\text{DC}}/2$ denotes the amplitude $\hat{v}_u$ of the inverter phase output voltage (modulation depth $M$). Assuming the load current to be in-phase with the induced motor voltage $v_{\text{ind}}$, in a complex phasor representation, the projection of the inverter output voltage phasor $\hat{v}_u$ on the real axis, i.e., $\hat{v}_u \cdot \cos(\varphi)$, corresponds to the induced motor voltage $v_{\text{ind}}$. According to (9), the amplitude of this projected voltage $v_{\text{ind}} = M \cdot V_{\text{DC}}/2 \cdot \cos(\varphi)$ is directly related to the rotational speed and thus constant and load-independent (typically, there is a superordinate speed controller that regulates $n_{\text{rpm}}$ to the desired value). For $n_{\text{rpm}} = 4000$ rpm and the given machine parameters [26], $M \cos(\varphi) = 0.68$ [1] and therefrom $P_u$ can be calculated straight-forward.

B. LOSSES AND VOLUME OF THE PASSIVE LC-dv/dt-FILTER

In a passive LC-dv/dt-filter the power semiconductors themselves are switching with a typically very high dv/dt and switching loss models obtained from device characterization (e.g., thermally measured [32]) with quadratic fitting coefficients $k_0$, $k_1$ and $k_2$ can be used. For a purely sinusoidal switched current, i.e., no current ripple (justified with the relatively large machine inductance), the semiconductor losses per phase (half-bridge losses $P_{\text{HB}}$) for a certain $i_u$ then equal

\[
P_{\text{HB}} = \frac{1}{2} R_{\text{DS, on}} i_{u, \text{ max}}^2 + f_{\text{sw}} \left( k_0 + \frac{2}{\pi} k_1 i_u + \frac{1}{2} k_2 i_{u, \text{ max}}^2 \right).
\]

Additional losses components are the charging/discharging losses $P_C = C_i V_{\text{DC}} f_{\text{sw}}$ of the filter capacitance $C_i$, which are dissipated mainly in the resistors of the DRC damping network, and the filter inductor conduction losses $P_L = \frac{1}{2} R_{\text{L, on}} i_{u, \text{ max}}^2$ (neglecting core losses due to the low fundamental frequency and the generally low current ripple given the large motor winding inductance; further neglected are hence the conduction losses arising from the current ripple and the contribution of the current pulse $\Delta i_u$ to the total RMS current, which is found to be negligible). In total, the per-phase losses of a bridge-leg featuring a passive LC-dv/dt-filter are

\[
P_{i, f} = P_{\text{HB}} + P_C + P_L.
\]

Neglecting the filter capacitor volume (high capacitance density), only the volume of the heat sink to dissipate the filter losses and the filter inductor volume have to be considered. The former can be approximated using the so-called Cooling System Performance Index (CSPI) [34] with a typical CSPI of 20 W/(K · dm$^3$), an assumed heat sink temperature of $\vartheta_{\text{HS}} = 85$ °C and an ambient temperature $\vartheta_{\text{amb}} = 40$ °C using

\[
R_{\text{th, HS, f}} = \frac{\vartheta_{\text{HS}} - \vartheta_{\text{amb}}}{3 \cdot P_{i, f}}.
\]

\[
V_{\text{HS, f}} = \frac{1}{\text{CSPI} \cdot R_{\text{th, HS, f}}} \propto P_{i, f}.
\]

As derived in Section II-A, the filter inductance directly follows from the selected dv/dr limit. For the given application the maximum phase RMS current equals $I_{u, \text{ rms, max}} = 18.3$ A and the peak current follows from $\hat{i}_{u, \text{ max}}$ in (11) and the additional current peak $\Delta i_u$ to charge $C_i$. Even though the VSD is primarily operating in part-load, the filter inductor has to be designed for full-load, i.e., for an RMS current rating $I_{\text{rated}} \geq I_{u, \text{ rms, max}}$ (as mentioned above, the contribution of the current pulse $\Delta i_u$ on the total RMS current is found to be
negligible) and for a saturation current $i_{\text{sat}} \geq i_{u,\text{max}} + \Delta i_{u}$.

The dots in the $n_P$-Pareto optimization in Fig. 4 show the design trade-off for the LC-dv/dt-filter for dv/dt limits between 3 V/ns and 15 V/ns with the total VSD power density $\rho$ and the part-load efficiency $n_{\text{eff,kW}}$ at $P_{\text{M,nom}} = 8$ kW. The filter capacitance $C_f$ is fixed to a value of 1.12 nF (two 560 pF capacitors in parallel, connected to the positive and negative DC-link rail) $a)$ to fulfill the filter output impedance criterion ($Z_{o,f} < Z_{M,U-VNPE}$) and $b)$ to minimize the load independent losses $P_{C_l}$. Generally, high dv/dt limits are accompanied by a higher power density due to the smaller $L_f$. At the same time, a low $L_f$ results in lower conduction losses $P_{L_l}$, hence also the efficiency improves (the other loss components in (14) are independent of the selected dv/dt limit). For IMDs, ideally the design with the highest power density is chosen to facilitate integration (highlighted with black circles for each dv/dt).

**C. LOSSES AND VOLUME OF THE GATE DRIVER BASED dv/dt-LIMITATION**

The GD-based dv/dt limitation leads to increased switching losses $E_{\text{sw, GD}}$, which for a switched current $i_u$ have been derived in [23] as

$$E_{\text{sw, GD}} = k_0 + k_{\text{on}} \cdot i_u + \begin{cases} 0 & \text{if } i_u \leq i_k \\ k_{\text{off}} \cdot (i_u - i_k) & \text{if } i_u > i_k \end{cases} \quad (17)$$

with $k_{\text{on}} = \frac{k_{\text{on}}}{} V_{\text{DC}} \frac{d\theta}{d\theta}$ and $k_{\text{off}} = \frac{1}{2} V_{\text{DC}}^2 \frac{d\theta}{d\theta}$. The factor $k_{\text{WF}} = 1.35$ is empirically determined and corrects inaccuracies due to the straight-line approximation of the voltage transient between 10% and 90% of $V_{\text{DC}}$, only of a concern for the turn-on transition [23]. Note that the term $k_2$ considering losses scaling quadratically with the switched current is neglected, since the linearly scaling loss contribution arising from the limited dv/dt is clearly dominating the overlap losses. Moreover, the ZVS losses attributed to the resonant charging/discharging of the transistor output capacitance $C_{\text{oss}} = C_{\text{DS}} + C_{\text{GD}}$ are neglected.

Evaluating (17) for a sinusoidal phase current with amplitude $\hat{i}_u$, including the semiconductor conduction losses and again neglecting the current ripple, the total per-phase losses $P_{l,GD}$ for the GD-based dv/dt-limitation are

$$P_{l,GD} = \frac{1}{2} R_{\text{DS,on,100}} i_u^2 + f_{\text{sw}} \left( k_0 + \frac{2}{\pi} k_{\text{on}} \hat{i}_u \right)$$

$$+ \begin{cases} 0 & \text{if } \hat{i}_u \leq i_k \\ \frac{2 f_{\text{sw}} k_{\text{off}}}{\pi} \sqrt{\hat{i}_u^2 - i_k^2} - i_k \arccos \left( \frac{i_k}{\hat{i}_u} \right) & \text{if } \hat{i}_u > i_k \end{cases} \quad (18)$$

where the values of $i_k$ for the two cases with a dv/dt-limitation of (I) 5 V/ns and (II) 12 V/ns are listed in Table 2. For a given $i_u$, $P_{l,GD}$ scales inversely proportional with the selected voltage slew rate dv/dt, which is intuitively clear that faster voltage transients lead to lower overlap losses.

Since the volume of the gate resistor and additional Miller capacitor is negligible (cf. Fig. 3(b)), consequently, only the heat sink volume has to be considered, which can be calculated with (15) and (16), replacing $P_{l,f}$ with $P_{l,GD}$ (cf. Fig. 7). The squares in Fig. 4 nicely show the trend of higher efficiency at higher voltage slew rates. Moreover, given the direct relation between losses and (heat sink) volume, there is no Pareto front and/or Pareto-optimal design but more efficient designs are automatically more compact. If no dv/dt-limiting would be employed, the losses would be solely defined by the characteristics of the utilized power semiconductor (conduction and switching losses $P_{l,HB}$ according to (13)) and for the given specifications result in an efficiency limit of $n_{\text{max,8 kW}} = 99.6\%$ (indicated with the dashed line in Fig. 4) to which the GD-based dv/dt-limiting approach converges for very high slew-rate limits.

**IV. COMPARATIVE EVALUATION**

Having defined the inverter loss and volume models considering both dv/dt-limiting approaches, the question therefore arises, which of the two concepts should be selected to limit the dv/dt of a three-phase VSD inverter system with a certain phase current amplitude $\hat{i}_u$ to a specific value (e.g., 5 V/ns for state-of-the-art electric motors or 12 V/ns for future motors with reinforced insulation). To not only theoretically but also experimentally verify the analyses, a characteristic three-phase SiC-based VSD to be integrated into a motor housing is designed and constructed as depicted in Fig. 5, in accordance with the specifications from Table 1. The VSD is equipped with a DRC-damped passive LC-filter for dv/dt-limitation but could alternatively also be realized without the filter as GD-based dv/dt-limitation. Two PCBs are vertically stacked to facilitate a compact and phase-modular realization. On the power PCB, besides the power semiconductors (16 mΩ, 1200 V SiC MOSFETs),
the $LC$-$dv$/dt-filter as well as voltage and current measurements are located. Table 2 lists the important component values and parameters for a nominal voltage slew rate of (I) 5 V/ns and (II) 12 V/ns. The power semiconductors as well as the filter inductors and damping resistors are thermally attached to a thin-finned heat sink with forced cooling. The overall system dimensions are 100 mm × 90 mm × 37 mm (3.94 in. × 3.54 in. × 1.46 in. [L × W × H]); including the control board featuring a Field-Programmable Gate Array (FPGA) and the heat sink), which corresponds to a total boxed volume of $V_{boxed} = 0.333$ dm$^3$ (20.3 in$^3$) and thereby a power density of 30 kW/dm$^3$ (493 W/in$^3$). The low inverter volume greatly facilitates integration directly into the machine, in which case the heat sink that contributes approximately one third of the total volume (height of 12 mm [0.47 in.], 0.108 dm$^3$ [6.56 in$^3$]) could potentially be omitted, if the machine housing would be used for passive cooling of the inverter [35]. Moreover, the control board - currently placed as external module and included in the boxed volume - could be fully integrated, enabling a pure inverter power density of roughly 61 kW/dm$^3$ (1000 W/in$^3$).

### TABLE 2. Components and Parameters of the Hardware Realization of the Three-Phase SiC-Based VSD With a Voltage Slew Rate of (I) 5 V/ns and (II) 12 V/ns for Both Considered $dv$/dt-Limitation Concepts

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Part</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Semiconductor</td>
<td>$1.2$ kV, 16 mΩ, SiC</td>
<td></td>
</tr>
<tr>
<td>$k_0$</td>
<td>$312.2$ μA</td>
<td></td>
</tr>
<tr>
<td>$\nu_{th}$</td>
<td>$2.5$ V</td>
<td></td>
</tr>
<tr>
<td>$9m$</td>
<td>$53$ Ω</td>
<td></td>
</tr>
<tr>
<td>$C_{dQ,GD}$</td>
<td>$16$ pF</td>
<td></td>
</tr>
<tr>
<td>Gate Driver</td>
<td>±6 A</td>
<td></td>
</tr>
<tr>
<td>Filter Capacitor $C_L$</td>
<td>$1.12$ nF</td>
<td></td>
</tr>
<tr>
<td>Damping Cap. $C_{P,n}$</td>
<td>$7$ nF</td>
<td></td>
</tr>
<tr>
<td>Clamping Diode $D_{P,n}$</td>
<td>$1.2$ kV, 5 A, SiC</td>
<td></td>
</tr>
<tr>
<td>Filter Inductor $L_f$ (I)</td>
<td>$11.2$ μH</td>
<td></td>
</tr>
<tr>
<td>Damp. Res. $R_{D,n}$ (I)</td>
<td>$15$ Ω</td>
<td></td>
</tr>
<tr>
<td>Filter Inductor $L_f$ (II)</td>
<td>$1.8$ μH</td>
<td></td>
</tr>
<tr>
<td>Damp. Res. $R_{D,n}$ (II)</td>
<td>$6$ Ω</td>
<td></td>
</tr>
<tr>
<td>Miller Capacitor $C_M$</td>
<td>0 pF</td>
<td></td>
</tr>
<tr>
<td>$R_{G,n}$ / $R_{G,n}$ (I)</td>
<td>$56$ Ω / 43Ω</td>
<td></td>
</tr>
<tr>
<td>$R_{G,n}$ / $R_{G,n}$ (II)</td>
<td>$151$ Ω / 15Ω</td>
<td></td>
</tr>
<tr>
<td>Pos. GD Sup. $V_{GD,p}$</td>
<td>$-15$ V</td>
<td></td>
</tr>
<tr>
<td>Neg. GD Sup. $V_{GD,n}$</td>
<td>$-4$ V</td>
<td></td>
</tr>
<tr>
<td>$I_u$ (I)</td>
<td>6.3 A</td>
<td>(calculated with (5))</td>
</tr>
<tr>
<td>$I_u$ (II)</td>
<td>18.2 A</td>
<td>(calculated with (5))</td>
</tr>
</tbody>
</table>

**FIGURE 5.** Photo of the ultra-compact 10 kW SiC-based three-phase VSD featuring a damped $LC$-$dv$/dt-filter to limit the voltage slew rate to a nominal value of 5.6 V/ns, i.e., suitable for state-of-the-art electric machines. The most important building blocks are labeled.

**FIGURE 6.** Per-phase losses of the loss-optimal $dv$/dt-limitation concept for a $dv$/dt-limit between 3 V/ns and 15 V/ns and phase current amplitudes $i_u \in [0 \text{ A}, 25 \text{ A}]$ (part-load and full-load operation). The thick black line depicts the boundary below which the $LC$-$dv$/dt-filter has lower losses compared to the GD-based limitation. In case of the $LC$-$dv$/dt-filter, $C_f = 1.12 nF$ and $I_u$ is always chosen for $i_u = 25.9 A$ (full-load).

### A. PER-PHASE LOSS COMPARISON

To promote motor integration of the inverter, the most compact design of the $LC$-$dv$/dt-filter is selected from the Pareto front in Fig. 4. Compared to the most efficient (lowest loss) design, the loss penalty is relatively low, whereas considerable volume benefits are apparent. Hence, a single Pareto-optimal filter design results for each $dv$/dt value for the damped $LC$-$dv$/dt-filter approach (highlighted with black circles in Fig. 4), which is compared to the GD-based limitation in terms of per-phase losses. Fig. 6 shows the calculated per-phase losses for both limiting approaches under full- and part-load operation ($i_u \in [0 \text{ A}, \ldots, 25 \text{ A}]$ with the $LC$-$dv$/dt-filter always designed for $i_u = i_{u,max} = 25.9 A$) for different voltage slew rates $dv$/dt from 3 V/ns to 15 V/ns. For each combination of $i_u$ and $dv$/dt, the losses of the better-performing approach are depicted. There exists a clear boundary between the $LC$-$dv$/dt-filter and the GD-based limitation (thick black line), where the former is best-suited for slow transitions at high $i_u$ and the latter is ideally used for higher $dv$/dt values. In particular for $dv$/dt $> 11$ V/ns the GD-based limitation leads to lower losses (< 25 W per phase) for full- and part-load operation. For lower $dv$/dt values there exists a certain boundary current amplitude $i_{B,lim}$ below which the GD-based $dv$/dt-limitation outperforms the $LC$-$dv$/dt-filter thanks to its lower part-load losses, e.g., $i_{B,5 V/ns} = 10.5 A$ for a voltage slew rate $dv$/dt $= 5$ V/ns, since the filter has always a constant loss offset of $P_{offset} = 11.5 W$ for $C_f = 1.12 nF$, $V_{DC} = 800 V$, $f_{sw} = 16$ kHz (dominant over the inductor conduction losses $P_{I,conduction}$). Conversely, for part-load operation with $i_{u,nom} = 20 A$,
the \( LC-\text{dv/dt} \)-filter outperforms the \( \text{GD-based limitation} \) for voltage slew rates below 9 V/ns because the losses of the latter scale inversely proportional to the \( \text{dv/dt} \) and thus exceed the constant \( P_{\text{C1}} \) losses of the former. Therefore, in theory, a boundary line parametrization \( \dot{i}_u = \alpha \cdot \text{dv/dt} \) with \( \alpha = \text{const.} \) would be expected. The deviation from this linear relationship results from the selection of discrete filter inductors from commercially available components, which leads to discontinuities in the \( LC-\text{dv/dt} \)-filter losses.

**B. PER-PHASE VOLUME COMPARISON**

A similar boundary is found in Fig. 7 when comparing the functional volume of the two limiting concepts (blue and orange lines for the \( LC-\text{dv/dt} \)-filter and \( \text{GD-based limitation} \), respectively) for the maximum phase current amplitude \( \dot{i}_u,_{\text{max}} = 25.9 \text{ A} \) (part-load operation does not change the volume, since the VSD must be designed to handle the full power of \( P_{\text{M, max}} = 10 \text{ kW} \)). For voltage slew rates above 9.4 V/ns the \( \text{GD-based dv/dt-limitation} \) can be realized with a lower volume (i.e., lower heat sink volume due to the lower losses with the direct relationship via the CSPI, cf. (16)), whereas in case of the \( LC-\text{dv/dt} \)-filter there is always a certain volume offset given by the filter inductors, which of course can be realized more compact for small inductance \( L_\ell \) (high \( \text{dv/dt} \)), but the volume reduction saturates due to mechanical constraints (current carrying conductors, minimum core thickness, etc.). The discontinuities in case of the \( LC-\text{dv/dt} \)-filter again result from discrete component selection.

**C. EXPERIMENTAL VERIFICATION**

To experimentally verify the occurrence of the above discovered boundary, the occurring per-phase losses have been measured on the hardware prototype equipped with either of the two described \( \text{dv/dt-limiting concepts} \). The \( LC-\text{dv/dt} \)-filter is realized with \( C_l = 1.12 \text{ nF} \) (two R76QF056050H0J capacitors in parallel, one connected to the positive and one to the negative DC-link rail) and \( L_\ell = 11.2 \mu \text{H} \) (two SRPI770TA-5R6M inductors in series) or with \( C_l = 1.12 \text{ nF} \) and \( L_\ell = 1.8 \mu \text{H} \) (CMLS136E-1R8MS) for a nominal \( \text{dv/dt} \) of 5.6 V/ns and 14 V/ns, respectively. Note that realizing \( C_l \) with two capacitors connected to the positive and negative DC-link rail does not influence the total energy dissipation, but results in a more symmetric layout and thus more symmetric (parasitic) ringing conditions. In both cases (\( \text{dv/dt} \) of 5.6 V/ns and 14 V/ns), the damping network is composed of two 10 nF capacitors \( C_p \) and \( C_n \) and implements critical damping with \( R_p = R_n = \frac{1}{\sqrt{LC}} \) (\( C_p \) denotes the additional damping capacitance in parallel to the damping resistor, cf. Fig. 2(a)). SiC Schottky diodes with low capacitive charge (24 nC, \( \approx 0.3 \text{ W} \) losses for \( V_\text{DC} = 800 \text{ V} \) and \( f_\text{sw} = 16 \text{ kHz} \) and low leakage current (12 \( \mu \text{A} \)) are used for \( D_p \) and \( D_n \) (IDM05G120CS). Due to component tolerances, additional parasitic capacitances and inductances (PCB, connections), finally, the desired voltage slew rates of 5 V/ns and 12 V/ns result (cf. Table 1). Note that for a smaller \( L_\ell \) (higher \( \text{dv/dt} \)) the impact of parasitic inductances and capacitances is more pronounced (larger deviation of the actual \( \text{dv/dt} \) from the nominally set value) due to the small nominal value of \( L_\ell \).

The \( \text{GD-based limitation} \) is implemented with increased gate turn-on and turn-off resistances of \( R_{G, on}/R_{G, off} = 56 \Omega/43 \Omega \) and \( 15 \Omega/15 \Omega \) (\( C_{GD} = 0 \text{ pF} \) for a \( \text{dv/dt} \) of 5 V/ns and 12 V/ns, respectively (cf. Table 2). Using (5) with \( v_\text{th} = 2.5 \text{ V}, V_{\text{GD,n}} = -4 \text{ V} \), \( C_{\text{dQ,DS}} = 320 \text{ pF} \) and \( C_{\text{dQ,GD}} = 16 \text{ pF} \) the “kink” current is \( I_k = 6.3 \text{ A} \) (5 V/ns) and \( I_k = 18.2 \text{ A} \) (12 V/ns) for the two cases.

Fig. 8 shows (a) the calculated and measured efficiency and (b) the per-phase losses for \( \text{dv/dt} = 5 \text{ V/ns} \) (calculated: dotted lines; measured: circles) and for \( \text{dv/dt} = 12 \text{ V/ns} \) (calculated: continuous lines; measured: diamonds) for the \( LC-\text{dv/dt} \)-filter (blue) and the \( \text{GD-based limitation} \) (orange) for phase current amplitudes \( \dot{i}_u = (5 \text{ A}, 10 \text{ A}, 15 \text{ A}, 20 \text{ A}, 25 \text{ A}) \). These operating points are also indicated in Fig. 6. The losses are measured electrically with a precision power analyzer (Yokogawa WT3000) and show good alignment with the calculations, in particular in case of the \( \text{GD-based limitation} \), whereas in case of the \( LC-\text{dv/dt} \)-filter and for low \( \dot{i}_u \) a certain mismatch is observed. This is primarily explained with the simplified assumption of zero current ripple in the calculation, essentially overestimating the switching losses at low currents (and hence the calculated total losses), since in practice more Partial-Hard Switching (PHSW) and Soft Switching (SSW) transitions occur, which generate lower losses compared to the assumed HSW transitions. In case of the \( \text{GD-based limitation} \) this effect is less severe, since also the PHSW and SSW transitions lead to overlap losses (for \( \dot{i}_u > I_k \)).

As expected from the observations in Fig. 6 based on calculated losses, for a \( \text{dv/dt} \) of 12 V/ns the \( \text{GD-based limitation} \) is always more efficient (lower losses) compared to the \( LC-\text{dv/dt} \)-filter, e.g., for the nominal phase current \( \dot{i}_u,_{\text{nom}} = 20.7 \text{ A} \) the measured losses are 20.5 W with the \( \text{GD-based limitation} \) and 23.6 W with the \( LC-\text{dv/dt} \)-filter. For a voltage slew rate \( \text{dv/dt} = 5 \text{ V/ns} \), the boundary current \( \dot{i}_u,_{5 \text{ V/ns}} \) is verified, i.e., for currents \( \dot{i}_u > 10.5 \text{ A} \) the \( LC-\text{dv/dt} \)-filter has lower losses than the \( \text{GD-based limitation} \) (27.6 W versus 36 W for \( \dot{i}_u,_{\text{nom}} \)). The filter losses do not significantly change.
between \( \frac{dv}{dt} = 5 \, V/\mu s \) (32.3 W for \( \hat{i}_{u,\text{max}} = 25.9 \, A \), i.e., \( \eta = 99.18 \% \)) and \( \frac{dv}{dt} = 12 \, V/\mu s \) (28.1 W for \( \hat{i}_{u,\text{max}} = 25.9 \, A \), i.e., \( \eta = 99.29 \% \)) as only the comparably low filter inductor conduction losses differ, whereas with GD-based limitation for the same current, the losses considerably increase for a low \( \frac{dv}{dt} \) (45.8 W for 5 V/\mu s and 25.9 W for 12 V/\mu s). This trend is also highlighted in Fig. 4 for the two exemplary voltage slew rates of 5 V/\mu s and 12 V/\mu s (thick circles/diamonds), to demonstrate that a higher efficiency (and power density) is achieved with the \( LC-dv/dt \)-filter for 5 V/\mu s, and with the GD-based limitation for \( dv/dt = 12 \, V/\mu s \). A very interesting property of the GD-based \( dv/dt \)-limitation is the high part-load efficiency, since the main loss component (overlap losses) scales linearly with the switched current (and thus \( \hat{i}_{u} \) and \( P_{\text{out}} \)), whereas the \( LC-dv/dt \)-filter has a constant loss offset \( P_{C_f} \), which inherently degrades efficiency at low output power.

Therefore, in future traction applications allowing voltage slew rates above 10 V/\mu s, a GD-based \( dv/dt \)-limitation is favorably used considering full-load and part-load efficiency as well as functional volume. For state-of-the-art applications operating with low \( dv/dt \)-values of, e.g., 5 V/\mu s, an \( LC-dv/dt \)-filter typically offers higher efficiency and lower volume unless the required mission profile contains mainly part-load operation below 40 \% of full-load \( (\hat{i}_{u} < 10 \, A) \), in which case also for low \( dv/dt \)-values the GD-based limitation becomes more attractive.

**D. THREE-PHASE VSD OPERATION WITH \( dv/dt \)-FILTER**

Finally, the three-phase with operation of the VSD depicted in Fig. 5 connected to a state-of-the-art motor (Siemens 1FT7084 [26]) is verified. Considering the power level of 10 kW and a required \( dv/dt \)-rating below typically 6 V/\mu s, the \( dv/dt \)-limitation is preferably realized with an \( LC \)-filter based on the theoretical findings from Fig. 6 and according to the experimental results in Fig. 8.

![FIGURE 9. Measured voltage slew rate of the rising edge in phase u with the selected PMSM connected to the output. The effective machine capacitance slightly reduces the nominally set \( dv/dt \) (10 \% to 90 \% of \( V_{DC} \)) from 5.6 V/\mu s to 4.71 V/\mu s (approximately 15 \% decrease). The small overshoot \( \Delta v_{u,n} \approx 100 \) V resulting from the finite filter resonance damping is further indicated.](image)

Fig. 9 shows the measured voltage slew rate of > 1 million rising transitions of phase \( u \) (color-coded intensity grading) with the PMSM directly connected to the output (IMD). The measured \( dv/dt \) of 4.71 V/\mu s is lower than the nominally set \( dv/dt \) (10 \% to 90 \% of \( V_{DC} \)) from 5.6 V/\mu s to 4.71 V/\mu s (approximately 15 \% decrease). The small overshoot \( \Delta v_{u,n} \approx 100 \) V resulting from the finite filter resonance damping is further indicated.
An additional effective capacitance $C_{\text{add}} \approx 460 \text{ pF}$ explains the reduction of the $dv/dt$ to 4.71 V/ns, where the machine itself contributes 300 pF as described in Section II-A, and the rest is attributed to component tolerances and impact of connections and PCB parasitics.

While it is true that the machine capacitance influences the set $dv/dt$ and therefore, a fully machine-independent inverter and filter design is not possible, a lower than expected $dv/dt$ is typically not critical, since it only reduces the detrimental effects of overvoltage, partial discharges and the like. At the same time, the additional losses (compared to operating the VSD without any $LC$-$dv/dt$-filter) are only defined by $C_t$ and $L_t$ and not the machine (the machine capacitance and - if present - the cable capacitance are anyway charged and discharged with the switching frequency, regardless of a $dv/dt$-limiting circuit). The impact of the load on the resulting voltage slew rate could obviously be minimized by increasing $C_t$, which, however, would directly increase the filter losses. Fig. 9 further indicates the slight voltage overshoot $\Delta v_{u,p,n} \approx 100 \text{ V} (12.5 \% \text{ for } V_{\text{DC}} = 800 \text{ V})$ resulting from the finite filter resonance damping with $C_{\text{p,n}}$, $D_{\text{p,n}}$ and $R_{\text{p,n}}$.

Fig. 10 shows the three phase currents of the VSD demonstrating operation at full load of $P_{\text{M, max}} = 10 \text{ kW}$ ($i_u = i_v = i_w = 25.9 \text{ A}$). For nominal load ($P_{\text{M, nom}} = 8 \text{ kW}$ with $i_{u,\text{nom}} = 20.7 \text{ A}$), measured overall system losses of $P_{\text{loss, tot}} = 580 \text{ W}$ and an efficiency of $\eta_{\text{nom, tot}} = \eta_{\text{nom, VSD}} \cdot \eta_{\text{nom, PMSM}} = 93.24 \%$ result (including the connected PMSM). Considering the nominal machine efficiency of 94% [26], the overall VSD losses can be approximated with $P_{\text{loss, VSD}} \approx 70 \text{ W}$ and $\eta_{\text{ nom, VSD}} = 99.19 \%$, which agrees very well with the calculations and the experimental loss measurements (cf. the highlighted point with $\star$ in Fig. 8(a)).

V. CONCLUSION

SiC power MOSFETs are promising candidates to improve the efficiency and power density of electric motor-driven systems and further to promote the emerging trend of full integration of the inverter system into the motor housing. A primary advantage of SiC power semiconductors is their low specific switching losses that allow to design VSD inverter systems with considerably higher switching frequencies. This comes, however, at the expense of very fast voltage transients (high $dv/dt$). The voltage slew rate applied to the motor must be limited to prevent surge overvoltage, unequal voltage distribution across the windings or inadmissibly high bearing currents that all lead to accelerated aging and/or destruction of the motor. For a typical industry application of a 10 kW VSD operating primarily under part-load (80 % rated load), this article compares two approaches to limit the applied $dv/dt$, namely a passive $LC$-$dv/dt$-filter (single-stage $LC$-filter) and a GD-based $dv/dt$-limitation. While state-of-the-art motors demand voltage slew rates below typically 6 V/ns, future motors with reinforced insulation are forecasted to withstand a $dv/dt$ of up to 15 V/ns, and therefore the question arises, which limiting concept is best-suited for a VSD for a certain $dv/dt$ and phase current amplitude (full- or part-load).

The passive $LC$-$dv/dt$-filter mainly contributes a constant loss offset and low current/load dependent losses, whereas the GD-based limitation generates voltage-current overlap losses that scale linearly with output power and the voltage transition times. It turns out that the latter is best-suited for $dv/dt$-limits above 11 V/ns under full- and part-load operation. For each $dv/dt$-limit below 11 V/ns there exists a boundary for the phase current amplitude above which the $LC$-$dv/dt$-filter is preferably used, since the overlap losses of the GD-based limitation dominate the (roughly) constant losses of the filter. For part-load operation with a phase current amplitude below the boundary, however, the GD-based limitation has lower losses. In any case, it is possible to realize a VSD with an efficiency above 99 % for nominal load operation ($8 \text{ kW}$). Similarly to the losses, the functional volume (considering the additional components as well as the required cooling to dissipate the additional losses) of the GD-based limitation is lower for high slew rates due to the lower losses compared to the $LC$-$dv/dt$-filter.

The theoretical findings are experimentally verified on an ultra-compact 10 kW $\text{tp}$ SiC-based VSD as IMD for a state-of-the-art PMSM, which according to the findings of this work, features a passive $LC$-$dv/dt$-filter to limit the voltage slew rate to a nominal value of 5.6 V/ns. With a power density of $30 \text{ kW/dm}^3$ ($493 \text{ W/in}^3$) it facilitates full integration of the inverter into the motor housing. The resulting measured $dv/dt$ (4.71 V/ns) during operation with the PMSM is about 15 % lower than the nominal value, attributed to the additional capacitive loading from the PMSM, which slightly alters the filter corner frequency. Nevertheless, a $dv/dt$ below the critical limit is non-problematic, as it further reduces the detrimental effects arising from fast voltage slew rates, while the losses are solely defined by the actual $LC$-filter components. The same system for a next-generation motor with higher $dv/dt$-rating would preferably be realized with a GD-based limitation, which not only reduces the total losses but also comes with an additional increase in power density, since no additional passive components must be placed. For Low-Voltage (LV) MOSFETs there exist already highly integrated “smart” GDs

![Image](image_url)
that allow to actively (programmatically) set the voltage slew rates without influence of external parasitic effects [36] and it is very likely that in the near future similar concepts will be available for High-Voltage (HV) MOSFETs (≥ 1.2 kV blocking voltage capability).

**APPENDIX**

In this Appendix the considered PMSM is characterized with impedance measurements and an intuitive, physically explainable lumped-element equivalent circuit is derived to justify the capacitor selection in the LC-\(\frac{dv}{dt}\)-filter design. From (4) follows a filter resonance frequency range between 760 kHz and 3.8 MHz for a \(\frac{dv}{dt}\)-limitation range between 3 V/ns and 15 V/ns. The impact of the machine on the voltage slew rate can be quantified with a model that is valid in this frequency range. Based on impedance measurements between one machine terminal (e.g., \(U\)) and the remaining two terminals (shorted to PE, e.g., \(V\) and \(W\) shorted to PE) as depicted with the blue curves in Fig. 11, the lumped-element circuit model of Fig. 12 with indicated component values results. The first and second parallel resonances at around 130 kHz and 340 kHz, respectively, are modeled with \(L_{m1}\) and \(C_{p1}\) (damping \(R_{p1}\)) and \(L_{m2}\) and \(C_{p2}\) (damping \(R_{p2}\)). The damped series resonance in between is composed of the combination of the six elements. The final series resonance at around 25 MHz (not visible in the measurements of Fig. 11) is modeled with \(L_{m3}\) and the series connection of \(C_{p1}\) and \(C_{p2}\) (damping \(R_{m3}\)). Finally, the capacitive coupling from the terminals and windings to the housing (PE) is modeled with the capacitance \(C_{p3}\). Despite its simple structure and the absence of frequency dependent machine inductances and resistances that would be required for accurate high-frequency characterization in the multi-ten-MHz range [19], this model accurately replicates the PMSM impedance in the frequency range of interest up to approximately 4 MHz (highlighted in light blue in Fig. 11). Observing the almost entirely capacitive nature of \(Z_{U-VWPE}\) in the highlighted frequency range of interest, the approximation of the PMSM impedance as single 300 pF capacitance from Section II-A to facilitate the filter design is therefore justified.

Fig. 11 further highlights the impact of a 10 m long shielded motor cable (Siemens 6FX5002-5DN56-1BA0) on the resultant impedance \(Z_{U-VWPE}\) (measurement: yellow). For the calculation model (purple curve), the cable is treated as series of ten distributed \(RLC\)-elements with 0.35 \(\Omega\), 154 nH, 170 pF each. In the highlighted frequency range the simplified approximation with a constant capacitance (2 nF; 1.7 nF from the 10 m cable and 300 pF from the PMSM) is clearly not valid anymore, since the first cable resonance occurs at 4 MHz, characterized by a drastic drop of the impedance. This is manifested in Fig. 13(a) that shows the simulated \(\frac{dv}{dt}\) of a voltage transient in one of the VSD bridge-legs compared to the set nominal values (\(C_{filt} = 1.12\ \text{nF}\) and \(L_{filt}\) resulting from (4)) in case of the unloaded filter (no machine; blue), a connected PMSM without motor cable (orange) and
a PMSM connected via a 10 m long shielded motor cable (yellow). Fig. 13(b) nicely shows that in case of a connected PMSM without motor cable the dv/dt-reduction below the set value can be explained with the additional effective machine capacitance of 300 pF calculated according to (19). If in addition a 10 m long motor cable is added, the resulting “cable-PMSM”-behavior is not purely capacitive anymore in the frequency range of interest, and the calculated additional capacitance to get the dv/dt from the yellow curve in Fig. 13 (a) is larger than the theoretical 2 nF (cable + PMSM) due to the “cable-PMSM” resonance that is located close to the filter resonance frequency. In any case, the dv/dt is always lower than the nominally set value and therefore allows safe operation of the machine.

REFERENCES


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