Comparison of Performance and Realization Effort of a Very Sparse Matrix Converter to a Voltage DC Link PWM Inverter with Active Front End

Simon Round∗ Non-member
Frank Schafmeister∗ Non-member
Marcelo Heldwein∗ Non-member
Eduardo Pereira∗ Non-member
Leonardo Serpa∗ Non-member
Johann Kolar∗ Member

This paper undertakes a comparison of the very sparse matrix converter (VSMC) and the back-to-back voltage DC-link converter (BBC) for a permanent magnetic synchronous motor drive application. The VSMC has the same functionality as the conventional matrix converter but a reduced number of switches and lower control complexity. The two converters are designed, using the same IGBT power modules, with a switching frequency of 40 kHz and a thermal rating of 6.8 kW at an ambient temperature of 45 °C. From the design, the volume of the VSMC is 2.3 liters and is half that of the BBC. The efficiency for the VSMC at full load is 94.5% compared to 92% for the BBC. At very low output frequencies the output current of the VSMC can be increased by 25% above nominal compared to a 54% decrease for the BBC. Overall the VSMC offers advantages in volume and efficiency for motor drive applications requiring switching frequencies above 10 kHz.

Keywords: matrix converter, back-to-back converter, efficiency comparison, volume comparison, converter design

1. Introduction

Traditional three-phase AC motor drive systems are constructed using a six-switch inverter, an uncontrolled rectifier mains connection and large electrolytic DC-link capacitors. Although the drive system is able to provide variable frequency and voltage to the motor at a high efficiency, the mains input currents are non-sinusoidal and the power flow is unidirectional. The matrix converter is an alternative topology that directly produces a variable amplitude and frequency three-phase output from a three-phase input source without any energy storage in a DC-link. In addition to a unity power factor mains current and bi-directional power flow, the main passive components the matrix converter has are small AC filtering capacitors, therefore the matrix converter is sometimes referred to as an “all silicon converter” (1)-(4). To achieve an equivalent functionality to the matrix converter, using more traditional converter topologies, requires a two-stage AC/DC/AC conversion process, where two voltage DC-link PWM converters are connected in a back-to-back configuration (BBC) as shown in Fig. 1(c). This paper undertakes a comparison of the matrix converter and BBC in terms of compactness, which includes the EMI filtering requirements, efficiency and torque rating for a permanent magnetic AC motor drive.

The conventional matrix converter (CMC) employs nine bi-directional switches (Fig. 1(a)), each presently constructed from two IGBTs and two diodes, to connect the input phases to the output phases (5). The use of the resulting 18 IGBTs and 18 diodes allows the selective turn-on of the switch for each current direction using a safe commutation strategy. The sparse matrix converter (SMC), implemented with 15 switches and not considered further in this paper, and very sparse matrix converter (VSMC), shown in Fig. 1(b), have been proposed (5). In the case of the VSMC the number of controlled switches reduces to 12 and results in an output inverter stage that is the equivalent to the conventional BBC implementation. The (V)SMC are functionally equivalent to the CMC but the (V)SMC offers a lower realization effort and less control complexity. In (6) Bernet et. al. compares the CMC and the BBC in terms of component count and losses. Therefore in this paper the BBC will be compared against the VSMC since the VSMC has the same number of switches as the BBC. The results obtained will be discussed in relation to the findings of Bernet.

In order to perform a converter comparison for a motor drive application, the same motor specification can not be used for both converter systems as this would disadvantage either of the converter types, depending on the motor specification. This can be explained by considering that in the case of the BBC, the active front end boosts the DC link voltage above the peak of the maximum operating voltage in order to ensure controllability. Therefore the motor’s nominal
operating voltage can be specified as the highest input voltage minus a control margin. For a constant output power this results in a reduced output current and an increased BBC efficiency compared to the case if a motor with a low voltage mains rating is used.

In the case of the matrix converter the maximum output voltage available is always lower than the input voltage. Therefore the motor specification should have a nominal voltage that is highest achievable output voltage when the matrix converter is operated from the lowest input voltage minus a control margin. This nominal output voltage level is much lower than the output voltage for the case of the BBC. Therefore for the same output power rating the matrix converter’s output current rating is higher and its losses are increased. By selecting a motor with a voltage rating that is suitable for the matrix converter, this would result in a BBC with higher output currents than for the case of a motor with a higher nominal voltage rating. Therefore to make a direct comparison, each converter type requires a special motor design to ensure the efficiency of each converter is maximized.

From Fig. 1(b) it can be seen that the VSMC has a DC link between the input and output stages, although it does not use any energy storage capacitors. To better compare the physical size of the BBC and VSMC, the BBC is considered using the minimum possible DC-link capacitance for normal operation. In Section 2 the basic operation of the VSMC and the BBC, including modulation strategies, and typical voltage and current waveforms are presented. Section 3 presents the analytical calculation of stresses on the converters’ components. The design of each converter, including thermal and EMI filter requirements, is presented in Section 4. The VSMC and the BBC are then evaluated, in terms of calculated efficiency and operating requirements, in Section 5.

2. Basic Principle of Operation

2.1 Matrix Converter For the conventional matrix converter the bi-directional switches must be operated so that at any time two phases of the input are not shorted together and that the output current is not open-circuited. To provide reliable current commutation between the switches a multi-step commutation strategy is employed that measures either

the output phase current or input line-to-line voltage. In contrast the VSMC configuration provides an additional degree of freedom in that the output stage can be switched into free-wheeling operation and this allows the input stage to commutate with zero DC link current. This allows zero switching losses for the input stage.

The matrix converters are limited to producing an output voltage that is 0.866 of the input voltage. Although the matrix converter does allow over-modulation operation, the penalty is an increase in the input current distortion.

For the VSMC, two modulation schemes have been previously presented. In both modulation schemes the commutation of the input stage at zero current can be seen in Fig. 2. The first modulation scheme (MS1) switches the input stage so that the voltage across the DC link goes from...
the highest and second highest positive line-line voltage, and this produces the maximum output voltage range (Fig. 2(a)). The second modulation scheme (MS2) proposed reduces the switching losses significantly for the case where the desired output voltage amplitude is less than half of the input voltage amplitude, e.g. low speed motor operation. In this modulation scheme the input stage switches the lowest positive and second highest input voltage into the DC link (Fig. 2(b)) and the output stage switches the highest and second highest positive line-line voltage. Therefore the switching losses can be reduced if an output stage bridge is not switched in the vicinity of an input phase voltage displacement angle of \( \Phi_2 = 0 \). The output frequency is 100 Hz, the input frequency is 50 Hz and the switching frequency is 40 kHz. From Fig. 3(a) it can be seen that the average DC link current is much higher (factor of \( \sqrt{3} \)) than for the low voltage modulation scheme in Fig. 3(b).

Fig. 3 shows simulated input and output waveforms of the VSMC when operated with the two modulation methods for a modulation index of \( M = 0.1 \) and an output phase displacement angle of \( \Phi_2 = 0 \). The output frequency is 100 Hz, the input frequency is 50 Hz and the switching frequency is 40 kHz. From Fig. 3(a) it can be seen that the average DC link voltage is much higher (factor of \( \sqrt{3} \)) than for the low voltage modulation scheme in Fig. 3(b). These can be determined using either a Fourier transform or an appropriate peak detection method over the entire input voltage fundamental period, as is implemented in the VSMC controller.

The BBC can also operate with unbalanced mains voltage conditions but the degree of unbalance that allows normal operation is dependent on the sizing of the DC-link capacitor. For low values of DC-link capacitance there will be an effect due to the positive or negative DC bus for an interval of \( \pi/3 \).

### 2.1.1 Unbalanced Mains

Under normal operation it is likely that the input supply voltage would contain a degree of unbalance and/or voltage distortion. Conventional matrix space vector modulation methods inherently prevent unbalance and distortion from appearing in the output voltages as long as the instantaneous input voltage amplitude within every pulse period is measured and the modulation index \( M \) (cf. (29)) is dynamically set. However conventional modulation strategies operating under unbalanced mains will affect the input current quality. In particular a minor third order harmonic (about 5.5% for 30% unbalance) will occur in the input current spectrum. For industrial standard applications this level of input current distortion is acceptable. If a high quality input current is desired, such as in aircraft applications, various improved modulation strategies to reduce/eliminate the harmonic components by dynamically modulating the input displacement angle can be applied. Additional computational effort is also required to determine the input voltage fundamental positive and negative sequence components. These can be determined using either a Fourier transform or an appropriate peak detection method over the entire input voltage fundamental period, as is implemented in the VSMC controller.

A general drawback of matrix converters operating under unbalanced/distorted mains is the resulting reduction in the voltage transfer ratio. Since no energy storage exists the maximum output voltage amplitude directly reduces with the minimum radius of the corresponding input voltage space vector locus.

### 2.2 Back-to-Back Converter

The BBC is constructed using a six-switch active rectifier and six-switch inverter connected together with a common DC-link. The rectifier is operated to draw unity power factor sinusoidal currents from the input mains, while the inverter provides the variable frequency and output voltage to the motor. Fig. 5 shows a comparison between the input and output waveforms generated by the BBC compared to the VSMC for nominal operation. In the case of the BBC it can be seen that the converter is operating from a constant DC bus by the level of the output voltage waveforms. As a consequence, considering the same motor output power level, this results in the output motor current being lower than the motor current for the VSMC. The input current waveforms for both converter systems have a very similar shape. The advantage of the BBC over the VSMC is that the output voltage could reach higher levels before going into the over-modulation region due to a higher DC-link voltage, which is produced by the boosting action of the rectifier.

The BBC input and output waveforms have been generated using symmetrical space vector modulation with a zero voltage vector. The input and output pulse patterns directly correspond to the VSMC output stage pulse patterns. Also the same clamping of the bridge leg that is conducting the maximum phase current (c.f. Section 2.1) is applied for the input and output stage of the BBC.

The BBC can also operate with unbalanced mains voltage conditions but the degree of unbalance that allows normal operation is dependent on the sizing of the DC-link capacitor.
where the DC-link voltage could be boosted up further by the BBC rectifier so that the voltage ripple does not have an impact but this is limited by the DC voltage rating of the capacitor. The BBC has a definite advantage over the matrix converter since the BBC has energy storage and can provide full output voltage under unbalanced input voltage conditions.

The input and output switching frequencies can be independently selected to optimize the input inductances, and switching losses. Although having non-synchronized switching frequencies increases the ripple current of the DC-link capacitor. In this comparison it is assumed that the application for both converters is for “more-electric” aircraft where high input frequencies and compact, low-weight designs are required. Therefore the switching frequency for both converters is selected to be 40 kHz.

3. Component Stresses

The stresses on the passive and switching components can be determined using analytical equations. In this section the analytical calculations for conduction and switching losses and passive component stresses are given for the VSMC and BBC. The same approach is used for the VSMC and BBC.

The conduction loss is determined from the average current and forward voltage drop plus the square rms current and differential on-resistance as in (1). These two on-state parameters have been experimentally measured for the IGBTs (index: $S$) and diodes (index: $D$) used to construct the two converters (13).

$$P_{CS/D} = U_{FS/D} \cdot I_{S/D} + r_{S/D} \cdot I_{S/D}^2 \cdot D_{rms}$$

where $U_F$ is the forward voltage drop and $r$ is the differential resistance.

To determine the switching losses the switching behavior of the IGBTs and diodes has been measured (13). To model the energy loss of one single switching action in one IGBT/diode pair a polynomial least-square approximation is used

$$w(u, i) = K_1 ui + K_2 u^2 + K_3 u^3 + K_4 u^4 i + K_5 u^2 i^2$$

where the voltage $u$ corresponds to the DC link voltage and the current $i$ to a phase current being switched.

Global averaging of the energy loss, which considers the $\pi/3$-interval of maximum phase current during which the corresponding VSMC/BBC transistor is clamped and therefore is not subject to any switching losses, gives

$$W = \frac{6}{\pi} \int_0^{\pi/6} \frac{1}{2\pi} \left[ \int_{-\pi/2}^{\pi/2} w(\varphi_1, \varphi_2) d\varphi_2 \right] d\varphi_1$$

and this then leads to the total power loss

$$P_{SW} = f_p \cdot W$$

$$= f_p(K_1 U_{avg} I_{avg} + K_2 U_{avg} I_{avg}^2 + \frac{1}{2} K_3 U_{avg}^2 + K_4 U_{avg} I_{avg}^2 + K_5 U_{avg} I_{avg}^2)$$

where $f_p$ is the switching frequency.

3.1 Very Sparse Matrix Converter

For the VSMC (10) it is important to accurately model the conduction losses of the switches and diodes since there are no rectifier switching losses.

3.1.1 Conduction Losses—Rectifier

The worst operating case for conduction losses is when both the modulation index and output power factor are one (14). In this case the average and rms worst case currents are

$$I_{Sapa} = I_{Dap} = \frac{\sqrt{3} I_2}{2\pi}; I_{Sapa,rms} = I_{Dap,rms} = \frac{\sqrt{3} I_2}{2\pi}$$

$$I_{Dpe} = I_{Dpe,rms} = 0$$

where $I_2$ is the peak output current.

Applying these currents and the two on-state parameters in (1) leads to the specific conduction losses of the three input stage components (IGBT and two diodes). It should be mentioned that an equivalent worst case condition occurs for $\Phi_2 = \pi$ (and/or power factor minus one). In this case the given current values for the two diodes (indices $Dap$, $Dpa$) have to be interchanged, while current value for the transistor stays the same.

The total VSMC rectifier conduction losses are calculated using

$$P_{C,Rex,VSMC} = 6(P_{C,Sapa} + 2P_{C,Dap} + 2P_{C,Dpa})$$

3.1.2 Conduction Losses—Inverter

Since the forward voltage drop and/or the differential resistance of the IGBTs is larger as compared to the diodes the worst operating case with respect to the inverter stage conduction losses occurs when the transistors have the greatest stress. This occurs again for the case of maximum modulation index and a zero output phase displacement angle ($\Phi_2 = 0$). The corresponding average and rms current values are given as

$$\bar{I}_S = \bar{I}_S = \frac{\pi}{2\pi} \cdot \frac{\sqrt{3} I_2}{2\pi}$$

$$\bar{I}_D = \bar{I}_D = \frac{\pi}{2\pi} \cdot \frac{\sqrt{3} I_2}{2\pi}$$

It is worth to mention that the inverter stage diodes have the greatest stress for $\Phi_2 = \pi$. In this case the given current...
values for transistors (index S) and diodes (index D) need to be interchanged.

The conduction losses of the entire inverter stage can be directly calculated by

\[ P_{C,\text{in},\text{VSMC}} = 6(P_{C,S} + P_{C,D}). \]  

#### 3.1.3 Switching Losses—Inverter

Since the rectifier stage switches with zero DC link current only switching losses occur in the inverter stage. The switching losses in the inverter stage for the IGBTs and diodes can be determined with (4) using the global average values for the currents given as

\[ I_{\text{avg}} = \frac{I_2^2}{2\pi}; \quad I_{\text{avg}}^2 = \frac{I_2^2}{2} \cdot \frac{4\pi - 3\sqrt{3}}{24\pi} \]  

and using the global average values of voltage given by

\[ U_{\text{avg}} = \frac{U_1^2}{2\pi}; \quad U_{\text{avg}}^2 = \frac{U_1^2}{2} \cdot \frac{12\pi + 9\sqrt{3}}{8\pi} \]

where \( U_1 \) is the peak input phase voltage.

The total VSMC switching losses can be expressed as

\[ P_{S,w,\text{VSMC}} = 6P_{S,w}. \]  

#### 3.1.4 AC Filter Capacitor Stresses

The stresses on the filter capacitors, in general, are dependent on the rms value of the current since this current is responsible for losses in the capacitor’s ESR. For low output voltage modulation (MS2) the capacitor current stress is increased as compared to the conventional modulation (MS1) and therefore is considered as the worst case for dimensioning purposes

\[ I_{\text{Cfilt,MS2,rms}}^2 = \frac{I_2^2}{2} \cdot \frac{40 - \pi^2}{8\pi^2}. \]

### 3.2 Back-to-Back Converter

The same mathematical model, as for the VSMC, to determine the IGBT/diode conduction and switching losses is used for the BBC.

#### 3.2.1 Conduction Losses—Rectifier

Calculating the IGBT and diode losses requires the average and rms current as given by

\[ I_{S} = \frac{I_2}{M_{Rct}} \quad \frac{2 - \sqrt{3}M_{Rct}}{4\pi} \]

\[ I_{S,rms}^2 = \frac{P_2^2}{M_{Rct}^2} \quad \frac{4\pi - \sqrt{3}(3 + 4M_{Rct})}{24\pi} \]

\[ I_{D} = \frac{I_2}{M_{Rct}} \quad \frac{2 + \sqrt{3}M_{Rct}}{4\pi} \]

\[ I_{D,rms}^2 = \frac{P_2^2}{M_{Rct}^2} \quad \frac{2\pi + \sqrt{3}(3 + 4M_{Rct})}{24\pi} \]

where \( M_{Rct} \) denotes the normalized rectifier stage modulation index defined as

\[ M_{Rct} = \sqrt{3}\frac{\tilde{U}_1}{U} \in [0..1]. \]

From the DC link voltage \( U \) (cf. (26)) and minimum amplitude of the input voltage \( \tilde{U}_1 \) (cf. section 4) the maximum conduction losses for this application occur for a modulation index of

\[ M_{Rct} = 0.73. \]

Accordingly, the device conduction losses of the rectifier stage can be calculated using (1) with (13) and (15). The total conduction losses of the rectifier stage are

\[ P_{C,Rct,BBC} = 6(P_{C,Rct,S} + P_{C,Rct,D}). \]

#### 3.2.2 Conduction Losses—Inverter

As the operating principle of the BBC inverter stage is equivalent to that of the VSMC the worst case conduction losses can be calculated with the identical equations (1), (7) and (8).

#### 3.2.3 Switching Losses

To calculate the switching losses the general formulation given in (4) is used for both rectifier and inverter stages. Since the principle of operation of the BBC rectifier and inverter stages is equivalent to the VSMC inverter stage the BBC switching losses for the IGBTs and diodes can be determined by applying (4) with current average values being identical to those for the VSMC inverter given in (9), where for the BBC rectifier stage \( I_2 \) is substituted with \( I_1 \).

As the DC link voltage \( U \) of the BBC is typical controlled to be a constant value the average voltage values are directly given by

\[ U_{\text{avg}} = U; \quad U_{\text{avg}}^2 = U^2. \]

Since (4) yields the switching losses of just one IGBT/diode pair of one bridge leg, the total BBC switching losses are given by

\[ P_{S,w,BBC} = 6P_{S,w,Ret} + 6P_{S,w,Im}. \]

#### 3.2.4 DC-Link Capacitor Sizing and Stresses

To determine the minimum DC-link capacitor value a formula, based on a DC/DC equivalent model, from pg. 56 of \(^{18}\) is used. This formulation, given by (19), sizes the capacitor to ensure that the capacitor voltage does not fall below a defined minimum value, \( U_{\text{min}} \), during the transient from full regeneration to full motoring.

\[ C_{DC,\text{min}} = \frac{LP_2^2}{2U_1^2} \left[ (\tilde{U}_{1,lt} - U)^2 - (\tilde{U}_{1,lt} + U)^2 \right] \]

\[ \left( U_{\text{min}} + \tilde{U}_{1,lt} \right)^2 - (U + \tilde{U}_{1,lt})^2 \]

\[ \left( U_{\text{min}} + \tilde{U}_{1,lt} \right)^2 - (U + \tilde{U}_{1,lt})^2 \]

\[ \left( \sum \right) \]

where \( L \) is dc equivalent inductance (2 times input inductance, Table 2.2 in \(^{18}\)), \( P_2 \) is the nominal output power, \( \tilde{U}_{1,lt} \) is the peak input line-line voltage, and \( U \) is the DC-link voltage.

To select a suitable capacitor for the link the ripple current the capacitor has to handle must be calculated. Using the method presented in \(^{18}\) the ripple current can be determined from the difference between the rectifier’s ripple current and the inverter’s ripple current.

The value of the DC-link rms current of the rectifier/inverter, calculated over a 60° interval, is given by

\[ I_{\text{rms,Ret/In}}^2 = \frac{5}{4\pi}I_{2/2}^2. \]

Neglecting the power loss in the inverter/rectifier, the dc component of the DC-link side rms current can be obtained, based
on the power balance, as

$$P_{\text{Rt/In}} = \frac{3}{2} P_{\text{L/1/2}}.$$  

(21)

Finally, the rms value of the inverter/rectifier current ripple is calculated from

$$I_{\text{Rms,Rt/1m}} = \sqrt{P_{\text{Rms,Rt/1m}}^2 - P_{\text{Rt/1m}}^2}.$$  

(22)

In order to obtain the DC-Link capacitor rms current, it is assumed that the switching of the rectifier and the inverter stages are synchronized. By summing the rectifier and inverter rms ripple currents, a worst case estimate of the capacitor rms ripple current can be obtained from

$$I_{\text{Rms,C}} = I_{\text{Rms,Rt}} + I_{\text{Rms,In}}.$$  

(23)

## 4. Converter Design

In this comparison it is assumed that each converter is operating from a 50 Hz, 400 V, +10%, -15%, three-phase mains voltage supply. Each converter supplies a variable frequency, output voltage to a permanent magnetic synchronous machine. For this application the output current phase angle is close to zero. Both the VSMC and BBC are thermally rated for 6.8 kVA operation. The minimal dynamic modulation margin is \(\Delta M_{\text{min}} = 5\%\).

For the VSMC operating at minimum voltage \(U_{1,\text{min}}\) the modulation margin \(\Delta M_{\text{min}}\) should be kept. Considering the maximal voltage transfer ratio of the matrix converter, the nominal output voltage (line-to-line) is

$$U_{2N} = \frac{\sqrt{3}}{2} (1 - \Delta M_{\text{min}}) U_{1,\text{min}} \approx 280 \text{ V}.$$  

(24)

The nominal output current is then defined by

$$I_{2N} = \frac{P_{2N}}{\sqrt{3} U_{2N}} = 14 \text{ A}.$$  

(25)

The ideal motor therefore has to be designed in order to reach its nominal operating point for \(U_{2N}\) and \(I_{2N}\) as specified.

For the case of the BBC, the DC link voltage \(U\) is determined, considering \(\Delta M_{\text{min}}\) and \(U_{1,\text{max}}\), from

$$U = (1 + \Delta M_{\text{min}}) \sqrt{2} \cdot U_{1,\text{max}} \approx 655 \text{ V}.$$  

(26)

The nominal output voltage (line-to-line) then is given by \(U\) and \(\Delta M_{\text{min}}\) and is

$$U_{2N} = (1 - \Delta M_{\text{min}}) \sqrt{2} \cdot U = U_{1,\text{max}} \approx 440 \text{ V}.$$  

(27)

With the specified power level it follows that the nominal output current \(I_{2N}\) is 8.9 A.

Using the analytical equations presented in section 3 the current stresses for the rectifier and inverter stages of the VSMC and BBC are calculated and presented in Fig. 6. As can be seen the switch rms current for the VSMC is much higher than the BBC due the lower maximum output voltage for the same power rating. For the BBC the diode rms current in the rectifier stage is significantly higher than the IGBT rms current due to the boost action.

![Fig. 6. Current Stresses (switch/diode rms and average) for the rectifier and inverter stages of the VSMC and BBC](image)

### Table 1. BBC and VSMC Components

<table>
<thead>
<tr>
<th>Description</th>
<th>BBC</th>
<th>VSMC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Semiconductors</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input</td>
<td>3 IXY FII 50-12E</td>
<td>3 IXY FII 50-12E</td>
</tr>
<tr>
<td>Output</td>
<td>6 IXY FIO 50-12E</td>
<td>3 IXY FII 50-12E</td>
</tr>
<tr>
<td>Boost Inductor</td>
<td>3.1 mH (toroidal)</td>
<td>Not used</td>
</tr>
<tr>
<td>DC-Link Cap.</td>
<td>4.8 (\mu) F, 400 V AC</td>
<td>Not used</td>
</tr>
</tbody>
</table>

## 4.1 Design Procedure

To produce a compact design it is desirable to use semiconductor modules that combine as many individual devices as possible into one package. For the BBC the IXY FII phase leg modules (see Table 1), which contain 2 IGBTs and 2 fast diodes, have been selected. This IXY module has a voltage rating of 1200 V and a current rating of 32 A at a case temperature of 90°C. The current rating is well within the rms and average currents as calculated and shown in Fig. 6. For the VSMC the same IGBT module is used for the inverter stage but a bi-directional IGBT module, comprising of one IGBT and a fast recovery bridge diode rectifier, is selected for the rectifier stage as it uses the same IGBT and ISOPLUS package as the BBC.

For BBC the other special components are the boost inducer and DC-link capacitors. Using (19) the minimum DC-link capacitance is calculated as 31 \(\mu\) F and this is constructed from 4 parallel connected 8 \(\mu\) F metal film capacitors. The total capacitor ripple current is 7.4 A as calculated from (23) and each capacitor would have 1.85 A of ripple current. Each boost inductor has an inductance of 1 mH and is constructed using two stacked Micrometals toroidal cores (diameter of 44.5 mm) with 60 turns.

After the selection of the components the next step is to undertake a thermal analysis to determine the size of the heatsink, followed by the design of the EMI filters.

## 4.2 Thermal Design

Both the VSMC and BBC have been thermally designed so that the maximum junction of any one semiconductor module is 150°C. The power dissipation of each switch module, at a switching frequency of 40 kHz, is calculated using the analytical equations of section 3 and is then used as the input to a 3-D thermal simulation. The length of the heatsink is adjusted to ensure that the maximum junction temperature is not exceeded. The results from the thermal analysis are shown in Fig. 7 where the highest spot temperature on the VSMC heatsink is 122°C, whereas it is 104.5°C for the BBC.

## 4.3 EMI Filter Design

In order to compare the EMC performance the standard CISPR 11/1997 is chosen for establishing the performance requirements, where the frequency...
Table 2. EMC input filter components and physical dimensions

<table>
<thead>
<tr>
<th>Topology</th>
<th>BBC</th>
<th>VSMC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total DM capacitance</td>
<td>15.54 µF</td>
<td>36 µF</td>
</tr>
<tr>
<td>Total DM inductance</td>
<td>2.19 mH</td>
<td>1.29 mH</td>
</tr>
<tr>
<td>Total CM capacitance</td>
<td>28.2 nF</td>
<td>28.2 nF</td>
</tr>
<tr>
<td>Total CM inductance</td>
<td>36 mH</td>
<td>36 mH</td>
</tr>
<tr>
<td>Total filter components volume</td>
<td>325 cm³</td>
<td>360 cm³</td>
</tr>
</tbody>
</table>

Fig. 8. EMC input filter schematic for the BBC system, designed to comply to CISPR 11 class B

Having common EMC requirements and applying the design procedure to both converters, for the same switching frequency, makes a comparison possible (Table 2) with regard to the physical dimensions and the total value of the components. The volume of the EMI filter for the VSMC is 10% larger than the BBC. The filter topology for the BBC is shown in Fig. 8 with the main components specified. For the VSMC system a filter with a similar structure, but different component values is used. It is interesting to note that the volume of the EMI filter increases as the switching frequency is increased, since more switching harmonics now fall into the EMC frequency range of interest.

4.4 Physical Layout

Fig. 9 shows the physical layout arrangement of the VSMC and the BBC, where the layout includes all power devices, gate drives, passive components, EMI filter, fan, control and power supply. Both converters can be directly compared as they are drawn with the same scale. A comparison of the physical size between the VSMC and BBC can be seen from the photograph in Fig. 10. The overall volume of the VSMC is 2.3 liters compared to a volume of 4.6 liters for the BBC. The volumes of both these converters compare favorably to the volume of a standard diode-rectifier input, commercial LUST CDD34.010 6.9 kVA PMSM drive inverter that has a volume of 5.3 liters (including the enclosure and user interface). For the VSMC the output terminals and housekeeping power supply are placed over the heatsink fan. For the BBC the input boost inductors are placed in a space created by cutting out a section of the heatsink below the EMI input filter.

4.5 Losses

Fig. 11(a) shows the power loss contributions for each switch and diode in the rectifier and inverter stages of the converters, and the passive components. For the passive components the BBC boost inductors have a significantly greater loss than the AC filter capacitors in the VSMC. The EMI filter losses of both converters have a similar value. It can be seen that the BBC has significantly higher semiconductor losses in the input stage than the VSMC. For the BBC the switching losses are the dominant factor for both stages. It can also be seen that there are no switching losses in the input stage of the VSMC. The thermally limiting semiconductor device, as shown in Fig. 11(b), for the converter design is the diode in the rectifier stage for the BBC and it is
5. System Evaluation

One key performance indicator is the system efficiency of the converters over the operating range. The efficiency is defined as

\[
\eta(M, I_2) = 1 - \frac{P_{\text{Loss}}(M, I_2)}{S_2(M, I_2)} \quad \text{(28)}
\]

where \(P_{\text{Loss}}\) only includes the semiconductor losses and \(S_2(M, I_2) = \frac{2}{\sqrt{3}} U_1 \cdot I_2 \cdot M\).

In order to undertake this efficiency comparison a normalized modulation index \(M\) is defined individually for the VSMC and BBC in (29).

\[
M = \begin{cases} 
\frac{2}{\sqrt{3}} \frac{U_2}{U_1} : \text{VSMC} \\
\sqrt{3} \frac{I_2}{I_1} : \text{BBC} 
\end{cases} \quad \in [0..1] \quad \text{(29)}
\]

By using this definition, \(M = 1\) for both converters means maximum modulation and as a consequence the same or maximum output power (cf. section 4).

Fig. 12 presents the efficiency for the converters over varying modulation indices and output current levels. It can be seen that the VSMC has an overall higher efficiency than the BBC, with the maximum efficiency at full load of the VSMC being 94.5% compared to 92% for the BBC.

To decrease the losses for the BBC it would be possible to decrease output switching frequency to 20 kHz while retaining the input switching frequency at 40 kHz in order to keep the boost inductor size small. This output switching frequency reduction would increase the efficiency by 1.5% but it would cause a higher DC link capacitor current ripple due to the non-synchronized switching. In performing this
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comparison it is decided to keep the switching frequency for both the input and output stages at 40 kHz.

The selection of a switching frequency of 40 kHz has resulted in the VSMC being more efficient than the BBC. By decreasing the switching frequency the high switching losses of the BBC will decrease and conduction to switching loss ratio will have a similar value as the VSMC, thus the BBC efficiency will increase. Fig. 13 graphically indicates the relative semiconductor loss difference, \( \Delta P_{\text{Loss}} = \frac{P_{\text{Loss, VSMC}} - P_{\text{Loss, BBC}}}{P_{2N}} \), between the BBC and VSMC for a varying switching frequency, \( f_P \), and modulation index \( M \). The light grey shaded area of the surface indicates a positive \( \Delta P_{\text{Loss}} \) and therefore an operating condition being advantageous for the BBC system. The transition from light to dark grey marks the intercept line of both converters’ loss curves. This means that under rated load condition (nominal output current and maximum output voltage (and/or \( M \))) the equal loss switching frequency is 14 kHz when the increased losses of the BBC passive components are not considered. Above this frequency the VSMC becomes more efficient. For partial loads, which is usually the case for steady state operation at the motor’s rated power, the switching frequency for equal power loss decreases as seen from the dashed lines in Fig. 13.

With regard to the loss characteristic, Fig. 13 affirms a significant difference between the CMC \(^{6}\) and the (V)SMC. In \(^{6}\) the CMC shows relatively high conduction losses that are independent of the modulation index (and output power factor). In contrast the (V)SMC is similar to the conventional BBC in that it has less input stage conduction losses for longer applied zero vectors at the output stage. However for a high modulation index (and output power factor) the (V)SMC, as well as the BBC, has conduction losses greater than the CMC. This, as Bernet \(^{6}\) shows, makes the CMC superior to the BBC (and also the (V)SMC) just near the full speed maximum modulation region.

An extreme operating point of the converters is for the case where the output frequency is close to zero. This effectively causes “DC” to occur in the output phases, and in the worst case one transistor/diode pair has to switch the maximum peak output current for numerous mains cycles. Therefore the junction temperature of this highly stressed IGBT/diode pair will determine the maximum output current of the converter system. From Fig. 14 it can be seen that for the BBC the output current has to be reduced to 46% of the nominal current for operation at zero output frequency.

For the VSMC, there is the possibility of applying the low dc-link voltage modulation strategy (MS2) and this results in a reduction of the output stage switching losses by more than 30%. In addition it is possible to force some output stage commutations by the appropriate switching actions of the input stage transistors \(^{13}\). This allows a certain amount of the switching losses to be shifted to the input stage and be equally distributed among all of the input stage transistors. These modulation options allow a significant reduction of the output device losses and as a consequence the maximum output current amplitude can be increased by 25% (Fig. 14) before the junction of the (clamping) output stage transistor reaches 150°C.

6. Conclusions

This paper has undertaken a comparison of the VSMC and the BBC. A VSMC has been used for the comparison as it is has the same functionality as the conventional matrix converter but a reduced number of switches and lower control complexity. Analytical equations detailing the conduction and switching losses of the both converter systems are presented. The VSMC and BBC design assumes special purpose PMSM motors are applied to each converter. The converters have been designed for a thermal rating of 6.8 kW, a mains
voltage range of 340 V to 440 V, a 5% modulation control margin and an ambient temperature of 45°C.

A limiting factor of the BBC is the diode in the IGBT module of the active rectifier for a switching frequency of 40 kHz. The volume of the VSMC (2.3 liters) is half that of the BBC (4.6 liters) and the efficiency for the VSMC is 94.5% compared to 92% for the BBC. The complexity of the two converters is very similar in terms of number of switches and control circuitry required. The volume of the EMI filter for the VSMC is only 10% larger than the BBC when the boost inductors are excluded. A further advantage of the VSMC is that the continuous rated output current can be increased by 25% for standstill motor operation, while for the BBC it has to be decreased by 54%. The BBC has an advantage over the VSMC for systems that have large unbalanced or distorted input voltages since the BBC can still supply full output voltage. Overall the VSMC offers significant advantages over the BBC for motor drive applications requiring high switching frequencies.

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References


Simon Round (Non-member) received the B.E. (Hons) and Ph.D. degrees from the University of Canterbury, New Zealand, in 1989 and 1993. From 1992 to 1995 he held Research Associate positions at the University of Minnesota and Norwegian Institute of Technology. From 1995 to 2003 he was a Lecturer/Senior Lecturer in the Department of Electrical and Computer Engineering at the University of Canterbury. In September 2004, he joined the Power Electronic Systems Laboratory at ETH Zurich as a Senior Research Associate.

Frank Schaafmeister (Non-member) was born in Niedermarsberg, Germany, on May 14, 1974. He studied electrical engineering at the University of Paderborn, Germany. During his studies he worked as a research assistant at the Tampere University of Technology, Finland on applications of DC-link inverter systems and dealt in his final theses with three-phase PFC rectification. He joined the Power Electronic Systems Laboratory, ETH Zurich, as a Ph.D. student in November 2001.

Marcelo Heldwein (Non-member) was born in Chapécó, Brazil, in 1974. He received the B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina, Florianópolis, Brazil in 1997 and 1999. From 1999 he worked as R&D engineer at the Federal University of Santa Catarina. Between 2001 and 2003, he was with the Power Electronic Systems Laboratory, ETH Zurich, where he is a PhD student.

Eduardo Pereira (Non-member) was born in Florianópolis, Brazil in 1975. He received the B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina, Florianópolis, Brazil in 2001 and 2003, respectively. During his studies he researched on Compact UPS, Electronic Ballasts and Three-Phase DC-DC Conversion. He was with the Power Electronic Systems Laboratory, ETH Zurich, and is now a development engineer at Tridonic/Atco Switzerland.

Leonardo Serpa (Non-member) was born in Florianópolis, Brazil, in 1980. He received the B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina, Brazil in 2002 and 2004. Between July and December 2001 he worked as an internship student at the Center for Power Electronics Systems in Virginia, USA. Since March 2004 he has been with the Power Electronic Systems Laboratory, ETH Zurich, where he is a Ph.D. student.
Johann W. Kolar (Member) studied industrial electronics at the University of Technology Vienna, Austria, where he also received the Ph.D. degree (summa cum laude). From 1984 to 2001 he was with the University of Technology in Vienna, where he was teaching and working in research in close collaboration with the industry. He has proposed numerous novel converter topologies, e.g., the VIENNA Rectifier and the Three-Phase AC-AC Sparse Matrix Converter concept. Dr. Kolar has published over 200 scientific papers in international journals and conference proceedings and has filed more than 50 patents. He was appointed Professor and Head of the Power Electronics Systems Laboratory at the Swiss Federal Institute of Technology (ETH) Zurich on Feb. 1, 2001. The focus of his current research is on ultra-compact intelligent AC-AC and DC-DC converter modules employing latest power semiconductor technology (SiC), novel concepts for cooling and active EMI filtering, multi-disciplinary simulation, bearing-less motors, power MEMS, and wireless power transmission.