

An Analysis of Three-Phase Rectifiers with Constant Voltage Loads

Predrag Pejović, *Member, IEEE*, and Johann W. Kolar, *Fellow, IEEE*

Abstract—In this paper, a numerical analysis of three-phase voltage loaded rectifiers is presented. The simulation is performed on the equation system level, for normalized circuit model. Possible combinations of diode states are analyzed, and it is shown that out of $2^6 = 64$ combinations only 13 might occur. For all of the combinations, circuit equations and boundary inequalities are derived. The circuit order is shown to be zero, one, or two, depending on the diode state combination. Number of boundary inequalities to be monitored is shown to vary from three to six, depending on the diode state combination. Phenomenon of instantaneous combination transitions is analyzed. Modes of the circuit operation are defined. Dependence of various circuit parameters on normalized output voltage is presented. Obtained diagrams may serve as a quick reference guide for the rectifier design, and presented analysis may be of interest in education.

Index Terms—AC-DC power conversion, converters, education, harmonic distortion, power conversion harmonics, power quality, rectifiers.

I. INTRODUCTION

THREE-PHASE diode bridge rectifier with capacitive filtering, depicted in Fig. 1, is popular due to its simplicity, reliability, and robustness. This qualified the rectifier for numerous applications in telecommunications. To model inductance of the supply lines, significant in rural environments where deployment of telecommunication equipment might be expected, in the schematic diagram of Fig. 1 three inductors of inductance L are added. In some applications, actual inductors are included in the rectifier design, to increase the inductance in order to reduce the current spikes.

Although it might be expected that analysis of the rectifier of Fig. 1 is readily available in literature, according to a detailed search presented in [1] it was not the case. In order to fill the gap, analysis of the continuous conduction mode is performed in [1] applying sinusoidal approximation [2]. In [3], an exact analytical solution for the continuous conduction mode is given, having the same complexity as the approximate solution of [1]. In [4]–[8] single-phase rectifiers with ac-side reactance are analyzed, but they cover discontinuous conduction mode only. Three-phase rectifiers are treated in [9]–[12], primarily focusing constant-current loads. An approach being the closest to the analysis presented in this paper is given in [11], where the same rectifier structure is analyzed and normalization of variables were applied, but the analysis included finite values of the filtering capacitor capacitance and considered only

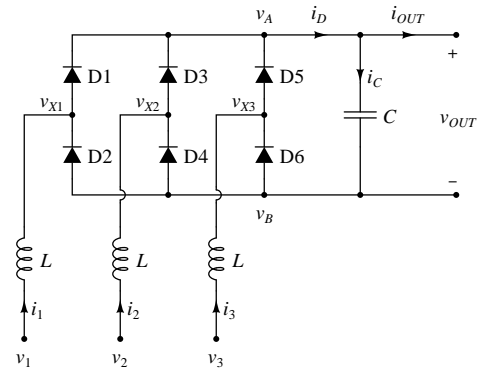


Fig. 1. The rectifier.

two operating modes, named the continuous current mode and the discontinuous current mode, despite the fact that the input currents are continuous in time due to the presence of inductors. Regardless the increased output voltage ripple, finite values of the filtering capacitor capacitance are of practical interest since low capacitance values improve the input current quality, reduce the inrush current problems, and do not require electrolytic capacitors characterized by limited lifetime.

Since the analytical solution of the rectifier of Fig. 1 is available only for the continuous conduction mode [3], numerical solution of the rectifier normalized model is presented in this paper, in order to include discontinuous conduction modes. Although there are many circuit simulation programs available today, simulation of the rectifier of Fig. 1 is not an easy task due to variations of circuit order depending on the diode state combinations. Also, in some diode state combinations unique solutions for the rectifier voltages do not exist. In circuit simulation programs, this would require significant patching with artificial parasitic elements usually characterized by improvised parameters. Furthermore, situations when the inductor currents are exactly equal to zero should be determined, which faces the simulation with numerical difficulties.

Results presented in this paper are obtained using a general purpose numerical analysis program, and analytical preparation required for such simulation improves understanding of the circuit behavior, enabling identification of operating modes. In this sense, the analysis presented in this paper might be of some educational interest, since the analytical preparation required by the simulation on the equation level required thorough analysis and understanding, including the circuit analysis in diode state combinations that result in singular systems of network equations.

P. Pejović is with the University of Belgrade, School of Electrical Engineering, 11120 Belgrade, Serbia (e-mail: peja@etf.rs).

J. W. Kolar is with Power Electronic Systems Laboratory, Swiss Federal Institute of Technology Zurich, ETH-Zentrum/ETL, CH-8092 Zurich, Switzerland (e-mail: kolar@lem.ee.ethz.ch).

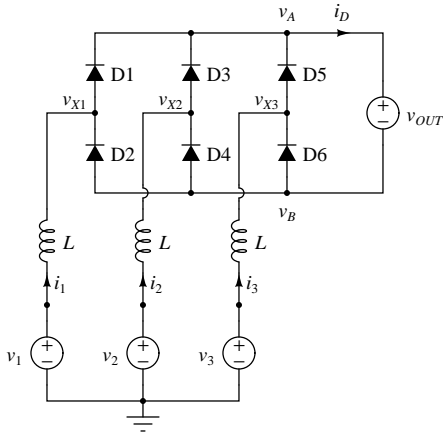


Fig. 2. The rectifier model.

II. PRELIMINARIES

A. The Rectifier Model

To analyze the rectifier, the diodes are modeled as ideal. This means that in its on state a diode is represented as a short circuit, $v_{Dn} = 0$, which applies for $i_{Dn} > 0$, for $n \in \{1, \dots, 6\}$. In its off state, the diode is modeled as an open circuit, $i_{Dn} = 0$, which applies for $v_{Dn} < 0$. For the analysis that follows, it is important to note here that in each of its states each of the diodes is accompanied by one inequality that states a condition when the assumed state is valid. This results in the total of six inequalities that bound the region where combination of diode states in the three-phase diode bridge is valid. In actual circuit, for $V_{OUT} > 0$ circuit interconnection sometimes excludes some of the inequalities that bound validity of specific diode state combinations. For example, if a diode $D(2k-1)$ conducts (for $k \in \{1, 2, 3\}$), diode $D(2k)$ cannot conduct before $D(2k-1)$ is off, thus state condition for $D(2k)$ needs not to be checked. The same applies for $D(2k-1)$ when $D(2k)$ is conducting.

To simplify the analysis further, ripple of the output voltage is neglected. In terms of circuit theory, this means that the filtering capacitor and the load are replaced by a constant voltage source V_{OUT} , as depicted in Fig. 2.

B. Input Voltages

In the analysis, it will be assumed that the rectifier is supplied by a three-phase symmetrical, balanced, and undistorted voltage system with the electromotive forces specified by

$$v_k = V_m \cos\left(\omega t - (k-1) \frac{2\pi}{3}\right) \quad (1)$$

for $k \in \{1, 2, 3\}$. It is possible that the sources are accompanied by the line inductance. Inductance of possibly added inductors and the line inductance are merged in L , as depicted in Fig. 3, where aL is the line inductance, and $(1-a)L$ is the inductance of added inductors. Knowing electromotive forces v_k and corresponding voltages at the diode bridge inputs v_{Xk} , voltage at the point of coupling is obtained as

$$v_{PCk} = (1-a)v_k + av_{Xk}. \quad (2)$$

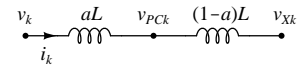


Fig. 3. Line inductance aL and the rectifier inductance $(1-a)L$.

C. Normalization

Normalization is performed in order to generalize the results and to reduce the number of variables, since some of them appear only in certain combinations, not independently. All of the rectifier voltages, labeled by v , are replaced by normalized equivalents m according to

$$m = \frac{v}{V_m}. \quad (3)$$

The rectifier currents are normalized by the rectifier short-circuit input current amplitude to

$$j = \frac{\omega L}{V_m} i \quad (4)$$

while normalization of time introduces the phase angle

$$\varphi = \omega t. \quad (5)$$

Applying listed normalizations, the inductor current equation

$$L \frac{di_k}{dt} = v_k - v_{Xk} \quad (6)$$

is represented by its normalized equivalent

$$\frac{dj_k}{d\varphi} = m_k - m_{Xk}. \quad (7)$$

In this manner, the number of variables is reduced by one, since L is avoided in the normalized equation, being merged with other variables in j .

III. COMBINATIONS OF DIODE STATES

Each of the diodes in the bridge may take one of two states. Since there are six diodes in the bridge, overall number of combinations of diode states is $2^6 = 64$. However, due to the circuit interconnections and voltage source values, states of the diodes are mutually dependent and some of the diode state combinations cannot appear. This reduces the number of possible combinations significantly.

The first reduction of the number of diode state combinations arises from the fact that $V_{OUT} > 0$. In that case, diodes located in the same leg of the diode bridge, indexed $2k-1$ and $2k$ for $k \in \{1, 2, 3\}$ cannot conduct simultaneously. In this manner, only three combinations of diode states in the same leg can occur, instead of four. Treating two diodes in the same leg of the diode bridge simultaneously, state of the two diodes could be coded as -1 when the diode indexed $2k$ is conducting, i.e. $i_k < 0$, 0 when the diodes are not conducting, i.e. $i_k = 0$, and $+1$ when the diode indexed $2k-1$ is conducting and $i_k > 0$. Since there are three legs in the diode bridge, overall number of combinations is reduced to $3^3 = 27$.

Further reduction of combinations is based on the fact that $i_1 + i_2 + i_3 = 0$. This condition prohibits combinations with all three of the legs in state $+1$ or -1 , reducing the total

TABLE I
COMBINATIONS OF DIODE STATES

combination	phase leg state		
	1	2	3
0	0	0	0
1	+1	-1	0
2	+1	0	-1
3	-1	+1	0
4	0	+1	-1
5	-1	0	+1
6	0	-1	+1
7	+1	+1	-1
8	+1	-1	+1
9	-1	+1	+1
10	+1	-1	-1
11	-1	+1	-1
12	-1	-1	+1

number of combinations to 25. Furthermore, there are three prohibited combinations having two legs in the state +1 and one in state 0, and another three with two legs in state -1 and the remaining leg in state 0. This reduces the number of combinations to 19. Final reduction is obtained excluding three combinations with one leg in state +1 and the remaining two in state 0, as well as another three combinations having one leg in state -1 and the two remaining legs in state 0, leaving the total of 13 possible combinations of diode states.

The same number of possible combinations may be obtained in a constructive manner, counting possible combinations. The first of them is a combination in which all legs are in state 0. Next, there are 6 combinations where two diodes are conducting, having one leg in state +1, other one in state -1, and the remaining one in state 0. Next, there are three combinations with two legs in state +1 and the remaining one in state -1. Finally, there are three combinations in which two legs are in state -1, and the remaining one in state +1. Again, the total number of 13 possible combinations of diode states is reached. The combinations are listed in Table I, accompanied by assigned code numbers.

IV. CIRCUIT EQUATIONS

To simulate the rectifier, equations that describe the circuit should be derived for all thirteen of possible diode state combinations, as well as the boundary inequalities and the combination transition rules that specify the next combination after a boundary inequality is violated. The combinations may be conveniently grouped according to the number of conducting diodes: none, two, or three.

The first of the combinations to be considered is the one with all diodes reverse biased. All of the currents are equal to zero,

$$j_1 = j_2 = j_3 = 0 \quad (8)$$

and the circuit order is zero. Voltages m_A and m_B cannot be uniquely determined, but it is known that

$$m_A \geq \max(m_1, m_2, m_3) \quad (9)$$

and

$$m_B \leq \min(m_1, m_2, m_3). \quad (10)$$

Fact that m_A and m_B cannot be uniquely determined causes some inconvenience with the boundary inequalities. For an odd-indexed diode $D(2k - 1)$ condition to remain reverse biased is

$$m_k - m_A < 0 \quad (11)$$

while for an even-indexed diode $D(2l)$ corresponding condition is

$$-m_l + m_B < 0. \quad (12)$$

Since m_A and m_B are not determined, original boundary inequalities cannot be directly applied. However, using

$$m_A - m_B = M_{OUT} \quad (13)$$

and adding (11) and (12), joined condition for the two diodes becomes

$$m_{kl} < M_{OUT}. \quad (14)$$

In the case this condition is violated, diodes $D(2k - 1)$ and $D(2l)$ will start to conduct simultaneously. Since there are six combinations of diodes consisting one odd-indexed diode and one even-indexed diode not belonging to the same rectifier leg, original six boundary inequalities defined on the diode level are replaced by six boundary inequalities on the diode pair level. There are six inequalities to be monitored, and six combinations the rectifier can switch to. In this manner, problem with the absence of a unique solution for m_A and m_B is resolved without a need to introduce artificial parasitic elements to enforce a unique solution.

The next situation to be analyzed is when two diodes are conducting. According to the analysis of diode state combinations and the notation introduced in Table I, let us assume that legs connected to phases k , l , and n are in states $\text{state}(k) = +1$, $\text{state}(l) = -1$, $\text{state}(n) = 0$, which is depicted in Fig. 4. The equations that describe the circuit are

$$\frac{dj_k}{d\varphi} = \frac{1}{2}(m_k - m_l - M_{OUT}) \quad (15)$$

$$j_l = -j_k \quad (16)$$

and

$$j_n = 0. \quad (17)$$

Voltages of the diode bridge output terminals are

$$m_A = \frac{1}{2}(M_{OUT} - m_n) \quad (18)$$

and

$$m_B = \frac{1}{2}(M_{OUT} + m_n). \quad (19)$$

The circuit is of the first order.

Regarding the boundary inequalities, since diodes $D(2k - 1)$ and $D(2l)$ share the same current, two boundary inequalities collapse into one

$$j_k > 0 \quad (20)$$

switching the rectifier to combination labeled 0 in Table I if violated. Since $D(2k - 1)$ reverse biases $D(2k)$, as well as $D(2l)$ reverse biases $D(2l - 1)$, boundary inequalities for $D(2k)$ and $D(2l - 1)$ should not be monitored since they cannot be violated. This reduces the number of boundary inequalities to

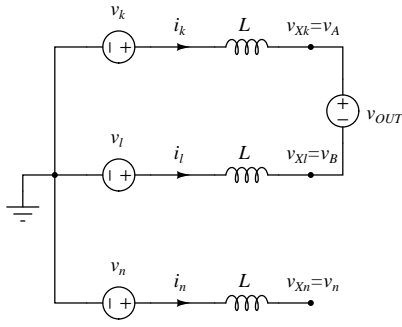


Fig. 4. Equivalent circuit for two conducting diodes.

be monitored to three. According to (18) diode $D(2n-1)$ will start conducting when

$$m_n < \frac{1}{3}M_{OUT} \quad (21)$$

is violated, switching leg n to state $+1$, while according to (19) $D(2n)$ will start conducting when

$$m_n > -\frac{1}{3}M_{OUT} \quad (22)$$

is violated, switching leg n to state -1 .

In states with two conducting diodes, there are three boundary inequalities to be monitored (20), (21), and (22), and three diode state combinations the rectifier could switch to, one of them without conducting diodes, the other two with three conducting diodes.

In cases when three diodes are conducting, there are two possibilities: when two rectifier legs are in state $+1$ and one is in state -1 , depicted in Fig. 5, and when two legs are in state -1 , and the remaining leg is in the state $+1$, as depicted in Fig. 6.

In the case of Fig. 5, equations that govern currents of the inductors are

$$\frac{dj_k}{d\varphi} = m_k - \frac{1}{3}M_{OUT} \quad (23)$$

$$\frac{dj_l}{d\varphi} = m_l - \frac{1}{3}M_{OUT} \quad (24)$$

and

$$j_n = -j_k - j_l. \quad (25)$$

The system is of the second order. Voltages of the diode bridge output terminals are

$$m_A = \frac{1}{3}M_{OUT} \quad (26)$$

and

$$m_B = -\frac{2}{3}M_{OUT}. \quad (27)$$

Three conducting diodes cause the remaining three diodes to be reverse biased with M_{OUT} , and their boundary inequalities need not to be monitored. Three inequalities for the conducting diodes are

$$j_k > 0 \quad (28)$$

$$j_l > 0 \quad (29)$$

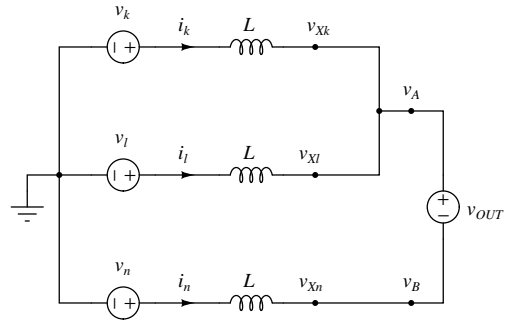


Fig. 5. Equivalent circuit for three conducting diodes, two to the positive output terminal.

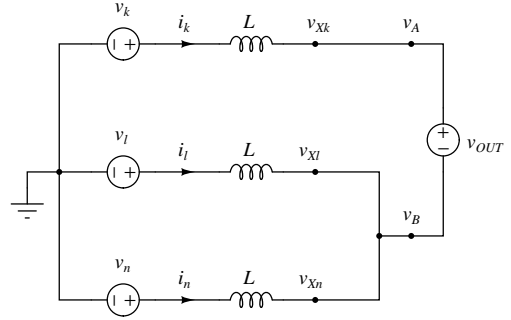


Fig. 6. Equivalent circuit for three conducting diodes, one to the positive output terminal.

and

$$j_n < 0. \quad (30)$$

According to (25), validity of (28) and (29) implies validity of (30), thus (30) needs not to be verified, except as an indicator that i_k and i_l simultaneously reached zero. However, this justifies monitoring of i_n , and if (30) is violated the rectifier switches to combination 0. If (28) or (29) are violated, corresponding rectifier leg switches to state 0. However, a phenomenon of instantaneous combination transitions might occur here. Let us suppose that $state(k) = 1$ and that $j_k > 0$ is violated. This switches the leg indexed k to 0, but it might not remain in that state, since the initial diode state change might initiate instantaneous switching of the rectifier leg to -1 , which occurs for

$$m_k < -M_{OUT}/3 \quad (31)$$

according to the combination transition rules for diode state combinations with two conducting diodes. The same applies for the leg indexed l . Thus, after one of these combination changes is detected, to determine final combination possible instantaneous combination changes should be checked for by checking of additional inequalities, like (31).

In the case of Fig. 6, where two of the legs are in state -1 and one is in state $+1$, the equations over currents are

$$\frac{dj_k}{d\varphi} = m_k - \frac{2}{3}M_{OUT} \quad (32)$$

$$\frac{dj_l}{d\varphi} = m_l + \frac{1}{3}M_{OUT} \quad (33)$$

and

$$j_n = -j_k - j_l \quad (34)$$

while the voltages of the diode bridge output terminals are

$$m_A = \frac{2}{3}M_{OUT} \quad (35)$$

and

$$m_B = -\frac{1}{3}M_{OUT}. \quad (36)$$

Inequalities that should be monitored are

$$j_k > 0 \quad (37)$$

$$j_l < 0 \quad (38)$$

and

$$j_n < 0 \quad (39)$$

Violation of (37) switches the rectifier combination to 0 of Table I, indicating simultaneous violation of (38) and (39). Violations of only one inequality of (38) and (39) switches the corresponding rectifier leg to state 0. Then, boundary inequalities for corresponding combination with two conducting diodes apply, possibly causing instantaneous transition to state +1. In the case of the rectifier leg indexed l , if (38) is violated, instantaneous switching of the leg to +1 occurs if

$$m_l > M_{OUT}/3. \quad (40)$$

Similar applies to the rectifier leg indexed n .

V. SIMULATION RESULTS

After the analysis is performed, the method is implemented in a program (GNU Octave script) available at <http://tnt.etf.rs/~peja/three-phase-voltage-loaded>. The simulation is performed with 10,000 points over line period, applying trapezoidal rule for numeric integration and fixed phase angle step. Simulations over line period are repeated until the steady state is reached, and as a criterion norm of the difference of the state vectors at the beginning of the period and at the end of the period is used. If this norm is smaller than 0.01% of the norm of the state vector at the end of the period, steady state is assumed to be reached. The simulation is performed for M_{OUT} starting from 2, being decreased for 0.0005 for each data collection point. To improve the efficiency of the algorithm, as an initial condition vector for each data collection point final vector of state variables from previous data point is used. This is proven to be a good practice in efficient reaching of the steady state, since small steps in M_{OUT} cause the state vectors at the beginning of the line period to be close in subsequent data collection points.

It should be noted here that this sort of numerical solution is not an exact solution of the rectifier model. Some error is present, which is common to all numerical methods. The most important contributors to the simulation error are numerical integration error and limited precision in determining combination transition instants. To reduce the error, relatively dense sampling over phase angle is performed, with 10,000 points per period, resulting in the phase angle step size of $2.16'$. In

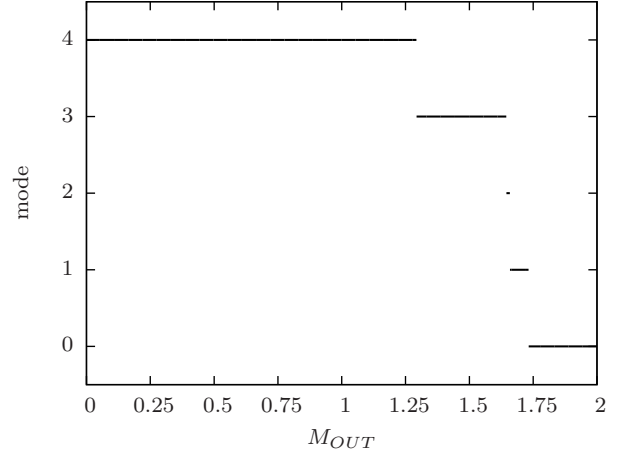


Fig. 7. Dependence of the operating mode on M_{OUT} .

cases where analytical results are available, numerical results will be compared to the exact solution.

Modes of the rectifier operation are defined such that mode 0 corresponds to the situation when the diodes are not conducting during the entire line period, in mode 1 intervals of non conducting and conducting of two diodes appear, in mode 2 there are intervals of none conducting, conducting of two diodes, and conducting of three diodes, in mode 3 there are intervals where two diodes conduct, as well as three diodes, but non conducting intervals are absent, and in mode 4 only intervals where three diodes are conducting are present, corresponding to the continuous conducting mode. Dependence of the operating mode on M_{OUT} is shown in Fig. 7. Numerically obtained values for boundaries between modes are $M_{OUT\ 0\leftrightarrow 1} = 1.73225$, $M_{OUT\ 1\leftrightarrow 2} = 1.65875$, $M_{OUT\ 2\leftrightarrow 3} = 1.64475$, and $M_{OUT\ 3\leftrightarrow 4} = 1.29275$. Exact analytical values are available for $M_{OUT\ 0\leftrightarrow 1} = \sqrt{3} \approx 1.73205$ and for $M_{OUT\ 3\leftrightarrow 4} = 9/\sqrt{9 + 4\pi^2} \approx 1.29261$ [3]. Comparing the numerically obtained values to the available exact results, it may be concluded that relatively good agreement is achieved.

In Figs. 8–11, waveforms of the input current, input voltage, and the voltage at the diode bridge input are presented for the first phase in all of the modes. In Fig. 8, corresponding to mode 1, non conducting intervals between two adjacent current spikes of the same polarity could be identified. These intervals are being reduced in the waveform of Fig. 9, corresponding to mode 2, by intervals of conducting of three diodes that also introduce additional small spikes, observable in the diagrams of [11]. Absence of nonconducting intervals between the spikes is observed in Fig. 10 that corresponds to mode 3, but other intervals in which the phase current does not flow are still observed. During these intervals the rectifier is not in combination 0, since the currents of the remaining two phases are flowing. Fig. 11 corresponds to the continuous conduction mode, i.e. mode 4, where phase angle intervals in which the input current is continuously at zero do not exist.

Dependence of M_{OUT} on J_{OUT} is shown in Fig. 12. In this diagram, as well as in subsequent diagrams, different operating modes are indicated varying the curve thickness

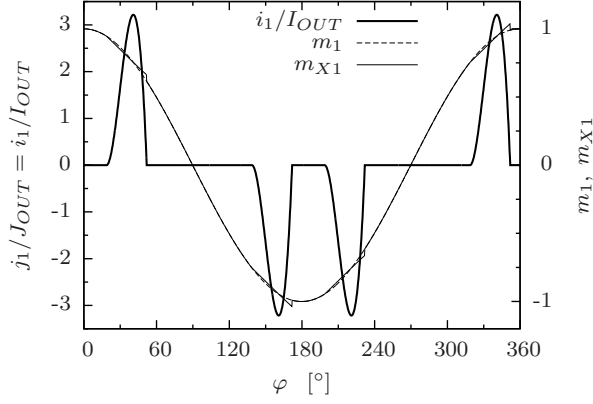


Fig. 8. Waveforms of i_1 , v_1 , and v_{X1} , mode 1, $M_{OUT} = 1.7$.

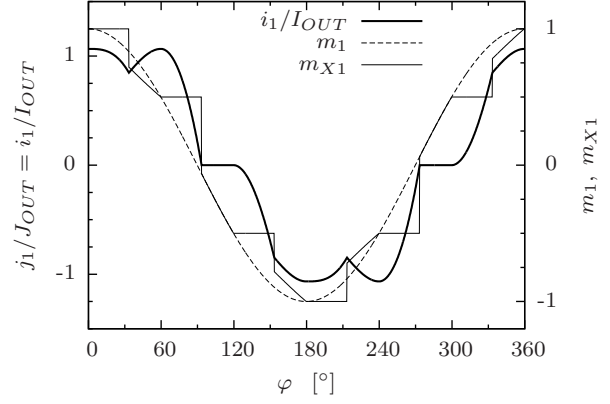


Fig. 10. Waveforms of i_1 , v_1 , and v_{X1} , mode 3, $M_{OUT} = 1.5$.

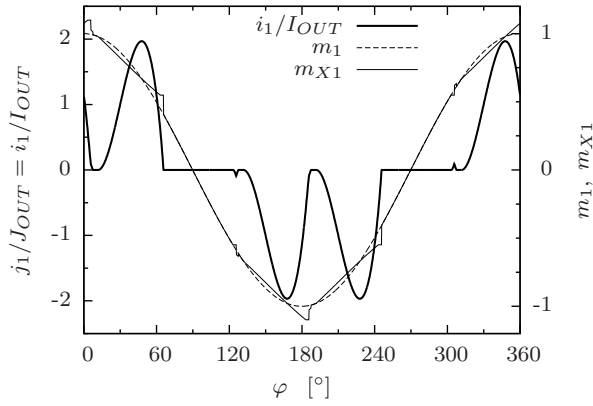


Fig. 9. Waveforms of i_1 , v_1 , and v_{X1} , mode 2, $M_{OUT} = 1.6475$.

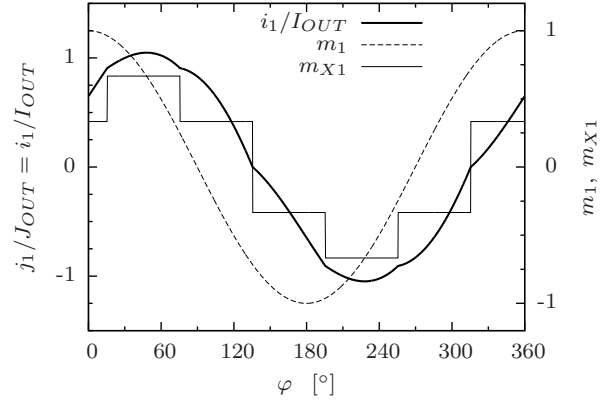


Fig. 11. Waveforms of i_1 , v_1 , and v_{X1} , mode 4, $M_{OUT} = 1$.

such that modes 0, 2, and 4 are presented in thick line, while modes 1 and 3 are presented in thin line. In modes 1 and 2, significant dependence of the output voltage on the output current is observed. Numerically obtained results for the continuous conduction mode correspond to the analytical results of [3].

Dependence of the rectifier power and the apparent power on M_{OUT} is presented in Fig. 13. Again, in the continuous conduction mode results are in good agreement with the analytical results of [3]. Maximum of the normalized power is numerically obtained as $P_{OUT\ max} = 0.68392$ at $M_{OUT} = 1.0130$, in the continuous conduction mode, i.e. mode 4. Extending the exact analysis of [3], closed-form exact expressions provided $P_{OUT\ max} = 27/(4\pi^2) \approx 0.68392$ at $M_{OUT} = 9\sqrt{2}/(4\pi) \approx 1.01286$.

Dependence of the power factor and the displacement power factor on M_{OUT} at the rectifier input is presented in Fig. 14, while the same parameters measured at the diode bridge input are presented in Fig. 15. In both diagrams, significant reduction of the power factor is observed for $M_{OUT} > 1.5880$, which is the point where the input power factor reaches its

maximum of 0.9190. Higher values of the output voltage result in significantly increased distortion of the input currents, bad power factor, but good displacement power factor. This can also be concluded from the diagram of Fig. 15. In the case there are line inductance and added inductors both present in the system, as depicted in Fig. 3, voltage at the point of coupling is computed according to (2), and corresponding power factor and the displacement power factor at the point of coupling may be computed. In mode 0, power factor and the displacement power factor are not defined.

Dependence of the total harmonic distortion of the voltages at the inputs of the diode bridge is presented in Fig. 16. Continuous conduction mode i.e. mode 4, is clearly identified, by a constant THD value of $\sqrt{(\pi/3)^2 - 1} \approx 31.084\%$, as well as mode 0 where $THD = 0$ since the voltages at the diode bridge inputs are equal to the input voltages in this case.

Dependence of the input current THD on M_{OUT} is presented in Fig. 17. Rapid growth of the THD can be observed for $M_{OUT} > 1.5880$, and especially in modes 1 and 2. These operating modes, although being extremely interesting for application, are characterized by significant harmonic distortion

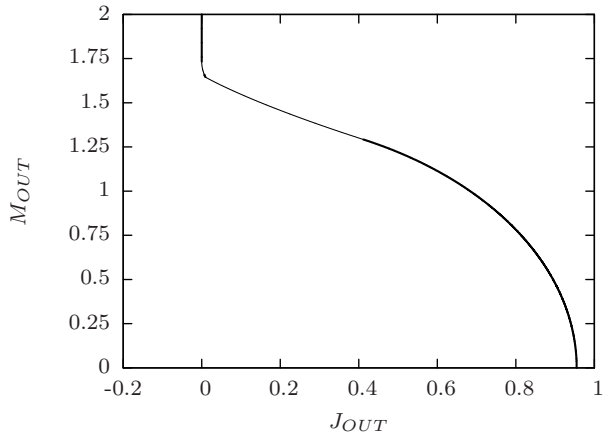


Fig. 12. Dependence of M_{OUT} on J_{OUT} .

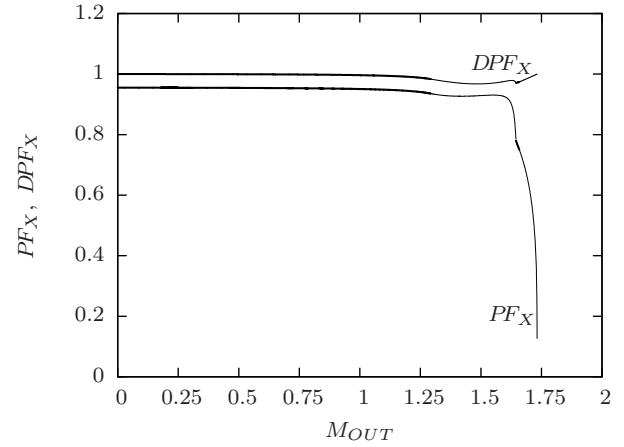


Fig. 15. Dependence of PF_X and DPF_X on M_{OUT} .

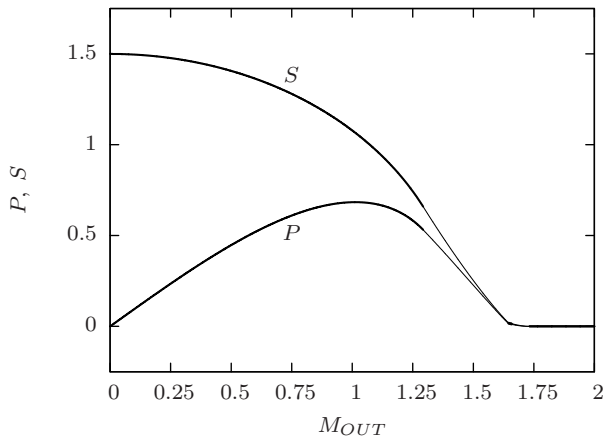


Fig. 13. Dependence of the rectifier power and apparent power on M_{OUT} .

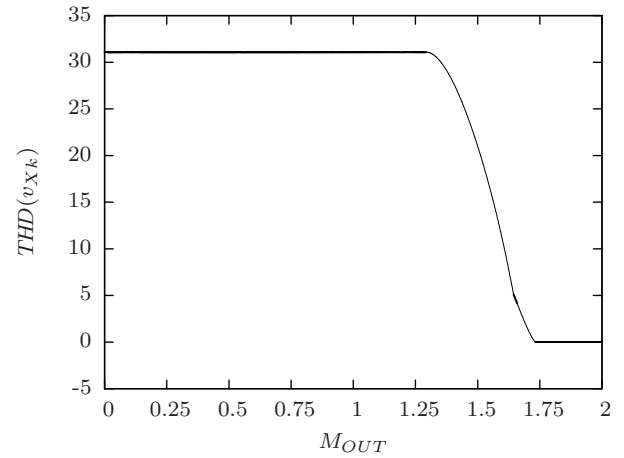


Fig. 16. Dependence of $THD(v_{Xk})$ on M_{OUT} .

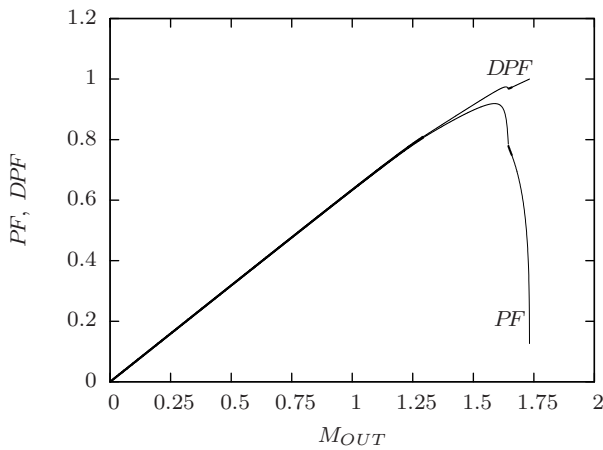


Fig. 14. Dependence of the rectifier power factor and the displacement power factor on M_{OUT} .

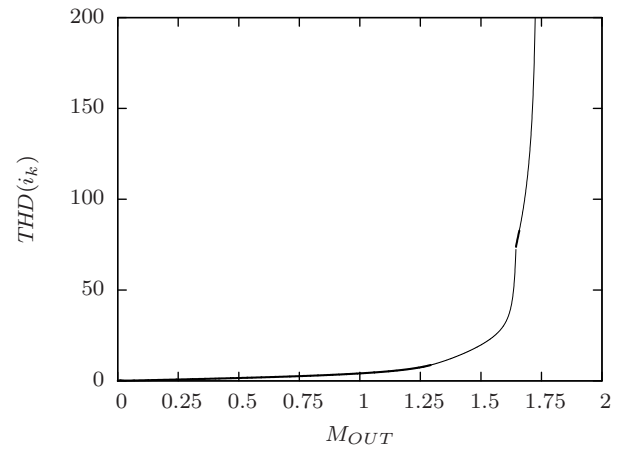


Fig. 17. Dependence of $THD(i_k)$ on M_{OUT} .

of the input currents. Maximum of the input current THD of 784.31% is recorded for $M_{OUT} = 1.7320$, which would be

significantly lower if finite capacitance was used.

Operating modes of the converter have been defined in somewhat arbitrary manner. After the results are obtained, the

definitions of modes should be revisited. In mode 0, order of the analyzed circuit is zero. Some parameters, like THD of the input current, power factor, and the displacement power factor, both at the rectifier input and at the diode bridge input, are not defined. Other parameters take defined values, but not dependent on M_{OUT} . In mode 1, the rectifier passes through intervals where order of the circuit is zero, as well as the intervals where order of the circuit is one. All of the analyzed parameters are defined, being dependent on M_{OUT} . In mode 2, in comparison to mode 1 intervals where the circuit is of the second order start to appear. On the boundary between modes 1 and 2 there is no obvious lack of differentiability in the curves of analyzed parameters, although this is not analytically proven. In mode 3, in comparison to mode 2, intervals where the circuit order is zero disappeared. On the boundary between modes 2 and 3, curves of analyzed parameters seem not to be differentiable. Mode 4 is the continuous conduction mode, where an analytical closed-form solution for the rectifier exists [3], and the circuit is of the second order during the whole period. In the parameter curves, there is no obvious lack of differentiability on the boundary between modes 3 and 4. In mode 4, THD of the voltages at the diode bridge input is constant, not dependent on M_{OUT} , since the waveforms maintain fixed six-step staircase pattern of Fig. 11 in this case.

VI. CONCLUSIONS

Numerical analysis of a three-phase voltage loaded rectifier coupled to the supply voltage sources with three inductors is presented in this paper. In contrast to the common approach based on the simulation on component level, the simulation is performed on the equation system level, which provides insight in the rectifier operation, identification of the operating modes, and much easier handling of the circuit order variations and model singularities. Voltages and currents of the rectifier are normalized in order to generalize the results.

In analysis of possible combinations of diode states, combinatorial approach is applied. Out of $2^6 = 64$ combinations of diode states, due to the limitations imposed by interconnections of the circuit elements only 13 combinations are shown to be possible to appear during the circuit operation. For all 13 of possible diode state combinations, circuit equations are derived, showing that the circuit order might be zero, one, or two, depending on the diode state combination. For each of the diode state combinations, boundary inequalities are derived, being accompanied by the combination transition rules that specify the next combination if a boundary inequality is violated. Again, due to the element interconnections number of inequalities that should be monitored varies from three to six, depending on the diode state combination. Actually, there are always six inequalities caused by six diodes, but some of them are implicitly satisfied in some of the diode state combinations, and should not be monitored. Phenomenon of instantaneous combination transitions is also analyzed, which is a situation when after a boundary condition is violated the rectifier switches from one combination to another, but the switching causes another transition instantaneously. Modes of the circuit operation are defined such that in mode 0 the circuit

is of the order zero during the whole period, in state 1 there are intervals when the circuit order is zero and intervals where the circuit is of the first order, in mode 2 the circuit order might be zero, first, and the second, depending on the time interval, in mode 3 there are only intervals where the circuit is of the first and the second order, and finally mode 4 corresponds to the continuous conduction mode where the circuit is of the second order during the whole line period.

Proposed method is implemented, and the simulation is performed for the normalized output voltage M_{OUT} in the range from 2 down to 0 in steps of 0.0005. Regions in M_{OUT} in which the rectifier operates in specific modes are determined, as well as the boundary values of M_{OUT} between the modes. Dependence of M_{OUT} on J_{OUT} is presented, as well as the diagrams that present dependence on M_{OUT} of the rectifier power, apparent power, power factor and the displacement power factor both at the rectifier input and the diode bridge input, as well as total harmonic distortions of the input currents and the voltages at the inputs of the diode bridge. Different behavior dependent on the operating mode is observed. For $M_{OUT} > 1.5880$, which is the value where the power factor at the rectifier input reaches its maximum, rapid growth in the distortion of the input currents occurs, resulting in rapid decrease of the power factor.

Applying mentioned techniques, analysis of the voltage loaded three-phase diode bridge rectifier is extended beyond the continuous conduction mode, where the closed-form exact solution of the rectifier model [3] exists, to four discontinuous conduction modes where the circuit varies its order from zero to two. Obtained normalized diagrams may serve as a quick reference guide for the rectifier design. Presented analysis might also be of interest in education.

REFERENCES

- [1] V. Caliskan, D. J. Perreault, T. M. Jahns, and J. G. Kassakian, "Analysis of three-phase rectifiers with constant-voltage loads," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 50, no. 9, pp. 1220–1226, Sep. 2003.
- [2] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, 2nd ed. Norwell, MA: Kluwer Academic, 2001, pp. 709–740.
- [3] P. Pejović, J. W. Kolar, "Exact analysis of three-phase rectifiers with constant voltage loads," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 55, no. 8, pp. 743–747, Aug. 2008.
- [4] O. H. Schade, "Analysis of rectifier operation," *Proc. IRE*, vol. 31, pp. 341–361, 1943.
- [5] P. Richman, "Wave factors for rectifiers with capacitor input filters, and other high crest factor loads," *IEEE Trans. Ind. Electron. Contr. Instrum.*, vol. IECI-21, no. 11, pp. 235–241, Nov. 1974.
- [6] A. G. Bogle, "Rectifier circuit performance: Some new approximate formulas," *Proc. Inst. Elect. Eng.*, vol. 124, pp. 1127–1134, 1977.
- [7] W. P. Gibbons, "Current and voltage waveform distortion analysis on three-phase "wye" power systems with rectifier loads," *IEEE Trans. Ind. Appl.*, vol. IA-19, no. 2, pp. 181–190, Mar./Apr. 1983.
- [8] K. S. Hall, "Calculation of rectifier-circuit performance," in *Proc. Inst. Elect. Eng. A*, 1980, vol. 127, pp. 54–60.
- [9] J. Schaefer, *Rectifier Circuits: Theory and Design*. New York: Wiley, 1965.
- [10] A. W. Kelley and W. F. Yadusky, "Rectifier design for minimum line-current harmonics and maximum power factor," *IEEE Trans. Power Electron.*, vol. 7, no. 4, pp. 332–341, Apr. 1992.
- [11] M. Grötzbach and R. Redmann, "Line current harmonics of VSI-fed adjustable-speed drives," *IEEE Trans. Ind. Appl.*, vol. 36, no. 2, pp. 683–690, Mar./Apr. 2000.
- [12] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics—Converters, Applications, and Design*, 3rd ed. Hoboken, NJ: Wiley, 2003, pp. 109–111.