Optimal Design of a Compact 99.3% Efficient Single-Phase PFC Rectifier

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***Abstract*—Due to rising energy costs the efficiency of power electronics converter systems is of higher and higher importance, especially for applications with continuous operation as e.g. server power supplies. For designing such supplies numerous parameters like the switching frequency and the characteristic values and the geometry of magnetic components must be determined. In this paper, an optimisation procedure, which automatically determines the parameter values of a single-phase bridgeless PFC rectifier for maximum efficiency is presented. There, continuous and discontinuous operation mode, as well as a concept for magnetic integration of the CM and DM filter inductors is included. For verifying the considerations, a prototype with 99.3% efficiency and a power density of 1.35kW/dm^3 is presented.**

I. Introduction

In the last decades, increasing the power density ρ has been one of the most important design criteria in power electronics [1]–[4] besides cost reduction. There, an increase of the efficiency η was only indirectly required, as a lower system volume results in a smaller surface for power loss dissipation. However, due to environmental concerns, efficiency became more and more important, so that now at least two design targets, i.e. high power density and high efficiency, have to be met at the same time. This results in a multi-objective optimisation problem, where the design parameters, as e.g. the component values or the geometry of magnetics, are selected under consideration of multiple performance indices like costs, volume, efficiency, etc.

In [5] single-phase PFC rectifier systems have been optimised for efficiency and alternatively for power density. Furthermore, the trade-off between the two competing design criteria has been investigated. Based on analytical expressions describing the relation between maximal achievable efficiency and power density, the limit (Pareto-Front) in the efficiency-power density performance space (η-ρ-plane) has been derived and the sensitivity of the Pareto-Front on the applied technologies has been investigated. Furthermore, a prototype with an efficiency of 99.09% and a power density of ≈1.1kW/dm^3 at f_P=33kHz switching frequency has been presented.

TABLE I: Specifications of the proposed ultra-efficient, bridgeless single-phase PFC rectifier with two interleaved systems.

Output Power P_O	2×1.6kW
Line Voltage U_N	230±10%
Output Voltage U_O	365V – 400V
Ambient Temperature	45°C
Power Density	1.35kW/dm^3
Efficiency	99.3%

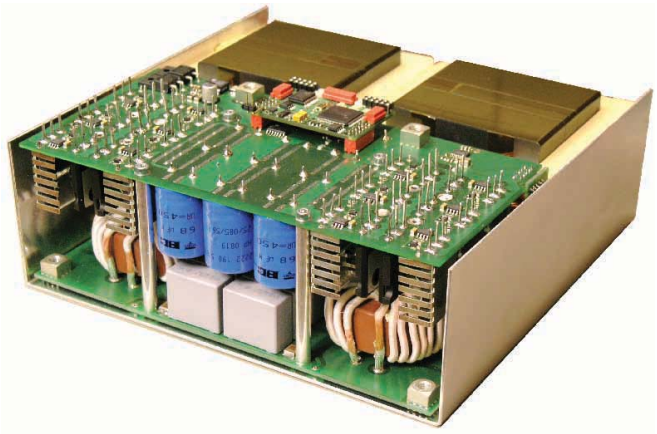

Fig. 1: Laboratory prototype of the proposed ultra-efficient 3.2kW dual-boost PFC rectifier composed of two interleaved 1.6kW units with f_P=16kHz; overall dimensions: 190mm×188mm×65mm; output power density: 1.35 kW/dm^3, efficiency: 99.3%.

However, the structure of the optimisation procedure has been only briefly explained. In this paper, the analytical models of the converter and of the magnetic components as well as the efficiency optimisation procedure are described in detail (section III). There, in contrary to [5] discontinuous (DCM) and continuous (CCM) conduction mode in sections of the mains period is covered. Furthermore, a magnetic integration of the common mode (CM) EMI filter inductor and the boost inductor into a single magnetic component is proposed (section II) which increases the system power density as well as the efficiency compared to [5]. Moreover, the system design and the cooling concept are improved.

Using the optimisation procedure, the parameter values and the combination of DCM and CCM resulting in maximum efficiency are determined in section IV Finally, in section V a prototype system and details of the system design are presented.

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II. High-Efficiency Single-Phase PFC Rectifier Topology

The basis of efficiency optimisation is the choice of the most suitable circuit topology that enables minimum semiconductor losses at low semiconductor chip area requirements, i.e. low realisation costs. The most used single-phase PFC boost rectifier concepts are the conventional boost, the bridgeless/dual boost and the dual-boost AC-switch PFC rectifier [5], [6]. There, the freewheeling boost diodes are frequently realised with SiC Schottky diodes in order to minimise the transistor turn-on losses. Accordingly, relatively complex soft-switching topologies as e.g. presented in [7], [8] do not provide an advantage concerning efficiency.

With the standard bridgeless PFC rectifier a switching frequency CM voltage occurs at the system output. According to [9] this can be avoided by adding clamping diodes from the negative rail n to the two mains connections. For reducing the volume of this approach a configuration with two inversely coupled DM/CM inductors with equal turn numbers and equal inductances of all windings has been presented in [10]. There, always one winding of each of the two series connected inductors is short circuited via the constantly turned on switch and the conducting clamping diode. Most of the return current flows via the clamping diode, so that the turned on switch and also the short circuited windings of the two inductors are not utilised during this interval. However, both cores are fully utilised, what is the benefit of this concept in contrast to two separate inductors [10].

An alternative solution, which has been proposed in [5], is to connect the midpoint or one of the two rails of the output via two capacitors to the two mains connections as shown in Fig. 2. This solution has a similar performance with respect to EMI as the solution with the two additional clamping diodes, but the chip area required for the clamping diodes and the related conduction losses are saved as most of the return current flows via the constantly turned on MOSFET. There it is important to note that with this concept one inductor is operating as CM inductor and one as differential mode (DM) boost inductor and both usually do not have the same number of turns and/or inductance values. This is in contrast to the diode clamped bridgeless converter with optimised inductors.

For reducing conduction losses, diodes commutated with mains frequency should be replaced by MOSFETs operating as synchronous rectifiers. A replacement of the freewheeling diodes is not possible as the nonlinear parasitic output capacitance of superjunction MOSFETs would significantly increase the switching losses. Considering the four above mentioned topologies, different amounts of silicon area are required for achieving the same conduction losses [5]. In the bridgeless PFC boost rectifier with capacitive coupling the current flow in the turn-on interval is only via two MOSFETs and via a fast diode and a power MOSFET in the turn-off/boost interval, if S_2 is continuously turned on for $u_N > 0$ (and/or S_1 for $u_N < 0$).

In the bridgeless PFC boost rectifier with clamping diodes, the clamping diodes must be replaced by synchronous rectifiers, in order to achieve the same conduction losses as for the bridgeless system with capacitive coupling. Thus, the total required chip area is 4 A_{Chip} (A_{Chip} is the chip area of a single boost transistor of the bridgeless PFC) for the MOSFETs plus 2 fast commutated diodes for the diode clamped and 2 A_{Chip} plus 2 fast commutated diodes for the capacitively coupled bridgeless PFC (cf. Fig. 3). There, it is assumed that the total line-frequency return current flows via the respective clamping diode and is not shared between the clamping diode and the inactive switch/inductor [6] as approximately given for most designs [10]. In case the current is dividing, the required chip area could be reduced.

If for a conventional PFC boost rectifier equally low conduction losses as for the capacitively coupled bridgeless PFC rectifier should be achieved, four power MOSFETs for synchronous rectification are required as replacement of the four mains-commutated input rectifier diodes. Consequently, a MOSFET chip area of 9 A_{Chip}, as well as one SiC freewheeling diode are required for the conventional PFC system (cf. Fig. 3 [5]). In the AC-switch PFC converter two of the four rectifier diodes could be replaced by MOSFETs. The other two diodes are commutated with switching frequency and have to be realised with SiC Schottky diodes. Consequently, for the

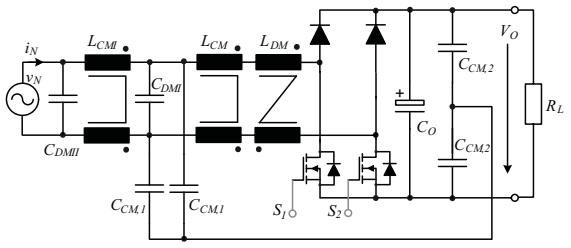

Fig. 2: Circuit diagram of the dual boost (bridgeless) rectifier with capacitive coupling of the output voltage to the mains and/or earth and EMI-filtering stage.

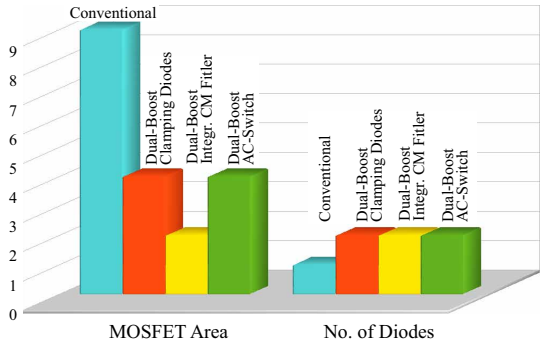

Fig. 3: *Left:* Total MOSFET chip area required for equal conduction losses of the conventional boost, the bridgeless/dual boost and the dual boost AC-switch PFC rectifier [5]. *Right:* Number of required fast recovery (SiC) freewheeling diodes. In the topologies all line-commutated diodes are replaced by MOSFETs for reducing the conduction losses by synchronous rectification.

AC-switch PFC rectifier a MOSFET chip area of 4 A_{Chip} and 2 fast SiC diodes are required.

In summary, with regard to high efficiency at given total semiconductor chip area, the capacitively coupled bridgeless PFC boost rectifier with integrated CM filter as shown in Fig. 2 is clearly preferable.

A. Integrated Magnetics

In the original design of the capacitively coupled bridgeless PFC (cf. Fig. 2) two independent inductors with two windings are utilised. One of the inductors operates as CM filter inductor and the other one realises the DM boost inductor. In normal operation switch S_2 is constantly turned on if the mains voltage u_N is positive, and S_1 in combination with D_1 and L_{DM}/L_{CM} performs the boost function. Due to capacitors $C_{CM,1}$ and $C_{CM,2}$ always one branch of the series connected inductors L_{DM}/L_{CM} is short circuited for higher frequencies via the constantly turned on MOSFET. Consequently, the

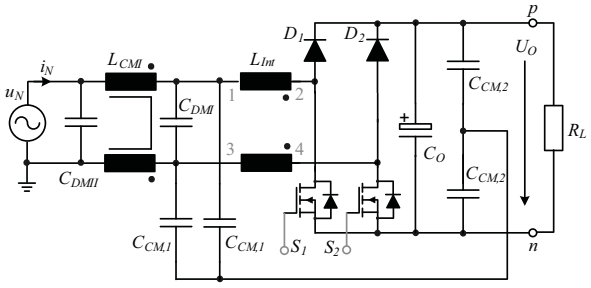

Fig. 4: Bridgeless PFC with integrated magnetics (w/o EMI filter).

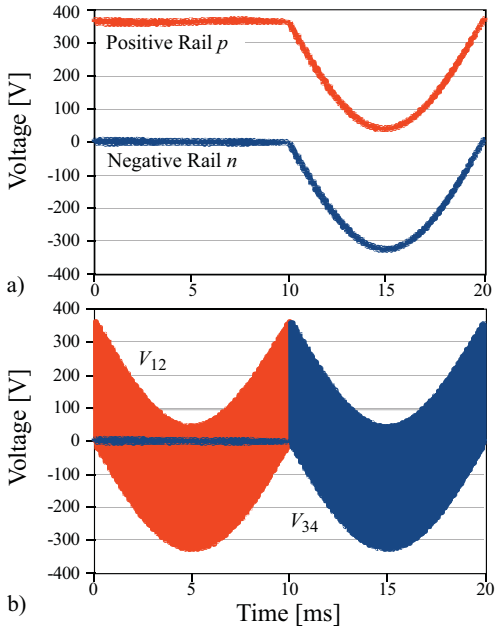

Fig. 5: a) Voltage of the positive p and negative n rail (cf. Fig. 4) to earth. b) Voltage across the two windings of the integrated magnetic device.

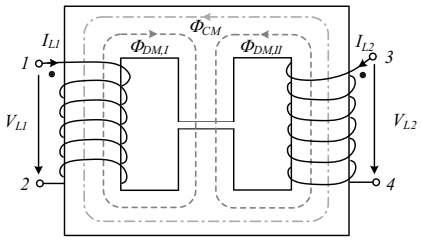

Fig. 6: Integrated magnetic device with CM and DM flux directions for positive mains voltage.

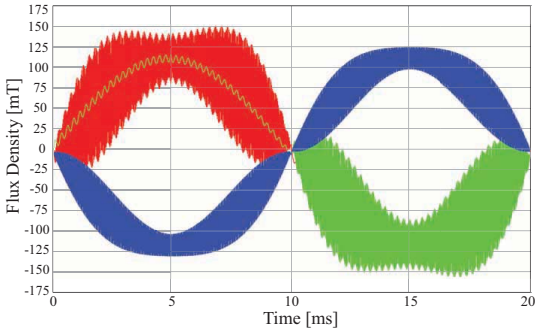

Fig. 7: Simulated flux density waveforms for the integrated magnetic device based on the design parameters given in section V. There the cross-sectional area of the middle leg is twice as large as for the outer legs (2 × E70 core).

negative rail n of the output voltage mainly varies at low frequencies (cf. Fig. 5). The high-frequency component of the CM voltage drops across the CM inductor, which also limits the high-frequency CM current flowing in the loop formed by L_{DM}/L_{CM}, $C_{CM,1}/C_{CM,2}$ and the MOSFETs. This also could be seen in the CM equivalent circuit given in [5]. The LF part of the CM voltage drops across capacitors $C_{CM,1}/C_{CM,2}$ and result in a LF variation of the CM output voltage as could be seen in Fig. 5a), where the voltage of the positive p and the negative rail n of the output voltage against earth is shown.

For integrating both inductors, the two windings are put on one core and paths for the CM and the DM flux are provided as shown in Fig. 6. The DM flux flows always through one of the two windings and the middle leg, where an air gap is used to determine the DM/boost inductance. The CM flux flows through both windings and the two outer legs of the core. By adjusting the number of turns and/or an air gap also in the outer legs the CM inductance value could be adjusted. However, usually a CM inductance as large as possible is required, so that no air gap is necessary in the outer legs, except for limiting the CM flux.

In Fig. 7 the simulated flux time behaviour for one mains period is shown for the design described in section V. It can be clearly seen, that the DM flux is proportional to the input current and that a HF flux is always present in only one of the two outer legs whereas and in the other leg only a LF flux with a small ripple occurs.

III. Models and Optimisation Procedure

In the following analytical models for the capacitively coupled and magnetically integrated bridgeless PFC rectifier are derived, which are used to optimise the system parameters for minimal losses. The degrees of freedom in the optimisation are the switching frequency f_P, the geometry of the boost inductance, and the power semiconductor chip area A_{Chip}, i.e. the number of power MOSFETs and SiC diodes connected in parallel for realisation of a power transistor S_1, S_2 and/or a freewheeling diode D_1, D_2. Furthermore, the value of the boost inductance is varied, what influences also the operation mode. In the algorithm CCM, and DCM as well as a combination of both modes in sections of the mains period is considered.

The optimisation is carried out for nominal power and nominal input and output voltages, but basically any power level and/or input/output voltage could be considered in the algorithm. Even a combination of the efficiencies at different operating points, e.g. at 100% and 50% load, could be used as quality criteria.

In the optimisation the volume of the boost inductor L_{DM} is limited to a fixed value, since the inductor volume would grow in the course of the optimisation above all limits, because the losses monotonically decrease with increasing inductor volume [5].

In Fig. 8 a flowchart of the developed procedure for optimising the design variables (f_P, chip area of MOSFETs and diodes, number of turns and geometry of boost inductor) is shown.

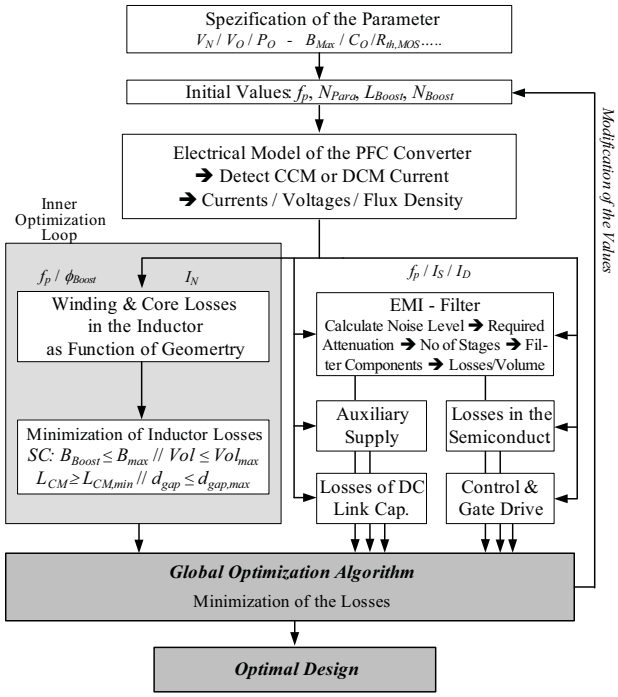

Fig. 8: Flow chart of the optimisation procedure for maximising the efficiency.

The starting point of the procedure is the specification of the converter system, including input/output voltages and the output power but also component limits as e.g. the maximal allowed flux density or the maximal junction temperature of the MOSFETs, which are the constraints during the optimisation. Also the starting values of the design variables are set. With these values the currents/voltages of all the components and the losses in the semiconductor elements are calculated. There, for each switching action the operation mode is determined, so that also combined DCM/CCM operation can be considered.

Furthermore, the flux variation in each pulse interval is calculated. This is used in an inner optimisation loop, which determines the number of turns and the geometry of the core and the winding resulting in minimum boost inductor losses. Since the aim of the optimisation is an ultra-high efficiency, no thermal models for the core and the windings is required, which would limit the design in case the volume of the inductor would be minimised. In the ultra-high efficiency system all components are operating well below their thermal limits, what is also advantageous with respect to life time and reliability.

The global optimisation algorithm adds the losses of the boost inductor, the CM filter inductor, the semiconductors and varies then the free parameters, so that the overall system losses are minimised. In the system losses also the losses in the control, the output capacitor and the EMI filter, which are assumed to be constant, are included. Furthermore, the gate drive losses and the auxiliary supply losses which slightly depend on the MOSFET´s chip area are added.

In the following briefly the equations for the currents and voltages, the losses of the semiconductors and the magnetic components as well as the auxiliary power are summarised.

A. Semiconductors

Besides the fundamental component of the input current with amplitude $\widehat{I}_N$, also the ripple current

$$i_{N,r} = \frac{1}{2}\frac{U_O T_P}{L_{DM}}\frac{1}{M}\sin(\omega_N t)\sin\left(1-\frac{1}{M}\sin(\omega_N t)\right) \quad (1)$$

must be considered, where the modulation index M is defined as $M = U_O/\left(\sqrt{2}U_N\right)$. With the input current fundamental and the ripple current as well as the duty cycle

$$d = 1 - \frac{1}{M}\sin(\omega_N t) \quad (2)$$

the RMS current in a MOSFETs and the average current in the rectifier diodes are calculated for CCM.

Also, in the DCM/mixed DCM and CCM operation the average current in each switching cycle must be equal to the instantaneous value of the input current reference value. This results in

$$d_1 = \frac{\sqrt{2\widehat{I}_N L_{DM}\left(U_O - \widehat{U}_N\sin(\omega_N t)\right)}}{\sqrt{\widehat{U}_N T_P U_O}} \quad (3)$$

$$d_2 = d_1\,\frac{\widehat{U}_N\sin(\omega_N t)}{U_O - \widehat{U}_N\sin(\omega_N t)} \text{ and } d_3 = 1 - d_1 - d_2$$

for the relative on-time d_1 of the switching MOSFET, the relative freewheeling time d_2 of the diode and the zero current time d_3, where no current flows from the input if the parasitic capacitances of the MOSFETs/diodes are neglected. By setting d_3 to zero, the currents for DCM/mixed DCM and CCM operation with variable switching frequency of the PFC converter could be calculated.

Based on the currents the conduction losses of the semiconductors are determined. Equation

$$R_{DSon} = R_{DSon,25} + \frac{R_{DSon,125} - R_{DSon,25}}{125°C - 25°C} (T_j - T_a) \quad (4)$$

is used for calculating the conduction losses in dependency of the junction temperature T_j (T_a is the ambient temperature). By solving

$$T_j - T_a = \frac{R_{th,MOS}}{N_{P,MOS}} \left(P_{on} + P_{off} + R_{DSon} I^2_{MOS,RMS} \right) \quad (5)$$

for T_j, the losses can directly be calculated, without any iteration. There, $N_{P,MOS}$ is the number of parallel connected MOSFETs and P_{on}/P_{off} are the switching losses, which are calculated below. A similar equation is used for determining the junction temperature of the rectifier diodes, which influences the forward voltage drop.

The power transistors are controlled such, that each transistor is switching during half a mains period where the other transistor is turned-on continuously for minimising the conduction losses.

In a next step, the current values at the turn-on and the turn-off of the switching MOSFET are determined based on the above calculated input current. The switched currents are required for calculating the switching losses based on measured loss curves.

Due to the large parasitic output capacitance of the parallel connected MOSFETs ZVS conditions are given during turn-off, so that the turn-off losses are very small and neglected in the considerations. This is also true for the switching losses of the SiC Schottky diodes employed as freewheeling diodes. Thus, the switching losses are mainly occurring during the turn-on of the MOSFETs.

B. Magnetic Components

Besides the semiconductors, the boost inductor is one of the major loss contributors. In the considered system the inductor is realised with foil windings and the geometric design of the inductors is determined by the four variables a, b, c and d as explained in [2]. With these variables for example the cross sectional area of the magnetic core or the core window area could be expressed and the losses in the core or the winding can be determined as function of these variables. This relation between the geometry and the losses then enables an optimisation of the number of turns and the geometry for minimal losses.

For calculating the winding losses first the harmonics of the winding current are calculated by Fourier analysis. The time behaviour of the inductor current is determined with the converter model and as worst case approximation it is assumed, that the complete return current flows via the inductor winding and not the coupling capacitors $C_{CM,\nu}$. With the amplitude and the frequency of the harmonics, the skin and proximity effect losses at each frequency are calculated with an 1-D approximation as e.g. presented in [11]–[13] and then – based on the orthogonality of the losses [14] – the losses at the single harmonics $\hat{I}_{L(i)}$ are added [5].

For calculating the proximity effect losses in the inductor, it is assumed that there is an air gap only in the middle leg, i.e. the H-field ramps from 0 to $+H_{max}$. Furthermore, the losses in the winding due to the fringing field of the gap are neglected in order to simplify the calculations, what does not result in a too large error in the considered case due to a relatively large distance between foil winding and air gap as FEM simulations have proven. In all the calculations the losses are expressed as function of the variables a, b, c and d, so that it is possible to optimise the geometry of the core and the winding for minimal losses.

For the core losses, the flux density time behaviour in the core must be determined (cf. Fig. 7). The DM flux density follows a 50Hz major loop and minor magnetisation loops with switching frequency in case of CCM and only minor loops in case of DCM. In both cases the core losses can be calculated based on the method proposed in [15], where the Steinmetz coefficients [16] are utilised for characterising the core material and where the rate of change of the flux density (dB/dt) is the basis for the loss calculation [5].

With an appropriate choice of the CM inductance and coupling capacitance value, the CM flux has a relatively high mains frequency fundamental and only small high frequency harmonics (cf. Fig. 7). Both result in relatively small losses compared to the DM flux and are therefore neglected here. But the peak value of the CM flux must be considered together with the peak DM flux in the optimisation in order to avoid saturation. The peak flux density $B_{m,max}$ in the middle leg is given by

$$B_{m,max} = \frac{L_{DM} I_{DM,max}}{N A_{core,m}} \quad (6)$$

and the $B_{o,max}$ of the outer leg by

$$B_{o,max} = \frac{L_{DM} I_{DM,max}}{2 N A_{core,o}} + \frac{L_{CM} I_{CM,max}}{N A_{core,o}}. \quad (7)$$

Current $I_{CM,max}$ is the CM mode current flowing in L_{CM}.The second constraint in the optimisation is the volume of the magnetic component, which must be limited as explained above [5].

C. Output Capacitor, EMI-Filter & Auxiliary Supply

For achieving a very high efficiency also minor loss contributions must be considered and minimised. The losses in the output capacitor can be calculated with the RMS current in the output capacitor and the ESR usually given in the data sheet.

The losses in the auxiliary supply are calculated with the efficiency curve of the auxiliary supply and the auxiliary power

consumption of the controller, gate drives, measurement circuits, etc. In order to minimise these losses an ultra-low power controller and low power sensors are employed. Furthermore, the design of the auxiliary supply is optimised for minimal losses. All these losses are independent of the converter design except for the gate drive power, which depends on the chip area of the MOSFETs, i.e. the total gate charge.

The DM EMI filter is designed with the simplified approach presented in [17], where a symmetrical arrangement of the filter inductors is chosen in order to attenuate also mixed mode noise. Furthermore, all filter stages have the same inductance and capacitance value, since this results in the minimum filter volume. For calculating the required attenuation, it is assumed, that the total noise current $I_{Noise,RMS}$ (which consists of several harmonics at multiples of the switching frequency with according sidebands) would appear as a single peak only at the switching frequency. This peak would then cause a noise voltage U_{LISN} at the test receiver. The noise current and U_{LISN} are given by

$$I_{Noise,RMS} = I_{DM,RMS} - I_{N,RMS} \tag{8}$$

$$U_{LISN} = 50\Omega \cdot I_{Noise,RMS}. \tag{9}$$

With U_{LISN} the required attenuation could be calculated by comparing the noise voltage with the limit value. In case the switching frequency is below 150kHz, the required attenuation is defined by the first harmonic above 150kHz. There, the decay of the amplitude of the harmonics with increasing frequency must be considered.

With the required attenuation, the component values for the DM inductor and capacitor are determined with equations, which have been derived by minimising the filter volume. There, the volume is given as empirical function of the component value and the current/voltage. The volume is calculated for different numbers of filter stages and the solution with the lowest volume is chosen.

The required attenuation for CM depends significantly on the mechanical design, which determines the parasitic capacitances to earth. In order to limit the modelling effort and the complexity of the model, empirical values for the volume and the losses obtained with the prototype presented in [5] are used.

IV. Optimisation Results

Based on the procedure described in the previous section, a dual-boost bridgeless PFC rectifier with integrated magnetics (cf. Fig. 4) has been optimised for minimal losses at nominal output power and the specifications given in Table I. A result of the calculations, where the global optimisation algorithm has been replaced by a for-next loop for varying the operating frequency and the boost inductance value, is shown in Fig. 9. There, the optimised efficiency is shown in dependency of the switching frequency and the inductance of the boost inductor, so that besides the optimal operating point also the sensitivity of the operating point to frequency/inductance value variations is shown.

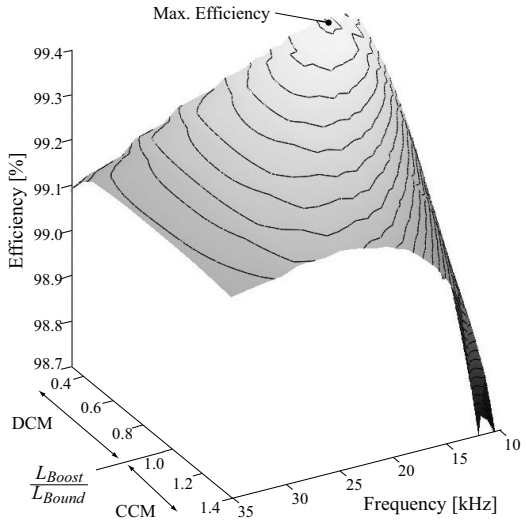

Fig. 9: Optimal efficiency and power density of the dual boost PFC in dependency of the switching frequency f_P and the inductance of the boost inductor. A value of 1 on the inductance axis is for an inductance value L_{Bound} resulting in an operation at the border of CCM. Decreasing the inductance value results in CCM and DCM operation in sections of the mains period.

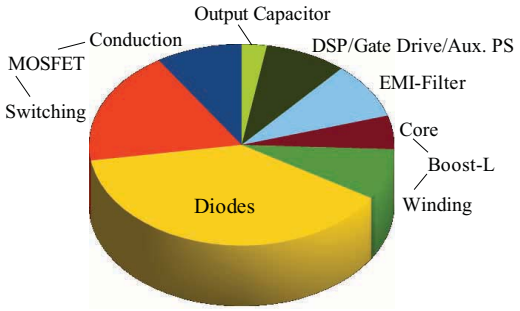

Fig. 10: Loss distribution of the optimised converter system with a switching frequency of 16kHz and a boost inductor of 400μH.

It is important to note, that the volume of the inductor is limited to maximal 0.3dm^3 for all considered operating points. This limit comes from practical considerations and available core shapes and sizes.

An optimal efficiency of 99.33% is achieved for an operating frequency of approximately 9.3kHz ($L_{DM} = 470\mu$H). There, the theoretical power density is roughly 2.8kW/dm^3. With decreasing frequency the efficiency drops relatively rapidly due the limit of the inductor volume. This limit results in increasing losses of the inductor, since a growing inductance value must be realised in a limited volume. Without this limitation, the optimal efficiency would be theoretically at $f_P = 0$ for an infinitely large inductor, what is not practical.

For higher switching frequencies, the losses in the semiconductors increase. First, the switching losses increase with increasing frequency and second, the optimal chip area resulting in minimal semiconductor losses decreases, so that also the conduction losses are increasing with switching frequency.

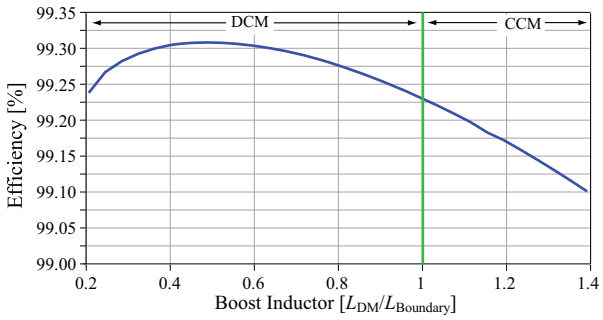

Fig. 11: System efficiency as function of the inductance value of the boost inductor L_{DM} related to the inductance $L_{Boundary}$ for which the limit of pure CCM operation is reached. The switching frequency is 16kHz.

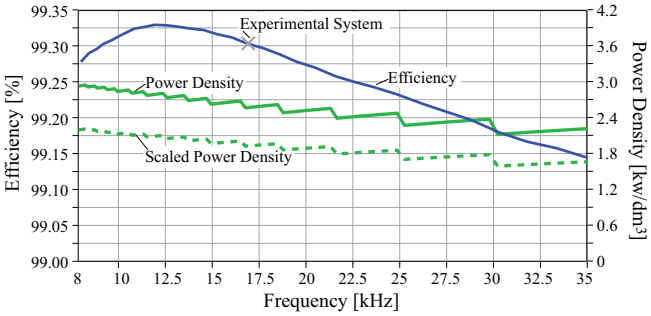

Fig. 12: System efficiency as function of the switching frequency for a fixed inductance L_{DM} = 400μH of the boost inductor. Furthermore, the power density obtained for considering the net component volume and the scaled power density, where also the volumes required for mounting of components, not matching component shapes, etc. is considered, are shown.

By shifting the operating frequency to 16kHz, i.e. out of the audible range, the efficiency just slightly decreases to 99.31%. Limiting the operation to the CCM results in a maximal efficiency of 99.24% at frequency slightly above 20kHz (L_{Boost} ≈800μH, 2.8kW/dm^3 theoretical power density based on net volumes).

The distribution of the losses for 16kHz switching frequency and L_{DM}=400μH is shown in Fig. 10. There, it could be seen that for the optimal system, the semiconductors cause the largest share of the system losses and that the forward voltage drop of the output diode has a significant influence on the efficiency. For the MOSFET losses it is important to note, that in the considered case the switching and the conduction losses are not equal for the optimal chip area, since additional effects as for example the parasitic capacitance of the freewheeling diodes are considered in the optimisation. Furthermore, it could be seen that the passive components and the auxiliary supply/control have a relatively low influence on the achievable efficiency.

In Fig. 11 the system efficiency as function of the boost inductance L_{DM} is shown for a switching frequency of 16kHz. A value of 1 on the x-axis means that the converter is operating at the boundary of CCM. This figure clearly shows that a mixed mode operation, i.e. a combination of CCM and DCM in sections of the mains period results in the highest efficiency at nominal load.

In Fig. 12 the system efficiency at nominal power is given as function of the switching frequency for a fixed inductance of 400μH of the boost inductor. Furthermore, the power density is shown as solid line and the scaled power density as dashed line. In the scaled power density also the additional volume resulting from mounting of components, not matching component shapes (e.g. cylindrical capacitors, rectangular magnetic cores) are considered besides the net component volumes. The steps in the power density result from the volume of the EMI filter, which increases with increasing switching frequency since lower order harmonics of higher amplitude move into the frequency band of 150kHz to 30MHz where the noise limits has to be met.

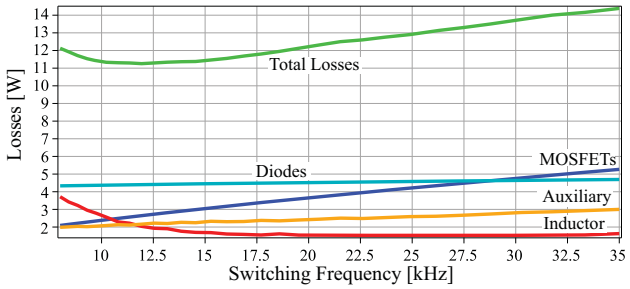

Fig. 13: Losses of the power semiconductors, the boost inductor L_{DM} and the auxiliary components in dependency on the switching frequency f_P. The boost inductor volume is set to a constant value and the inductance is adapted inversely proportional to f_P. Therefore, for increasing f_P a lower inductance value has to be realised in the same volume resulting in lower boost inductor losses.

V. Experimental Results

In order to verify the results of the optimisation, an ultra-efficient single-phase PFC boost rectifier system was realised. The system specifications were set to the values given in Table I. Two parallel subsystems are arranged, each with 1.6kW rated output power. To lower the level of EMI emissions, both systems include a triangular variation of the switching frequency between 17kHz and 20kHz with a period of 45ms, corresponding to the averaging time constant of the EMI measurement according to CISPR 22. This assures that the EMI measurement acquires the spectrum broadened by frequency modulation and reduced in amplitude.

The output capacitance is realised with parallel connected electrolytic capacitors with low ESR and low leakage currents, which also decrease during operating due to self healing effects. The output capacitance is 816μF resulting in a ripple voltage amplitude of 17V at nominal power.

Because of the low semiconductor losses, no heat sink is required and/or the cooling can take place directly via natural convection. Nevertheless, small heat sinks have been added in order to reduce the junction temperature for a lower $R_{DS,on}$. In connection with a current measurement with low intrinsic power consumption (75mW each) and the reduction of the

TABLE II: Components of the ultra-efficient bridgeless capacitively coupled and magnetically integrated PFC rectifier.

	Components
MOSFETs	Per Leg 0.011Ω
Diodes	600V SiC Schottky
Integrated Inductor	2 × E70 Core / 2 × 18turns
L_{DM}	2 × 200μH
L_{CM}	2.4mH
C_{CM1}=C_{CM2}	220nF (Foil)
Output Cap.	12×450V/68μF
Capacitor	Vishay BC2222198
C_{DMI}	2μF
L_{CMI}	1.2mH
C_{CMI}	22nF
C_{DMII}	2μF

calculating capacity of the DSP TI TMS 320 LF 2808 used for control from 100MIPS to 50MIPS, the overall auxiliary power consumption for the 3.2kW system can be limited to less than 2W. In the next step an ultra-low power micro controller (TI MSP430) will be used to reduce the control power further. The power components employed for realising the system (Fig. 1) are listed for one 1.6kW subsystem in Table II.

Unfortunately, the new generation of SiC Schottky diodes, which were assumed in the optimisation, have not been delivered in time, so that in the prototype system replacement diodes had to be used for the measurements. With these diodes, the system efficiency was determined to be 99.17% at the nominal operating point by means of a highly precise calorimeter measurement setup. This agrees very well with the calculation results of 99.2% if the data of the replacement diodes is inserted also in the calculations. The inaccuracy of the efficiency measurement is ±0.03% in worst case. The calorimeter was calibrated with comparative DC measurements and ultra-precise shunts and multimeters.

Overall, the 3.2kW system shows dimensions of 190mm×188mm×65mm and thus a power density of 1.35kW/dm^3.

VI. Conclusion

In the paper analytical models for calculating the losses of a bridgeless PFC rectifier with integrated magnetics are presented. With the models an optimisation of the converter for minimal losses is performed. The resulting optimal loss distribution is discussed and the sensitivity of the efficiency on the switching frequency and the operation mode – DCM or CCM – is investigated. Highest efficiency is achieved for mixed operation mode, i.e. a combination of CCM and DCM in sections of the mains period.

A maximal efficiency of more than 99.33% could be achieved for a switching frequency of 9.3kHz and of 99.31% for mixed DCM and CCM operation at 16kHz. For pure CCM mode operation at nominal power the maximal efficiency is 99.24% at a switching frequency slightly above 20kHz. For validating the results a prototype system operating at 16kHz has been built, which could achieve an efficiency of 99.3% at a power density of 1.35kW/dm^3. The measured losses agree very well with the theoretical predictions and the systems meets the required EMI standards.

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