Abstract — In this paper, a gate drive circuit for a 1300V/4A SiC-JFET is proposed and evaluated experimentally for a switching frequency of 200kHz. Furthermore, a comparison of the switching behavior of a SiC-JFET/Si-MOSFET cascode and of the SiC-JFET driven by the proposed gate drive circuit is shown.

Index Terms — gate drive circuit; silicon carbide; JFET; switching behavior.

I. INTRODUCTION

Novel silicon carbide (SiC) power semiconductors are characterized by outstanding performance concerning voltage blocking capability, on-state voltage drop, switching speed, and thermal resistance [1]. Accordingly, future SiC devices will allow the realization of highly compact converter systems with low switching and conduction loss. Furthermore, due to the wide band gap and/or blocking capability SiC devices are suitable for high voltage applications. SiC Schottky-diodes are already available commercially [2] and the SiC turn-off power semiconductors are currently under development [3].

The characteristics of the gate current \( I_G \) versus the gate voltage \( V_G \) (with reference to source) of a SiC-JFET are shown in Fig.1. Since the SiC-JFET is normally-on, a negative gate voltage is required for turning the device off. The pinch-off voltage is approximately \( V_G \approx -30\text{V} \) [4]. However, considering the variation of the pinch-off voltage with junction temperature and the influence of highly dynamic changes of the drain-source voltage on \( V_G \) via the Miller capacitance, a larger negative voltage should be applied for guaranteeing the power transistor turn-off state. This is complicated by the fact that the breakdown limit of the gate-source junction is around \(-40\text{V}\) and/or close to the pinch-off voltage and varies between samples and shows a dependency on the junction temperature.

Fig.2: SiC-JFET / Si-MOSFET cascode.

A SiC-JFET/Si-MOSFET cascode (hereafter called cascode) shown in Fig.2 can be turned off by using a silicon MOSFET (Si-MOSFET) connected in series with SiC-JFET [3]. However, there are several limitations of this concept as:

1) the maximum operating temperature of the cascode is limited by the Si-MOSFET,
2) the Si-MOSFET internal diode shows a low dv/dt-rating and therefore does limit the admissible switching speed for applications in bridge-type circuit configurations, and
3) the conduction losses do increase as two devices are connected in series.

Therefore, in this paper a gate drive circuit is proposed which does allow to safely operate a SiC-JET without employing a Si-MOSFET. The principle of operation of the gate drive is described in section II and experimentally verified in section III where also a comparison of the switching behavior of the SiC-JFET against the cascode arrangement is presented.

II. GATE DRIVE CIRCUIT FOR SiC-JFET

A simplified schematic of the proposed gate drive circuit is depicted in Fig.3. The SiC-JFET is turned on by turning on transistor \( T_{r1} \) (cf. Fig.4) and turned off by \( T_{r2} \) where an additional circuit is provided for limiting the gate current \( I_G \) as described in the following:

\( i1: \) we have \( V_G = 0\text{V} \) right after \( T_{r2} \) is turned on, the resulting voltage \( V_r \) across the limiting circuit is shared by \( R_a \) and \( R_b \) and \( T_{r3} \) is turned on. The gate current \( I_G \) is limited by \( R_g \) where

Fig.1: Gate characteristic of JFET samples at \( T_j = 25\degree\text{C} \) and \( T_j = 125\degree\text{C} \).
The SiC-JFET is turned off when $V_g$ exceeds the pinch-off voltage. Subsequently, $T_3$ is automatically turned off due to the decreasing voltage $V_r$.

$t_2$: The transistor $T_3$ is turned off and the current $I_g$ is limited by the resistors $R_a$ and $R_b$ to a low value

$$I_g = \frac{V_{gps} - V_g - V_{r_{T2}}}{R_a + R_b}$$

where $V_{gps}$ is supply voltage of the gate drive circuit and $V_{r_{T2}} \approx 0V$ is the voltage across $T_2$.

$t_3$: $T_1$ is turned on and $I_g$ is flowing through $T_1$, $D_1$ and $R_g$. As $V_g$ reduces to zero the SiC-JFET is turned on.

In summary, the proposed gate drive circuit does prevent a high gate current in the turn-off interval also for applying a gate voltage higher than the pinch-off voltage and does ensure a high switching speed.

### III. EXPERIMENTAL RESULTS

#### A. Experimental Condition

The gate drive circuit being employed for the experimental analysis is illustrated in Fig.5. In order to increase the turn-off speed of the SiC-JFETs, $R_a$ (cf. Fig.3) is divided to $R_1$ and $R_2$, and a capacitor $C_{g_1}$ is connected in parallel with $R_2$. Furthermore, a resistor $R_4$ is provided for limiting the reverse current of the base-emitter junction of $T_3$. In period $t_1$ (cf. Fig. 4), the base current in $T_3$ is flowing largely via $C_{g_1}$ as $R_2$ shows a comparably high impedance what does result in a fast switching action of $T_3$ and/or in a fast turn-off of the SiC-JFET. The DC supply voltage for the gate drive circuit is $V_{gps} = 45V$ and $V_{gps}$ is converted to 5V for supplying the driving optocoupler providing isolation of the gate drive signal. The Schottky diodes $D_3$ and $D_2$ are employed for increasing the turn-off speed in $T_4$ and $T_2$. The components employed in the gate drive circuit are listed in Table I. As the gate resistor, four 20Ω/250mW resistors are connected in parallel ($R_5 = 5\Omega$ in total) because the design is for a switching frequency of 200kHz. Based on (2), $I_g \leq 370\mu A$ is guaranteed for a breakdown voltage of $V_{g} < 35V$. 

![Fig.5: Schematic of the proposed gate drive circuit.](image-url)
The circuit configurations for testing cascades and the corresponding SiC-JFETs are shown in Fig. 6. The input voltage of the bridge leg is defined by a low inductance film capacitor $C_s$ (9µF/630V), the load current is impressed by an inductor $L_1$. The transistors $S_1$ are remaining in the turn-off state and are performing a free-wheeling diode function. There, for testing the SiC-JFETs a negative gate voltage $V_{ug} = -37V$ is applied (cf. Fig.6(b) and for testing the cascode the terminals $G$ and $S$ of $S_1$ are short circuited (cf. Fig.6(a)). A conventional gate drive circuit with output voltage levels 0V, +14V is employed for driving the Si-MOSFET.

Two subsequent turn-on pulses are generated by a control circuit (not shown in Fig.6). Within the first pulse, the load current increases via $S_2$. After a given current level has been reached the turn-off behavior of $S_2$ is recorded and the load current is commuted to the body diode of $S_1$. When $S_2$ is turned on again, the turn-on behavior of $S_2$ and the reverse recovery behavior of $S_1$ are acquired.

The SiC-JFETs and the cascodes are mounted on a heatsink equipped with a heating resistor, which allows to operate the setup at an elevated junction temperature of 125°C. The gate drive and the testing power circuit which are placed on the same PCB are shown in Fig.7. The instruments utilized for the measurements were a Tektronix TDS 544A (500MHz, 1GS/s) oscilloscope, voltage probes LeCroy PP005 (10:1, 500V, 10MΩ/11pF, 500MHz), and an 1:50 AC current transducer employing a R10/N30 toroidal ferrite core, a burden resistor of 5Ω and an adaptation network to a 50Ω coaxial cable. The switching energy losses were calculated by multiplying the measured voltages and currents and integrating the resulting power losses.

Reducing the parasitic capacitance of the load inductor is important for testing the actual switching performance and for reducing the switching losses [7]. Therefore, the load inductor $L_1$ (380µH/9A) is realized with low parasitic capacitance $C_1$. There, four inductors each employing a ferrite core EPCOS B66291 with approximately 0.1mm air gap and 10 turns are connected in series and the individual turns are separated by selecting a wire of 1mm isolation thickness. According to the impedance measurement shown in Fig.8, $C_1$ is reduced to 2.7pF.
B. Gate drive circuit

The operation of the proposed gate drive circuit was verified at zero drain current for a SiC-JFET showing a breakdown voltage of the gate-source junction lower than the gate drive supply voltage $V_{gps}$ (sample 2, cf. Fig.1). The gate voltage waveforms $V_g$ resulting for a switching frequency of 200kHz and a junction temperature of $T_j=125^\circ C$ are shown in Fig.9. In accordance to the theoretical considerations the maximum negative gate voltage is automatically limited to $-38.5\,V$ where a gate current $I_g$ of approximately $300\mu A$ does occur (cf. Fig. 1 and (2)). Then fall time and rise time of $V_g$ are 40ns and 71ns respectively what does guarantee a high switching speed of the SiC-JFET.

C. Switching behavior

The results of a comparative analysis of the switching behavior of the cascode and the SiC-JFET in combination with

Fig.9: Gate voltage waveforms of the SiC-JFET (sample 2) driven by the proposed gate drive circuit at 200kHz, $T_j=125^\circ C$ and $I_D=0$.

Fig.10: Turn-on behavior for $I_D=4A@T_j=125^\circ C$.

Fig.11: Turn-off behavior for $I_D=4A@T_j=125^\circ C$.

Fig.12: Reverse recovery behavior for $I_D=4A@T_j=125^\circ C$. 
the proposed gate drive circuit are shown in Fig.10, Fig.11 and Fig.12 for $T_{j}=125^\circ$C. According to the specification of the body diode of the Si-MOSFET the $dv/dt$ occurring across the transistor is limited to 6kV/µs by selecting a turn-on gate resistor of 390Ω and a turn-off gate resistor of 5Ω.

As compared to the cascode the SiC-JFET shows a reduced ringing at the switching transients [3]. Accordingly, no snubber circuit is required what does result in a compact converter design and low realization effort. The power semiconductor circuit is required what does result in a compact converter realization of the SiC turn-off power semiconductor without impairing the switching performance. This does significantly reduce the realization effort and does make feasible an operation at elevated junction and/or heatsink temperatures and/or does enable the realization of converter systems showing high power density.

**IV. CONCLUSION**

A novel gate drive circuit for SiC-JFETs being able to operate at 200kHz switching frequency and ensuring high speed was proposed. As compared to a SiC-JFET/Si-MOSFET cascode the SiC-JFET in combination with the novel gate drive shows lower switching and conduction losses and reduced ringing at the switching transients.

In summary, a Si-MOSFET can be omitted for the realization of the SiC turn-off power semiconductor without impairing the switching performance. This does significantly reduce the realization effort and does make feasible an operation at elevated junction and/or heatsink temperatures and/or does enable the realization of converter systems showing high power density.

**REFERENCES**


