

and/or to provide a basis for the estimation of the reduction of the converter losses or of the system weight and volume which could be expected by an extension of the basic converter topology to soft-switching or by increasing the switching frequency.

The DC/DC converter topology which has been selected in accordance with the above-listed requirements is shown in **Fig.1**. In order to make the application of power semiconductors with a blocking capability of only 600V possible the system is formed by an input series connection of individual converters *a* and *b* which is connected to the output voltage of the VIENNA Rectifier. The converter outputs are connected in parallel due to the high output current [2, 3]. The converter transformers T_a and T_b are operated with unidirectional magnetization and do not require a center tap of the secondary winding (as opposed, e.g., to full bridge converter topologies). The system employs only a single output inductor [4, 5], therefore, no special measures for balancing the output current between the partial systems have to be provided. The ripple of the output current (and/or the size of the output filter) is minimized by operating the partial systems 180° out of phase in switching frequency (ripple cancellation).

In the following in **section 2** the advantages of employing a common output inductor for both partial converter systems are verified by a comparison to a conventional realization with an individual output inductor for each partial system. In **section 3** the system control is discussed briefly and in **section 4** the dimensioning of the power components is treated and the distribution of the losses to the system components and the dependency of the efficiency on the system output power are shown in graphical form. **Section 5** shows results of an experimental analysis of a 10kW prototype of the system. Finally, in **section 6** an outlook towards the planned further development of the converter is given.

2 Selection of the Converter Topology

An output-side parallel operation of partial converter systems can basically be achieved by a direct parallel connection of the output terminals of the individual systems or by paralleling the systems at the freewheeling diodes. In this case advantageously only a single output filter stage has to be provided. In the following the stresses on the power components and the inherent stability of the potential of the capacitive input voltage center point M' will be briefly analyzed and compared for both system topologies.

As already mentioned the partial converter systems share a single output inductor L and are switched with a phase-shift of 180° in switching frequency, in order to double the frequency and the duty cycle d of the voltage being applied to the output filter. For a given peak-to-peak value $\Delta i_{L,p-p}$ of the output current ripple and/or of the output capacitor current $i_{C,p-p} = \Delta i_{L,p-p}$ the required inductance of the output choke is:

$$L = \frac{1}{i_{L,p-p}} \cdot \frac{u_O(1-2\delta)}{2f_p} \quad (1)$$

In order to achieve an equal value $i_{C,p-p}$ for a two output inductor converter one gets the relation:

$$\Delta i_{L,p-p} = \frac{1-\delta}{1-2\delta} \cdot i_{C,p-p} \quad (2)$$

Consequently, the inductance ratio of a single-inductor converter compared to a two-inductor system shows a value:

$$L_i = 2L \quad (3)$$

($i = a, b$) independent of the operating parameters. Since the average inductor current of the two-inductor converter is half the value given for the single-inductor converter, the total magnetic energy storage of both converters and/or the total inductor size is about the same.

A main drawback of the two-inductor converter is the higher inductor current ripple which is transferred to the primary side of the transformer and causes higher current (turn-off) and higher voltage stresses on the power transistors. E.g. for a duty cycle of $d = 0.4$ the inductor ripple current is three times higher as compared to the single-inductor converter; since the average inductor current is half the total output current the ratio of the peak-to-peak ripple current $\Delta i_{L,p-p}$ to the average inductor current i_L is 6 times higher. So the primary turn-off current increases from 105% of the transformed inductor current to 130%. When using laminated or iron-powder cores also the core losses due to the alternating magnetization will increase over-proportional in comparison to the decrease of the losses due to the lower frequency. The advantage of the two-inductor converter is the lower current stress on the rectifier diodes D_a and D_b .

In **Tab.1** for the single-inductor and for the two-inductor converter formulas for the inductance, the peak-to-peak inductor ripple current, and the voltage and average current stresses on the rectifier and free-wheeling diodes are given and corresponding typical numerical values are listed.

According to Tab.1 the freewheeling diode of the single output inductor converter could be realized with 100V Schottky

	Single output inductor		Two output inductors	
Output inductance	L	10 μ H	$2L$	20 μ H
Output Inductor current	i_O	200 A	$\frac{i_O}{2}$	100 A
Output inductor Ripple current	$\Delta i_{L,p-p}$	20 A	$\frac{1-\delta}{1-2\delta} \cdot i_{C,p-p}$	60 A
Rectifier diode Voltage stress	$\frac{u_O}{\delta}$	120 V	$\frac{u_O}{\delta}$	120 V
Free-wheeling diode Voltage stress	$\frac{u_O}{2\delta}$	60 V	$\frac{u_O}{\delta}$	120 V
Rectifier diode Current stress, avg	$i_O \cdot \delta$	80 A	$\frac{i_O}{2} \cdot \delta$	40 A
Free-wheeling diode Current stress, avg	$i_O \cdot (\frac{1}{2} - \delta)$	20 A	$\frac{i_O}{2} \cdot (1 - \delta)$	60 A

Tab.1: Inductance values, inductor currents, secondary side diode blocking voltages and average current stresses and typical values for a 10kW 48V/200A converter (input voltage: 800V) with $d = 0.4$ for the single-inductor and two output inductor converter (switching overvoltages neglected).

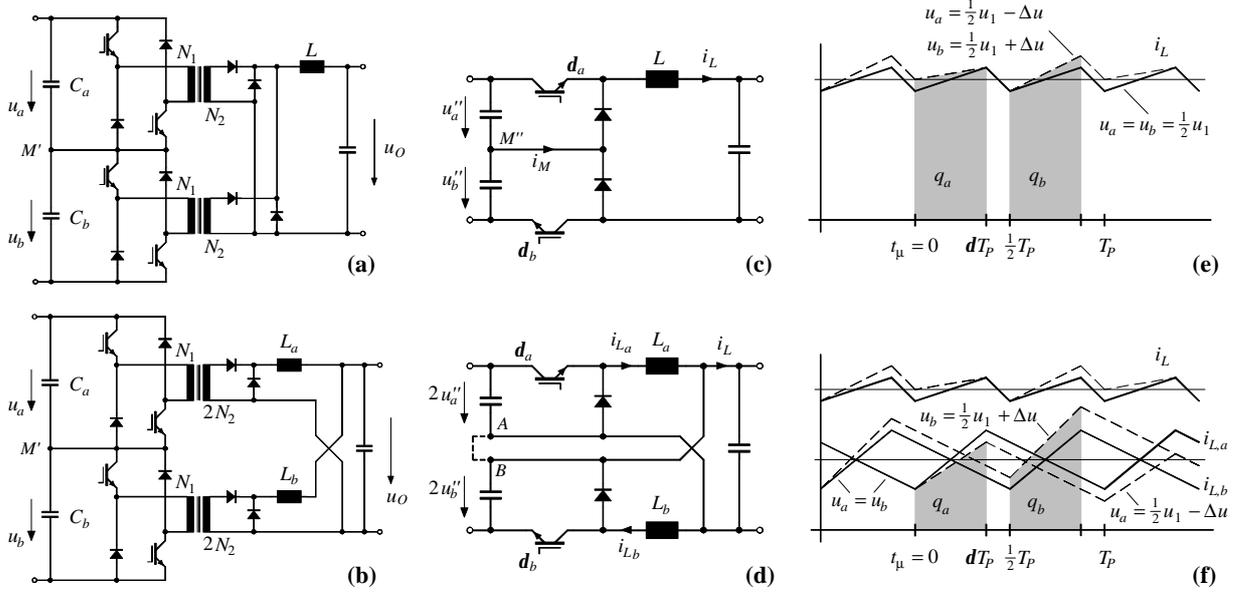


Fig.2: Basic structure of the power circuit of the DC/DC converter for (a) employing a common output inductor or (b) individual inductors for the partial systems a and b . (c) and (d): equivalent circuits for omission of the transformer isolation; the indicated connection of the terminals A and B in Fig.2(d) should only clearly show the formation of the total input voltage by the partial converter input voltages. (e) and (f): time behavior of the total output current and/or of the partial output currents for the systems shown in (a) and (b) for the assumption of an asymmetry $u_a = \frac{1}{2}u_1 - \Delta u$, $u_b = \frac{1}{2}u_1 + \Delta u$ of the partial input voltages occurring in a step like manner; q_a and q_b denote the electric charges being drawn from the input capacitors C_a and C_b within subsequent pulse half periods.

diodes to reduce their conduction losses (in the realized experimental converter system 200V diodes are employed).

2.1 Input Voltage Balancing

In order to achieve a high reliability of the converter system and/or for limiting the blocking voltage stress on the power semiconductors one has to ensure a symmetric distribution of the VIENNA Rectifier output voltage to the series connected inputs of the partial converters a and b .

In the following the inherent stability of the capacitive center point M' of the total input voltage u_1 (cf. Fig.1) shall be investigated for the single output inductor converter (cf. Fig.2(a)) by analyzing the effect of an asymmetry of the partial input voltages

$$u_a = \frac{1}{2}u_1 - \Delta u \quad u_b = \frac{1}{2}u_1 + \Delta u \quad (4)$$

on the current drawn from the input capacitors C_a and C_b in comparison to the known system behavior for individual output inductors of the partial converters [6] (cf. Fig.2(b)). As is obvious by considering the equivalent circuit Fig.2(c) and the time behavior of the partial input currents (Fig.2(e)) we have for the system shown in Fig.2(a) independent of Δu

$$u_O = \frac{N_2}{N_1} \cdot (u_a + u_b) \cdot \delta \quad (5)$$

($d_a = d_b = d$ denotes the relative turn-on time of the power transistors of the converters a and b). For the local (related to a pulse period) average value $i_{M,avg}$ of the current i_M drawn out of the input voltage center point M' there results

$$i_{M,avg} = 0. \quad (6)$$

As Fig.2(e) clearly shows, due to the common output inductor equal electric charge quantities $q_a = q_b$ are taken from C_a and C_b , therefore, the potential of M' does not show inherent stability but can be shifted without direct influence on the system behavior.

On the contrary, an unbalance of the partial input voltages according to Eq.(4) would result in a continuous decrease of the partial current $i_{L,a}$ and/or a corresponding increase of $i_{L,b}$ for the system shown in Fig.2(b); only the total output current i_L shows a time behavior identical with Fig.2(e). An increase/decrease of a partial voltage therefore is connected with an increase/decrease of the current drawn from the corresponding input capacitor. Therefore, the center point potential shows inherent stability and no special measures for stabilizing the input voltage distribution are required.

In summary, for the system shown in Fig.2(a) a controller $G(s)$ has to be provided for balancing the partial input voltages u_a and u_b (cf. Fig.3). In case a voltage unbalance Δu is present, the controller output slightly increases/ decreases the relative turn-on time ($d_a = d \pm \Delta d$, $d_b = d \mp \Delta d$) and/or the current consumption of the system being connected to the higher/lower partial voltage what results in a system behavior as given for individual output inductors and/or in a correction of the voltage unbalance [7]. As can be verified by a simple calculation, there the voltage transformation ratio still is defined by Eq.(5); therefore, the correction of an unbalance of u_a and u_b in a first approximation does not take influence on the control of the system output voltage.

Furthermore balancing windings $N_{3,a}$ and $N_{3,b}$ with equal numbers of turns $N_{3,a} = N_{3,b} = N_1 - \Delta N$ are provided (cf. Fig.1 and Fig.4), which recharge the input capacitor showing a

lower voltage out of the higher partial voltage within the corresponding converter turn-on time for voltage asymmetries being higher than

$$\Delta u \approx u_1 \frac{1}{4} \frac{\Delta N}{N_1} \quad (7)$$

(because the charging is in the forward mode resistors R_a and R_b are provided for limiting the compensating current). Therefore, also the maximum voltage unbalance occurring without controller action is defined by Eq.(7).

3 System Control

3.1 Output Voltage Control

The control of the system is realized in a two-loop structure, i.e., by an average-mode output current control with a superimposed output voltage controller. The output current reference value is defined mainly by the output capacitor current i_C which is measured using a simple AC current transformer. With this, a pre-control of the output current and an increased phase margin of the output voltage control (i_C is equivalent to the output of a D-type component of the output voltage controller) can be achieved with low additional realization effort. Consequently, the output voltage controller $R(s)$ only has to guarantee the stationary accuracy of the output voltage. Furthermore, the measurement of i_C gives a signal which allows a direct detection of an output short circuit condition [8].

Alternatively, the current control could also be realized as peak current mode control based on, e.g., sensing of the primary transformer currents. However, drawbacks of this control method as compared to average current mode control are the increased sensitivity to noise and the fact that the control and limitation of the output current is performed only indirectly which impairs the output short circuit behavior (cf. Fig.10 in [3]). Therefore, in the case at hand a direct average mode output current control is preferred because the power circuit topology in principle avoids transformer saturation and/or a direct measurement of the

transformer primary current is not necessary in principle.

The active balancing of the partial voltages is performed by an inverse displacement of the duty cycles of the two partial systems by the controller $G(s)$ (cf. Fig.4). If $u_{C,a}$ and $u_{C,b}$ are not of equal magnitude the duty cycle of the system showing the higher/lower partial voltage is increased/decreased. This results in a higher/lower average current drawn from the input capacitor showing the higher/lower partial voltage which finally leads again to $u_{C,a} = u_{C,b} = \frac{1}{2} u_I$.

3.2 Synchronization to the VIENNA Rectifier

The output capacitors of the VIENNA rectifier and the input capacitors of the DC/DC converter have been separated by a common-mode choke in order to avoid a priori a disturbance of the DC/DC converter control circuitry by switching frequency common-mode output voltage component of the rectifier. (A common-mode component with switching frequency is present in principle in the output voltage of all three-phase PWM rectifier systems.) This furthermore gives the possibility of performing the stabilization of the potential of the input voltage center point M' without consideration of details of the control of the VIENNA rectifier balancing the partial output voltages u_+ and u_- .

It has to be noted, however, that a direct parallel arrangement of C_+ , C_- and C_a , C_b would make possible a significant reduction of the capacitor current stress by synchronization of the switching of the rectifier and of the DC/DC converter (extended electrolytic capacitor service life and/or reduction of the minimum capacitance value required). This can be explained by the fact that C_+ is charged by the VIENNA Rectifier symmetrically at the beginning and at the end of a pulse interval T_p and the charging of C_- is shifted in time by $\frac{1}{2}T_p$. The DC/DC converter draws current at the beginning of a pulse period from C_a and shifted in time by $\frac{1}{2}T_p$ from C_b (according to the phase shifted operation of the converters a and b). Therefore, for equal switching frequency and proper phase displacement [9] the current consumption of the DC/DC converter can be provided directly by the rectifier avoiding the capacitor by-pass. With this, depending on the

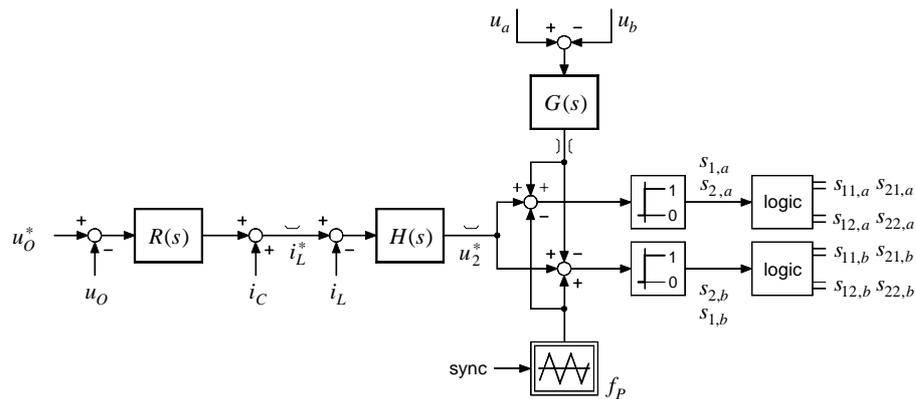


Fig.3: Block diagram of the system control. By the combinatorial logic circuit connected in series with the comparator, e.g., the switching signal $s_{1,a}$ is applied to the power transistors $S_{11,a}$ and $S_{12,a}$ (cf. Fig.4) alternatively, i.e., for turning on the transistor $S_{11,a}$, $S_{12,a}$ remains in the turn-off state and vice versa. Therefore, each power transistor of the parallel arrangement of $S_{11,a}$, $S_{12,a}$ and $S_{11,b}$, $S_{12,b}$ ($i=1,2$) is operated with only half the partial converter switching frequency and the problem of a simultaneous switching of two power transistors (equal sharing of the switching losses) and of a symmetric distribution of the total current and/or of the conduction losses between devices showing a negative temperature coefficient of the forward voltage drop is a priori avoided.

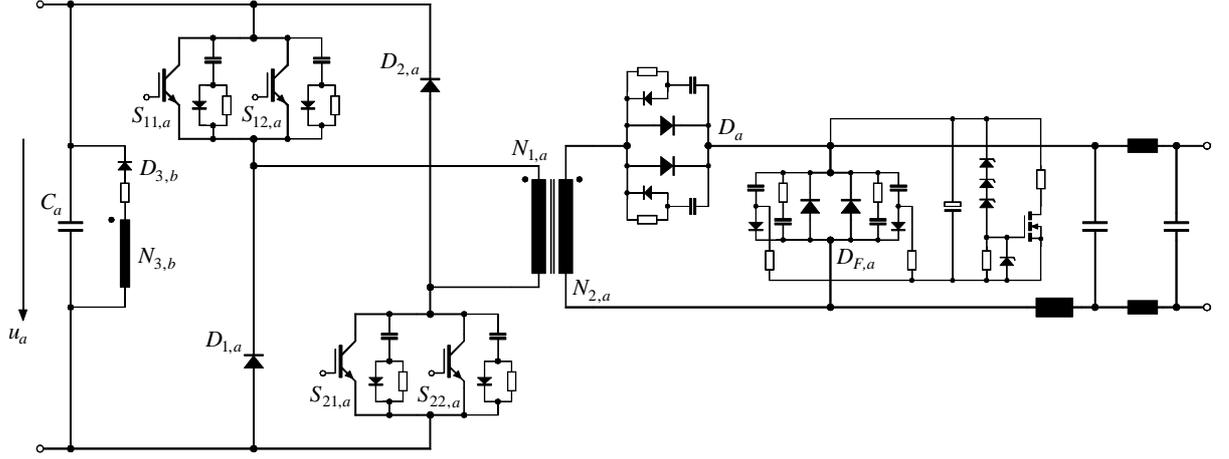


Fig.4: Detailed structure of the power circuit of the partial converter a comprising the parallel arrangement of switches $S_{11,a}$ and $S_{12,a}$ and/or $S_{21,a}$ and $S_{22,a}$ with associated RCD-snubber circuits. The secondary side rectifier diodes D_a are also equipped with RCD-snubbers, the blocking voltage of the freewheeling diodes $D_{F,a}$ is clamped by means of a Zener-type circuit. On the input the balancing winding $N_{3,b}$ corresponding to converter b is shown.

modulation indices of both units, a reduction of the total capacitor current stress of typically 50% can be achieved. A more detailed analysis of the optimum phase displacement of the partial systems and of the residual capacitor current stress will be given in a future publication.

4 Dimensioning of the Power Circuit

The converter power losses are calculated for a partial converter. This means that the input voltage is 400V, the output power is $P_{O,i} = 5\text{kW}$; only the output inductor being common to both partial systems is calculated based on the total output power of 10kW.

4.1 Transformer

The transformers are realized using two core sets of type E70 each. The switching frequency is $f_p = 25\text{kHz}$; the duty cycle has to be limited to $d_{max} < 0.5$. In order to provide a safety margin the maximum duty cycle is set to $d_{max} = 0.45$. The saturation limit of the ferrite material N67 (SIEMENS) used is about $B_{sat} = 380\text{mT}$ @ 100°C . So a maximum magnetic induction of $B_{max} = 300\text{mT}$ can be chosen. Based on these assumptions one gets a resistance of the transformer primary winding of $R_{N1} = 17\text{m}\Omega$ in case of using high frequency litz wire. The DC resistance of a foil-type winding would be lower but experiments have shown disadvantages of this solution concerning the HF losses due to skin and proximity effect. The maximum primary rms current is $I_{N1,rms} = 21.5\text{A}$, with the assumption of an increase of the winding temperature of $\Delta T = 75^\circ\text{C}$ the primary-side copper losses amount to:

$$P_{v,N1} = I_{N1,rms}^2 \cdot R_{N1} \cdot (1 + \alpha \cdot \Delta T) = 10.4 \text{ W.} \quad (8)$$

The power loss of the secondary winding is obtained taking into account a resistance $R_{N2} = 488\mu\Omega$ and a current of $I_{N2,rms} = 129\text{A}$:

$$P_{v,N2} = I_{N2,rms}^2 \cdot R_{N2} \cdot (1 + \alpha \cdot \Delta T) = 9.9 \text{ W.} \quad (9)$$

The core loss density at $B_{pk} = B_{max}/2 = 150\text{mT}$ and 25kHz using ferrite material N67 amounts to $p_{v,Fe} \gg 50\text{kW/m}^3$, with a core-volume of $2 \cdot 102000\text{mm}^3$ this results in core losses of $P_{v,T,Fe} = 10.2\text{W}$. In summary the total losses of one transformer add up to:

$$P_{v,T} = 30.5 \text{ W.} \quad (10)$$

4.2 Output Inductor

Considering the phase-shifted operation of the partial converters and/or the corresponding doubling of the effective frequency and duty cycle of voltage u_2 (as compared to a partial convert output) and with the assumption of a peak-to-peak ripple current $\Delta i_{L,p-p} = 0.1I_O = 20.8\text{A}$ the required inductance of the output inductor is $L = 10.7\mu\text{H}$. Choosing an Allied Signal Powerlite Metglass Alloy SA1 C-Core AMCC 20 with an air-gap of 2mm results in a winding resistance of $R_L = 476\mu\Omega$ and/or in a copper loss of:

$$P_{v,L,Cu} = I_{O,rms}^2 \cdot R_L \cdot (1 + \alpha \cdot \Delta T) = 27.2 \text{ W.} \quad (11)$$

The core loss density at $B_{pk} = 52\text{mT}$ and 50kHz for Allied Signal powerlite metglass material amount to $p_{v,Fe} \gg 15\text{W/kg}$, considering the weight the magnetic core of 0.35kg this results in core losses of $P_{v,L,Fe} = 5.3\text{W}$. The total output inductor losses therefore amount to:

$$P_{v,L} = 32.5 \text{ W.} \quad (12)$$

4.3 Power Transistors

The power transistors are realized using 600V Warp-Speed IGBTs IRG4PC50W (International Rectifier). Overheating of the switches S_1 and S_2 is avoided by employing a parallel arrangement of two IGBTs for each switch and by operating the individual IGBTs alternatively [10] (halving of the conduction and switching losses for the individual device). The conduction losses of one converter leg amount to:

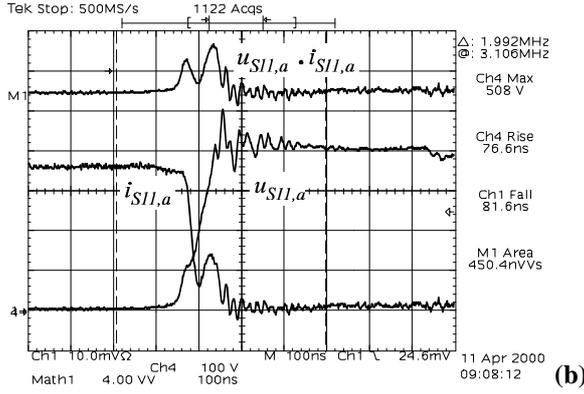
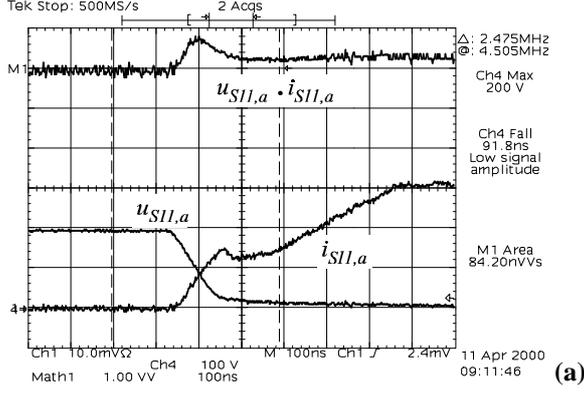


Fig5: Switching behavior of the switch $S_{11,a}$; (a): turn-on behavior, (b): turn-off behavior; IGBT current $i_{S_{11,a}}$ (5A/div), IGBT voltage $u_{S_{11,a}}$ (100V/div) and product $u_{S_{11,a}} \cdot i_{S_{11,a}}$ (2kW/div) which can be used for estimating the switching losses (there, the time-delay of current probe has to be considered).

$$P_{v,S,c} = I_{S,avg} \cdot U_{CE,sat} = 23.9 \text{ W.} \quad (13)$$

Due to the stray-inductance of the transformer in principal no turn-on losses of the IGBTs do occur; therefore, the switching losses are mainly due to turn-off (the turn-on loss due to the RCD snubbers is considered in section 4.6). With a measured turn-off energy of $E_{off} = 0.225\text{mJ}$ (Fig.5 (b)) at half the nominal load ($I_C = 18\text{A}$, junction temperature $\approx 50^\circ\text{C}$) the switching losses for one leg result at full load to:

$$P_{v,S,s} = \frac{I_{S,off}}{I_{CE}} \cdot E_{off} \cdot f_P = 10.9 \text{ W.} \quad (14)$$

Consequently, the total IGBT losses per converter are:

$$P_{v,S} = 2 \cdot (P_{v,S,c} + P_{v,S,s}) = 69.6 \text{ W.} \quad (15)$$

4.4 Output Diodes

The output diodes are of type Motorola *MURP20020CT*. The losses of one converter result with a forward voltage drop of $U_D = 0.9\text{V}$ and an average forward current of $I_{D,avg} = 104\text{A}$ to:

$$P_{v,D} = U_D \cdot I_{D,avg} = 93.6 \text{ W.} \quad (16)$$

4.5 Auxiliary Power Supply

The auxiliary power supply provided for supplying the control board, the IGBT gate drives and the fans is realized by two flyback converters connected to the partial input voltages (primary side series connection, secondary side parallel connection). One converter acts as master converter and is controlled for getting a constant value of output voltage; the second converter is controlled with equal duty cycle in order not to cause an unbalance of the partial input voltages. The total power consumption of the auxiliary supply is:

$$P_{v,H} = 20 \text{ W.} \quad (17)$$

4.6 Snubbers

For each of the IGBTs a RCD snubber with $C_{S,S} = 2.2\text{nF}$ is provided (cf. Fig.4, [11,12]), which results with a switching frequency $f_P = 25\text{kHz}$ and a turn-on voltage of $U_{S,on} = 200\text{V}$ (see Fig.5 (a)) in a power loss:

$$P_{v,S,on} = 4 \cdot \frac{C_{S,S} \cdot U_{S,on}^2}{2} \cdot f_P = 4.4 \text{ W.} \quad (18)$$

Also, a RCD-snubber is connected in parallel to each rectifier diode D_i ($i = a, b$); with $C_{S,Di} = 4.7\text{nF}$ and $f_P = 25\text{kHz}$ and a turn-on voltage of $U_{Di,on} = 130\text{V}$ the resulting power loss is:

$$P_{v,Di,on} = 2 \cdot \frac{C_{S,Di} \cdot U_{Di,on}^2}{2} \cdot f_P = 2.0 \text{ W.} \quad (19)$$

The snubber of the free-wheeling diodes $D_{F,i}$ is realized by a Zener-clamp-type circuit (cf. 4) in order to handle the overshoot occurring for discontinuous output inductor current mode (cf. Fig.16). The snubber power loss is assumed to be comparable with the loss of the snubbers of the rectifier diodes, i.e.:

$$P_{v,D,on} = 2.0 \text{ W.} \quad (20)$$

4.7 Loss Distribution, Efficiency

The distribution of the total converter power loss to the different components is shown in Fig.6. Based on this diagram the efficiency of the DC/DC converter system results in:

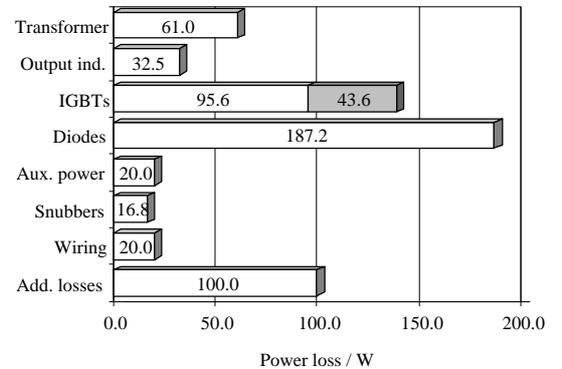


Fig.6: Loss distribution, all main loss contributions of components of the DC/DC converter system are shown, the losses of the IGBTs are divided into conduction and switching losses.

$$\eta = \frac{1}{1 + P_{v,tot}/P_O} = 94.5\% \quad (21)$$

The measured individual efficiencies of the DC/DC converter and of the VIENNA Rectifier and the overall efficiency are shown in **Fig.7**. The maximum overall efficiency is achieved at about half the nominal load. The efficiency of the DC/DC converter decreases more than expected at full load, this could be due to the over-proportional increase of the copper losses which occurs due to under-dimensioning of the secondary side wiring and the output inductor winding.

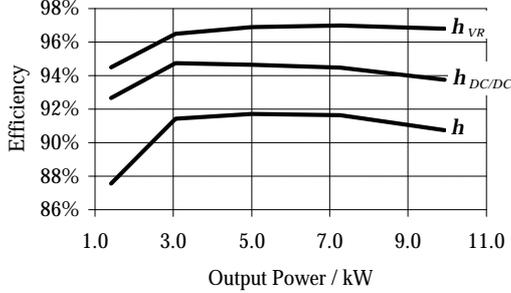


Fig.7: Measured overall efficiency h of the power supply module, and individual efficiencies of the VIENNA Rectifier h_{VR} and of the DC/DC converter $h_{DC/DC}$ for a load range of 1.5...10kW.

4.8 Discussion

In section 4.1 the switching frequency has been set to $f_p=25\text{kHz}$. This leads to relatively large volume of the transformers (2 core sets and/or 4 cores E70 per transformer) and a larger output inductor as compared to higher switching frequencies. Doubling the switching frequency would allow to have a transformer employing 4 cores E65, under the assumption of equal core loss density ($p_{v,Fe} = 50\text{kW/m}^3$). As listed in **Tab.2** this would lead to lower core losses (-23%) due to the lower core volume, but would not significantly lower the copper losses (the winding resistance could be reduced by only 5%).

Switching frequency f_p	25kHz	50kHz
Core type	4 x E70	4 x E65
Volume	0.56dm ³	0.42dm ³
Weight	1.2kg	1.0kg
Core loss	10.2W	7.8W
Copper loss	20.3W	19.3W

Tab.2: Comparison of the characteristics of the transformer of a partial system for switching frequency $f_p=25\text{kHz}$ and $f_p=50\text{kHz}$.

The main drawback of increasing the switching frequency is that also the IGBT switching losses, the snubber losses and the gate drive losses increase linearly. This means that for selecting $f_p=50\text{kHz}$ one would have to increase the size of the heatsink by about 13% (+0.33dm³) and would have to accept a decrease of the efficiency of $\approx 0.5\%$.

5 Experimental Analysis

The measurements were done using an industrial realization of a VIENNA Rectifier in connection with a prototype of the

DC/DC-converter at half the rated output current. The operational conditions for the analysis of the system operating in continuous output inductor current mode (CCM) are given in **Tab.3**; **Tab.4** details the operational conditions for the investigation of the system behavior for discontinuous output inductor current (DCM).

5.1 Continuous Output Inductor Current

The operational conditions are given in **Tab.3**.

Input voltage: $U_I = 460\text{V}$	Output voltage: $U_O = 47.9\text{V}$
Input current: $I_I = 6.6\text{A}$	Output current: $I_O = 102\text{A}$
Input power: $P_I = 5.3\text{kW}$	Output power: $P_O = 4.9\text{kW}$
Power factor: $\lambda = 0.998$	Efficiency: $h = 91.7\%$

Tab.3: Operational conditions for the analysis of the CCM.

Figure 8 clearly shows the basic principle of operation of the DC/DC converter by depicting the primary side transformer voltages $u_{NI,i}$ ($i=a, b$) and currents $i_{NI,i}$ which are shifted by 180° in phase. Due to manufacturing inaccuracies the magnetization inductance is lower for transformer T_a than for

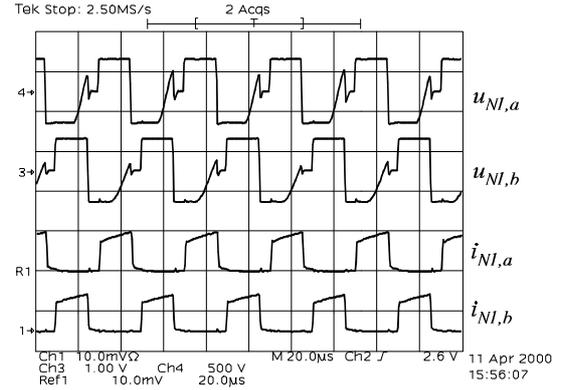


Fig.8: Time behavior of transformer primary voltage $u_{NI,i}$ (250V/div) and transformer primary current $i_{NI,i}$ (20A/div) of the partial converters $i=a, b$.

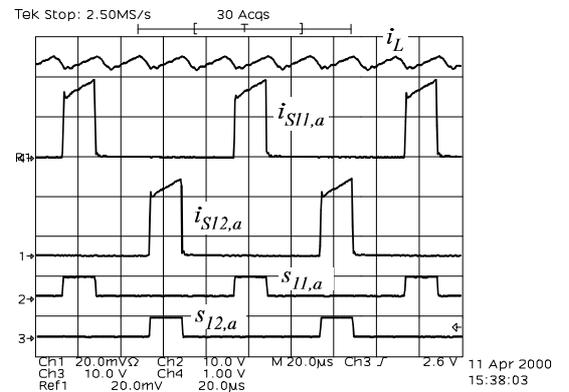


Fig.9: Output inductor current i_L (40A/div), IGBT currents $i_{S11,a}$ and $i_{S12,a}$ (10A/div) and corresponding drive signals $s_{11,a}$ and $s_{12,a}$ (10V/div).

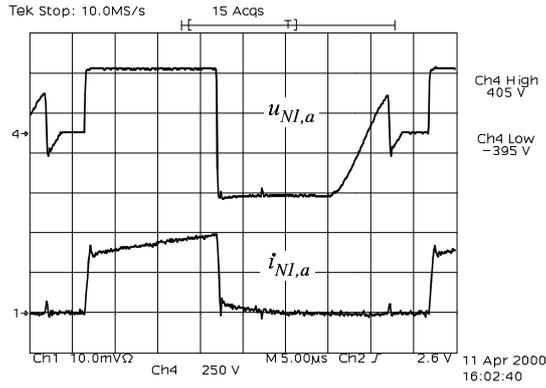


Fig.10: Transformer primary voltage $u_{N1,a}$ (250V/div) and transformer primary current $i_{N1,a}$ (10A/div) for a partial converter operating in CCM.

transformer T_b . Accordingly, the resonant frequencies and the voltage peak values occurring immediately before a free-wheeling diode starts conduction are different for T_a and T_b .

Figure 9 shows the alternate switching of the parallel connected IGBTs $S_{11,a}$ and $S_{12,a}$. This mode of operation distributes the conduction and switching losses equally to the individual devices and guarantees a low junction temperature (60°C housing temperature at full load, heatsink temperature: 42°C). In Fig.9 also the output inductor current i_L is shown in order to demonstrate the relation between IGBT switching frequency and output inductor current ripple frequency.

Figure 10 demonstrates the conditions of transformer T_a in greater detail. First, the primary winding $N_{1,a}$ is connected to the partial input voltage u_{Ca} via the switches $S_{1,a}$ and $S_{2,a}$ for $t_{on} = dt_P \approx 15\mu s$. After turn-off of the switches the transformer core demagnetization is via the diodes $D_{1,a}$ and $D_{2,a}$. The magnetizing current can also be seen in Fig.10. At the end of the demagnetization interval the transformer windings start to oscillate with a resonant frequency determined by the main inductance of the transformer (and the transformer stray inductance and wiring inductances) and the parasitic capacitances of the transformer, the power transistors and the primary and secondary side snubber capacitors. This oscillation is interrupted at the end of the conduction interval

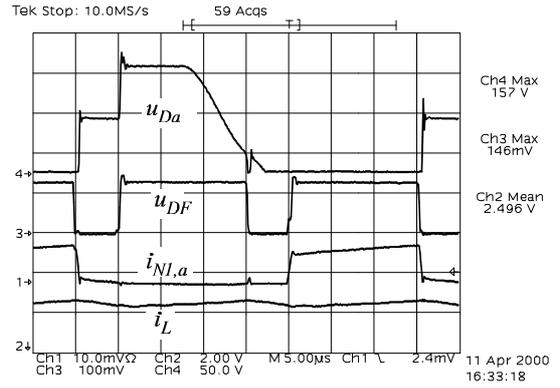


Fig.12: Secondary side rectifier diode voltage u_{Da} (50V/div), free-wheeling diode voltage u_{DF} (50V/div), transformer primary current $i_{N1,a}$ (20A/div) and inductor current i_L (80A/div).

of the second partial converter b where the free-wheeling diode is forced into conduction (cf. **Fig.11**) and then continues until the secondary side diode snubber capacitors are fully discharged and the primary side IGBT snubber capacitors are charged to half the partial input voltage each. It is advantageous in terms of turn-on or snubber-losses to allow the transformer voltage to recover to zero before the beginning of the subsequent conduction interval (by proper selection of the snubber capacitances) because in this case the turn-on voltage of each switch is only half the partial input voltage (200V).

The inverse voltage is applied on the rectifier diode in two steps (cf. **Fig.12**). The first voltage step occurs at the end of the conduction interval of converter a , i.e., when $S_{1,a}$ and $S_{2,a}$ are turned off and the demagnetization of transformer T_a starts; the second voltage step occurs at the beginning of the conduction state of the second partial converter b , i.e., when $S_{1,b}$ and $S_{2,b}$ are turned on. The advantage of applying the inverse voltage in two steps as compared to immediately applying the full inverse voltage in a single step is the slower decrease of the rectifier forward current which reduces the diode reverse recovery current.

5.2 Discontinuous Output Inductor Current

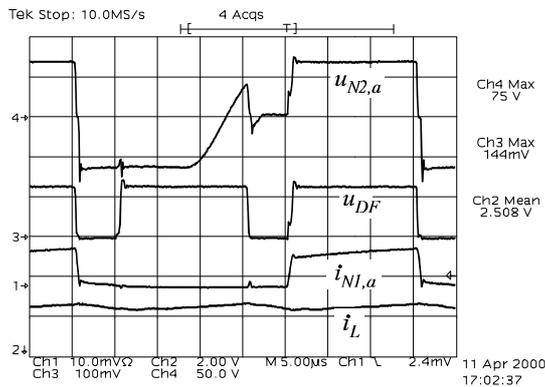


Fig.11: Transformer secondary voltage $u_{N2,a}$ (50V/div), free-wheeling diode voltage u_{DF} (50V/div), transformer primary current $i_{N1,a}$ (20A/div) and inductor current i_L (80A/div) for a partial converter operating in CCM.

Output voltage:	$U_O = 48.1V$
Output current:	$I_O = 5A$
Output power:	$P_O = 240W$

Tab.4: Operational conditions for the analysis of the DCM.

Figure 13 demonstrates the system behavior for discontinuous output inductor current (the inductor current reaches $i_L = 0$ at the cursor position). The duty cycle has been reduced to $d \gg 0.3$. Due to the lower load current the magnetizing current of the transformer can be recognized more clearly as compared to Fig.10. When the inductor current i_L reaches zero an oscillation between the parasitic capacitors, the primary IGBT snubbers and secondary diode snubbers and the output inductor is initiated (cf. **Fig.14** and **Fig.15**). Due to this oscillation a voltage showing an amplitude of about twice the maximum output voltage (in the case at hand $2 * 56V = 112V$) would occur across the free-wheeling diode

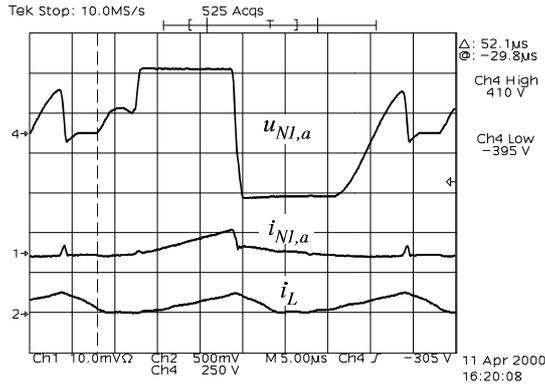


Fig.13: Transformer primary voltage $u_{N1,a}$ (250V/div), transformer primary current $i_{N1,a}$ (5A/div) and inductor current i_L (20A/div) for a partial converter operating in DCM.

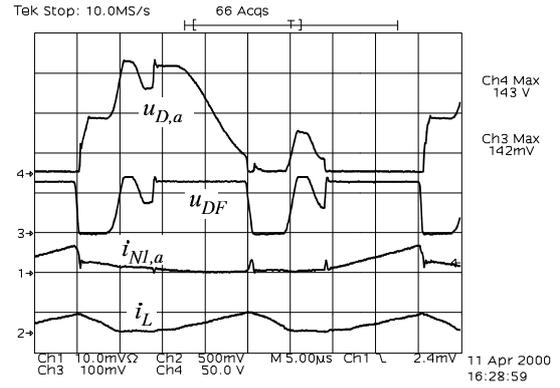


Fig.15: Secondary side rectifier diode voltage $u_{D,a}$ (50V/div), free-wheeling diode voltage u_{DF} (50V/div), transformer primary current $i_{N1,a}$ (5A/div) and inductor current i_L (20A/div) for DCM.

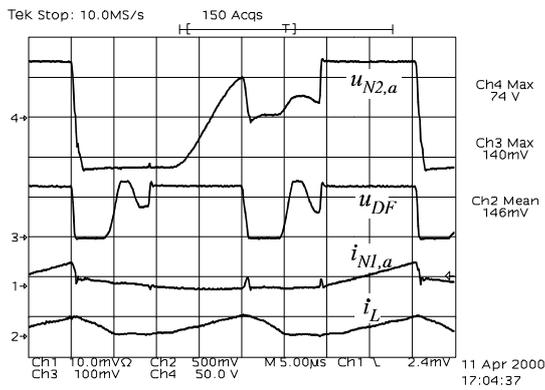


Fig.14: Transformer secondary voltage $u_{N2,a}$ (50V/div), free-wheeling diode voltage u_{DF} (50V/div), transformer primary current $i_{N1,a}$ (5A/div) and output inductor current i_L (20A/div) for a partial converter operating in DCM.

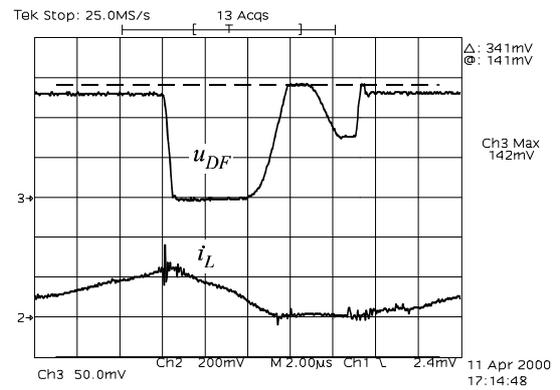


Fig.16: Detail of the time behavior of the free-wheeling diode voltage u_{DF} (50V/div) and inductor current i_L (20A/div) for DCM (compare Fig.15).

$D_{F,i}$. This oscillation is clamped with a Zener-type circuit (cf. Fig.16) which is set to $u_z \approx 70V$ what in principle would allow to employ a 100V Schottky-diode as free-wheeling diode. Furthermore, the clamp circuit reduces the maximum voltage stress on the rectifier diodes D_i ($i=a,b$) which also would be higher for DCM than for CCM.

5.3 Realization, Performance Data

Photos of the experimental system are shown in Fig.17. The converter volume is $V = 240 \times 320 \times 170 \text{mm}^3 = 13 \text{dm}^3$ (length x width x height), the weight is $m = 12 \text{kg}$. This translates into a power-density of $r_V = 760 \text{W/dm}^3 = 13 \text{W/in}^3$ and a power-weight of $r_P = 830 \text{W/kg}$.

6 Conclusions

As shown in this paper for a 10kW DC/DC output stage of a telecommunications power supply module one can achieve a high efficiency of the energy conversion and a high power density and low weight

$$\begin{aligned} \eta &\approx 0.94 \text{ (at rated power)} \\ \rho_P &= 830 \text{W/kg} \\ \rho_V &= 760 \text{W/dm}^3 \approx 13 \text{W/in}^3 \end{aligned}$$

also for

- omission of non-dissipative turn-off snubbers [13] of the power transistors (application of RCD-snubbers instead of soft-switching or quasi-resonant operation) and
- unidirectional transformer magnetization (and/or avoidance of special measures for ensuring a symmetric transformer magnetization as required, e.g., for bridge-type circuits)

by proper combination of partial converter systems of simple structure. The application of converter topologies of higher complexity which possibly could show a slightly higher efficiency or power density therefore in general seems not to be justifiable, especially if the resulting reduction of the system reliability is taken into account.

In the course of a further development of the proposed system in a first step the power transistors and primary side diodes shall be replaced by devices in a novel isolated package (IXYS ISOPLUS247™, [14]). Besides a reduction of the effort for assembling the system as compared to non-isolated devices with external isolation foils this will provide a reduction of the thermal resistance of the power semicon-



Fig.17: Photos of the industrial realization of the DC/DC converter system, top view (left), bottom view (right).

ductors by a factor of 2.8 (cf. p. 13 in [14]). Therefore, for equal junction temperature the thermal resistance of the heatsink can be reduced and/or the power density of the converter will be increased considerably.

Furthermore, the conducted and radiated EMI emissions of the converter shall be minimized by proper placement of the power components and by inserting Faraday shields between the transformer primary and secondary windings [15].

In a second step a realization of the proposed system and/or of the system shown in Fig.2(b) with only a single transformer (cf. **Fig.18**) shall be analyzed. The resulting system structure could be considered as a full bridge circuit where one bridge leg (transistors $S_{1,a}$, $S_{2,a}$) is connected to the upper and the second bridge leg (transistors $S_{1,b}$, $S_{2,b}$) is connected to the lower partial input voltage. As compared to employing individual transformers in each partial system there the wiring and assembling effort can be reduced (single secondary winding, only two output diodes) and a higher utilization of the magnetic material can be achieved due to the bidirectional magnetization of the transformer magnetic core. Disadvantages consist in the direct coupling of both partial systems and the possibility of a transformer saturation.

Furthermore, in order to keep the construction of the transformer as simple as possible and for achieving a high utilization of the secondary winding the secondary circuit shall be realized by a current doubler rectifier [16]. The topology of this rectifier can be thought to be derived by modification of the topology of the secondary circuit of the system shown in Fig.2(b) (cf. Figs.18(b), (c)) and requires only a single secondary winding which participates in the conduction of $i_o/2$ for positive and negative magnetization of the transformer (within $2dT_p$) and therefore shows a higher utilization as compared to the partial secondary windings $N_{2,a}$ and $N_{2,b}$ of the circuit according to Fig.18(c) (conduction of $i_o/2$ in dt_p , respectively). Concerning the output inductors L_a and L_b and the current stresses on the diodes the circuits according to Fig.18(b) and (c) do not show a difference (e.g., diode D_+ can be thought to be realized by a parallel connection of the diodes D_a and $D_{F,a}$). Therefore, only a marginal improvement of the efficiency as compared to the system discussed in this paper can be expected. Therefore,

the resulting increase of the power density and reduction of the converter weight will be of special interest.

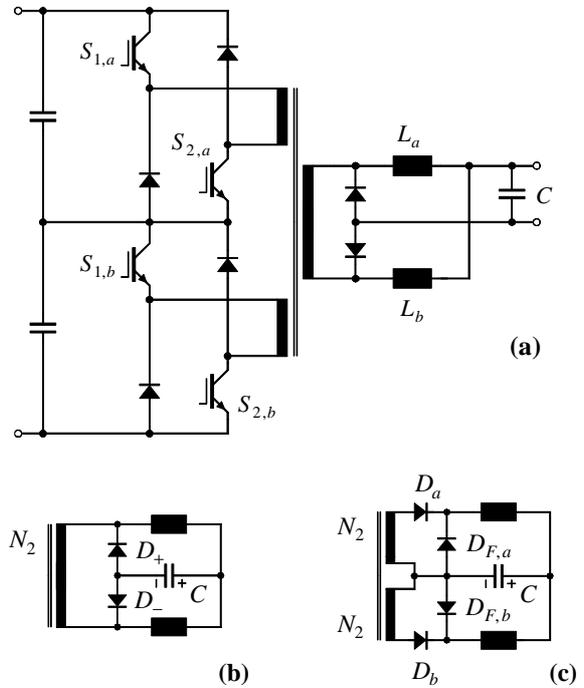


Fig.18: Basic structure of the DC/DC converter power circuit comprising only a single transformer for both partial systems and realization of the secondary circuit by a current doubler rectifier (cf. (a)); (b) and (c): comparison of the realization effort of the secondary circuit of the circuit shown in Fig.2(b) with a current doubler rectifier.

ACKNOWLEDGMENT

The authors are very much indebted to the *Hochschuljubiläumsstiftung der Stadt Wien* which generously supports the research of the Power Electronics Group of the Department of Electrical Drives and Machines at the Technical University Vienna.

References

- [1] **Kolar, J.W., and Zach, F.C.:** *A Novel Three-Phase Utility Interface Minimizing Line Current Harmonics of High-Power Telecommunications Rectifier Modules.* Proceedings of the 16th IEEE International Telecommunications Energy Conference, Vancouver, Canada, Oct. 30 – Nov. 3, pp. 367 – 374 (1994).
- [2] **Miller, M., Buffin, A., and Carlsson, U.:** *High Frequency ZVS for High Power Rectifiers.* Proceedings of the 15th IEEE International Telecommunications Energy Conference, Paris, Sept. 27–30, Vol.1, pp. 424 – 430 (1993).
- [3] **Vescovi, T.F., Vun, N.C.H.:** *A Switched-Mode 200A 48V Rectifier/Battery Charger for Telecommunications Applications.* Proceedings of the 12th IEEE International Telecommunications Energy Conference, Orlando, Oct. 21 – 25, pp. 112 – 118 (1990).
- [4] **Feng, H., Xu, D., and Lee, Y.S.:** *Comparison of Interleaving Methods of Two-Transistor Forward Converters.* Proceedings of the IEEE International Conference on Power Electronics and Drive Systems, Hong Kong, July 27 – 29, Vol.2, pp. 632 – 637 (1999).
- [5] **Zhang, M.T., Jovanovic, M.M., and Lee, F.C.:** *Analysis and Evaluation of Interleaving Techniques in Forward Converters.* IEEE Transactions on Power Electronics, Vol. 13, No.4, pp. 690 – 698 (1998).
- [6] **Nagai, Y., Tomokuni, Y., and Hirachi, K.:** *A 48V 100A Switching Power Supply Unit and its Application.* Proceedings of the 10th IEEE International Telecommunications Energy Conference, San Diego, Oct. 30 – Nov. 2, pp. 421 – 428 (1988).
- [7] **Redl, R., and Sokal, N.O.:** *How to Use Current-Mode Control with Capacitively Coupled Half Bridge Converters.* Proceedings of the 2nd IEEE Applied Power Electronics Conference, San Diego, March 2 – 6, pp. 257 – 265 (1987).
- [8] **Nagai, Y., Tomokuni, Y., and Hirachi, K.:** *A 48V 50A Switching Regulator Unit.* Proceedings of the 8th IEEE International Telecommunications Energy Conference, Toronto, Oct. 19 – 22, pp. 101 – 107 (1986).
- [9] **Kolar, J.W., and Miniböck, J.:** *Verfahren und Vorrichtung zur Stabilisierung und Verlustminimierung einer an den Ausgangsteilspannungen eines Dreipunkt Pulsleichrichtersystems liegenden Serienschaltung von Gleichspannungs-Gleichspannungswandlern.* Austrian Patent Application A25/2000, filed: Jan. 10, 2000.
- [10] **Kolar, J.W., and Miniböck, J.:** *Verfahren zum Parallelbetrieb elektronischer Leistungsschalter mit negativem Temperaturkoeffizient der Durchlaßspannung oder hoher Toleranz der Schaltschwellspannung.* Austrian Patent Application A1396/99, filed: Aug. 13, 1999.
- [11] **Kolar, J.W., Erhardt, L.L., and Zach, F.C.:** *Analysis of Turn-Off Behavior and Switching Losses of a 1200V/50A Zero-Voltage or Zero-Current Switched IGBT.* Proceedings of the 26th IEEE Industry Applications Society Annual Meeting, Dearborn, USA, Sept. 28 – Oct. 4, Vol. II, pp. 1508 – 1514 (1991).
- [12] **Torvetjonn, G.J., Undeland, T.M., Schmidt, O.R., and Bryde, J.H.:** *A DC-DC Converter Topology with Phase Shift Control and Lossless Snubbers for Use in a 200A Battery Charger Working on 400V Mains.* Proceedings of the 7th IEEE International Telecommunications Energy Conference, The Hague, The Netherlands, Oct. 29 – Nov. 1, pp. 489 – 495 (1995).
- [13] **Kim, E.S., Joe, K.Y., Byun, Y.B., and Kim, Y.H.:** *An Improved Soft Switching Forward DC/DC Converter Using Energy Recovery Snubber.* Proceedings of the 19th IEEE International Telecommunications Energy Conference, Melbourne, Australia, Oct. 19 – 23, pp. 46 – 49 (1997).
- [14] **IXYS Semiconductor GmbH:** *Semiconductors 2000/2001*, Databook, Publication D2000E, 01/2000.
- [15] **Knurek, D.F.:** *Reducing EMI in Switch Mode Power Supplies.* Proceedings of the 10th IEEE International Telecommunications Energy Conference, San Diego, Oct. 30 – Nov. 2, pp. 411 – 420 (1988).
- [16] **Kutkut, N.H.:** *A Full Bridge Soft Switched Telecom Power Supply with a Current Doubler Rectifier.* Proceedings of the 19th IEEE International Telecommunications Energy Conference, Melbourne, Australia, Oct. 19 – 23, pp. 344 – 351 (1997).