

High-performance rectifier system with 99.2% efficiency

Using a suitable operating mode, it is possible to build a converter system of the highest efficiency without SiC power components. This article unveils the main results of a research project.

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The development of power-electronic converters is marked by demands for a simultaneous reduction in size, losses and power-related costs. For example, in the field of telecommunication power supplies, an efficiency of 97% (for 230 V_{rms} mains power) at a power density of 2.5 to 3 kW/dm³ is typically expected today for conversion of the single-phase mains power to a galvanically isolated direct current (feeding of the 48 V rail) at a nominal power of 50%. Assuming that the power density and efficiency of the rectifier and DC/DC converter stages are identical, it is therefore necessary to achieve an efficiency of 98.5% per subsystem at a power density of 5 kW/dm³. A further demand is a flat efficiency curve over the power range, i.e. high partial load efficiency.

For any next-generation product, therefore, it is necessary to answer the questions of what objective is suitable and can be achieved with existing technologies and of what compromise is to be reached regarding the other variable when maximising one of the performance parameters. In any event it is only possible to improve an existing design while retaining the technology if the existing solution has not yet been optimised to the full or has not yet reached the frontier of performance (Pareto front).

Based on these considerations, concepts for single-phase rectifier circuits with sinusoidal current consumption were analysed with respect to the maximum efficiency attainable in a research project of the European Center for Power Electronics (ECPE, www.ecpe.org) conducted at the ETH Zurich (www.pes.ee.ethz.ch).

A rectifier topology without input diode bridge

The main results of this report are summarised briefly below using a high-efficiency rectifier system as example. They clearly show the de factor limit of loss reduction that exists today and the power density that can still be reached with it. In view of applications in the field of IT power supplies and the increasingly important battery charges of electric motor vehicles, the nominal power of the system was defined at $P = 3.3$ kW with a power density of at least $p > 1$ kW/dm³.

Considering the demand for extreme efficiency, it seems obvious to use a rectifier topology without input diode bridge, i.e. a bridgeless or double-boost PFC rectifier concept. In the concrete case two phase-offset subsystems with SiC superjunction MOSFETs (CoolMOSTM C6) and SiC free-wheeling diodes were used and operated in continuous conduction mode (CCM) to achieve a high partial load efficiency. The common-mode component of the output voltage characteristic for the bridgeless concept was mainly suppressed by internal capacitive connection of the output terminals to the AC side and insertion of a common-mode inductor in this inner loop. To achieve the required level of efficiency, a relatively low switching frequency of $f = 33$ kHz was also implemented as was double line-frequency switching frequency modulation with 6 kHz deviation to spread and lower the EMI spectrum.

The nominal load efficiency achieved in this way at nominal voltage is 99.1% (including all auxiliary power supplies). Although increasing the number of parallel MOSFETs and diodes would result in a reduction in the conduction losses, the capacitive switching losses would rise at the same time (the efficiency value named above is valid for an optimal number of components). If the capacitive switching losses are to remain unchanged in spite of a higher number of components, the switching frequency would have to be lowered, which would, however, lead to a larger size of the boost inductors and thus to a reduction in the already low power density of 1.1 kW/dm³.

Fewer losses from a different circuit concept

It is therefore only possible to reduce the losses while retaining the same power density by changing the circuit concept. To reduce the conduction loss part of the diodes in the loss balance, it seems obvious here to use MOSFETs instead of diodes, i.e. synchronous rectification. However, due to the relatively high reverse recovery time of the internal diodes in the MOSFETs and the – for small drain source voltages – high parasitic output capacitance of the synchronous rectifier MOSFETs on being re-energised, i.e. on receiving the current from the free-wheeling diodes (CCM), high reverse currents and thus high switching losses arise. These losses can be avoided by changing the operating mode to boundary conduction mode (BCM). In this case the current becomes zero at the end of the free-wheeling interval and the voltage then oscillates by the line voltage at the point the inductivity is connected from the positive output voltage rail. For line voltages up to half the output voltage, the negative output voltage rail is then reached, thereby enabling zero voltage switching (ZVS).

Capacitive switching losses would, however, arise again for higher instantaneous line voltage values. This can be reduced with a minor modification of the controller. A synchronous rectifier MOSFET is then kept in on-state at the end of the free-wheeling phase until a sufficiently high negative current value is reached. When it is switched off, it ensures a complete reversal in the voltage through the negative current of the inductor. Switching losses are therefore (ideally) avoided completely.

Triangular current pattern with few negative parts

It is therefore possible, in contrast to CCM mode, to reduce the conduction losses by increasing the components operated in parallel. The current flowing into the inductor then has a virtually triangular form with few negative parts and therefore the operating mode can then no longer be called BCM, but rather, for example, triangular current mode (TCM) or resonant transition mode. As in the case of BCM, there is also a switching frequency here that varies over the mains period, whereby, however, a constant switching frequency could be set by an appropriate choice of the duration of the interval with negative current (while simultaneously adjusting the duration of the current build-up phases).

In order to achieve a relatively smooth input and output current flow or relatively low current loading of the input and output capacitances already without EMI filtering, it is advantageous to operate n phase-offset switching stages in parallel. The circuit used in the case under review is shown in figures 1 and 2. Here the input voltage is rectified by a second bridge arm clocking only at line frequency. Six switching stages were chosen because of the then favourable current load on the MOSFETs (single switches), the generally compact converter build due to appropriate magnet core shapes and the easily realisable partial load efficiency.



Figure 1: Demonstrator of the ultra-efficient 3.3 kW single-phase PFC rectifier system

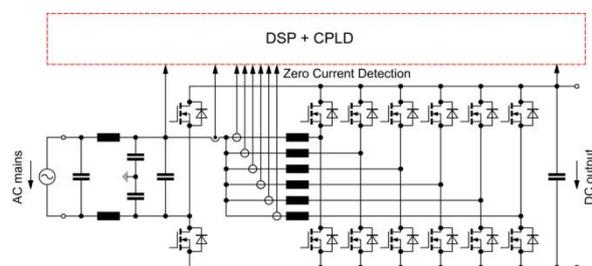


Figure 2: Basic circuitry of the power unit

Implementation of the concept with DSP and CPLD

Since the reaction time of a DSP to an external hardware interrupt signal is not defined exactly, the system is controlled by a CPLD. The duration of the individual stages of the triangular wave form are calculated by the DSP in dependence on the line and output voltage and the mean current value that is to be set (superimposed output voltage controller) and sent to the CPLD via the SPI interface. The control sequence of the switches is triggered by the digital output signal of a zero current instant detector (a saturable toroid magnet core (R6.3) that only leaves saturation and picks up current or induces a positive or negative voltage in a secondary winding, thereby switching a comparator, near the zero current instants, figure 3). Thanks to the CPLD, reaction within 40 ns is possible. The end of the individual time intervals (including the locking times of the switches of a bridge arm) is defined by a state machine that also monitors the maximum times.

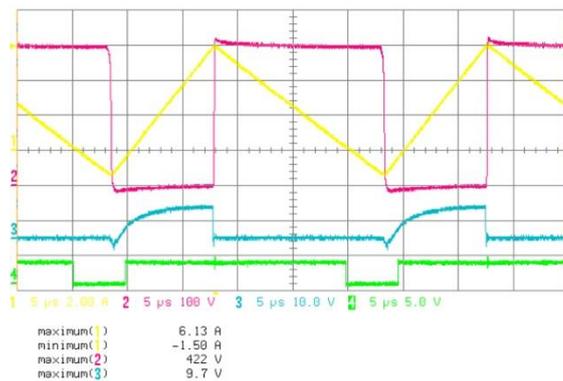


Figure 3: Progression of the input current of a cell, drain source voltage and gate source voltage of the assigned MOSFETs and output signal of the zero current instant

Due to the triangular wave shape of the current, the switching frequency varies over the mains period, resulting advantageously in a broad spread of the pulse-frequency harmonic power and thus in a low local level of power-related interference. In consideration of the core and winding losses, the mean switching frequency is kept relatively low and the maximum switching frequency limited to 100 kHz, which leads to currentless intervals or low current distortions near the zero voltage instants. The optimum phase shift of the arms in operation (arms are switched off in partial load) is set by a controller. For this the CPLD measures the duration of a switching period of the triangular current of a master phase and the edges of the zero current instant signals in the other phases related to reference time points defined by the active phase number. The time differences vis-à-vis the reference points are then control deviations for synchronisation control circuits, which change the switch-on times of the arms such that the differential times are adjusted to zero.

3.3 kW output power and only 20 W loss

As a loss analysis and efficiency measurement with a power analyser (Yokogawa WT3000, accuracy of the efficiency measurement 0.04%) shows, the system (power density 1.1 kW/dm³) has a nominal load efficiency of 99.23% at nominal voltage and an efficiency of 99.34% at the upper input voltage tolerance limit, meaning that the desired increase in efficiency over CCM mode while retaining the power density is achieved. Generally speaking, therefore, losses of only about 20 W occur at an output power of 3.3 kW! As far as the authors know, this is the highest efficiency measured so far for single-phase PFC rectifier circuits taking all auxiliary power supplies/loss shares into consideration. Due to the low losses, forced cooling can be dispensed with. The maximum increase in temperature over the environs after an operating time of one hour is only 23°C. Almost 50% of the losses can be attributed to the power MOSFETs and about 25% to the boost inductors, which are specially made from a core material (Ferroxcube 3C95) that minimises losses at a relatively low temperature. The losses of the output capacitors, implemented as film capacitors (polyester) instead of as electrolytic capacitors (leakage currents, equivalent series resistance) in the interests of loss minimisation, are

about 1.7 W (8%). A further 1.1 W can be attributed to the gate drives (5%, gate drive voltage 10 V), 1.5 W (7%) to the DSP and CPLD and about 2 W (10%) to the zero current instant detector and current measurement. By reducing the number of active arms, it is possible to keep the efficiency at values >99% up to an output power of 500 W.

According to the measurement of the line-based electromagnetic interference emissions, the interference level lies 6 dB under the limit value of CISPR 22/Class B at 150 kHz in spite of only a single-stage EMI filter (see figure 1) being used due to the relatively low mean switching frequency and the fact that this switching frequency varies greatly over the mains period. Due to the lack of steep switching edges, this interference level also has a monotonously falling characteristic as the frequency rises.

In summary, therefore, it can be said that it is possible to realise a converter system of the highest efficiency without SiC semiconductor power components by choosing a suitable operating mode. The significant features of the approach described here are the ideally switching-loss free resonant transition mode realised directly with the basic topology of the converter, i.e. without auxiliary networks, and the high number of phase-offset arms. Lossless switching is in the end enabled here by accepting discontinuous currents, which, however, due to the excellent conduction properties of superjunction MOSFETs, result in only minor conduction losses. Advantageously, the triangular current shape requires only low inductivity values, thereby supporting a small size. Thanks to the high number of arms, it is possible through appropriate synchronisation to achieve a largely smooth overall current in spite of the high single-current ripple. This mode of operation is only possible in simple form using digital control components (DSP, CPLD). The selected converter concept therefore achieves improved performance mainly by resorting to two dynamically developing technologies and by minimising components with slow development (e.g. magnet materials).

A further improvement in performance is therefore likely as the state of the art develops further (presented annually in comprehensive form by the exhibition and conference of PCIM Europe).

As can be seen directly from the basic topology of the converter, the PFC rectifier system shown also allows energy to be returned to the grid (e.g. for vehicle-to-grid applications). Without galvanic isolation of the load, however, it is necessary to take the line-frequency rectangular CM voltage caused by the polarity switching arm into consideration here.

Finally it must still be said that the other performance variables such as power density and realisation costs must also be considered when assessing the efficiency of a converter system. Only a combination of these variables imparts a complete picture of the "technology node" achieved by realisation. As a more detailed analysis shows, an efficiency/combined efficiency of 99.2%/1.1 kW/dm³ or alternatively of 98.5%/5 kW/dm³ is possible with the rectifier concept presented here. High efficiency can therefore only be attained with a reduction in power density (in the current case: halving of the losses by reducing the power density by a factor of 5). Or lower efficiency enables more compact construction until a thermal limit is reached, which, however, is relatively flexible thanks to forced cooling methods.

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