of autonomous, plug-and-play-type systems with minimal coordination in their power flow and energy management was foreseen.

The session concluded with a positive outlook of the ongoing changes that are currently transforming the grid and its capabilities. The attendees also acknowledged the multiple opportunities in new emerging regions to develop new power networks virtually from scratch, where the role of power electronics would be preponderant from the beginning.

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Power Electronics Design Methods and Automation in the Digital Era

Evolution of design automation tools

by Antonio J. Marques Cardoso

Last June at the 10th IEEE Future of Electronic Power Processing and Conversion (FEPPCON X) workshop, I chaired the session "Power Electronics Design Methods and Automation in the Era of Digitalization," which was held 26 June 2019 at Scandic Ishavshotel in Tromso, Norway. To foresee the evolution of design automation tools in the power systems arena, this session offered presentations from two distinguished speakers, Prof. Alan Mantooth from the University of Arkansas, Fayetteville, and Prof. Johann W. Kolar from ETH Zurich, Switzerland.

In his presentation "Power Electronics Design Methods and Automation in the Era of Digitalization," Prof. Mantooth

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initiated the session by anticipating the following potentially controversial conclusions:

- power electronics design is lacking in automation
- current approaches limit penetration
- Power Electronics Design 4.0 demands a change in the IEEE Power Electronics Society (PELS) composition.

Subsequently, Prof. Mantooth presented some evidence to support his initial claims: the multidisciplinary integrated design methodology (Figure 1) and the multidisciplinary hierarchical optimization design flowchart (Figure 2). These illustrations highlighted key bottlenecks limiting automation in power systems, such as the difficulties of combining system-level with component-level designs, the absence of industry interchangeable models, the lack of software standards, and the need for better algorithms and open source libraries.

Prof. Mantooth continued by stating that what limits penetration is not just nominal design, but robustness, resiliency, and reliability. Although certain applications with specific voltage/current/power specifications may first see the penetration of automated design tools, the key barrier to design automation seems to be the device data sheets, which are not a true representation of the device's performance. In reality, the current situation demands more automation, concluded Prof. Mantooth.

Prof. Mantooth continued by stating that what limits penetration is not just nominal design, but robustness, resiliency, and reliability.

Also, based on the road map to Power Electronics Design 4.0 (Figure 3), Prof. Mantooth questioned the current PELS composition to achieve the road map's demanding targets. He would like to see a PELS initiative, comprising the right folks, to drive this road map in the future.

Continuing, Prof. Mantooth presented the second Design Automation for Power Electronics workshop, which was held on 6 September 2019 at the same venue as that of the PELS-sponsored European Conference on Power Electronics and Applications at the Magazzini del Cotone Conference Center in Genova, Italy. The intent here was to understand the problems hindering the growth of design automation in power electronics and how best to address them. It brought together experts in both power electronics and design automation from the academia and industry, all of whom presented their perspectives on the emerging needs.

Finally, several illustrative examples taken from the Workshop on Wide Bandgap Power Devices and Applications Asia 2019 held in Taipei, Taiwan, regarding advances in silicon carbide power integrated circuits were presented and discussed, which included μ-cooled flip-chip modules and integrated CMOS gate drivers.

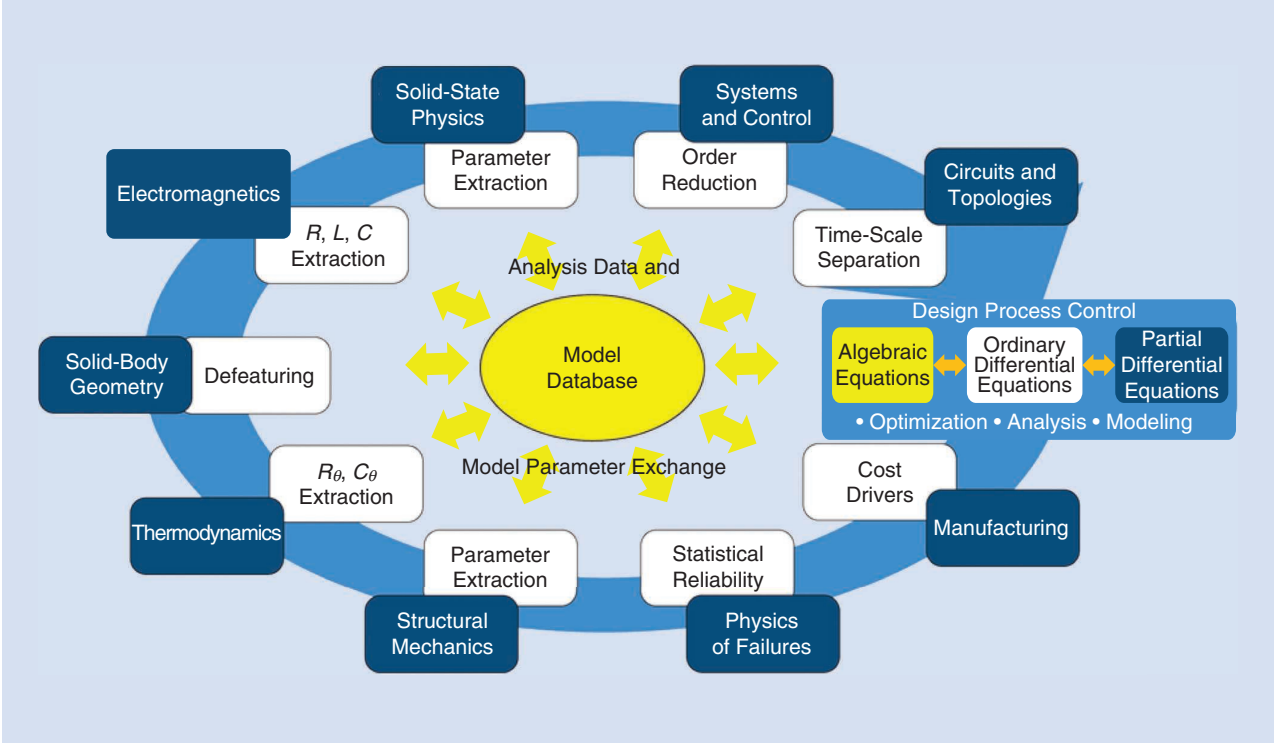

FIG 1 A multidisciplinary integrated design methodology.

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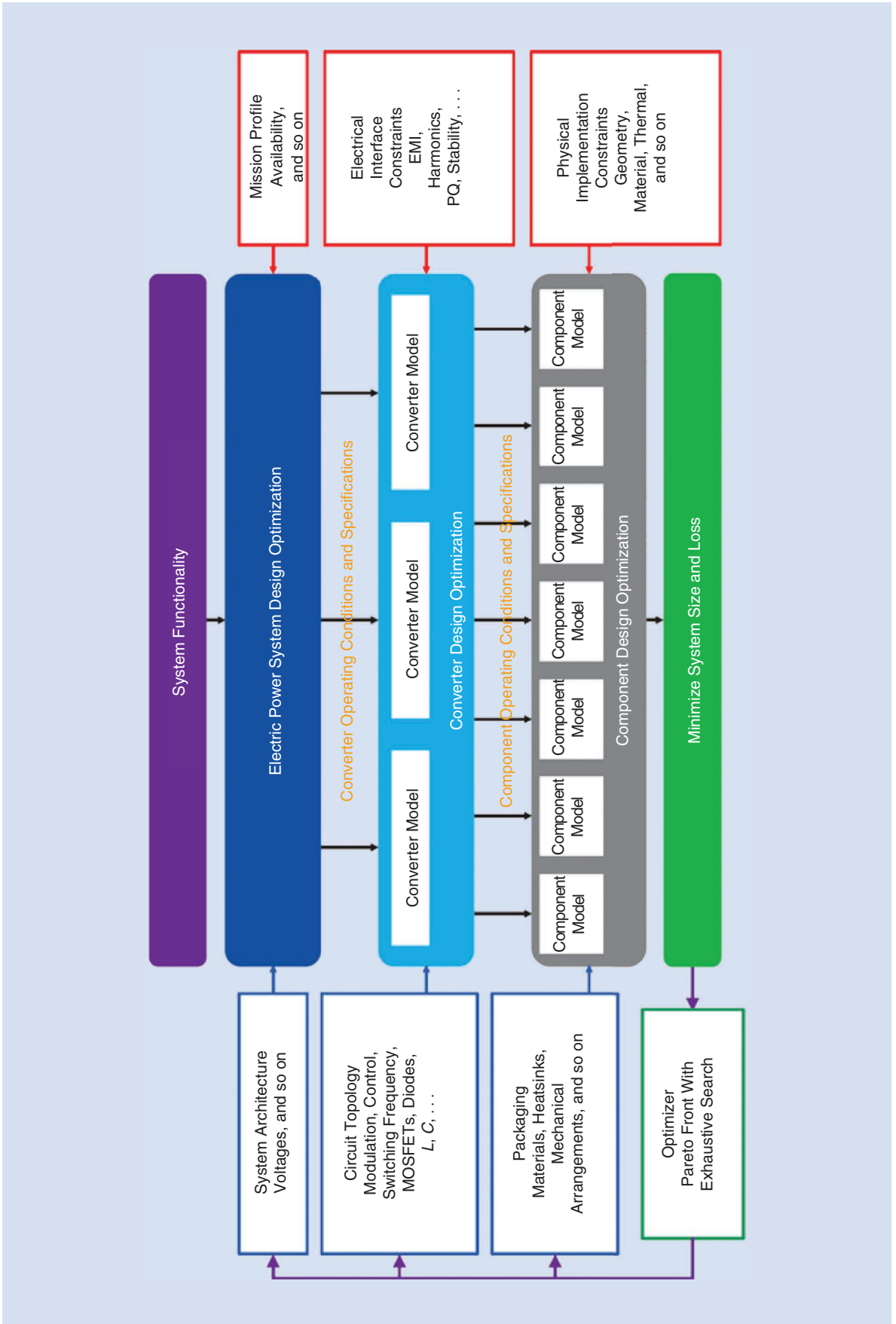

FIG 2 A multidisciplinary hierarchical optimization design flowchart. EMI: electromagnetic interference; PQ: power quality.

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Peeking Into the Future

Prof. Kolar focused his presentation on the topics of automated design, digital twin, and Industry 4.0. Under the scope of automated design, he discussed the design and performance spaces [Figure 4(a) and (b)], showing the functions and parameters that divide the two. In fact, his talk suggested that automation can deliver the technologies needed to optimally map the design space into the performance space. In addition, he also introduced absolute performance limits, labeled as a Pareto front. Concurrently, Prof. Kolar also introduced the concept of a digital twin, which means that for every physical device there is a digital mirror image.

> ***Prof. Kolar's talk suggested that automation can deliver the technologies needed to optimally map the design space into the performance space.***

Based on the aforementioned presentations and the involved discussion that ensued, the following general conclusions were drawn jointly by myself and Prof. Prasad Enjeti of Texas A&M University:

- Current power electronics design is lacking in automation, but it is not just nominal design, it is also missing the following characteristics:
  - robustness (design centering and tolerancing, and uncertainty)
  - resiliency (over environment and compromise)
  - reliability.
- Automated design tools for certain applications with specific voltage/current/power levels is probably the first set of applications.
- One of the key barriers to design automation seems to be that the device data sheets are not a true representation of the device's performance.
- Design automation can simplify the design of passive components, introduce sensitivity analysis, affect component tolerances on system performance, and so forth.
- Digital twin—physics-based digital mirror image. The digital replica of a physical asset such as a power electronic converter/system, which can merge live data from its physical counterpart using an interactive visual interface, has the potential to drastically enhance performance.
- Current approaches limit penetration.
- Power Electronics Design 4.0 demands a change in PELS composition.
- A second workshop on design automation has been organized. A new initiative on design automation in power electronics will probably have good traction.

FIG 3 The road map to Power Electronics Design 4.0.

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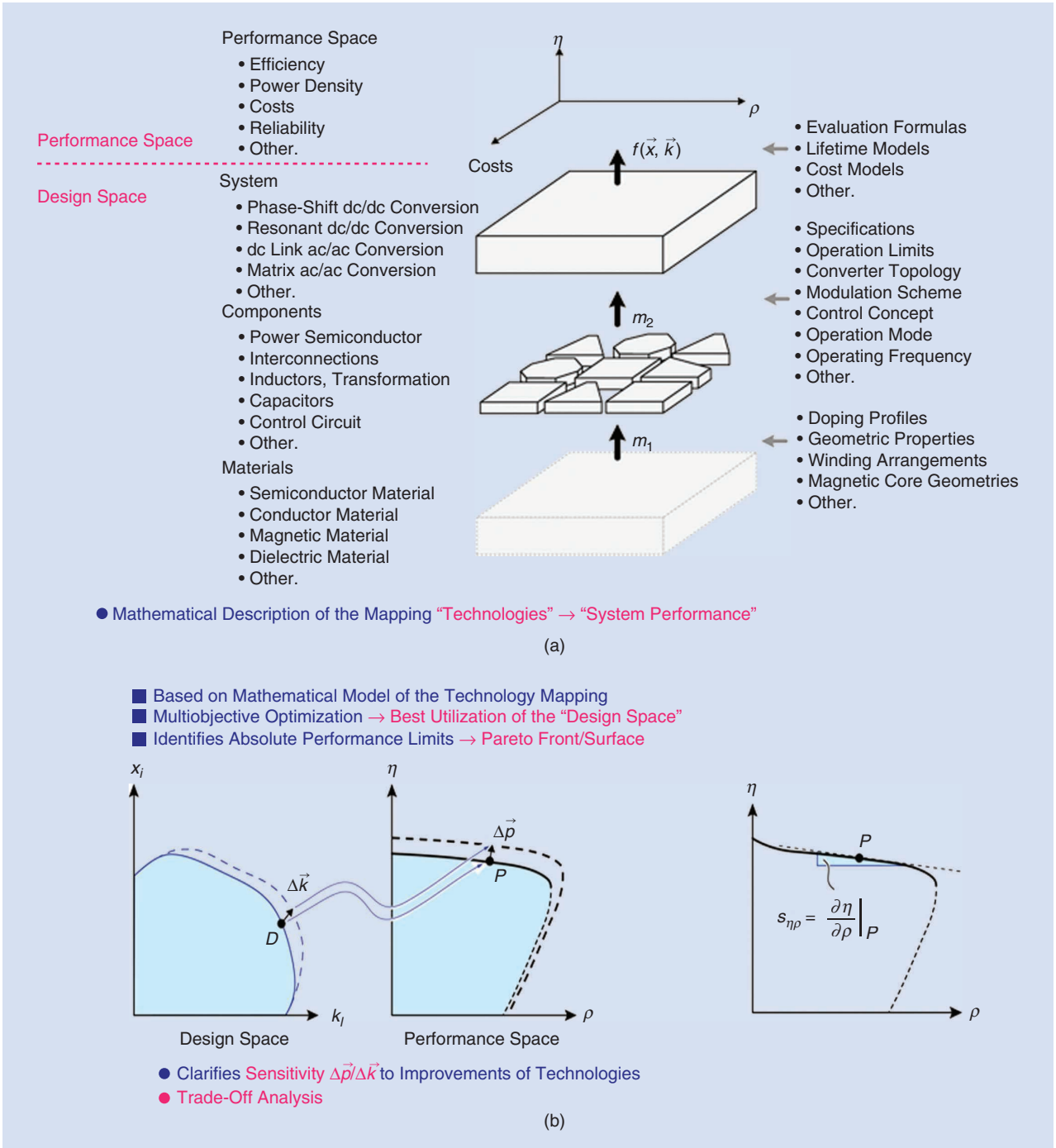

FIG 4 (a) The automated design maps plot space into performance and (b) identify its absolute performance limits, denoted as the Pareto front.

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