

A 100 kHz SiC Sparse Matrix Converter

T. Friedli, S. D. Round, and J. W. Kolar
 ETH Zurich, Power Electronic Systems Laboratory
 Zurich, 8092 SWITZERLAND

Abstract – A Sparse Matrix Converter (SMC) is a direct AC/AC converter that contains no large energy storage components. A 100 kHz, 1.5 kW SiC SMC is presented, which uses 1300 V, 4 A SiC JFET cascode devices. The SMC is operated from a 50 Hz, 230 V mains supply and has a predicted efficiency of 94%. A tower-like construction results in a volume of 1 liter and a power density of 1.5 kW/liter (25 W/in³). The measured waveforms verify matrix operation and show that the SiC JFET cascode devices have turn-on switching times of 30 ns. Analysis shows that the SMC heat sink and EMI filter volume can be minimized to 0.14 liters if the switching frequency is reduced to 40 kHz.

I. INTRODUCTION

Matrix converters (MC) are direct three-phase, AC/AC, switching power converters capable of providing simultaneous amplitude and frequency transformation of three-phase voltages. As opposed to conventional two-stage AC/DC/AC Back-to-Back (BBC) DC link PWM systems, the power stage of a matrix converter does not require energy storage elements and can consequently be implemented in an “all silicon solution” [1]. Since there are no large passive components the volume can be reduced compared to BBC systems that have input boost inductors and DC link capacitors [2]. MCs are inherently bi-directional and thus allow for regeneration of energy back into the mains. The input phase displacement factor can be adjusted by suitable modulation techniques, irrespective of the load type and MCs are also capable of operating under abnormal input voltage conditions [3].

As described in [4], Sparse Matrix Converters (SMC) are functionally equivalent to Conventional Matrix Converters (CMC) but offer a lower realization effort and less control complexity. A CMC requires 9 bidirectional power switches, usually constructed using 18 IGBTs, to switch the three input phases between the three output phases. The SMC is an Indirect Matrix Converter (IMC) that is split into an input stage

and an output stage (Fig. 1). The input and output stages are linked by a DC link that does not have any capacitance. The input stage is arranged so that only 9 switches are required, while the output stage has a standard 6 switch configuration. The SMC has a total of 15 switches compared to 18 for a CMC. At high operating frequencies and lower modulation indices the SMC has been shown to have a higher efficiency than an equivalent BBC [5]. However, the maximum output voltage is limited to 86.6% of the input voltage for all MCs. This might be a disadvantage if the MC is connected to standard industrial machine. For applications where a complete motor drive system (converter and machine) is supplied, the machine can be custom-designed for the MC’s output voltage range. Even considering the higher output currents required for the same output power level, the SMC’s efficiency is higher and the volume is smaller compared to a BBC [5]. Therefore, MCs provide an interesting alternative topology to BBCs.

One suitable application for the SMC is in More Electric Aircraft (MEA), where the power quality requirements have become more demanding as new electrical actuators are introduced into the flight control systems. Most aircraft supply their primary electrical power via an AC three-phase distribution system. Aerospace standards, such as DO-160 [6], define the aircraft power converter’s characteristics and input power quality. Typical specifications of a 1.5 kW AC supplied converter system would be:

Input RMS phase voltage	115 V
Input frequency range	360 – 800 Hz
Continuous output power	1.5 kW
Peak output power	5 kW for 1 s
Input current THD	< 0.05 I_1
Power factor (inductive load)	> 0.95
Ambient temperature range	-55°C to +85°C

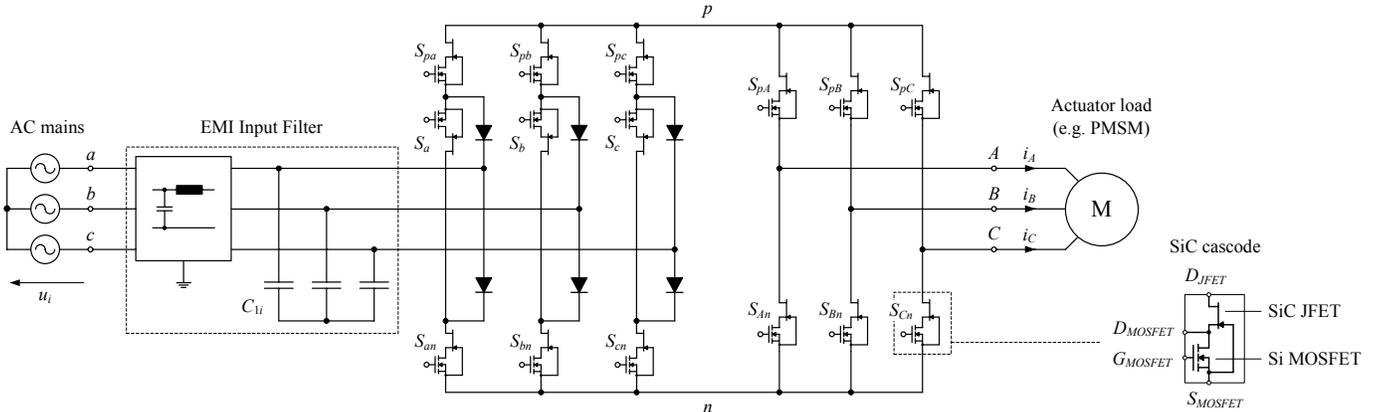


Figure 1. Power circuit of the SiC Sparse Matrix Converter. The SiC JFET devices are implemented with a SiCED cascode of a Si MOSFET and a SiC JFET. The SiC JFET has an inherent body diode for reverse current conduction (anti-parallel diodes not shown). All discrete diodes are SiC Schottky diodes.

In view of such challenging requirements, an application specific design of a SMC is attractive for motor loads connected to the AC on-board grid [7]. The absence of electrolytic capacitors in a SMC facilitates a compact, light-weight design and allows higher operating temperatures, and should result in an increase in reliability and lifetime. A compact converter enables the integration of the SMC and the machine into one unit [8].

In typical aircraft applications, a unidirectional power flow is demanded for equipment connected to the AC on-board grid. The SMC can be simplified into the Ultra Sparse MC (USMC) by replacing the three upper and the three lower switches of the input stage with diodes [9]. These diodes guarantee unidirectional power flow. The USMC therefore only has 9 switches, which reduces the realization effort even further. A disadvantage of the USMC is that the output phase angle is limited to $\pm 30^\circ$, although this is not a limitation if permanent magnet synchronous motors are used as the load machine.

For the power input frequency range of 360 to 800 Hz, the capacitor at the matrix converter input (Fig. 1, C_{li} is usually part of the EMI input filter) needs to be a small value compared to a standard 50/60 Hz mains application in order to keep the reactive power low and to meet the power factor requirements. However, to provide a high peak output power demands a larger input capacitor value to limit the input voltage ripple and harmonic distortion. This is typically not practical due to the reactive power limitation. The solution is instead to increase the switching frequency. The selection of an optimal switching frequency is dependent on performance, efficiency, volume and weight requirements. SiC power devices are better suited for high voltage and high switching frequency operation compared with IGBTs or power MOSFETs [10]. In this paper, an output stage switching frequency of 100 kHz is selected in order to show performance of the SMC with SiC power devices.

SiC switch technology is still under development and devices are not commercially available. The SMC presented in this paper is implemented with first generation SiCED SiC JFET cascode devices (Fig. 1) [11]. The cascode is a single package device that contains a low voltage Si MOSFET and a SiC JFET (Fig. 1). The SiC JFET provides the high voltage blocking capability while the MOSFET provides the cascode with a normally-off characteristic and allows the use of conventional high-speed gate drive ICs. Due to the high frequency operation, the design of the SMC is very challenging in terms of drive circuitry, layout, and signal generation.

This paper first describes the system requirements of the SMC in section II. In order to maintain high efficiency particular attention must be paid to the switching losses of the power semiconductors. The results of analytical loss calculations, the design of the SMC, and the physical construction are discussed in section III. In section IV the experimental results from the SiC SMC are shown. In section V an optimal switching frequency is estimated in terms of volume and power density. Finally, a new All-SiC JFET IMC is presented in section VI.

II. SPARSE MATRIX CONVERTER (SMC)

The SMC topology, presented in [4], is formed by the “DC side” coupling of a current-source-type rectifier and a

conventional voltage-source inverter. The operating principle is based on impressed voltages at the input by AC filtering capacitors and impressed currents at the output from an inductive load (machine inductance). With the restriction of a unipolar “DC link” voltage ($u > 0$) the input stage bridge leg structure (Fig. 1) provides independent controllability of both current directions as required by the output stage, and therefore enables four-quadrant operation.

An essential point in favor of the SMC topology is the possibility of changing the switching state of the input stage when the DC link current is zero. By switching the output stage into the free-wheeling state prior to switching the input stage the DC link current is reduced to zero (Fig. 2). Consequently, no continuous connection of the DC link to the mains has to be considered for changing the input stage switching state. This results in a reduced-complexity modulation scheme compared to the CMC and a higher system reliability.

For the SMC modulation scheme shown in Fig. 2 it can be seen that the DC link voltage is formed by switching the input stage between the largest and the second largest phase-to-phase input voltage. Due to this modulation scheme the input stage is switching at half the output stage switching frequency.

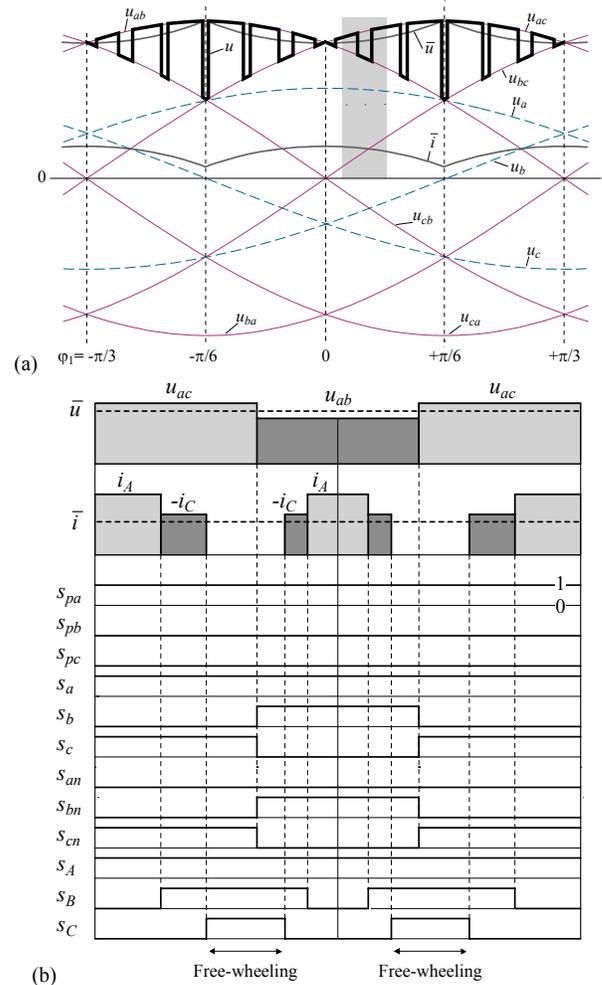


Figure 2. (a) DC link voltage waveform over a 120° input voltage interval. (b) Zoomed waveforms of one switching cycle (DC link voltage u and current i) with PWM pulse pattern shown for the grey shaded area in (a).

III. DESIGN OF THE SiC SMC

A. Specifications and Power Semiconductor Selection

The design of the SiC SMC is first considered for a conventional 50/60 Hz mains application, although the same system can be applied to aircraft systems, with a modification of the input stage capacitance and EMI filter. The target specifications for nominal operation of the SiC SMC are:

$$\begin{aligned} \text{Input RMS phase voltage} & U_1 = 230 \text{ V} \\ \text{Continuous output power} & P_2 = 1.5 \text{ kW} \\ \text{Output switching frequency} & f_{\text{Out}} = 100 \text{ kHz} \end{aligned}$$

The switching device selected for this design is the SiC JFET cascode provided by SiCED [11]. The cascode has voltage rating of 1300 V and a current rating of 4 A. For the six discrete diodes of the input stage (Fig. 1) commercially available SiC Schottky diodes, CSD05120 ($V_{RRM} = 1200 \text{ V}$, $I_F = 5 \text{ A}$), from CREE [12] are used.

B. Loss Calculation

By using loss calculations the requirements for the heat sink are determined in order to find a compact construction and cooling concept. The average losses are analytically calculated, based on the equations derived in [13] and [14] for the SiC JFET cascode. For system dimensioning, the generalized worst case occurs when the modulation index (1) is one and the converter output displacement angle, Φ_2 , equals 0° .

$$M_{12} = \frac{2 \hat{U}_2}{\sqrt{3} \hat{U}_1} = 1 \quad (1)$$

As experimentally analyzed and explained in [15], the switching losses of the input stage using SiC cascode devices can be neglected due to the zero current commutation strategy. The only losses in the input stage are due to the conduction losses. Therefore, the overall power semiconductor losses $P_{SC,tot}$ consist of the conduction losses of the input stage $P_{C,Inp}$ and the conduction $P_{C,Out}$ and switching losses $P_{S,Out}$ of the output stage

$$P_{SC,tot} = P_{C,Inp} + P_{C,Out} + P_{S,Out} \quad (2)$$

The loss parameters of the SiC cascode are taken from the measurements performed in [15], whereas the on-state parameters of the CSD05120 diodes of the input stage are based on their datasheet characteristics.

For the sake of brevity, the determined input and output stage losses are summarized in Tab. I and depicted in Fig. 3 for the worst case conditions and junction temperatures of $T_j = 25^\circ\text{C}$ and $T_j = 120^\circ\text{C}$. This results in a worst case efficiency defined by

$$\eta_{WC} = \left(\frac{P_2}{P_2 + P_{SC,tot}} \right)_{WC} \quad (3)$$

At the nominal operating point $\eta_{WC} = 93\%$ at $T_j = 120^\circ\text{C}$ and $\eta_{WC} = 95\%$ at $T_j = 25^\circ\text{C}$. Assuming an ambient temperature of $T_a = 20^\circ\text{C}$ leads to an estimated efficiency of 94%.

The semiconductor losses can also be plotted as a function of the output stage switching frequency as depicted in Fig. 4(a). This figure compares the total semiconductor losses of the SiC JFET cascode with a Si IGBT. The IGBT selected for this comparison is the IXYS FII50-12E, which has a similar

package type as the cascode. However, the current rating of the IGBT is 8 times higher than the cascode. Fig. 4 shows the trend for the total semiconductor losses and the proportion of switching losses to total losses for the SiC cascode and the Si IGBT. As seen in Fig. 4(a), above switching frequencies of approximately 50 kHz the SiC devices result in lower losses. This is mainly due to their lower switching losses. For lower frequency operation an SMC with IGBTs has lower semiconductor losses as the on-state losses of the Si devices are smaller. Fig. 4(b) shows that the SiC cascode devices have a lower proportion of switching losses compared to the IGBTs over the considered switching frequency range.

TABLE I. LOSS DISTRIBUTION

Junction temperature	Input Stage		Output Stage		Total losses
	Conduction losses	Conduction losses	Conduction losses	Switching losses	
25 °C	32 W	10 W	33 W		75 W
120 °C	53 W	22 W	40 W		115 W

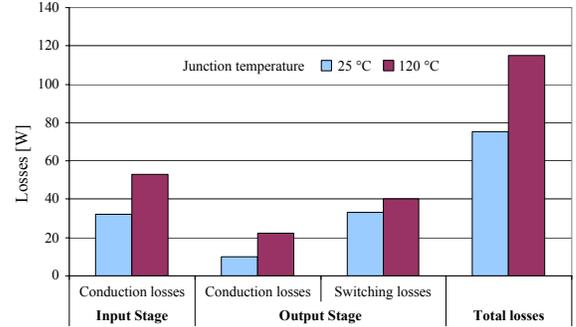


Figure 3. Average loss distribution of the input and output stage for $T_j = 25^\circ\text{C}$ and $T_j = 120^\circ\text{C}$.

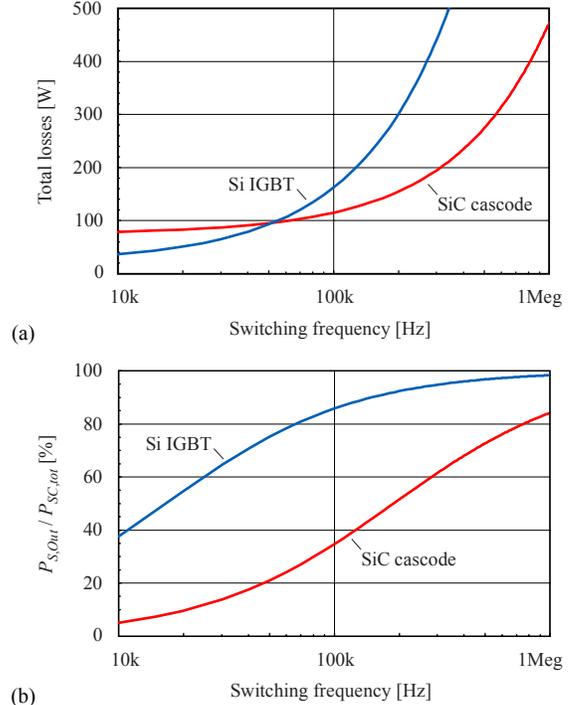


Figure 4. Comparison of the SMC with SiC cascodes and Si IGBTs. (a) Trend of total semiconductor losses. (b) Proportion of switching losses to total semiconductor losses.

C. Physical Construction

The physical construction of the SMC consists of a tower arrangement (Fig. 5) in which a stack is assembled from a fan, heat sink and 5 individual printed circuit boards. The PCBs, starting at the bottom, are the power board, gate drive and auxiliary board, measurement board, PWM signal generation board, and DSP control board.

The DSP control board, based on an Analog Devices ADSP-21992, provides the overall system and motor control, calculation of the modulation times and required switching vectors, and emergency shut-down operation. The PWM generation board contains two CPLDs in which the modulation times and vectors are written by the DSP and the switching signals are generated. The measurement board provides signal conditioning and level-shifting to convert the analog measurements to the DSP input voltage range. The gate drivers are based on the opto-coupler gate drive IC (HCPL 3180), where the isolated gate drive power (+12V / -5V) is supplied through individual transformers.

In view of the demand for compactness and the thermal design constraints a tower-like architecture is most advantageous. This design approach enables a converter cross-section similar to that of modern 1.5 kW to 2 kW permanent magnet synchronous machines. Therefore the SMC could be directly attached to such a machine. A photograph of the final laboratory prototype SMC is presented in Fig. 5. The outer dimensions are 92 mm x 92 mm x 120 mm, corresponding to a volume of 1 liter, leading to a power density of 1.5 kW/liter (25 W/in³).

In order to minimize the overall volume and to maximize the space for at prototype input filter, the heat sink was designed through numerical simulation. A special feature of this heat sink is that it does not have the usual fins but is manufactured with drill holes to increase the active cooling surface (Fig. 6).

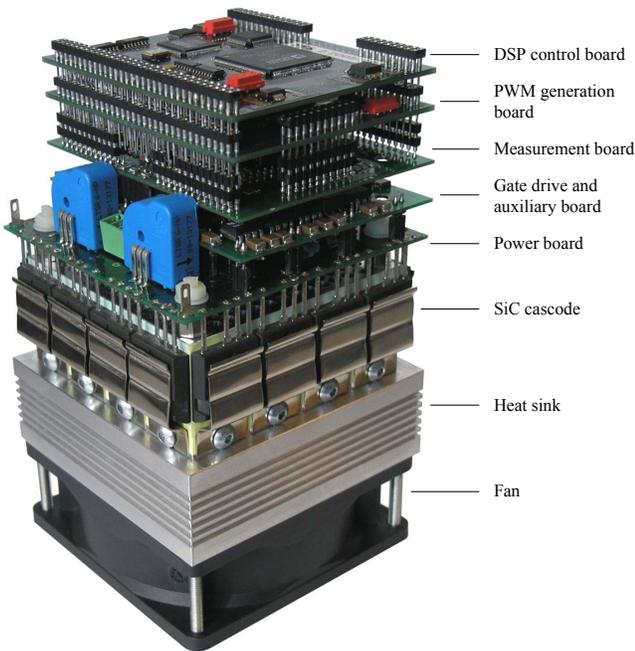


Figure 5. Prototype of the SiC JFET cascode SMC showing the different building blocks. Dimensions: 92 mm x 92 mm x 120 mm.

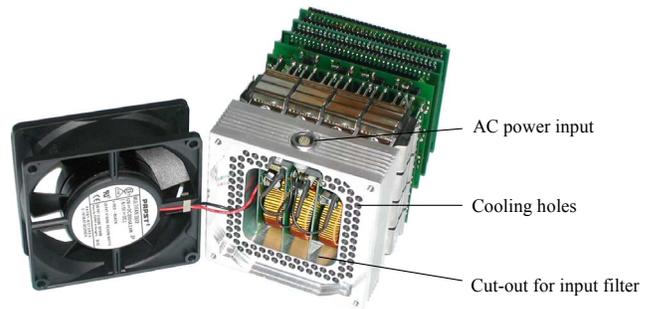


Figure 6. Heat sink with cut-out for EMI filter ($R_{th} = 0.3$ K/W).

IV. EXPERIMENTAL RESULTS

In this section measurements of the laboratory prototype are presented to demonstrate the in-circuit switching behavior of the SiC cascode devices. A 3-phase star-connected RL-load is connected to the output of the SMC. The oscilloscope waveforms in Fig. 7 show matrix operation and the switching and current waveforms of the output stage. The measurements were performed with a LeCroy Wavepro oscilloscope using LeCroy P005 and DXC100A voltage probes and a Tektronix A6312 current probe. The operating point of the SMC is:

Input switching frequency	$f_{inp} = 50$ kHz
Output switching frequency	$f_{out} = 100$ kHz
Input RMS phase voltage	$U_1 = 120$ V
Input frequency	$f_1 = 50$ Hz
Output RMS phase currents	$i_A = i_B = i_C = 1$ A
Output frequency	$f_2 = 200$ Hz

Fig. 7(a) shows the measured DC link voltage u and the output stage phase C current i_C . As can be seen, the DC link voltage waveform has the same shape as the idealized waveform in Fig. 2(a), except for the higher switching frequency. This shows that the input line-to-line voltages can be switched to the DC link to provide the required unipolar voltage. The output current is nearly sinusoidal with only a high frequency ripple component. Fig. 7(b) shows a zoomed-in view of the DC link voltage where the input stage is switching at 50 kHz. The gate-source and drain-source voltage of the output stage high-side switch S_{pC} are also shown. It can be seen that the output stage is switching at 100 kHz. The repetitive spikes in the dc link voltage waveform originate from the output stage switching at a 100 kHz.

Fig. 7(c) and (d) show zoomed-in switching waveforms for the turn-on and turn-off of the output stage switch S_{pC} . The switching performance of the output stage is important since the devices are hard-switched. Fig. 7(c) shows the turn-on of S_{pC} (for a positive output phase c current, $i_C > 0$), where the current commutates from the low-side diode to the high-side cascode occurs within 30 ns. In Fig. 7(d) the turn-off of S_{pC} is presented, where in this case the current commutates from the high-side cascode to the low-side diode. Compared to the turn-on time, the turn-off time is longer as a result of the relatively low output current and the limited Si MOSFET diode performance. The measurements show smooth switching transients, little ringing and almost no overshoot of the cascode drain-source voltage $u_{DS,SpC}$. This is a result of the symmetric and compact layout of the power board that provides short tracks between the individual power semiconductors, thus reducing the influence of any parasitic inductance.

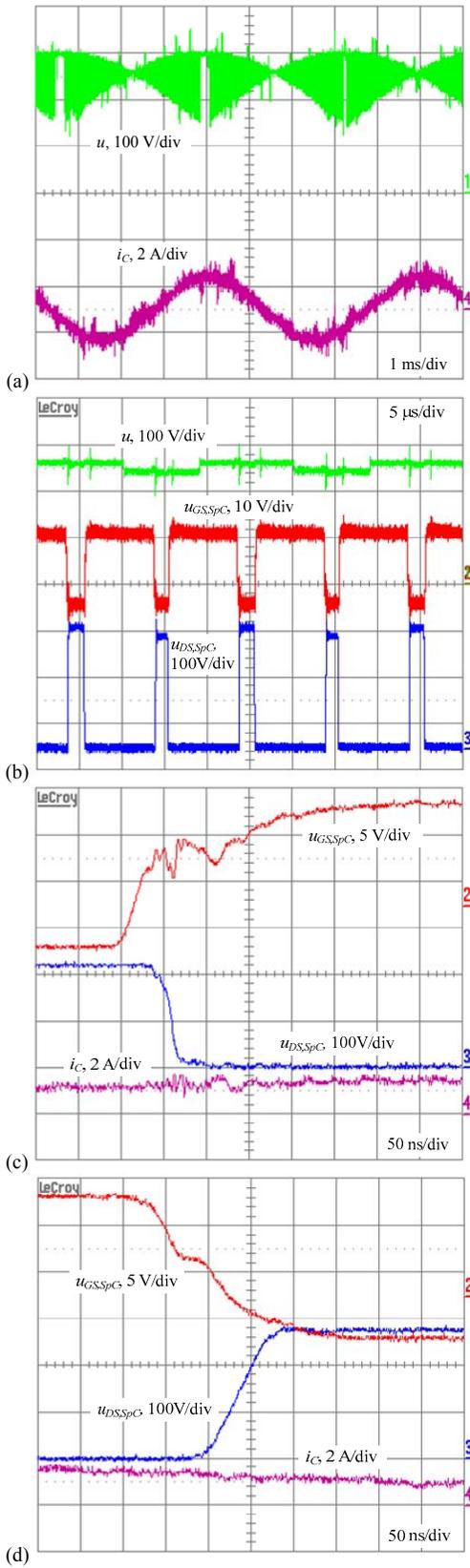


Figure 7. (a) DC link voltage u and output current i_C . (b) DC link voltage u , gate-source voltage $u_{GS,S_{pC}}$, and drain-source voltage $u_{DS,S_{pC}}$ of output stage switch S_{pC} , showing the switching frequency of 100 kHz. (c) Turn-on of output switch S_{pC} . (d) Turn-off of output stage switch S_{pC} .

To further verify matrix operation and to show that the input and output can operate with different frequencies, Fig. 8 shows the input phase c voltage and the output phase C current for the operating conditions of:

$$\begin{aligned} \text{Input RMS phase voltage} & U_1 = 175 \text{ V} \\ \text{Output RMS phase currents} & i_A = i_B = i_C = 1.8 \text{ A} \\ \text{Output frequency} & f_2 = 30 \text{ Hz.} \end{aligned}$$

As can be seen, for operation at an output power of 1 horsepower (736 W), the output current has a sinusoidal shape and can be generated from the input voltage without the need for an energy storage in the DC link.

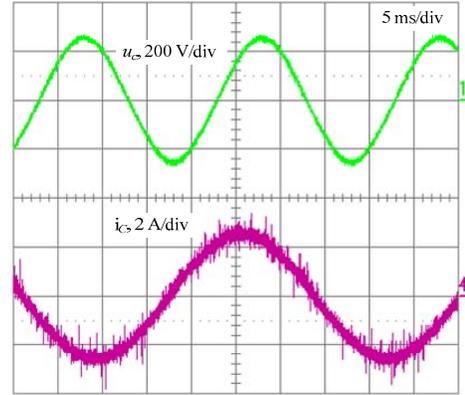


Figure 8. Input voltage and output phase current at 1 hp.

V. SWITCHING FREQUENCY SELECTION

The output stage of the SMC is a standard 6-switch inverter that is operated with hard-switching. Therefore, as the switching frequency is increased the total semiconductor losses also increase. Thus the switching frequency should be selected to minimize the losses and to minimize the overall SMC volume (or maximize the power density). Using the procedure presented in [16] Fig. 9 shows the volume occupied by a forced air cooled heat sink and the various EMI filter components as a function of switching frequency. The assumptions made for the analysis are: the volume does not account for the interconnection of components, only their boxed volume is used, a total load capacitance to PE of $C_g = 5 \text{ nF}$ is assumed, the EMI filter (a two stage filter as in Fig. 10) and a CM output filter are designed according to [16] to meet CISPR Class B - 6dB, and the forced air cooled heat sink has a cooling system performance index (CSPI) of $15 \text{ W}\cdot\text{K}^{-1}\cdot\text{dm}^{-3}$ [17].

With increasing switching frequency, the semiconductor losses and the heat sink volume both increase. However, the volume of the AC filter (C_1) capacitors is decreasing. The volume occupied by the DM and CM filters is dependent on the frequency with respect to the EMI standard requirements. It is observed that the DM filter dominates the filter volume for lower switching frequencies. The CM filter volume is highly dependent on the capacitance to ground and the increased volume of the CM filter at lower frequencies is a result of the increasing size of the output CM inductor. A step increase in the total EMI filter volume is seen at 150 kHz due to the Class B requirements and the necessity of filtering low order switching frequency harmonics.

It is shown that the minimum volume occurs within an output switching frequency range of 30 to 50 kHz, which is

lower than the 100 kHz used for the SMC in this paper. For aerospace applications it may be necessary to operate at higher switching frequencies in order to meet input current quality requirements, especially for high input frequencies. It is therefore important for the on-state resistance and internal capacitance of the SiC JFETs to be reduced in future devices in order to reduce the losses and to increase the optimal switching frequency.

A minimum volume of 0.14 liter would result in a maximum power density of 10.7 kW/liter (175 W/in³) for a SMC using the SiC cascode, although the layout fill factor and manufacturing volume is not included. Assuming that the SiC/Si dies would fit on the surface of a heat sink with a volume of 0.08 liter, a realistic or achievable power density would be a factor of 2.5 times lower or approximately 4.3 kW/liter.

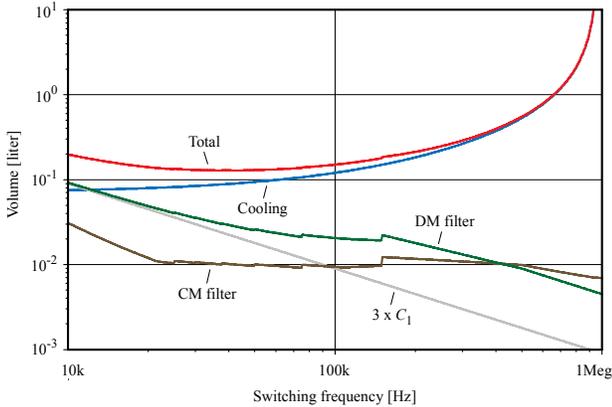


Figure 9. Boxed volume of a forced air cooled heat sink and filter components as a function of output stage switching frequency. Valid for 1.5 kVA, CSPI=15 W·K⁻¹·dm³, 5 nF load capacitance to PE, and DM/CM input and CM output filter designed for Class B-6dB. $T_a=45^\circ\text{C}$, $T_j=125^\circ\text{C}$.

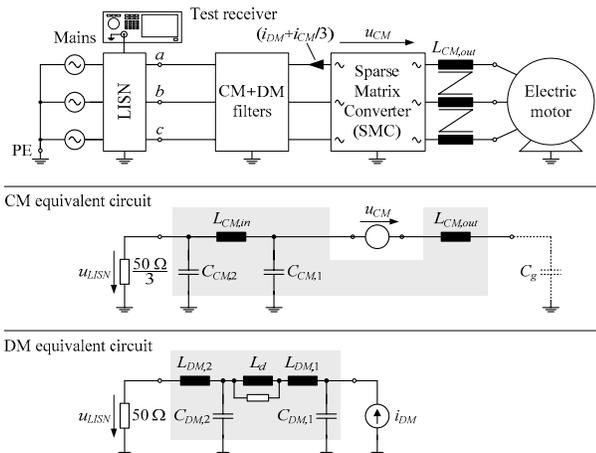


Figure 10. EMI Filter placement in the SMC and the equivalent circuit topologies used for the CM and DM filter design.

VI. ALL-SiC JFET INDIRECT MATRIX CONVERTER

One promised advantage of SiC devices is their operation with high junction temperatures, allowing higher ambient temperature or higher power density. The packaging is currently a limitation. For the tower SMC, the cascode device contains a Si MOSFET, which immediately limits the maximum case temperature. To overcome this limitation a new

All-SiC JFET Indirect Matrix Converter (Figs. 11 and 12) has been constructed. The IMC has 18 JFETs and reverse conduction is provided through their intrinsic body diodes. The IMC topology has been selected in order to use only JFETs in the construction and not to have any additional SiC diodes. The nominal output power is 2.5 kVA and this power level is presently restricted by the available JFET devices, which are SiCED 1200 V, 6 A devices. The JFETs are connected in a common source configuration. Their normally-on behavior, small pinch-off voltage variation, the requirement for a 25 V negative voltage for turn-off, means that a special gate drive circuit is used [18]. The target switching frequency is 200 kHz in order to test the SiC JFET performance. The other challenge comes from the high dv/dt generated from switching high voltages in tens of nanoseconds.

The SiC IMC has a complete input EMI filter and an output CM filter, and the layout of the IMC has been designed to provide space for testing different output filter topologies. The aluminum base plate serves as the thermal interface to the heat sink or motor case, and results in a flat layout structure. The splitting of power circuit into a separate gate drive board and a power board results in a small footprint design and enables a low-inductance connection of the gate drive circuit to the pins of the JFETs. Furthermore, it allows the ceramic input capacitors to be physically placed close to terminals of the JFET devices on the power board.

A new single FPGA modulation and measurement board has been developed to provide greater freedom in the implementation of new modulation strategies and easy interfacing of the analog measurement circuits and the motor encoder interface.

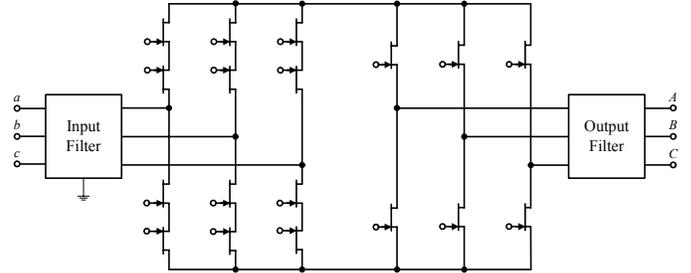


Figure 11. All-SiC JFET Indirect Matrix Converter power circuit schematic with SiCED 1200 V 6 A devices (anti-parallel body diodes not shown).

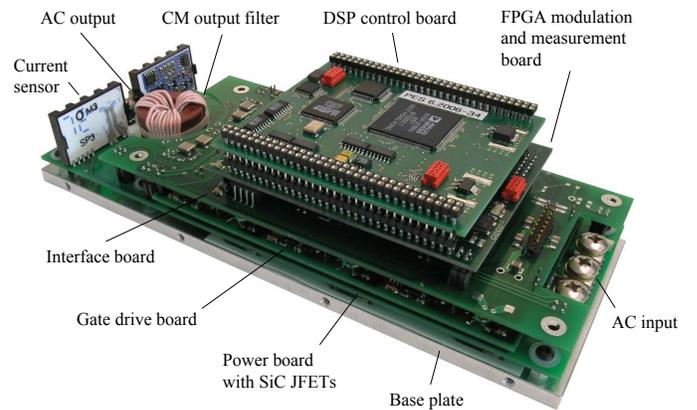


Figure 12. All-SiC JFET IMC prototype power circuit without input filter. Base area dimensions: 220 mm x 80 mm.

VII. CONCLUSIONS

Matrix converters are direct AC to AC converters that require no large energy storage components. A Sparse Matrix Converter is an indirect MC that has a separate input and output stage connected by a DC link. The SMC has a reduced number of power switches compared to the conventional MC. The SMC, as presented in this paper, is a possible converter for aerospace applications where a low volume/weight converter is desired. The aerospace AC power requirements demand the SMC to be operated at a high switching frequency to reduce reactive power and produce a high quality input current waveform. A 100 kHz output stage switching frequency is used in the SMC. To operate at this high frequency requires the use of SiC power semiconductors. The SMC is constructed with 1300 V, 4 A SiC JFET cascode devices.

A prototype SMC is designed for initial operation from a 50 Hz, 230 V mains system and has a power output capability of 1.5 kW with a predicted efficiency of 94%. A tower construction of the SMC results in a volume of 1 liter and a power density of 1.5 kW/liter. The measured switching waveforms show that the SiC JFET cascode devices achieve turn-on switching times of 30 ns. The SMC output stage can generate sinusoidal currents and matrix operation has been demonstrated. By considering the volume occupied by a forced air cooled heat sink and the EMI filter components as a function of output stage switching frequency, it is possible to determine the optimal switching frequency that results in minimum volume or maximum power density. For the 1.5 kW SiC JFET SMC the minimum volume of the heat sink and EMI filter is 0.14 liter for a switching frequency of 40 kHz. This would lead to a realistic SMC power density of 4.3 kW/liter.

The results from the SiC cascode SMC has been used as the basis to design a new All-SiC JFET IMC that is currently under test. An All-SiC IMC enables the heat sink temperature to increase and therefore to fully utilize the potential of SiC technology for challenging AC/AC matrix converter applications.

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