

# A High Efficiency Indirect Matrix Converter Utilizing RB-IGBTs

T. Friedli, M. L. Heldwein, F. Giezendanner, and J. W. Kolar

ETH Zurich, Power Electronic Systems Laboratory

ETL H23, Physikstrasse 3

CH-8092 Zurich, SWITZERLAND

friedli@lem.ee.ethz.ch heldwein@lem.ee.ethz.ch giezendanner@lem.ee.ethz.ch kolar@lem.ee.ethz.ch

**Abstract** — This paper presents the design and construction of an Indirect Matrix Converter (IMC) utilizing newly available IGBTs with reverse voltage blocking capability (RB-IGBTs). The design process involves the characterization of the RB-IGBTs by measuring the on-state parameters and the switching behavior in the rectifier stage of an IMC topology. Based on analytical equations the semiconductor losses are calculated and are used to perform the thermal design and simulation of the cooling system. Experimental measurements demonstrate that the designed IMC is capable of generating sinusoidal input and output currents and that the RB-IGBTs ensure low rectifier stage conduction losses and/or high IMC power conversion efficiency.

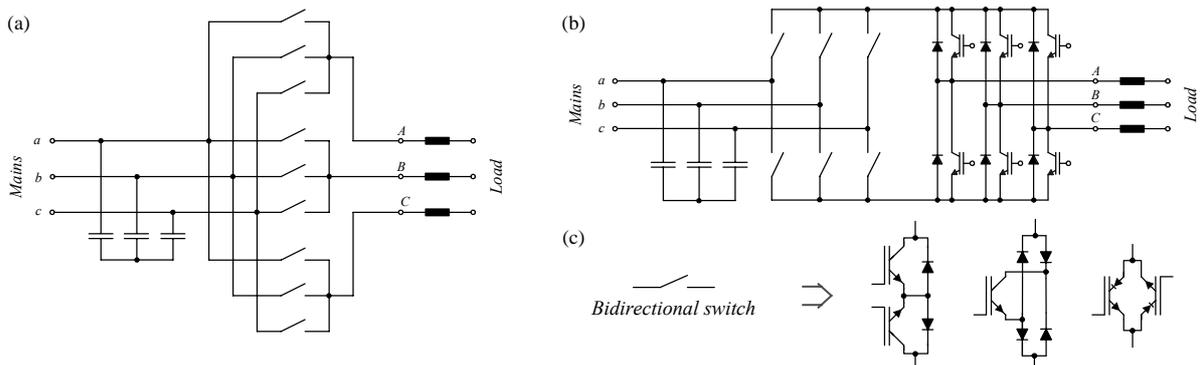
## I. INTRODUCTION

A survey of the technology state for motor drives shows that industrial interest in Matrix Converters (MC) is increasing [1-4] and commercial products are already on the market [2]. This motivates continuing research on this topic with the objective to overcome challenges of existing MC structures. Different indirect (two-stage) matrix converter topologies have been proposed in the literature [4-6], which require the same or a lower number of turn-off semiconductors as the Conventional Matrix Converter (CMC). The basic structure of an Indirect Matrix Converter (IMC) for four quadrant operation is depicted in Fig.1, showing different examples of the bi-directional switches in the rectifier stage. IMCs offer a reduced complexity modulation, allowing the system to commute safely [4-5] without special voltage or current sensing mechanism, as required for the CMC [7]. A further advantage compared to the CMC is that no additional over-voltage protection circuit is required. However, indirect topologies have more semiconductor devices in the current path from an input to an output terminal than the CMC. This tends to increase the conduction losses at their nominal operating point. Recently, Reverse Blocking IGBTs (RB-IGBT) [8-11] have become available that enable the construction of a bi-directional bipolar switch by employing only two transistors connected in

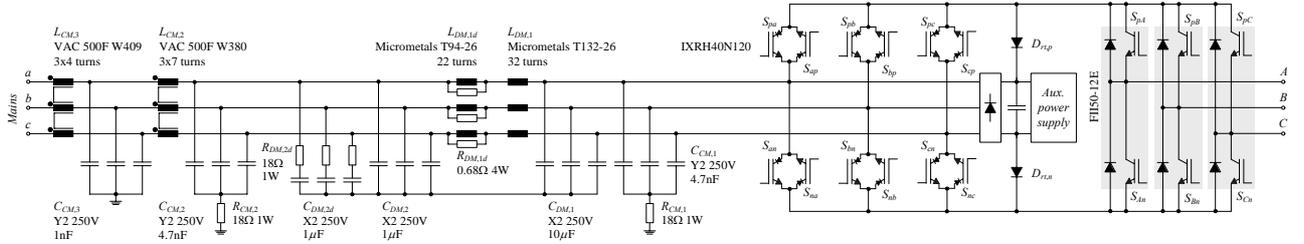
anti-parallel. The use of such devices in a CMC potentially lowers the dissipated power due to the low on-state conduction losses of the semiconductors [12-17], but as described in the following sections of this work the switching performance of the available RB-IGBTs tends to degrade the system efficiency unless very low switching frequencies are employed. In order to take advantage of the lower conduction losses of RB-IGBTs this paper presents an Indirect Matrix Converter (IMC) topology with RB-IGBTs in the rectifier stage and conventional IGBTs in the inverter stage, as depicted in Fig.2. The RB-IGBTs of the rectifier stage switch at zero-current, thus reducing the switching losses and allowing the converter to switch with higher switching frequencies while maintaining a high efficiency. The objective of this work is to design a complete IMC for motor drive application, which takes advantage of the lower conduction losses provided by the use of RB-IGBTs. The paper describes, in Section II, the experimental evaluation of the conduction and switching performances for the RB-IGBT [11], the advantageous use of zero-current commutation, and the choice of the switching frequency based on the measured RB-IGBT's characteristics. The device parameters are used for the analytical loss calculations [18] carried out in Section III, which also presents the thermal requirements and the design of a customized heat sink aiming for highest system compactness. The completion of the design for a compact prototype is finally illustrated in Section IV including the hardware structure, input EMC filter specifications, estimated efficiency and a photo of the constructed prototype. The ex-

**Table I** – Electrical specifications for the designed IMC.

Input RMS line voltage	$U_1$	3 x 230 V
Input displacement	$\Phi_1$	0°
Output RMS line voltage	$U_2$	3 x 0-199 V, 0-200 Hz
Max. output power	$S_{2,max}$	6.8 kVA
Max. ambient temperature	$T_a$	55°C
Rectifier switching frequency	$f_{p,R}$	10 kHz
Inverter switching frequency	$f_{p,I}$	20 kHz



**Fig.1:** Topologies: (a) Conventional Matrix Converter; (b) Indirect (two-stage) Matrix Converter topology; (c) examples of bi-directional switches.

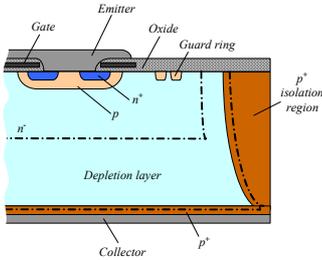


**Fig.2:** Designed Indirect Matrix Converter (IMC) schematic, showing the power circuit including the input EMC filter and auxiliary power supply connected to both the input mains and “DC link” in order to implement ride-through capability.

perimental results are presented in **Section V**. The rated specifications for the designed system are given in **Table I**. Finally, conclusions and an outlook for further research are summarized, including the design of a new IMC employing bi-directional power switch modules in ISOPLUS packages and IGBTs with reverse conduction capability (RC-IGBT).

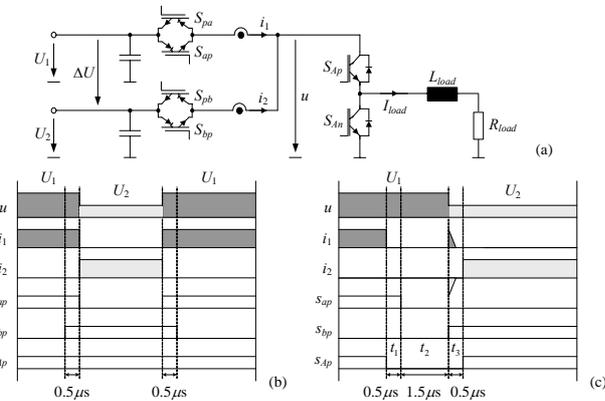
## II. EXPERIMENTAL SWITCHING PERFORMANCE CHARACTERIZATION OF THE RB-IGBT

RB-IGBTs are usually constructed as NPT devices [10] with a proper termination. A possible structure is shown in **Fig.3**, where a heavily p-doped isolation region is added at the side



**Fig.3:** Internal structure of a Diffusion Isolation RB-IGBT constructed as a NPT structure with an additional isolation region ( $p^+$ ).

perimeter of the basic structure of an IGBT in order to improve the reverse voltage blocking capability. Due to this, a similar switching and conducting behavior as for an NPT IGBT is expected, including a low on-state forward voltage drop. An important characteristic is that the devices are not designed for a diode commutation type of switching because the p-n collector junction is optimized for conduction, leading to a high reverse recovery current and a long current tail. These device characteristics are measured for the commercially available RB-IGBTs IXRH40N120 from IXYS [10-11], rated for 1.2 kV and 55 A, in order to provide a basis for the IMC design.



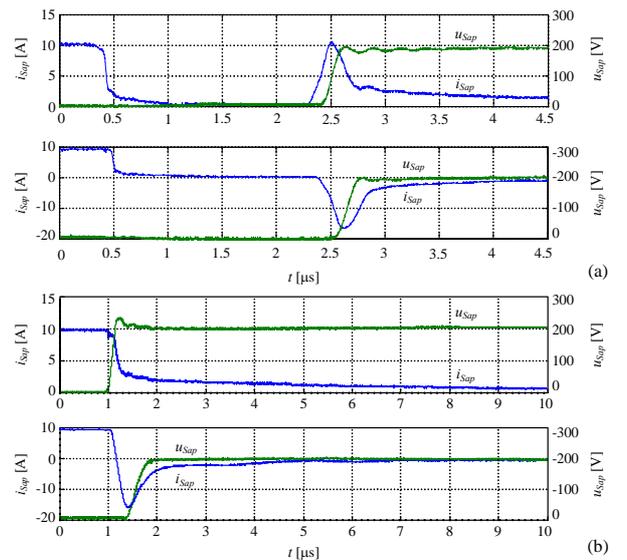
**Fig.4:** (a) Switching losses measurement setup and applied pulse patterns with (b) commutation under full current and (c) commutation under zero current. Not mentioned switch signals are constantly OFF.

**Table II** – On-state characteristics for the IGBTs used in the IMC (measurement results for  $T_j = 25^\circ\text{C}$ ).

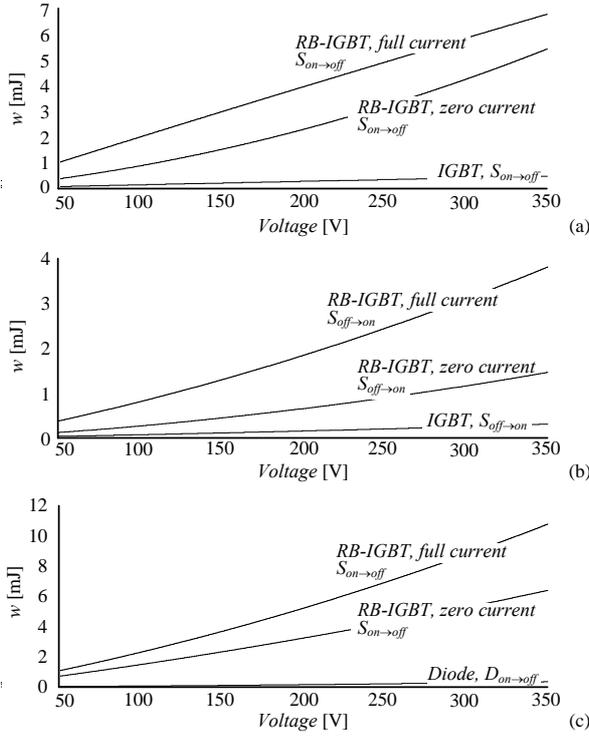
Characteristic	RB-IGBT IXRH40N120	IGBT FII50-12E
$U_F$ [mV]	878	940
$r$ [m $\Omega$ ]	71.4	52.4

For the conduction losses calculation it is important to determine the forward voltage drop  $U_F$  and the differential resistance  $r$ . This is performed for the IXRH40N120 RB-IGBT and, for comparison, for an IGBT in the IXYS FII50-12E module [19], which is implemented in the inverter stage of the designed IMC. In view of the achieved results, presented in **Table II**, low conduction losses are expected.

The switching performance of the RB-IGBT is evaluated utilizing the measurement setup, shown in **Fig.4**, that aims to acquire data for the switching losses calculation and deciding on switching frequency and commutation strategy for the IMC. Two types of commutation strategies are applied and all IMC switching sequences are simulated in the measurements. The pulse pattern shown in Fig.4(b) is used in the first measurements, where the RB-IGBTs are forced to switch the full load current. In the scheme illustrated in Fig.4(c) however, the output stage ( $S_{Ap}$  and  $S_{An}$ ) is switched into a free-wheeling state before the input stage switches ( $S_{ap}$  and  $S_{bp}$ ) change their states, thus providing a commutation under zero current. For both types of commutation different operating points are analyzed



**Fig.5:** Examples of the measured switching waveforms for a switched voltage  $\Delta U = 200$  V (cf. Fig.4(a)) and a switched current  $I_{load} = 10$  A. Different commutation strategies are used for positive and negative voltage differences  $\Delta U$ . (a) Switch turn-off under zero current and (b) switch turn-off under full current.



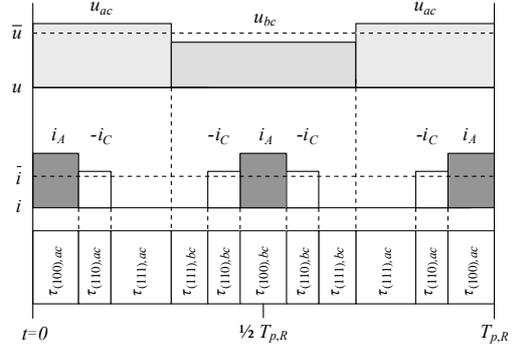
**Fig.6:** Examples of the least-square approximated switching losses curves for different commutation strategies of the RB-IGBT (IXRH40N120) and for comparison of the IGBT module (FII50-12E) for  $T_j = 25^\circ\text{C}$ . (a) Turn-off; (b) Turn-on; (c) Turn-off (diode, FII50-12E). Note: different vertical scales of (a), (b), and (c).

by varying the load current and the amplitude of the input voltages ( $u_1$  and  $u_2$ ). The currents ( $i_1$  and  $i_2$ ) and the voltages across  $S_{ap}$  and  $S_{pa}$  are measured with Tektronix A6312 current probes and LeCroy DA1855A differential probes with a LeCroy WavePro 950 oscilloscope. The scope is connected to a computer to transfer the measured data directly to a Matlab program where the instantaneous power is calculated and the energy involved in the commutations is determined. The layout for the measurement setup is similar to that of the expected final IMC layout in order to reproduce the parasitic elements.

The energy involved in the commutations is dependent on the voltage and current levels. Four characterizing commutation types are of relevance, namely turn-on and turn-off when the input voltage difference  $\Delta U$  is either positive or negative. The measured switching waveforms are depicted in **Fig.5** for both commutation strategies. The final result is a least-square approximation of the measured switching losses to provide polynomial coefficients for the analytical loss calculations [18].

**Table III** – Coefficients  $K_1 \dots K_5$  derived by least-square approximations of the measured switching losses at  $T_j = 25^\circ\text{C}$  for the specified semiconductors. Single commutation loss  $w$  is approximated by a polynomial equation  $w(u, i) = K_1 u i + K_2 u i^2 + K_3 u^2 + K_4 u^2 \cdot i + K_5 u^2 \cdot i^2$  dependent on the switched voltage, current and device characteristics [18].

	Commutation	$K_1$ [nWs(VA) $^{-1}$ ]	$K_2$ [nWs(VA $^2$ ) $^{-1}$ ]	$K_3$ [nWs(V $^2$ ) $^{-1}$ ]	$K_4$ [nWs(V $^2$ A) $^{-1}$ ]	$K_5$ [nWs(V $^2$ A $^2$ ) $^{-1}$ ]
IGBT + Diode [24] FII50-12E "Full current"	$S_{on \rightarrow off}$	129.0	-947.10 $^{-3}$	471.10 $^{-3}$	-84.1.10 $^{-3}$	2.52.10 $^{-3}$
	$S_{off \rightarrow on}$	41.6	1.75	308.10 $^{-3}$	60.7.10 $^{-3}$	-923.10 $^{-6}$
	$D_{on \rightarrow off}$	66.6	-2.54	332.10 $^{-3}$	95.4.10 $^{-3}$	2.90.10 $^{-3}$
RB-IGBT IXRH40N120 "Full current"	$S_{on \rightarrow off, for}$	3.06.10 $^3$	-167.0	13.10	-4.37.10 $^{-3}$	0.263
	$S_{on \rightarrow off, nat}$	9.23.10 $^3$	56.0	-4.59	30.30	-3.490
	$S_{off \rightarrow on, nat}$	5.88.10 $^2$	38.3	2.27	2.53	-0.370
RB-IGBT IXRH40N120 "Zero current"	$S_{on \rightarrow off, \Delta U > 0}$	1.85.10 $^3$	-124	13.00	-3.46	0.506
	$S_{on \rightarrow off, \Delta U < 0}$	3.16.10 $^3$	-182	16.70	-5.74	0.550
	$S_{off \rightarrow on, \Delta U > 0}$	98	-3.81	1.29	0.22	-6.93.10 $^{-3}$
	$S_{off \rightarrow on, \Delta U < 0}$	446	-24.30	3.51	-0.22	-47.9.10 $^{-3}$



**Fig.7:** Time behavior of the DC link quantities for the implemented modulation [4] in the interval  $\varphi_1 \in [\pi/6 \dots \pi/3]$  and  $\varphi_2 \in [0 \dots \pi/6]$ . The Rectifier stage switches at zero DC link current.

Examples of the fitted curves are shown in **Fig.6** for different commutation sequences and devices. **Table III** summarizes the approximated polynomial coefficients for the RB-IGBT and the conventional IGBT bridge-leg module (FII50-12E) used in the inverter stage for both commutation types. The index "for" denotes a forced commutation (IGBT) and "nat" a natural (diode) commutation.

Based on the switching energy levels involved in the different types of commutation, shown in Fig.6, it is evident that the zero current commutation strategy [4-5] is especially attractive for RB-IGBTs and makes the IMC the preferred topology. To guarantee low switching losses a minimal width of the zero current interval is needed. This interval leads to a dead time in the IMC which has to be considered for determining the switching frequency. Fig.4(c) illustrates the sequence for minimum commutation times with an overall dead time of 2.5  $\mu\text{s}$ . In order to limit the dead time to 5% of the switching period, the rectifier switching frequency is set to 10 kHz. This results in an inverter stage switching frequency of 20 kHz (cf. Fig.7, two inverter switching periods per rectifier switching period  $T_{p,R}$ ). This is a reasonable choice for low power motor drives (< 10 kW).

### III. ANALYTICAL LOSS CALCULATIONS AND THERMAL DESIGN

The loss calculations for the IMC are based on the procedure presented in [3] and [18] for a Very Sparse Matrix Converter (VSMC) with identical operating behavior. Unlikely the VSMC designed in [3], which utilizes fast switching devices in both rectifier and inverter stage, the switching losses in an IMC rectifier stage, built with RB-IGBTs, are not neglectable and therefore must be calculated. The inverter stage losses and

rectifier stage conduction losses can be calculated based on the equations in [18]. The derivation of the equations for the calculation of the rectifier stage switching losses is presented below in (1) to (9).

Due to the symmetry properties of the circuit topology and the input and output voltage and current waveforms, the following analysis is constrained to the interval where the input phase  $\varphi_1 \in [\pi/6 \dots \pi/2]$  and the output phase  $\varphi_2 \in [0 \dots \pi/3]$ .  $\Phi_2 \in [0 \dots \pi/6]$  is assumed for the output displacement angle. The switch  $S_{ap}$  switches complementarily with  $S_{bp}$  whereas  $S_{nc}$ , is on constantly. **Fig.7** shows the DC link voltage and current for one rectifier switching period for unity power factor at the output, where the voltage and current values within a pulse period are considered to be constant due to the high switching frequency. For the calculation of the switching losses, the appropriate voltages and currents can be taken from Fig.7, where the switched voltage equals to  $u_{ab}$  and the switched current corresponds to the current block  $i_A$  or  $-i_C$  depending on the output phase  $\varphi_2$ . The local average switching losses of a bi-directional switch over the relevant output phase interval  $\varphi_2 \in [0 \dots \pi/3]$  is given by

$$\overline{P_{sw,S}}(\varphi_1) = f_{p,R} \cdot \frac{3}{\pi} \cdot \left( \int_0^{\pi/6} w(|u_{ab}|, -i_C) d\varphi_2 + \int_{\pi/6}^{\pi/3} w(|u_{ab}|, i_A) d\varphi_2 \right) \quad (1)$$

where

$$w(u, i) = K_1 u i + K_2 u i^2 + K_3 u^2 + K_4 u^2 i + K_5 u^2 i^2 \quad (2)$$

$$u_{ab} = \hat{U}_1 \cdot \sqrt{3} \cdot \cos(\varphi_1 + \pi/6) \quad (3)$$

$$i_A = \hat{I}_2 \cdot \cos(\varphi_2 - \Phi_2) \quad (4)$$

$$-i_C = -\hat{I}_2 \cdot \cos(\varphi_2 + 2\pi/3 - \Phi_2) \quad (5)$$

The global average switching losses are the result of the integration of the local losses over  $\varphi_1 \in [\pi/6 \dots \pi/2]$

$$P_{sw,S} = \frac{1}{\pi} \cdot \int_{\pi/6}^{\pi/2} \overline{P_{sw,S}}(\varphi_1) d\varphi_1 \quad (6)$$

In the interval  $\varphi_1 \in [\pi/6 \dots \pi/3]$  the coefficients  $K_i$  for  $\Delta U > 0$  are used, because  $u_{ab} > 0$ , whereas for  $\varphi_1 \in [\pi/3 \dots \pi/2]$  the coefficients for  $\Delta U < 0$  are applied ( $u_{ab} < 0$ ). The evaluation of the integral leads to

$$P_{sw,S} = \frac{f_{p,R} \hat{U}_1}{16\pi^2} \left\{ \pi \left[ -6\sqrt{3}K_3 \hat{U}_1 + 4\pi K_3 \hat{U}_1 + \hat{I}_2^2 \left( -12K_2 + 8\sqrt{3}K_2 - 3\sqrt{3}K_3 \hat{U}_1 + 2K_5 \pi \hat{U}_1 \right) \right] + 6\hat{I}_2 \left[ 4(9 - 5\sqrt{3})K_1 + (3(-3 + \sqrt{3}) + 2(-1 + \sqrt{3})\pi)K_4 \hat{U}_1 \right] \cos(\Phi_2) \right\} \quad (7)$$

with

$$K_i = K_{i,S_{on \rightarrow off}, \Delta U > 0} + K_{i,S_{off \rightarrow on}, \Delta U > 0} + K_{i,S_{on \rightarrow off}, \Delta U < 0} + K_{i,S_{off \rightarrow on}, \Delta U < 0} \quad (8)$$

$$i = 1..5$$

The total switching losses for the rectifier stage are

$$P_{sw,Rec} = 6 \cdot P_{sw,S} \quad (9)$$

The time between the turn-off of the inverter stage and the switching of the rectifier stage is given by the freewheeling interval  $\tau_{(111),ac}$ , which is dependent on the modulation index  $M$ . For the maximum modulation index  $M_{max}$ ,  $\tau_{(111),ac}$  is determined by the minimum commutation time, which is the sum of

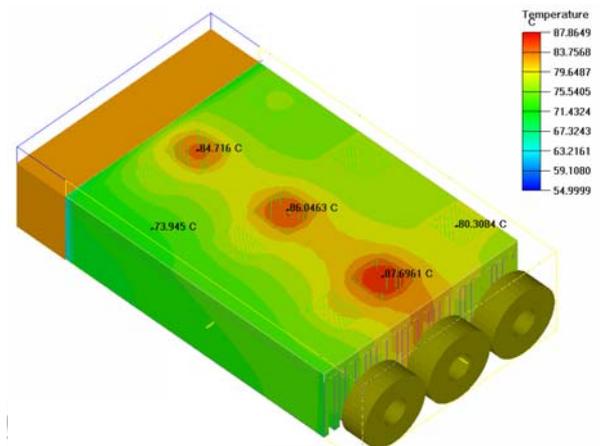
$t_1$ ,  $t_2$ , and  $t_3$  (Fig.4(c)). The rectifier stage switching losses are calculated for this operating condition. For lower modulation indices,  $\tau_{(111),ac}$  is longer and the switching losses are smaller because more of the remaining charge carriers in the RB-IGBTs recombine.

For the sake of brevity **Fig.10** summarizes the calculated semiconductor losses for the designed IMC at the rated power for a junction temperature  $T_j = 25^\circ\text{C}$ . Based on the semiconductor losses for  $T_j \cong 125^\circ\text{C}$  a cooling system is designed in order to maintain the maximum junction temperatures  $T_{j,max}$  in all semiconductors below  $130^\circ\text{C}$ . The cooling system comprises three high performance fans (SanAce 40/28 1U) and a customized heat sink ( $R_{th} \cong 0.07 \text{ K/W}$ ), designed according to [20]. The result of the thermal simulation for the given operating condition is shown in **Fig.8**. Along the center line of the heat sink, where the highest temperatures can be observed, the three output stage bridge leg packages are placed. The influence of the input filter inductors on the airflow is taken into account by placing them 15 mm from the end of the heat sink to provide an outlet for the cooling air.

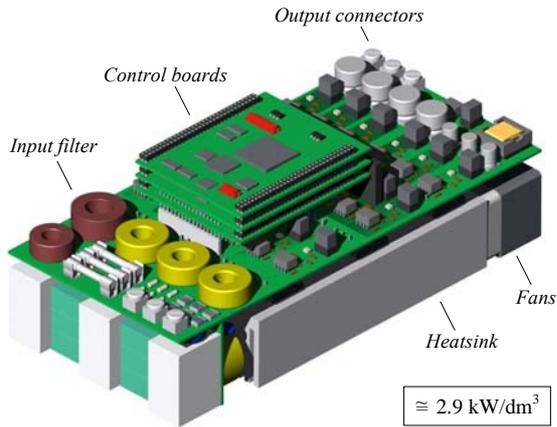
#### IV. FINAL DESIGN AND EVALUATION OF AN IMC UTILIZING RB-IGBT TECHNOLOGY

In order to achieve a compact layout with an optimal placement of the components, a 3D prototype model **Fig.9** is used, where the main parts of the converter system are indicated. The IMC is composed of five PCBs: (1) main board, which includes the power semiconductors, gate drives, auxiliary power, current sensors, and parts of the input filter; (2) filter board with parts of the differential mode (DM) input filter and surge protection; (3) measurement and signal conditioning board; (4) PWM generation board (CPLDs) incorporating different modulation strategies; and (5) DSP control board providing a software link to a computer and hardware monitoring.

As this IMC is designed for motor drive application it should provide a safe operating concept in case of mains loss. The approach chosen is to decelerate the machine after the mains loss has been detected (and all power transistors of the rectifier stage have been turned off) and to feed back energy through the diodes  $D_{rt,p}$  and  $D_{rt,n}$  (cf. Fig.2) to the auxiliary power sup-



**Fig.8:** Thermal analysis of the designed cooling system including the customized heat sink (28 fins –  $43 \times 120 \times 180 \text{ mm}^3$ ). Ambient temperature is  $55^\circ\text{C}$  and maximum expected junction temperature is  $130^\circ\text{C}$ . Input filter inductors are placed 15 mm from the heat sink.



**Fig.9:** 3D prototype model of the designed IMC illustrating the mechanical placement of the different components.

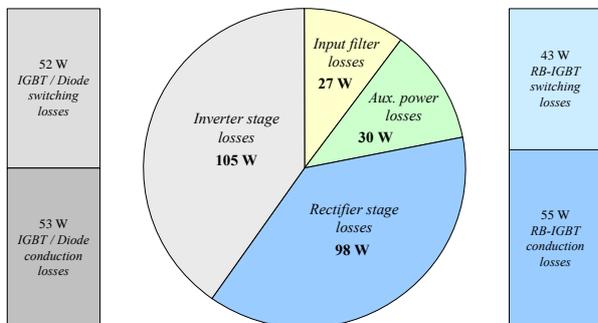
ply. The main advantage of such a ride-through capability is that the whole motor drive system remains controllable also through mains failure.

The input filter, presented in Fig.2, is designed in order to meet CISPR 11 specifications for Class A equipment. The differential mode stages are designed as in [21] and the common mode stages are designed with reference to [3]. The expected losses in the filtering elements sum to approximately 27 W. For the gate drives, fans supply and control electronics a value of 30 W is projected. The final power distribution for the complete IMC system at the rated power is shown in Fig.10. The expected overall efficiency based on the losses measurements and calculations for the nominal operating point (cf. Table I) is  $\eta \cong 95\%$ .

The losses in a CMC can be calculated with [18] for the same specifications and operating conditions. For a CMC, built with the same RB-IGBTs the total losses are considerably larger than for the IMC due to the large switching losses of the RB-IGBTs. This makes the IMC the preferred topology for utilizing RB-IGBTs, once the above mentioned zero current commutation can not be directly applied to a CMC.

## V. EXPERIMENTAL RESULTS

In this section measurements of the prototype IMC are presented to demonstrate its operation and the in circuit switching behavior of the RB-IGBTs. The converter is supplied with a 4-quadrant linear amplifier emulating a symmetric three phase grid. At the output a star-connected linear RL-load is con-



**Fig.10:** Calculated losses distribution at the rated power of 6.8 kVA (cf. Table I),  $U_1 = 230$  V,  $M = M_{max}$ , and  $\Phi_2 = 0^\circ$ ;  $T_j = 25^\circ\text{C}$  is assumed for all power semiconductors.



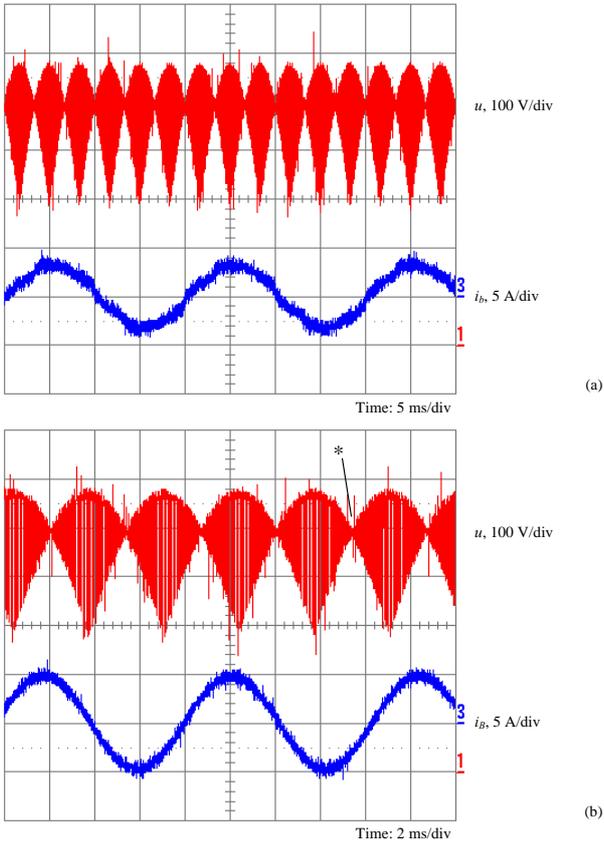
**Fig.11:** Photo of the developed RB-IGBT IMC based on the 3D prototype model. Power circuit dimensions: 76 x 120 x 260 mm<sup>3</sup>.

nected to the IMC. The measurements are performed with a LeCroy Waverunner LT584L oscilloscope for the operating point defined as follows:

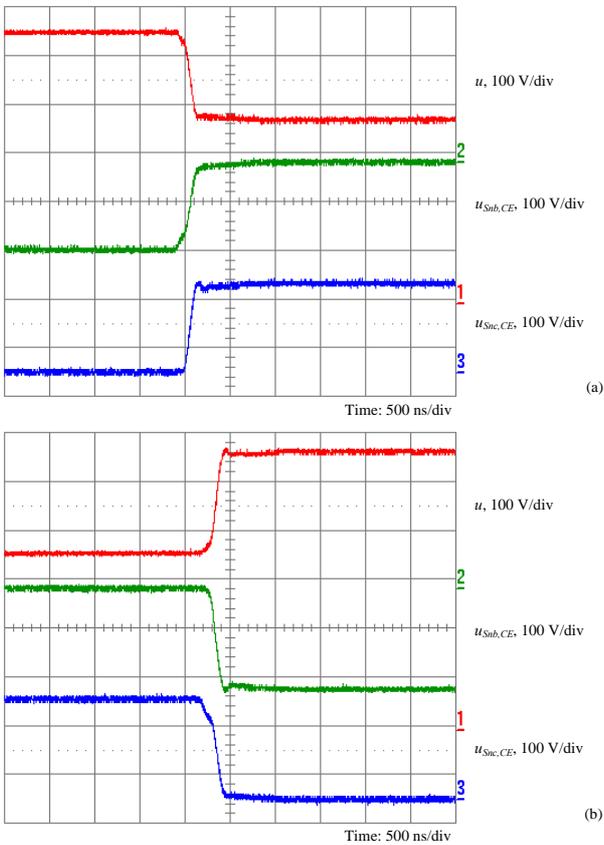
Input RMS line voltage	$U_1 = 230$ V
Input frequency	$f_1 = 50$ Hz
Output power	$P_2 = 1.5$ kW
Output frequency	$f_2 = 120$ Hz
Modulation index	$M = 0.78$ .

**Fig.12(a)** and **Fig.12(b)** depict the DC link voltage  $u$ , the input phase current  $i_b$  and the output phase current  $i_B$ . The DC link voltage shows the characteristic pattern for the conventional space vector based modulation scheme [4]. As it can be seen, the IMC is capable of generating sinusoidal currents of different frequencies at the output and input terminals. The implemented rectifier stage interlock delay time of 1.5  $\mu\text{s}$ , shown in Fig.4(b), is determined based on measurements and adjusted to achieve minimum switching losses in the rectifier stage. A further increase of this delay time would not lead to a considerable reduction of the rectifier stage switching losses. It has to be taken into account that for lower interlock delay times the input current waveforms and therefore also the *THD* can be improved. However, the switching losses would then increase because the time for the remaining charge carriers to recombine before the next switching action takes place is reduced.

In order to evaluate the in-system switching behavior of the RB-IGBT, two switching waveforms are considered where  $S_{ap}$  is clamped to the positive DC link bus bar and the DC link current commutates from  $S_{nb}$  to  $S_{nc}$  and vice versa. The measurements are performed for the worst case condition. This is when the RB-IGBTs have to conduct the maximum output current for the given operating point right before the inverter stage is switched to the free-wheeling state. The resulting switching transients are presented in **Fig.13(a)** and **Fig.13(b)** by measuring the collector-emitter voltages of the switches  $S_{nb}$  and  $S_{nc}$ . The achieved switching time is approximately 200 ns. Due to the reverse recovery effect slight overshoots can be observed for the device which is turned off. The measured switching behavior and transients prove that the RB-IGBTs are suitable for use in an IMC.



**Fig.12:** (a) DC link voltage  $u$  and input current  $i_b$ ; (b) DC link voltage and output current  $i_b$ . (\* equal instantaneous values of the line-to-line mains voltages defining the DC link voltage).



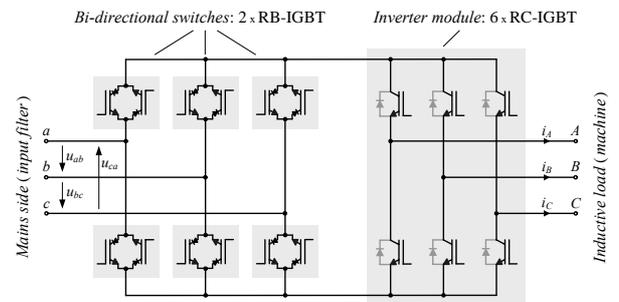
**Fig.13:** DC link voltage  $u$  and collector-emitter voltages  $u_{Snb,CE}$  and  $u_{Snc,CE}$  of the RB-IGBTs  $S_{nb}$  and  $S_{nc}$  for the switching from the (a) higher to the lower DC link voltage level and (b) vice versa.

## VI. CONCLUSIONS AND OUTLOOK

The design and realization of an IMC, utilizing available RB-IGBTs, is presented by considering different aspects of its conception. The analysis focuses on the analytical calculation of the switching losses for the implemented power semiconductors, which is carried out through measurements with device samples. The results show that the tested RB-IGBTs (IXRH40N120) present very low on-state characteristics, which lead to low conduction losses in a converter that requires bi-directional switches. However, the switching losses can be high due to the non-optimal switching behavior. A solution is the application of a zero current switching strategy, which is possible in an IMC topology and leads to reasonable total switching losses, indicating the IMC as a well suited topology for the use of RB-IGBTs. The work shows the derivation of equations to calculate the switching losses in the rectifier stage of an IMC, which along with equations from [18], allow for the theoretical calculation of the total losses. The complete IMC design comprises different aspects such as the thermal design, EMC filtering, protection, auxiliary power and ride-through strategy. The measurements show that the designed IMC is capable of generating sinusoidal input and output currents and that the desired matrix converter functionality can be achieved with RB-IGBTs in the rectifier stage.

An important aspect of the RB-IGBT rectifier stage of the IMC is the commutation between the corresponding switches, when the difference of the two input voltage levels applied to the DC link equals zero. In this case the resulting commutation voltage is zero (similar to  $\Delta U$  in Fig.4), which leads to a slow commutation and results in increased input current distortion. This occurs six times within an input period and corresponds with the contractions in the DC link voltage pattern (cf. Fig.12, \*). As the RB-IGBTs have an unfavorable switching behavior, future analysis will focus on this special case for the commutation of the rectifier stage to improve the performance.

In a next step, a new version of the IMC with RB-IGBTs will be designed employing ISOPLUS packages configured with two RB-IGBTs in anti-parallel, forming a bi-directional switch. This enables an even more compact design and allows further reduction in the wiring inductances. Another point for future research is the use of RC-IGBTs [22-23], which could be employed in the inverter stage of an IMC, thus reducing the total semiconductor silicon volume and lowering the final costs. The schematic of the power circuit for this future generation IMC is illustrated in Fig.14.



**Fig.14:** Future IMC concept based on the use of “state-of-the-art” power semiconductors to achieve maximum wafer utilization. In the rectifier stage, RB-IGBTs are used forming a bi-directional switch. In the inverter stage, RC-IGBTs are employed.

## REFERENCES

- [1] Klumpner, C., Blaabjerg, F., and Nielsen, P.: *Speeding-up the Maturation Process of the Matrix Converter Technology*. Proceedings of the 32nd IEEE Power Electronics Specialists Conference, Vancouver, Canada, Vol. 2, pp. 1083-1088 (2001).
- [2] Kang, J.-K., Hara, H., Hava, A.M., Yamamoto, E., Watanabe E., and Kume, T.: *The Matrix Converter Drive Performance Under Abnormal Input Voltage Conditions*. IEEE Transactions on Power Electronics, Vol. 17, No. 5, pp. 721-729 (2002).
- [3] Round, S., Schafmeister, F., Heldwein, M.L., Pereira, E., Serpa, L., and Kolar, J.W.: *Comparison of Performance and Realization Effort of a Very Sparse Matrix Converter to a Voltage DC Link PWM Inverter with Active Front End*. Proceedings of the 2005 International Power Electronics Conference (IPEC'05), Niigata, Japan, April 4 - 8, CD-ROM, ISBN: 4-88686-065-6 (2005).
- [4] Kolar, J.W., Baumann, M., Schafmeister, F., and Ertl, H.: *Novel Three-Phase AC-DC-AC Sparse Matrix Converter. Part I - Derivation, Basic Principle of Operation, Space Vector Modulation, Dimensioning*. Proceedings of the 17th Annual IEEE Applied Power Electronics Conference and Exposition, Dallas (Texas), USA, March 10 - 14, Vol. 2, pp. 777 - 787 (2002).
- [5] Wei, L., and Lipo, T.A.: *A Novel Matrix Converter Topology with Simple Commutation*. Record of the IEEE Industry Applications Society Annual Meeting, Chicago, USA, pp. 1749-1754 (2001).
- [6] Himori, K., Shinohara, K., Tarumi, O., Fu, Z., and Muroya, M.: *New Current-Controlled PWM Rectifier-Voltage Source Inverter without DC Link Components*. Proceedings of the Power Conversion Conference, Nagaoka, Japan, Aug. 3-6, Vol. II, pp. 783-786 (1997).
- [7] Wheeler, P.W., Clare, J.C., Empringham, L., Bland, M., and Apap, M.: *Gate Drive Level Intelligence and Current Sensing for Matrix Converter Current Commutation*. IEEE Transactions on Industrial Electronics, Vol. 49, No. 2, pp. 382-389 (2002).
- [8] Takei, M., Naito, T., and Ueno, K.: *The Reverse Blocking IGBT for Matrix Converter With Ultra-Thin Wafer Technology*. Proceedings of the 15th International Symposium on Power Semiconductor Devices & ICs (ISPSD) pp. 156-159 (2003).
- [9] Tokuda, N., Kaneda, M. Minato, T.: *An Ultra-small Isolation Area for 600V Class Reverse Blocking IGBT with Deep Trench Isolation Process (TI-RB-IGBT)*. Proceedings of the 16th International Symposium on Power Semiconductor Devices and ICs (ISPSD '04), pp. 129-132, ISBN: 4-88686-060-5 (2004).
- [10] Lindemann, A.: *A New IGBT With Reverse Blocking Capability*. Record of the 9th European Conference on Power Electronics and Applications (EPE), Graz, Austria, Aug. 27-29 (2001).
- [11] IXYS Corporation: *IXRH 40N120 - IGBT with Reverse Blocking Capability*. Advanced technical information (2005).
- [12] Itoh, J., Sato, I., Odaka, A., Ohguchi, H., Kodatchi, H., and Eguchi, N.: *A Novel Approach to Practical Matrix Converter Motor Drive System with Reverse Blocking IGBT*. Proceedings of the 35th Annual IEEE Power Electronics Specialists Conference, Aachen, Germany, pp. 2380-2385 (2004).
- [13] Klumpner, C., and Blaabjerg, F.: *Using Reverse Blocking IGBTs in Power Converters for Adjustable Speed Drives*. Record of the IEEE Industry Applications Society Annual Meeting, Paris, France, Vol. 3, pp.1516-1523 (2003).
- [14] Motto, E.R., Donlon, J.F., Tabata, M., Takahashi, H., Yu, Y., and Majumdar, G.: *Application Characteristics of an Experimental RB-IGBT (Reverse Blocking IGBT) Module*. Record of the IEEE Industry Applications Society Annual Meeting, Seattle, USA, Vol. 3, pp.1540-1544 (2004).
- [15] Bland, M.J., Wheeler, P.W., Clare, J.C., and Empringham, L.: *Comparison of Bi-Directional Switch Components for Direct AC-AC Converters*. Proceedings of the 35th Annual IEEE Applied Power Electronics Conference and Exposition, Aachen, Germany, pp. 2905 - 2909 (2004).
- [16] Jia, S. Tseng, K.J., and Wang, X.: *Study on Reverse Recovery Characteristics of Reverse-Blocking IGBT Applied in Matrix Converter*. Proceedings of the 20th Annual Applied Power Electronics Conference and Exposition, Austin (TX), USA, Vol. 3, pp. 1917-1921 (2005).
- [17] Adamek, J., Hofmann, W., and Lindemann, A.: *Switching Performance and Demands of Bidirectional IGBT-Configurations in Matrix Converters*. Record of the 9<sup>th</sup> European Conference on Power Electronics and Applications (EPE), Toulouse, France, Sep. 2-4, CD-ROM, ISBN: 90-75815-07-7 (2003).
- [18] Schafmeister, F., Rytz, C., and Kolar, J.W.: *Analytical Calculation of the Conduction and Switching Losses of the Conventional Matrix Converter and the (Very) Sparse Matrix Converter*. Proceedings of the 20th Annual IEEE Applied Power Electronics Conference and Exposition, Austin (Texas), USA, March 6 - 10, Vol. 2, pp. 875 - 881 (2005).
- [19] IXYS Corporation: *FII 50-12E - IGBT Phaseleg*. Advanced technical information (2000).
- [20] Drogenik, U., Laimer, G., and Kolar, J. W.: *Theoretical Converter Power Density Limits for Forced Convection Cooling*. Proceedings of the International PCIM Europe 2005 Conference, Nuremberg, Germany, June 7 - 9, pp. 608 - 619 (2005).
- [21] Heldwein, M.L., Nussbaumer, T., and Kolar, J.W.: *Differential Mode EMC Input Filter Design for Three-Phase AC-DC-AC Sparse Matrix PWM Converters*. Proceedings of the 35th IEEE Power Electronics Specialists Conference, Aachen, Germany, June 20 - 25, CD-ROM, ISBN: 07803-8400-8 (2004).
- [22] Takahashi, Y., Yoshikawa, K., Soutome, M., Fujii, T., Kirihata, H., and Seki, Y.: *2.5kV-1000A Power Pack IGBT (High Power Flat-Packaged NPT type RC-IGBT)*. IEEE Transactions on Electron Devices, Vol. 46, NO. 1, pp. 245-250 (1999).
- [23] Takahashi, H., Yamamoto, A., Aono, S., and Minato, T.: *1200V reverse conducting IGBT*. Proceedings of the 16th International Symposium on Power Semiconductor Devices and ICs (ISPSD '04), pp. 133-136, ISBN: 4-88686-060-5 (2004).
- [24] Schafmeister, F., Herold, S., and Kolar, J.W.: *Evaluation of 1200V-Si-IGBTs and 1300V-SiC-JFETs for Application in Three-Phase Very Sparse Matrix AC-AC Converter Systems*. Proceedings of the 18th Annual IEEE Applied Power Electronics Conference and Exposition, Miami Beach (Florida), USA, February 9 - 13, Vol. 1, pp. 241-255 (2003).