Part II: Experimental Analysis of the Very Sparse Matrix Converter

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VII. SIMULATION RESULTS

In this section the theoretical considerations of Section IV are verified by digital simulation using CASPOC®. The simulation parameters are defined with reference to the operating conditions of the experimental investigations described in Section VIII.

\[ U_{L1,J} = 400 \text{ V} \quad P = 2 \text{ kW} \quad f_1 = 50 \text{ Hz} \]
\[ U_2 = 95 \text{ V} \quad f_{P1} = 15.625 \text{ kHz} \quad f_2 = 100 \text{ Hz} \]

For the sake of simplicity no LC input filter was considered but the input voltage has been assumed to be directly applied to the converter input. There, the time behavior of the mains phase currents \( i_{N1}, \ldots, i_{N3} \) of the input filter inductor currents of a practical system was obtained by averaging the discontinuous rectifier input currents over one pulse half period. The simulation results are compiled in Fig. 19, where (d) shows the purely sinusoidal behavior of input and output quantities. The local average \( \bar{i}_a \) of the rectifier stage input phase current \( i_a \) is lying in phase with the corresponding mains phase voltage \( u_a \), accordingly the system shows ohmic fundamental mains behavior (cf. Eq.(4)). As Fig.19(a) clearly shows, each power transistor is clamped within a \( \pi/3 \)-wide interval of an input and/or output fundamental period what is indicated by a voltage across the power transistors of \( u_{SBp} = 0 \) and/or \( u_{SBn} = 0 \). In Fig.19(f) the time behavior of the DC link current \( i \) is given where \( i > 0 \), and/or \( i = i_{1+}, i_{1-} \) is valid (cf. Eq.(50)), according to the output power factor of \( \cos \Phi = 0.961 \) (cf. Fig.19(d), load phase displacement of \( \Phi = \pi/6 \)).

![Fig. 19: Simulation results for operating conditions given in Eq.(66)](image)

VIII. PRACTICAL REALIZATION

A prototype of the Very Sparse Matrix Converter (VSMC) having the following rated operating parameters

\[ P = 10 \text{ kW} \quad f_1 = 50 \text{ Hz} \]
\[ U_{L1,J} = 400 \text{ V} \quad f_{P1} = 15.625 \text{ kHz} \]

has been realized using standard power semiconductors, i.e.

- IGBTs: IXYS FII 50-12E in ISOPLUS i4-PACTM package [24]. The package does contain a full IGBT bridge leg, i.e. two power transistors of latest IGBT technology which can be directly employed in the output stage. For the realization of the input stage only one transistor per package has been utilized, due to the fact that no package containing only a single IGBT of latest technology is currently available.
- Diodes: IXYS DSEP 29-12A in TO220 [25].

An isolated package containing a four-quadrant switch (cf. Fig. 20) consisting of one IGBT of type FII 50-12E and of four diodes of type DSEP 29-12A rated for 50 A/1200 V is currently under development in collaboration with IXYS Semicond. GmbH [26]. This switch will be employed in the experimental system in a next step.

Furthermore, we would like to point out that for realizing the input stage of the USMC a power module VUI 30-12N1 containing the power semiconductors of one bridge leg is available (cf. [27, 28]).
to-emitter voltages of the switching power transistors are depicted (power transistor $S_{a,b,p}$ is turned on and power transistor $S_{a,b,p}$ is turned off) where a delay-time $t_d = 700 \text{ms}$ between turn-off of a transistor and turn-on of the subsequent transistor is provided in order to avoid a short circuit between the mains phases during a commutation. However, when $S_{a,b,p}$ is turned on a current peak occurs which results from

- the charging current of the parasitic DC link capacitance, and
- the tail-current of the IGBT which has been carrying current in the prior switching state.

This current peak has been found to be approximately independent from the load conditions and does result in switching losses of the input power transistors. In Fig. 22(c) the transition from a lower to a higher DC voltage level is depicted where the behavior is basically identical to Fig. 22(b). One has to point out that power transistor $S_{a,b,p}$ is taking over the blocking voltage only when the gate-to-emitter voltage of power transistor $S_{a,b,p}$ has reached the threshold-voltage, i.e. when $S_{a,b,p}$ is turned on. Furthermore, we want to note that due to the low-inductance biplanar wiring of the power semiconductors the measurement of the power semiconductor currents was partly obtained by subtracting and/or adding currents through neighboring diodes by a clip-on type current probe.

### B. Three-Phase Operation

The simulation results given in Section VII are verified by the experimental analysis as derived from the VSMC prototype shown in Fig. 21 for the operating parameters given in Eq. (66), cf. Figs. 23 and 24. An excellent consistency of the simulation results and of experimental results has been found, as can be seen immediately by comparing Figs. 19, 23 and 24. Insignificant differences are due to the fact that

- input and output frequency of the prototype are not synchronized what does result in a varying phase displacement of the fundamentals of the input and output phase quantities,
- the output frequency for the experimental investigation has not been set to exactly twice the input frequency, accordingly the envelope of, e.g., the voltages across the output power transistor $S_{a,b,p}$ does show a slightly different shape for the simulation and the experimental analysis (cf. Figs. 19(a) and 23(a)), and

In Fig. 21 the prototype of the VSMC is shown. The overall dimensions of the system are $20.0 \times 24.0 \times 8.5 \text{ cm}^3$ (i.e. $7.9 \times 9.45 \times 3.45 \text{ in}^3$), the total weight is 3.6 kg. The LC input filter was realized employing

- 3 iron powder core inductors, $L = 270 \text{ uH}$ @ zero current (diameter: 60 mm, height: 30 mm), and
- 3x4 foil capacitors in Delta-connection, $C = 1 \text{ uF}$ (dimensions: $(21 \times 26 \times 15) \text{ mm}^3$) [29].

![Prototype of the 10kW VSMC](image)

**A. Switching Behavior of Input Stage Power Transistors**

The switching behavior of the input stage power transistors for the transition from switching state $u_a = u_b = u_{a,b} \rightarrow u_a = u_b = u_{a,b}$ and vice versa has been investigated in detail for the following operating conditions

$$U_{N,M} = 440 \text{ V} \quad U_{S,M} = 86 \text{ V} \quad P_h = 700 \text{ W}. \quad (66)$$

According to Section IV (cf. Fig. 9) the commutation of the input stage is placed in the free-wheeling interval of the output stage, therefore, basically no switching losses are expected for the input stage. In Fig. 22(a) the time behavior of the DC link voltage $u$ and of the current via the power transistor $S_{a,b,p}$ within a part of a pulse period $T_p$ are shown for the transition from a higher to a lower DC voltage level (and vice versa); due to the free-wheeling operation of the output stage we have zero current via $S_{a,b,p}$. In Fig. 22(b) the gate-

![Results of the experimental investigation](image)

**Fig. 20**: Structure and package style of the novel four-quadrant VSMC switch FIO 50-12BD. (a) sectional view and (b) internal structure.

**Fig. 21**: Prototype of the 10kW VSMC. The control unit (realized using a floating point digital signal processor ADSP-21061) SHARC [14] in combination with programmable logic devices MAX 7000S) is not shown.
As proposed in this paper, the functionality of a conventional three-phase AC-AC matrix converter (CMC) could be achieved by employing only 15 IGBTs based on the Sparse Matrix Converter Concept (SMC). There, a zero DC link current commutation scheme does provide lower control complexity and potentially higher reliability as known multi-step commutation strategies. Zero DC link current commutation also would allow to realize the input stage of an Indirect Matrix Converter (IMC) by four-quadrant switches resulting in the Very Sparse Matrix Converter topology (VSMC) comprising only 12 IGBTs. An isolated four-quadrant switch will be available commercially in near future, therefore, the SMC and the VSMC are of high interest to the industry as alternative to the CMC concept.

In case a limitation to essentially unidirectional power flow could be accepted, the Ultra Sparse Matrix Converter (USMC) should be considered for three-phase AC-AC energy conversion. There, only 9 IGBTs are required in total for the system realization where a bridge leg of the input stage is available in form of an isolated power module.

The dimensioning of the power semiconductors of the SMC, VSMC and USMC can be based on analytical approximations of excellent accuracy as given in the paper. Furthermore, the current stresses on the input filter capacitors and the output current ripple could be calculated analytically what has been omitted here for the sake of brevity and will be shown in a future paper. Further topics of research will be

- the transfer of minimum switching loss strategies known for DC voltage link and DC current link converters to the SMC, VSMC and USMC,
- a comparison of the proposed matrix converter topologies to the CMC concerning conduction and switching losses and/or efficiency, where the realization of the CMC will be by unipolar IGBTs and reverse blocking IGBTs of type IXRH 50N80 [30]
- pre-correction of pulse pattern distortions introduced by the output stage dead-times and by the power semiconductor conduction voltage drops,
- analysis of the operation of the SMC under unbalanced mains condition,
- application of the SMC and VSMC for feeding a permanent magnet synchronous machine and application of the INFORM concept for sensorless control, where also a novel concept for emergency braking of the machine which does allow to dissipate the mechanical energy in the stator resistance will be tested [31]. This concept is of special interest in connection with the matrix converter in case a failure of the mains does occur while the machine is operating in braking mode. The research in this area will be in collaboration with the Department of Electrical Drives and Machines at the Vienna University of Technology.

Finally, we would like to point out, that the input stage of the SMC also could be connected to a three-level voltage DC link inverter output stage. The resulting topology is depicted in Fig. 25 and will also be investigated in the course of future research.

IX. CONCLUSIONS
ACKNOWLEDGEMENT

The authors are very grateful to Dr. Andreas Lindemann, IXYS Semiconductor GmbH, Lampertheim, Germany, for his efforts in connection with the design and practical realization of the novel four-quadrant switch IXYS FIO 50-12BD.

REFERENCES


