The Google Little Box Challenge

Ultra-Compact GaN- or SiC-Based Single-Phase DC/AC Power Conversion

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Outline

► The Google Little Box Challenge
► Little Box 1.0
► Concepts & Performances of Other Finalists
► Analysis of Advanced Concepts
► Optimization of Little Box 1.0
► Little Box 2.0
► Little Box 3.0 / Conclusions
Google
Little Box Challenge
Requirements
The Grand Prize
Finalists & Finals

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LiTTLE BOX CHALLENGE

- Design / Build the 2kW 1-Φ Solar Inverter with the Highest Power Density in the World
- Power Density > 3kW/dm³ (> 50W/in³, multiply kW/dm³ by Factor 16)
- Efficiency > 95%
- Case Temp. < 60°C
- EMI FCC Part 15 B

Push the Forefront of New Technologies in R&D of High Power Density Inverters
The Grand Prize

- Highest Power Density (> 50W/in³)
- Highest Level of Innovation

$1,000,000

Timeline
- Challenge Announced in Summer 2014
- 2000+ Teams Registered Worldwide
- 100+ Teams Submitted a Technical Description until July 22, 2015
- 18 Finalists (3 No-Shows)
Finalists

- 5 Companies
- 6 Consultants
- 4 Universities

Univ. of Illinois
Cambridge Active Magnetics
Tommasi Bailly
Virginia Tech
Schneider Electric
AMR
Venderbosch
OKE Services
AHED

Univ. of Tennessee
Rompower

* and FH IZW / Fraza d.o.o.

ETH zürich

15 Teams/Participants in the Final @ NREL
Final Presentations

- Finalists Invited to NREL / USA
- Presentations on Oct. 21, 2015
- Subsequent Testing by NREL
Little Box 1.0

Converter Topology
Modulation & Control
Technologies / Components
Mechanical Concept
Exp. Analysis

Acknowledgement
Derivation of Converter Concept
1-Φ Output Power Pulsation Buffer
**Power Pulsation Buffer**

- **Parallel Buffer @ DC Input**

- **Series Buffer @ DC Input**

- **Parallel Approach for Limiting Voltage Stress on Converter Stage Semiconductors**
Passive Power Pulsation Buffer (1)

- Electrolytic Capacitor

\[ V_{C,max} = 450 \text{ V} \]
\[ \Delta V_C / V_{C,max} = 3\% \]

- C > 2.2mF / 166 cm³ → Consumes 1/4 of Allowed Total Volume!

\[ S_0 = 2.0 \text{ kVA} \]
\[ \cos \Phi_0 = 0.7 \]

Electrolytic Capacitor:

5 x 493μF/450 V

\[ C = 2.46 \text{ mF} \]
Passive Power Pulsation Buffer (2)

- Series Resonant Circuit / Used in Rectifier Input Stage of Locomotives

\[ C_r = 20 \, \mu F \]
\[ L_r = 127 \, mH \]
\[ v_{lr} = 400 \, V \]

- Unacceptably Large Inductor Volume!

\[ f_r = 120Hz \]

- Electronic Inductor
Partial Active Power Pulsation Buffer

- Coupling Capacitor & “Electronic Inductor” Processing Only Partial Power

\[ V_i \rightarrow i \rightarrow i_k \rightarrow i_i \]

- Low \( U_{C,\text{aux}} \) \( \rightarrow \) Low Converter Losses
- High Values of \( C_k, \ C_{\text{aux}} \) Required for Low \( U_{C,\text{aux}} \)
- Full-Bridge Aux. Converter Allows Lower \( U_{C,\text{aux}} \)

* Ertl (1999)  
* Enslin (1991)  
* Pilawa (2015)
Partial Active Power Pulsation Buffer

- Coupling Capacitor & “Electronic Inductor”

Low $U_{C,aux} \rightarrow$ Low Converter Losses
- High Values of $C_K$, $C_{aux}$ Required for Low $U_{C,aux}$
- Full-Bridge Aux. Converter Allows Lower $U_{C,aux}$

Properties of Full-Bridge Aux. Conv.
Full Active Power Pulsation Buffer

- Large Voltage Fluctuation Foil or Ceramic Capacitor
- Buck- or Boost-Type DC/DC Interface Converter
- Buck-Type allows Utilizing 600V Technology

\[ C_k \approx 140 \, \mu F \]
\[ V_{Ck} = 23.7 \, cm^3 \]

108 x 1.2 \( \mu F / 400 \, V \)

- Significantly Lower Overall Volume Compared to Electrolytic Capacitor

* Kyritsis (2007)
Derivation of Output Stage Topology (1)

- Inversion of Basic 1-Φ PFC Rectifier Topology

- Boost-Type 1-Φ PFC Rectifier

- DC/|AC| Buck Converter & Mains Frequency “Unfolder”

* Erickson (2009) → Analysis Only for cos Φ = -1
Advanced DC/AC - Buck Conv. & Unfolder

- Temporary PWM Operation of Unfolder @ $U < U_{min}$ to Avoid AC Current Distortion

- CM Component of Output Voltage $v_o$
- Larger EMI Filtering Requirement Due to Temporary High-Freq. Switching of Unfolder
**Full-Bridge AC/DC Conv. Topology**

- Example of (Bidirectional) 1-Φ Telecom Boost-Type PFC Rectifier
- Low-Frequency Unfolder Operation of One Bridge Leg
- Interleaving for High Part Load Efficiency
- Si Superjunction MOSFETs

![Graph showing efficiency vs. input power for different voltages](graph.png)

*72W/in³ (4.5kW/dm³) incl. Holdup Capacitors @ 98.6% Efficiency*
Advanced Full-Bridge DC/AC Conv. Topology

- New Control Concept - PWM Operation of Mains Freq. Unfolder Bridge Leg @ $|u| < u_{0,\text{min}}$

- CM Component $u_{CM}$ of Generated Output Voltage
- Potentially Larger EMI Filtering Requirement
Symmetric PWM Full-Bridge AC/DC Conv. Topology

- Symmetric PWM Operation of Both Bridge Legs
- No Low-Frequency CM Output Voltage Component

DM Component of $u_1$ and $u_2$ Defines Output $u_0$
CM Component of $u_1$ and $u_2$ Represents Degree of Freedom of the Modulation (!)
Remark: AC Side Power Pulsation Buffer

- Full Bridge Output Stage / Full PWM Operation
- CM Reactive Power of Output Filter Capacitors used for Comp. of Load Power Pulsation

* Serban (2015)
ZVS of Output Stage / TCM Operation

- TCM Operation for Resonant Voltage Transition @ Turn-On/Turn-Off

- Requires Only Measurement of Current Zero Crossings, \( i = 0 \)
- Variable Switching Frequency Lowers EMI

* Henze (1988)
**CM-Enhanced TCM Modulation**

- CM Comp. of $u_1$, $u_2$ Changes Sw. Frequency
- Limits Sw. Frequency Variation
- Lower Residual Sw. Losses
4D-Interleaving

- Interleaving of 2 Bridge Legs per Phase – Volume / Filtering / Efficiency Optimum
- Interleaving in Space & Time – Within Output Period
- Alternate Operation of Bridge Legs @ Low Power
- Overlapping Operation @ High Power

Remark: iTCM Inverter Topology

- TCM: Challenging Inductor Design → Superposition of HF & LF Currents
- iTCM: Adding LC-Circuit between Bridge Legs → Separation of LF & HF Currents → $L \gg L_B$

- TCM

- iTCM

iTCM:
- Low Output Current Ripple
- PWM Modulation Applicable
- Dedicated LF and HF Inductor Designs Possible

→ Reduced Filtering Effort
→ Simple Control Strategy
→ Improved Converter Efficiency

* P. Jain (2015)
Selection of Switching Frequency

- Significant Reduction in EMI Filter Volume for Increasing Sw. Frequency

- Doubling Sw. Fequ. $f_S$ Cuts Filter Volume in Half
- Upper Limit due to Digital Signal Processing Delays / Inductor & Sw. Losses – Heatsink Volume
**EMI Filter Topology (1)**

- Conventional Filter Structure
  - DM Filtering Between the Phases
  - CM Filtering Between Phases and PE

- CM Cap. Limited by Earth Current Limit – Typ. 3.5mA for PFC Rectifiers (GLBC: 5mA then 50mA !)
- Large CM Inductor Needed – Filter Volume Mainly Defined by CM Inductors
EMI Filter Topology (2)

- Filter Structure with Internal CM Capacitor Feedback
- Filtering to DC- (and optional to DC+)

- No Limitation of CM Capacitor $C_1$ Due to Earth Current Limit $\rightarrow \mu$F Instead of nF Can be Employed
- Allows Downsizing of CM Inductor and/or Total Filter Volume
Final Converter Topology

- Interleaving of 2 Bridge Legs per Phase
- Active DC-Side Buck-Type Power Pulsation Buffer
- 2-Stage EMI AC Output Filter

- ZVS of All Bridge Legs @ Turn-On/Turn-Off in Whole Operating Range (4D-TCM-Interleaving)
- Heatsinks Connected to DC Bus / Shield to Prevent Cap. Coupling to Grounded Enclosure
Technologies

Power Semiconductors
Cooling
DSP/FPGA
Auxiliary
Evaluation of Power Semiconductors (1)

- Accurate Measurement of ZVS Losses Using Calorimetric Approach
- High Sw. Frequency for Large Ratio of Sw. and Conduction Losses

- Direct Measurement of the Sum of Sw. and Conduction Losses
- Subtraction of the Conduction Losses Known from Calibration
- Fast Measurement by $C_{th} \cdot \Delta T / \Delta t$ Evaluation
Evaluation of Power Semiconductors (2)

- Comparison of Soft-Switching Performance of ~60mΩ, 600V/650V/900V GaN, SiC, Si MOSFETs
- Measurement of Energy Loss per Switch and Switching Period

- GaN MOSFETs Feature Highest Soft-Switching Performance
- Similar Soft-Switching Performance Achieved with Si and SiC
- Almost No Voltage-Dependency of Soft-Switching Losses for Si-MOSFET
Selected Power Semiconductors

- 600V IFX Normally-Off GaN GIT - ThinPAK8x8
- 2 Parallel Transistors / Switch
- Antiparallel CREE SiC Schottky Diodes

- 1.2V typ. Gate Threshold Voltage
- 55 mΩ $R_{DS,on}$ @ 25°C, 120mΩ @ 150°C
- 5Ω Internal Gate Resistance

CeraLink Capacitors for DC Voltage Buffering
High dv/dt-Immunity Gate Drive (1)

- Low Threshold-Voltage of GaN GIT Devices $\rightarrow$ Negative Gate Voltage During Off-State Needed
- Internal Diode Characteristic $\rightarrow$ Gate Current Limitation During On-State Needed
- State-of-the-Art Gate Drive with Additional RC-Circuit

- $C_s$ Enables High Gate Current for Fast Turn-On
- $R_3$ Discharges $C_s$ During Off-State

- Duty Cycle and Frequency Dependent Gate Voltage
- Risk of Parasitic Turn-on Due to Switching of Complementary Switch
High $dv/dt$-Immunity Gate Drive (2)

- Improved Gate Drive Circuit with RC-Circuit and Added Clamping Diodes
- High Current for Fast Turn-On as Conventional Approach

- Diode $ZD_2$ Quickly Discharges $C_s$ to $V_{ZD_2}$ @ Turn-Off
- Diode $ZD_1$ Prevents $C_s$ from Complete Discharge During Off-State

- Fixed Neg. Turn-Off Gate Voltage Independent of Duty Cycle and @ Start-Up
High dv/dt-Immunity Gate Drive (3)

- Improved Gate Drive Circuit with RC-Circuit and Added Clamping Diodes
- High Current for Fast Turn-On as Conventional Approach

- Diode $ZD_2$ Quickly Discharges $C_s$ to $V_{ZD2}$ @ Turn-Off
- Diode $ZD_1$ Prevents $C_s$ from Complete Discharge During Off-State

- Fixed Neg. Turn-Off Gate Voltage Independent of Duty Cycle and @ Start-Up
- RC-Circuit in Neg. Rail Enables Precharge of $C_s$ with $R_4$
Final Advanced Gate Drive

- Fixed Negative Turn-off Gate Voltage - Independent of Sw. Frequency and Duty Cycle
- Extreme dv/dt Immunity (500 kV/μs) - Due to CM Choke at Signal Isolator Input

- Total Prop. Delay < 30ns incl. Signal Isolator, Gate Drive, and Switch Turn-On Delay
High Frequency Inductors (1)

- Multi-Airgap Inductor with Multi-Layer Foil Winding Arrangement Minim. Prox. Effect
- Very High Filling Factor / Low High Frequency Losses
- Magnetically Shielded Construction Minimizing EMI
- Intellectual Property of F. Zajc / Fraza

- L = 10.5\mu H
- 2 x 8 Turns
- 24 x 80\mu m Airgaps
- Core Material DMR 51 / Hengdian
- 0.61 mm Thick Stacked Plates
- 20 \mu m Copper Foil / 4 in Parallel
- 7 \mu m Kapton Layer Isolation
- 20m\Omega Winding Resistance / Q≈600
- Terminals in No-Leakage Flux Area

Dimensions - 14.5 x 14.5 x 22 mm$^3$
High Frequency Inductors (2)

- High Resonance Frequency $\rightarrow$ Inductive Behavior up to High Frequencies
- Extremely Low AC-Resistance $\rightarrow$ Low Conduction Losses up to High Frequencies
- High Quality Factor

- Shielding Eliminates HF Current through the Ferrite $\rightarrow$ Avoids High Core Losses
- Shielding Increases the Parasitic Capacitance
High Frequency Inductors (3)

- Cutting of Ferrite Introduces Mech. Stress
- Significant Increase of the Loss Factor
- Reduction by Polishing / Etching (5 μm)

* Knowles (1975!)

Comparison of Temp. Increase of a Bulk and a Sliced Sample @ 70mT / 800kHz

Graph showing temperature increase over time for different samples.
Thermal Management

- 30°C max. Ambient Temperature
- 60°C max. Allowed Surface and Air Outlet Temperature
- Evaluation of Optimum Heatsink Temperature for Thermal Isolation of Converter

Minimum Volume Achieved w/o Thermal Isolation with Heatsink @ max. Allowed Surface Temp.

\[ CSPI = \frac{V^{(W)}}{K^{(liter)}} = \frac{G^{(HS)}}{Vol_{CS}^{(liter)}} \cdot \frac{1}{R^{(HS)}} \cdot \frac{K^{(W)}}{Vol_{CS}^{(liter)}} \]
Thermal Management

- Overall Cooling Performance Defined by Selected Fan Type and Heatsink
  - Radial Blower
  - Axial Fan
  - Square Cross Section of Heatsink for Using a Fan
  - Flat and Wide Heatsink for Blower

Optimal Fan and Heat Sink Configuration Defined by Total Cooling System Length
Cooling Concept with Blower Selected → Higher $CS\Phi I$ for Larger Mounting Surface
Final Thermal Management Concept (1)

- 30mm Blowers with Axial Air Intake / Radial Outlet
- Full Optimization of the Heatsink Parameters
  - 200um Fin Thickness
  - 500um Fin Spacing
  - 3mm Fin Height
  - 10mm Fin Length
  - CSPI = 37 W/(dm$^3$.K)
  - 1.5mm Baseplate

- Two-Side Cooling → Heatsink Temperature = 52°C @ 80W (8W by Natural Convection)
Final Thermal Management Concept (2)

- CSPI = 37 W/(dm$^3$.K)
- 30mm Blowers with Axial Air Intake / Radial Outlet
- Full Optimization of the Heatsink Parameters

- Two-Side Cooling → Heatsink Temperature = 52°C @ 80W (8W by Natural Convection)
**i=0 Detection**

- **Analyzed Methods**
  - Shunt Current Measurement
  - Measurement of the $R_{ds,on}$
  - Two Antiparallel Diodes
  - Giant Magneto-Resistive Sensor
  - Hall Element
  - Saturable Inductor

- **Various Drawbacks**
  - Losses, No Galvanic Isolation, Low Signal-to-Noise Ratio (SNR), Size, Bandwidth, Realization Effort

- **Galvanic Isolation, High SNR, Small Size, High Bandwidth, Simple Design**

- **Min. Core Volume/Cross Section for Min. Core Losses**

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**i=0 Detection**

- **Saturable Inductor**
- **Toroidal Core**
- **Core Material**
  - R4 x 2.4 x 1.6, EPCOS (4mm Diameter)
  - N30, EPCOS

- Operation Tested up to 2.5MHz Switching Frequency
**i=0 Detection**

- Saturable Inductor
- Toroidal Core: R4 x 2.4 x 1.6, EPCOS (4mm Diameter)
- Core Material: N30, EPCOS

Operation Tested up to 2.5MHz Switching Frequency
Control Board & $i=0$ Detection

- Fully Digital Control – Overall Control Sampling Frequency of 25kHz
- TI DSC TMS320F28335 / 150MHz / 179-pin BGA / 12mm x 12mm
- Lattice FPGA LFXP2-5E / 200MHz / 86-pin BGA / 8mm x 8mm

- TCM Current / Induced Voltage / Comparator Output

- $i=0$ Detection of TCM Currents Using R4/N30 Saturable Inductors
- Galv. Isolated / Operates up to 2.5MHz Switching Frequency / <10ns Delay
Active Power Pulsation Buffer Capacitor (1)

- Electrolytic Capacitors  - Limited by Lifetime-Relevant Current Limit
- $2.2 \mu F$, 450 V Class II X6S MLCC  - Highest Energy Density but Cap. Decreases with DC Bias
- Novel $1 \mu F / 2 \mu F$, 650 V CeraLink™ Cap. (PLZT Ceramic) Features High Cap. @ High DC Bias
- Allows $125^\circ C$ Operating Temp. & Shows Very Low ESR @ High Frequencies

- CeraLink Resonance Frequency at Several MHz
- Small-Signal ESR of CeraLink in MHz Frequ. Range Sign. Lower Comp. to X6S MLCC
Active Power Pulsation Buffer Capacitor (2)

- **CeraLink**
  - Large-Signal Excitation with 2xLine-Freq. Reveals Large Hysteresis
  - Significantly Higher Losses @ 2xLine-Freq. Comp. to X6S MLCC
  - ESR Drops Significantly @ Higher Temperatures
  - 36μF (27μF) Blocks of Prepackaged Single Chips
  - Reliable Mech. Construction

- **X6S MMLC**
  - Only Available as Single Chips
  - Complicated Packaging

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**Graphs**

- **ESR (%)** vs Temperature (°C)
  - **CeraLink**

- **ΔQ (mAs)** vs Capacitor Voltage (V)
  - **CeraLink**
  - **X6S**

- **P_\text{loss} (\text{Watt})** vs \(V_{ac,pp} (\text{V})\)
  - **CeraLink**
  - \(T_{op} = 60°C\)
Final Active Power Pulsation Buffer

- High Energy Density 2\textsuperscript{nd} Gen. 400VDC CeraLink Capacitors Utilized as Energy Storage
- Highly Non-Linear Behavior $\rightarrow$ Optimal DC Bias Voltage of 280VDC
- Losses of 6W @ 2kVA Output Power

- 108 x 1.2\(\mu\)F /400 V
- 23.7\(\text{cm}^3\) Capacitor Volume

\[ \text{Effective Large Signal Capacitance of } C \approx 160\mu\text{F} \]
Active Power Pulsation Buffer Control (1)

- New Cascaded Control Structure

- P-Type Resonant Controller
- Feedforward of Output Power Fluctuation
- Underlying Input Current ($i_i$) / DC Link Voltage ($u_C$) Control
Active Power Pulsation Buffer Control (2)

- Multiple Controller Outputs Combined in a Single Current Reference

- Regulation of Mean Buffer Voltage (Bias Voltage)
- Tight Control of Inverter DC Link Voltage also During Transients
- Active Power Decoupling – Rejection of 2 x Line-Frequ. Ripple in Inverter DC Input Voltage
Auxiliary Supply

- Constant 50% Duty Cycle Half Bridge w. Diode Rect. or Synchr. Rectification (SR)
- ZVS → Compact / Efficient / Low EMI

Only Marginal Eff. Gain with Synchr. Rectification for Output Power Levels > 5W
Auxiliary Supply & Measurement Circuits

- Constant 50% Duty Cycle Half Bridge with Synchr. Rectification
- ZVS → Compact / Efficient / Low EMI \( (f_s=465\ kHz) \)

- 10W Max. Output Power
- 390V...450V Input Operating Range
- 13.8V...16.8V DC Output in Full Inp. Voltage / Output Power Range
- 90% Efficiency @ \( P_{\text{max}} \)

- 19mm x 24mm x 4.5mm \( (2\text{cm}^3\text{Volume}) \)
3D-CAD Construction
Mechanical Construction (1)

- Built to the Power Density Limit @ $\eta = 95\% / T_c < 60^\circ C$

- 88.7mm x 88.4mm x 31mm = 243cm$^3$ (14.8in$^3$) $\rightarrow$ 8.2 kW/dm$^3$
Mechanical Construction (2)

- Built to the Power Density Limit @ $\eta = 95\% / T_c < 60^\circ C$

- Dimensions: 88.7mm x 88.4mm x 31mm = 243cm³ (14.8in³) → 8.2 kW/dm³
**Mechanical Construction (3)**

- Built to the Power Density Limit @ $\eta = 95\%$, $T_c < 60^\circ C$

- $88.7\text{mm} \times 88.4\text{mm} \times 31\text{mm} = 243\text{cm}^3 (14.8\text{in}^3)$ → $8.2\text{ kW/dm}^3$
Mechanical Construction (4)

- Built to the Power Density Limit @ \( \eta = 95\% / T_c < 60^\circ C \)

- 88.7mm x 88.4mm x 31mm = 243cm\(^3\) (14.8in\(^3\)) \(\rightarrow\) 8.2 kW/dm\(^3\)
**Mechanical Construction (5)**

- Built to the Power Density Limit @ $\eta = 95\% / T_c < 60^\circ C$

- **88.7mm x 88.4mm x 31mm = 243cm^3 (14.8in^3) → 8.2 kW/dm^3**
Experimental Results

Hardware
Output Voltage/Input Current Quality
Thermal Behavior
Efficiency
EMI
Little Box 1.0 - Prototype I

- System Employing Electrolytic Capacitors as 1-Φ Power Pulsation Buffer

273cm³
7.3 kW/dm³
97.5% Efficiency @ 2kW
$T_c = 58°C @ 2kW$

$\Delta u_{DC,pp} = 2.85\%$
$\Delta i_{DC,pp} = 15.4\%$
$THD+N_U = 2.6\%$
$THD+N_I = 1.9\%$

97mm x 90.8 mm x 31mm (16.6 in³)

- Compliant to All Specifications
Little Box 1.0-I Measurement Results (1)

- System Employing Electrolytic Capacitors as 1-Φ Power Pulsation Buffer

Compliant to All Specifications
Little Box 1.0–I Measurement Results (2)

- System Employing Electrolytic Capacitors as 1-Φ Power Pulsation Buffer

\[
\eta_w = 96.4\% \quad \text{Weighted Efficiency}
\]

- Heating of System Lower than Specified Limit \( (T_{C,\text{max}} = 60°C @ T_{\text{amb}} = 30°C) \)
Little Box 1.0–I Measurement Results (3)

- System Employing Electrolytic Capacitors as $1-\Phi$ Power Pulsation Buffer

$P_{out} = 400\text{W}$

- Compliant to All Specifications
Little Box 1.0 - Prototype II (Final)

- System Employing Active Ceralink 1-Φ Power Pulsation Buffer

- 8.2 kW/dm³
- 8.9cm x 8.8cm x 3.1cm
- 96.3% Efficiency @ 2kW
- $T_c=58^\circ C$ @ 2kW

- $\Delta u_{DC, pp} = 1.1\%$
- $\Delta i_{DC, pp} = 2.8\%$
- $THD+N_U = 2.6\%$
- $THD+N_I = 1.9\%$

- Compliant to All Original Specifications (!)
- No Low-Frequ. CM Output Voltage Component
- No Overstressing of Components
- All Own IP / Patents
Little Box 1.0 - Prototype II (Final)

- System Employing Active Ceralink 1-Ø Power Pulsation Buffer

- 8.2 kW/dm³
- 8.9cm x 8.8cm x 3.1cm
- 96.3% Efficiency @ 2kW
- $T_c=58°C$ @ 2kW

- $\Delta u_{DC} = 1.1\%$
- $\Delta i_{DC} = 2.8\%$
- $THD+N_U = 2.6\%$
- $THD+N_I = 1.9\%$

- Compliant to All *Original* Specifications (!)
- No Low-Frequ. CM Output Voltage Component
- No Overstressing of Components
- All Own IP / Patents

★ 135 W/in³
Little Box 1.0-II Measurement Results (1)

- System Employing Active Ceralink 1-Φ Power Pulsation Buffer
  - Ohmic Load / 2kW

Output Current (10 A/div)
Inductor Current Bridge Leg 1-1 (10 A/div)
Inductor Current Bridge Leg 1-2 (10 A/div)

DC Link Voltage (AC-Coupl., 2 V/div)
Buffer Cap. Voltage (20 V/div)
Buffer Cap. Current (10 A/div)
Output Voltage (200 V/div)

- Compliant to All Specifications
Little Box 1.0-II Measurement Results (2)

- System Employing Active Ceralink 1-Φ Power Pulsation Buffer

\[ \eta_w = 95.07\% \]  Weighted Efficiency

Compliant to All Specifications
Little Box 1.0-II  Measurement Results (3)

- System Employing Active Ceralink 1-Φ Power Pulsation Buffer

![Diagram showing measurement results]

- Buffer Cap Voltage (50V/div)
- Output Voltage (50V/div)
- Buffer Cap. Current (5 A/div)
- Ind. Curr. Bridge Leg 1-1 (5 A/div)

- Start-up and Shut-Down (No Load Operation)
Little Box 1.0-II Measurement Results (4)

- System Employing Active Ceralink 1-Φ Power Pulsation Buffer

Stationary Operation @ 2kW Output Power
Little Box 1.0-II Measurement Results (5)

- System Employing Active Ceralink 1-Ω Power Pulsation Buffer

- Transient Response for Load-Step of 0 Watt → 700 Watt
Little Box 1.0-II Measurement Results (6)

- System Employing Active Ceralink 1-Ω Power Pulsation Buffer

Transient Response for Load-Step of 700 Watt → 0 Watt
**Little Box 1.0-II Volume and Loss Distribution**

- **Volume Distribution (240cm³)**
  - Power Pulsation Buffer 71.3cm³
  - Inverter Stage 169.1cm³
  - MOSFETs
  - Capacitor
  - Electronics
  - Inductor
  - Inductors
  - Electronics
  - Housing
  - Others
  - Output Filter

- **Loss Distribution (75W)**
  - Power Pulsation Buffer 28.1W
  - Inverter Stage 46.3W
  - MOSFETs
  - Capacitor
  - Electronics
  - Inductor

- Large Heatsink (incl. Heat Conduction Layers)
- Large Losses in Power Fluctuation Buffer Capacitor (!)
- TCM Causes Relatively High Conduction & Switching Losses @ Low Power
- Relatively Low Switching Frequency @ High Power – Determines EMI Filter Volume
Other Finalists

Topologies
Switching Frequencies
Power Density / Efficiency Comparison

Detailed Descriptions:
www.LittleBoxChallenge.com
Finalists - Performance Overview

- 18 Finalists (3 No-Shows)
- 7 Groups of Consultants / 7 Companies / 4 Universities

Note: Numbering of Teams is Arbitrary

- 70...300 W/in³
- 35 kHz...500kHz...1 MHz (up to 1MHz: 3 Teams)
- Full-Bridge or DC/AC Buck Converter + Unfolder
- Mostly Buck-Type Active Power Pulsation Filters (Ceramic Caps of Electrolytic Caps)
- GaN (11 Teams) / SiC (2 Teams) / Si (2 Teams)
Finalists - Performance Overview

- 18 Finalists (3 No-Shows)
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Note: Numbering of Teams is Arbitrary

(1) Virginia Tech
(2) Schneider Electric
(3) EPRI (Univ. of Tennessee)
(4) Venderbosch
(5) Energy Layer
(6) ETH Zurich
(7) Rompower
(8) Tommasi-Bailly
(9) Red Electric Devils
(10) AHED
(11) FH IISB
(12) Univ. of Illinois
(13) AMR
(14) OKE
(15) Cambridge Magnetics
**Finalists - Performance Overview**

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Note: Numbering of Teams is Arbitrary

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- Mostly Buck-Type Active Power Pulsation Filters (Ceramic Caps of Electrolytic Caps)
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(9) Red Electric Devils
(10) AHED
(11) FH IISB
(12) Univ. of Illinois
(13) AMR
Category I: 300 – 400 W/in³ (1 Team)

- “Over the Edge”
- Hand-Wound Overstressed & Too Small Electrolytic Capacitors (210uF/400V)
- No Voltage Margin of Power Semiconductors (450V GaN, Hard Switching)
- 50V Voltage Source for Semicond. Voltage Stress Reduction
- Low-Freq. CM AC Output Component

- Alternate Switching of Full-Bridge Legs
- Input Cap. of Full-Bridge Used for Power Pulsation Buffering

- 256 W/in³ (400 W/in³ Claimed) / 1MHz
- Multi-Airgap Toroidal Inductors (3F46, C_p≈1.5pF)
- Bare GaN Dies Directly Attached to Pin-Fin Heatsink
- High Speed Fan (Mini Drone Motor & Propeller)
Category I: 300 – 400 W/in³ (1 Team)

- “Over the Edge”
- Hand-Wound Overstressed Electrolytic Capacitors (210uF (?)/400V)
- No Voltage Margin of Power Semiconductors (450V GaN, Hard Switching)
- 50V Voltage Source for Semicond. Voltage Stress Reduction

- Alternate Switching of Full-Bridge Legs
- Input Cap. of Full-Bridge Used for Power Pulsation Buffering

- 256 W/in³ (400 W/in³ Claimed) / 1MHz
- Multi-Airgap Toroidal Inductors (3F46, C_p≈1.5pF)
- Bare Dies Directly Attached to Pin-Fin Heatsink
- High Speed Fan (Mini Drone Motor & Propeller)
Category II: 200 – 300 W/in$^3$ (4 Teams) – Example #1

- "At the Edge"
- High Complexity
- 7-Level Flying Capacitor Converter
- Series-Stacked Active Power Buffer

- 216 W/in$^3$
- 100V GaN
- Integrated Switching Cell
- 720kHz Eff. Sw. Freq. (7 x 120kHz)
Category II: 200 – 300 W/in$^3$ (4 Teams) – Example #2

- “At the Edge”
- Very Well Engineered Assembly (e.g. 3D-Printed Heatsink w. Integr. Fans, 1 PCB Board, etc.)
- No Low-Frequ. Common-Mode AC Output Component

- 201W / in$^3$
- Multi-Airgap (8 Gaps) Inductors
- 900V SiC @ 140kHz (PWM, Soft Sw. Around $i=0$ & Hard Switching)
- Buck-Type Active DC-Side Power Pulsation Filter / Ceramic Capacitors (X6S)
Category III: 100 – 200 W/in³ (8 Teams) – Example

- “Advanced Industrial”
- Sophisticated 3D Sandwich Assembly incl. Cu Honeycomb Heatsink
- Shielded Multi-Stage EMI Filter @ DC Input and AC Output
- No Low-Frequ. Common-Mode AC Output Component

- 143 W/in³
- GaN @ ZVS (35kHz...240kHz)
- 2 x Interleaving for Full-Bridge Legs
- Buck-Type DC-Side Active Power Pulsation Filter (<150μF)
Category III: 100 – 200 W/in³ (8 Teams) – Example

- “Advanced Industrial”
- Sophisticated 3D Sandwich Assembly incl. Cu Honeycomb Heatsink
- Shielded Multi-Stage EMI Filter @ DC Input and AC Output
- No Low-Freq. Common-Mode AC Output Component

143 W/in³
- GaN @ ZVS (35kHz...240kHz)
- 2 x Interleaving for Full-Bridge Legs
- Buck-Type DC-Side Active Power Pulsation Filter (<150μF)
Category IV: 50 – 100 W/in³ (1 Team)

- “Industrial”
- $400V_{\text{max}}$ Full-Bridge Input Voltage
- DC-Link Cap. Used as Power Pulsation Buffer (470uF)
- GaN Transistors / SiC Diodes (400kHz DC/DC, 60kHz DC/AC)
- Multi-Stage EMI Filter @ AC Output and $L_{\text{CM}} +$ Feed-Trough $C_{\text{CM}}$ @ DC Inp. (Not Shown)

- $\approx 70$ W/ in³
- 98% CEC (Weighted) Efficiency
- 4.4% DC Input Current Ripple
- 54°C Surface Temp. / Cooling with 10 Mirco-Fans
Competition
Conclusions

Key Technologies
Power Density Limit
Google Little Box Challenge Summary

- **Overall**
  - Engineering “Jewels”
  - No (Fundamentally) New Approach / Topology
  - Passives & 3D-Packaging are Finally Defining the Power Density
  - Careful Heat Management (Adv. Heat Sink, Heat Distrib., 2-Side Integr. Cooling, etc.)
  - Careful Mechanical Design (3D-CAD, Single PCB, Avoid Connectors, etc.)
  - Clear Power Density / Efficiency Trade-Off

- **200W/in³ (12kW/dm³) Achievable**
  - $f_s < 150$kHz (Constant)
  - SiC (Not GaN)
  - ZVS (Partial, i.e. Around $i=0$)
  - Full-Bridge Output Stage
  - Active Power Pulsation Buffer (Buck-Type, X6S Cap.)
  - Conv. EMI Filter Structure
  - Multi-Airgap Litz Wire Inductors
  - DSP Only (No FPGA)

---

100+ Teams
3 Members / Team, 1 Year
300 Man-Years
3300 USD / Man-Year
Analysis of Advanced Concepts & Technologies

X6S Capacitors
Series Power Pulsation Buffer
Optimal Frequency Modulation
Flying Cap. Converter Topology
Autotrafo-Based Inverter
Eff. Optimal Freq. / Current-Ampl. Modulation (1)

- **TCM** -- Enables ZVS but Suffers From Large Current Ripple & Wide Frequency Variation
- **PWM** -- Const. Sw. Frequency but Hard Switching Around AC Current Maximum

- Optimal Combination of TCM and PWM → Optim. Freq. / Curr. Ripple Variation Over Mains Period
- Experimental Determination of Loss-Opt. Sw. Frequency $f_{OFM}$ Considering DC/DC Conv. Stage
- DC/AC Properties Calculated Assuming Corresponding Local DC/DC Operation

- Loss-Optimal Local Sw. Freq. $f_{OFM}$ for Given $V_{DC}$ & Local Avg. Value of $i_L$ & Local Outp. Cap. Voltage $v_{CO}$
Eff. Optimal Freq. / Current-Ampl. Modulation (2)

- Calculated Optimal Sw. Freq. & Power Loss as Function of the Position in a Mains Half Cycle
- Comparison with 140 kHz Const. Frequency PWM

- Higher Average Switching Frequency @ Light Loads
- Reduction of $f_{sw}$ Around Peak of Mains Voltage (for Ohmic Load) in Order to Sustain ZVS

- Resulting Inductor Current Envelope for Different Output Power Levels

![Graph showing inductor current envelope for different output power levels](image)

- Higher Average Switching Frequency @ Light Loads
- Reduction of $f_{sw}$ Around Peak of Mains Voltage (for Ohmic Load) in Order to Sustain ZVS
CeraLink / X6S Large-Signal Analysis (1)

- 2.2 µF/450V Class II X6S MLCC (TDKs) Features Highest Energy Density
- Performance Comparison with Novel CeraLink Capacitor

- Experimental Setup for Generation of DC Bias & Superimposed AC Voltage

- PPB Design Optimiz. Requires Large-Signal Capacitance and Power Loss Data in All Operating Points
CeraLink / X6S Large-Signal Analysis (2)

- Variation of DC Bias and Superimposed AC Voltage @ 60°C Operating Temp.

≠ Designed Op. Point

EPCOS/TDK
CeraLink 2µF, 600V

TDK Class II
X6S MLCC 2.2µF, 450V

■ PPB Design Optimiz. Requires Large-Signal Capacitance and Power Loss Data in All Operating Points
Power Pulsation Buffer – Partial-Power Approach (1)

- Performance Comparison of Full-Power and Partial-Power Power Pulsation Buffer (PPB) Concepts
- Capacitor Volumes are Incl. Heatsink Vol. for Loss Dissipation ($CSPI_{eff} = 25 \text{ W/(dm}^3 . \text{K)}$)

(i) Buck-Type
(ii) Boost-Type
(iii) Partial-Power Series-Stacked
(iv) Partial-Power Series-Connected

Buck-Type PPB Realized with 2.2μF/450 V X6S MLCC Features Smallest Cap. Volume

*Pilawa
** Schneider Electric
Power Pulsation Buffer – Partial-Power Approach (2)

- Performance Comparison of Full-Power and Partial-Power Power Pulsation Buffer (PPB) Concepts
- Partial-Power Concepts Feature Higher Efficiency Especially @ Light Load

- Peak Efficiency of 99.75% Reached with Series-Connected PPB @ 600 Watt
- Part-Load Efficiency of Buck-Type PPB Expected to be Higher with PWM

Buck-Type with CeraLink
Vol. = 76.6 cm³
η = 98.7 %

Series-Conn. Partial-Power
Vol. = 57.31 cm³
η = 99.5 %

Series-Stacked Partial-Power*
Vol. = 80 cm³
η = 98.9 %

* Pilawa
Performance of Series-Type Partial-Power PPB (1)

- Stationary Operation @ Rated Power of 2 kW

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>Input Voltage, $v_i$</td>
<td>10 V/div</td>
</tr>
<tr>
<td>Filter Voltage, $v_f$</td>
<td>20 V/div</td>
</tr>
<tr>
<td>Input Current, $i_i$</td>
<td>5 A/div</td>
</tr>
<tr>
<td>Pulsating Current, $i_o$</td>
<td>5 A/div</td>
</tr>
<tr>
<td>Buffer Voltage, $v_{buf}$</td>
<td>20 V/div</td>
</tr>
<tr>
<td>DC-Link Voltage, $v_{dc}$</td>
<td>50 V/div</td>
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<tr>
<td>Filter Voltage, $v_f$</td>
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<tr>
<td>Filter Current, $i_f$</td>
<td>2 A/div</td>
</tr>
</tbody>
</table>
Performance of Series-Type Partial-Power PPB (2)

- **Buffer Voltage,** $v_{buf}$ (20V/div)
- **DC-Link Voltage,** $v_{dc}$ (200V/div)
- **Filter Voltage,** $v_f$ (20V/div)
- **Filter Current,** $i_f$ (5A/div)

- **Startup of the Converter**
- **Load Step 2kW → 1kW**
**Sw. Frequ. Auto-Transformer Approach**

- Multi-Tap Switching Frequ. Multi-Air-Gap Autotransformer Realizing a Multi-Tap Voltage Divider
- Tap Switch & Series Active Filter for Gen. of Sinus. Output Voltage from Multi-Step Waveform
- Low-Voltage Power Semiconductors

- Concept Presented by “Cambridge Active Magnetics” @ Final
- Power Density Unclear (Presentation @ Final: 159W/in³, 290W/in³ Shown as Target in Report)
- Efficiency Unclear (10W of Losses @ 2kW in Documentation, Equal to Only $R = 150m\Omega$ in Total?)
Multi-Tapped Sw. Frequ. Auto-Transformer (1)

- Multi-Stage Multi-Level Inverter
- DC-AC-DC
  - (I) Resonant ZVS Half-Bridge
  - (II) Multi-Tapped Auto-Transformer
  - (III) Voltage-Doubler Rectifier
- DC-AC
  - (IV) PWM Tap-Selector
  - (V) Output Filter
  - (VI) Full-Bridge Unfolder

Topology & Operation Different to Approach Presented by “Cambridge Active Magnetics”
Multi-Tapped Sw. Freq. Auto-Transformer (2)

- $\eta_\rho$-Pareto Optimization of the Converter System

- Efficiency: 97.7% @ 2kW (97.4% CEC)
- Power Density: 120W/in^3 (7.4kW/dm^3)

- Efficiency of Resonant Multi-Level DC/DC Stage > 99%
Multi-Level Converter Approach

- Multi-Level PWM Output Voltage - Minimizes Ind. Volume
- Flying Cap. Conv. – No Splitting of DC Inp. Voltage Required
- Low-Voltage GaN or Si Power Semiconductors


FIG. 1

Full-Bridge Topology or DC/AC Buck-Type + Unfolder

FIG. 4
Multi-Level Conv. Approach – Flying Cap. Conv. (1)

- 5 Voltage Levels
- 320 kHz Single-Cell Sw. Frequency
- 12μF Flying Capacitors
- Improved Phase-Shift PWM
Multi-Level Conv. Approach – Flying Cap. Conv. (2)

- Analysis of Symmetry of FC Voltages During Start-Up, Shut-Down, Stand-By, Output S.C. Missing
- Inverter & Rectifier Operation

(I) Rectifier Operation – No Load, PWM Disabled @ $t=0$, FCs Discharging over Balance Resistors, Voltage Symmetry Maintained, PWM Re-Enabled @ $t=150\text{ms}$, $U_{\text{out}}$ Control @ $t=300\text{ms}$

(II) Rectifier Operation Under Load, Loss of Mains or PWM Disabled (Load Still Present), FCs Discharging over Diodes – Voltage Unbalance, Bridge Leg Re-Enabled @ $t=150\text{ms}$, Dedicated Control Procedure Req. for Regaining FC Volt. Symmetry

(III) Inverter Operation – Start-Up from DC-Side, Pre-Charge Resistors Bridged @ $t=500\text{ms}$

(I) FC Voltages

(II) Switch Voltages

(III) FC Voltages

(II) Switch Voltages
Optimization of Little-Box 1.0

η-‐Pareto Front
TCM vs. Large Ripple PMW
The Ideal Switch is Not Enough (!)
Design Space Diversity
Multi-Objective Optimization

- Detailed System Models - Power Buffer/Output Stage/EMI Filter
- Detailed Multi-Domain Component Models (incl. GaN & SiC)
- Consideration of Very Large # of Degrees of Freedom

Pareto Optimization Shows Trade-Off Between Power Density and Efficiency
Little Box 1.0 $\eta$-Performance Limits

- Multi-Objective Optimization of Little-Box 1.0 (incl. CeraLink $\rightarrow$ X6S)
- Absolute Performance Limits (I) - DSP/FPGA Power Consumption
  (II) - Heatsink Volume @ $(1-\eta)$

Further Performance Improvement for Triangular Current Mode (TCM) $\rightarrow$ PWM
Power Pulsation Buffer (PPB) vs. Electrolytic Capacitor (1)

- Lower Volume Comp. to Electrolytic Caps only for $\Delta V/V < 6\%$
- No Efficiency Benefit of PPB (!)

Electrolytics Favorable for High Efficiency @ Moderate Power Density
Electrolytics Show Lower Vol. & Lower Losses if Large $\Delta V/V$ is Acceptable (e.g. for PFC Rectifiers)
Power Pulsation Buffer (PPB) vs. Electrolytic Capacitor (2)

- Analysis for Google Little Box Challenge Specification \( \Delta V/V < 3\% \)
- Efficiency Benefit of PPB only for \( \rho > 9kW/dm^3 \)

- Electrolytics Favorable for High Efficiency @ Moderate Power Density \( (\Delta \eta = +0.5\%) \)
- Electrolytics Show Lower Vol. & Lower Losses if Large \( \Delta V/V \) is Acceptable (e.g. for PFC Rectifiers)
Little Box 1.0 -- TCM → PWM

- Very High Sw. Frequency $f_S$ of TCM Around Current Zero Crossings
- Efficiency Reduction due to Residual TCM Sw. Losses & Gate Drive Losses Reduction
- Wide $f_S$ -Variation Represents Adv. & Disadvantage for EMI Filter Design

- PWM -- Const. Sw. Frequency & Lower Conduction Losses
- PWM @ Large Current Rippel -- ZVS in Wide Intervals
Little Box 1.0 -- TCM → PWM

- Optimization for GaN GIT & No Interleaving
- Resulting Opt. Inductance of Output Inductor $L=10 \mu\text{H (TCM)}, \ L=30 \mu\text{H (PWM@140 kHz)}$

$\rho=11.9\text{kW/dm}^3 \ \ \ \ \eta=97.4\%$

$\rho=12.5\text{kW/dm}^3 \ \ \ \ \eta=97.4\%$

- PWM vs. TCM → Slightly Higher Max. Power Density @ Same Efficiency
The Ideal Switch is Not Enough (!)
Little Box 1.0 @ Ideal Switches

- Multi-Objective Optimization of Little-Box 1.0 (X6S Power Pulsation Buffer)
- Step-by-Step Idealization of the Power Transistors
- Ideal Switches: $k_c = 0$ (Zero Cond. Losses); $k_s = 0$ (Zero Sw. Losses)

@ TCM

Analysis of Improvement of Efficiency @ Given Power Density & Maximum Power Density
Little Box 1.0 @ Ideal Switches -- TCM

- Δη = +0.5% @ ρ = 6kW/dm³ – Main Benefit from Zero Conduction Losses (kć=0)
- Δη = +1.5% @ ρ = 12kW/dm³ – Add. Benefit from Zero Sw. Losses (kś=kć=0)

- Minor Improvement of Max. Power Density - ρ= 12kW/dm³ → 15kW/dm³ (PPB Cap. & Inductors)
- Finite Remaining Volume & Losses → The Ideal Switch is Not Enough (!)
Little Box 1.0 @ Ideal Switches -- PWM

- $\Delta \eta = +1.0\%$ @ $\rho = 6\text{kW/dm}^3$ – Benefit from Zero Cond. & Zero Sw. Losses ($k_s = k_c = 0$)
- $\Delta \eta = +1.75\%$ @ $\rho = 12\text{kW/dm}^3$ – Benefit from Zero Cond. & Zero Sw. Losses ($k_s = k_c = 0$)

- 50% Improvement of Max. Power Density - $\rho = 12\text{kW/dm}^3 \rightarrow 19\text{kW/dm}^3$ (PPB & Inductors)
- Finite Remaining Volume & Losses → The Ideal Switch is Not Enough (!)
Little Box 1.0 @ Ideal Switches -- PWM

- L & \( f_s \) are Independent Variables (Dependent for TCM)
- Large Design Space Diversity (Mutual Compensation of HF and LF Loss Contributions)

\( \rho = 6\text{kW/dm}^3 \)
\( \eta \approx 99.35\% \)

\( L = 50\mu\text{H} \)
\( f_s = 500\text{kHz} \) or \( 900\text{kHz} \)
Little Box 2.0

DC/AC Converter + Unfolder
PWM vs. TCM incl. Interleaving
ηP-Pareto Limits for Non-Ideal Switches
Preliminary Exp. Results
Final 3D-CAD

250 W/in³
**Little Box 2.0 – New Converter Topology (1)**

- Alternative Converter Topology → Only Single HF Bridge Leg + 60Hz-Unfolder
- DC/AC - Buck Converter + Full-Bridge Unfolder OR HF Half-Bridge & Half-Bridge Unfolder

- $v_{C0}$ Easy to Generate/Control
- Higher Conduction Losses Due to FB-Unfolder
- Lower CM-Noise (DC & n x 120Hz-Comp.)
- $C_{CM}=700\text{nF}$ Allowed for 50mA Gnd Current

- $v_{AC1}$ More Difficult to Generate/Control
- Lower Conduction Losses
- Higher CM-Noise (DC and n x 120Hz-Comp.)
- $C_{CM}=150\text{nF}$ Allowed for 50mA Gnd Current
Little Box 2.0 – New Converter Topology (2)

- Alternative Converter Topology - DC/AC - Buck Converter + Unfolder
- 60Hz-Unfolder (Temporary PWM for Ensuring Continuous Current Control)
- TCM or PWM of DC/AC - Buck-Converter

Full Optimization of All Converter Options for Real Switches / X6S Power Pulsation Buffer
**Little Box 2.0 – Multi-Objective Optimization**

- DC | AC | Buck Converter (Single Bridge Leg) + Unfolder & PWM Shows Best Performance
- Full-Bridge Would Employ 2 Switching Bridge Legs - Larger Volume & Losses
- Interleaving Not Advantageous – Lower Heatsink Vol. but Larger Total Vol. of Switches and Inductors

![Graph showing efficiency vs. power density](image)

- $\rho = 250\text{W/in}^3 (15\text{kW/dm}^3) @ \eta = 98\%$ Efficiency Achievable for Full Optimization

---

**4D-Interleaving Considered for TCM**

![Diagram showing interlacing currents](image)
**Little Box 2.0 – Volume & Loss Distribution @ (P1...5)**

- **Volume:** Dominated by Heatsink & PPB (Power Pulsation Buffer)
- **Losses:** for Buck+Unfolder Dominated by Switches & PPB

---

**ETH zürich**
Experimental Results

Control Block Diagram
Output Voltage/Input Current Quality
Efficiency
Little Box 2.0 – Control Structure

- Each Stage (Buck & Unfolder) Controlled with Cascaded Current and Voltage Loop
- Without Switching of Unfolder Control Like for Conventional Boost PFC Rectifier
Analysis of DC/AC - Buck Converter & Unfolder

- Voltage Zero Crossing Behavior With (Right) & Without (Left) Switching of Unfolder

- Output Voltage (200 V/div)
- Output Current (10 A/div)
- Buck Inductor Current (10 A/div)
- Unfolder Output Voltage (200 V/div)

- Output Voltage & Current Fully Controlled Around Voltage Zero Crossings
Little Box 2.0 – Measured Waveforms

- DC/|AC| Buck-Stage Output Voltage & Inductor Current

- Resistive Load
- Inductive Load
- Capacitive Load
Little Box 2.0 – Preliminary Efficiency Measurements

- Performance of First DC/AC - Buck Converter + Unfolder Prototype
- PWM Operation
- Without Power Pulsation Buffer

98% for Res. Load Achievable if Cond. Losses of PCB (Copper Cross Sect.) & Unfolder ($R_{ds,on}$) are Red.
3D-CAD Construction of the Final System

250 W/in\(^3\)
**Little Box 2.0 – Final Mechanical Construction (1)**

- **Output Filter**
- **PPB Capacitor**

- 60 mm x 50 mm x 45 mm = 135 cm³ (8.2 in³) → 14.8 kW/dm³ (243 W/in³)
Little Box 2.0 – Final Mechanical Construction (2)

- Output Filter
- PPB Capacitor
- Heat Sink + Fans

- 60 mm x 50 mm x 45 mm = 135 cm³ (8.2 in³) \(\rightarrow\) 14.8 kW/dm³ (243 W/in³)
Little Box 2.0 – Final Mechanical Construction (3)

- 60 mm x 50 mm x 45 mm = 135 cm³ (8.2in³) → 14.8 kW/dm³ (243 W/in³)

Inductors (Buck-Stage & Unfolder)
Output Filter

Heat Sink + Fans
PPB Capacitor
Little Box 2.0 – Final Mechanical Construction (4)

- Power Board
- Inductors (Buck-Stage & Unfolder)
- Output Filter
- Heat Sink + Fans
- PPB Capacitor

- 60 mm x 50 mm x 45 mm = 135 cm³ (8.2in³) → 14.8 kW/dm³ (243 W/in³)
Little Box 2.0 – Final Mechanical Construction (5)

Control Board
Power Board
Inductors (Buck-Stage & Unfolder)
Output Filter

Heat Sink + Fans
PPB Capacitor

60 mm x 50 mm x 45 mm = 135 cm³ (8.2in³) → 14.8 kW/dm³ (243 W/in³)
Little Box 3.0

5...10MHz Switching Frequency
Performance of Low-μ HF Magnetic Materials
Digital Control
Magnetics Operation Frequency Limit (1)

- Serious Limitation of Operating Frequency by HF Losses
  - Core Losses (incr. @ High Frequ. & High Operating Temp.)
  - Temp. Dependent Lifetime of the Core
  - Skin-Effect Losses
  - Proximity Effect Losses

Source: Prof. Albach, 2011

Adm. Flux Density for given Loss Density

Skin-Factor $F_s$ for Litz Wires with $N$ Strands

$F_s = r / \sqrt{N}$
Magneetics Operating Frequency Limit (2)

- (Modified) “Core Material Perform. Factor” $F_{0.75} = B_{pk} f^{0.75}$ Defined for Def. Core Loss
- Performance Factor prop. to VA Handling Capability – Min. Vol. @ Max. of $F_{0.75}$
- Little Benefit of Increased $f_S$ for Conv. Ferrites in 200kHz…2MHz
- Peak Performance of Low-µ HF Core Materials @ 5-10 MHz

Source: Hanson et al. ECCE 2015

$\mu_r = 40$

All Inductors w. $Q=200$

$f_S$ in the MHz-Range Results in Very Low EMI Filter Volume
TCM Digital Control / Timing Challenges @ $f_s > 1\text{MHz}$

- Dead Times Required for Res. Transition (ZVS)
- $i = 0$ Detection Time Delay
- Signal Isolator & Gate Drive Time Delays
- Large Reactive Power for ZVS
- Rel. Large Cond. Losses @ Low Output Current

- New High Speed / Low-Volume / Low-Loss $i=0$ Detection Concepts Required
- Integrated Gate Drive w. (Hysteresis) Current Control Functionality Required
Performance Limits / Future Requirements

- New Integr. Control Circuits and i=0 Detection for Sw. Frequency >1MHz
- Integrated Gate Drivers & Switching Cells
- High Frequency Low Loss Magnetic Materials
- High Bandwidth Low-Volume Current Sensors
- Low Loss Ceramic Capacitors Tolerating Large AC Ripple
- Passives w. Integr. Heat Management and Sensors
- 3D Packaging

- 220...250W/in³ for Two-Level Bridge Leg + Unfolder
- 250...300W/in³ for Highly Integrated Multi-Level Approach
- Isol. Distance Requirements Difficult to Fulfill
- Fulfilling Industrial Inp. Overvoltage Requirem. would Signific. Reduce Power Density

- Low Frequency (20kHz...120kHz) SiC vs. HF (200kHz...1.2MHz) GaN
- Multi-Cell Concepts for LV Si (or GaN) vs. Two-Level SiC (or GaN)

- New U-I-Probes Required for Ultra-Compact Conv. R&D
- Specific Systems for Testing → Devices Equipped with Integr. Measurement Functions
- Convergence of Sim. & Measurem. Tools → Next Gen. Oscilloscope
- New Multi-Obj. Multi-Domain Simulation/Optim. Tools
References

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Other Finalists
Non-Finalists
General
Publications of ETH Zurich


► Publications of Other Finalists


► General Publications


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Johann W. Kolar (F’10) received his Ph.D. degree (summa cum laude) from the Vienna University of Technology, Austria. He is currently a Full Professor and the Head of the Power Electronic Systems Laboratory at the Swiss Federal Institute of Technology (ETH) Zurich. He has proposed numerous novel PWM converter topologies, and modulation and control concepts and has supervised over 60 Ph.D. students. He has published over 750 scientific papers in international journals and conference proceedings, 3 book chapters, and has filed more than 140 patents. He has presented over 20 educational seminars at leading international conferences, has served as IEEE PELS Distinguished Lecturer from 2012 through 2016, and has received 25 IEEE Transactions and Conference Prize Paper Awards, the 2014 IEEE Power Electronics Society R. David Middlebrook Achievement Award, the 2016 IEEE William E. Newell Power Electronics Award, the 2016 IEEE PEMC Council Award, and the ETH Zurich Golden Owl Award for excellence in teaching. He has initiated and/or is the founder of 4 ETH Spin-off companies. The focus of his current research is on ultra-compact and ultra-efficient SiC and GaN converter systems, wireless power transfer, Solid-State Transformers, Power Supplies on Chip, as well as ultra-high speed and ultra-light weight drives, bearingless motors, and energy harvesting.

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Thank You!