Comprehensive Evaluation of Three-Phase AC-AC PWM Converter Systems

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Outline

► Review of AC-DC-AC Converters
► Derivation of Basic MC Topologies

► MC Dimensioning
► Extended MC Topologies

► Methodology for Converter Comparisons
► Comparative Evaluation of AC-AC Converters

► Multi-Domain Simulator Demonstration (GECKO)  GeckoCIRCUITS
► Conclusions / Questions / Discussion
Classification of Three-Phase AC-AC Converters

- Converters with DC-link
- Hybrid Converters
- Indirect / Direct Matrix Converters
DC-link AC-AC Converter Topologies

- **V-BBC**

- **I-BBC**

\[ P = \frac{3}{2} U_1 \cdot I_1 \cos \Phi_1 \]
Symmetric Three-Phase Mains

**Phase Voltages**

\[
\begin{align*}
    u_a &= \hat{U}_1 \cos(\omega_1 t) \\
    u_b &= \hat{U}_1 \cos(\omega_1 (t - \frac{T}{3})) \\
    u_c &= \hat{U}_1 \cos(\omega_1 (t + \frac{T}{3}))
\end{align*}
\]

**Phase Currents**

\[
\begin{align*}
    i_a &= \hat{I}_1 \cos(\omega_1 t - \Phi_1) \\
    i_b &= \hat{I}_1 \cos(\omega_1 (t - \frac{T}{3}) - \Phi_1) \\
    i_c &= \hat{I}_1 \cos(\omega_1 (t + \frac{T}{3}) - \Phi_1)
\end{align*}
\]

**Instantaneous Power**

\[
p(t) = u_a i_a + u_b i_b + u_c i_c = \frac{P}{3} (1 + \cos 2\omega_1 t) + \frac{Q}{3} \sin 2\omega_1 t + \frac{P}{3} \left(1 + \cos 2\omega_1 \left(t - \frac{T}{3}\right)\right) + \frac{Q}{3} \sin 2\omega_1 \left(t - \frac{T}{3}\right) + \frac{P}{3} \left(1 + \cos 2\omega_1 \left(t + \frac{T}{3}\right)\right) + \frac{Q}{3} \sin 2\omega_1 \left(t + \frac{T}{3}\right)
\]

\[
\begin{align*}
    P &= \frac{3}{2} \hat{U}_1 \cdot \hat{I}_1 \cos \Phi_1 \\
    Q &= \frac{3}{2} \hat{U}_1 \cdot \hat{I}_1 \sin \Phi_1
\end{align*}
\]

\[
p(t) = \frac{P}{3} (1 + \cos 2\omega_1 t) + \frac{P}{3} \left(1 + \cos 2\omega_1 \left(t - \frac{T}{3}\right)\right) + \frac{P}{3} \left(1 + \cos 2\omega_1 \left(t + \frac{T}{3}\right)\right) = \frac{3P}{3} = P
\]
All-SiC JFET I-BBC Prototype

- $P_{\text{out}} = 2.9 \text{ kVA}$
- $f_S = 200 \text{ kHz}$
- 2.4 kVA / liter (42 W/in$^3$)
- 230 x 80 x 65 mm$^3$

![Image of the prototype]

$U_{\text{out}} = 400 \text{ V}$

$U_{\text{in}} = 400 \text{ V}$

$I_{\text{in}} = 4.3 \text{ A}$

DC Link Inductor 320 $\mu$H/6 A
Basic Matrix Converter Topologies

\[
\frac{Q}{3} \left( \sin 2\omega_1 t + \sin 2\omega_1 \left( t - \frac{T}{3} \right) + \sin 2\omega_1 \left( t + \frac{T}{3} \right) \right) \equiv 0
\]
V-BBC

Voltage Space Vectors

Modulation

DC Link Current
VSI Space Vector Modulation (1)

\[ \bar{u}_{2,j} = \frac{2}{3} (u_{A,j} + a u_{B,j} + a^2 u_{C,j}) \]

\[ u_{0,j} = \frac{1}{3} (u_{A,j} + u_{B,j} + u_{C,j}) \]

Output Voltage Reference Value

\[ \bar{u}_2^* = \hat{U}_2^* e^{j \varphi \bar{u}_2^*} = \hat{U}_2^* e^{j \omega_2^* t} \]

\[ 2^3 = 8 \text{ Switching States} \]

- Switching with Interlock Delay

\[ M_2 = \frac{\hat{U}_2^*}{U/2} \]

\[ M_{2,\text{max}} = \frac{2}{\sqrt{3}} \]
VSI Space Vector Modulation (2)

Switching State Sequence

\[ t_\mu = 0 \quad (nnn) - (pnn) - (ppn) - (ppp) \quad t_\mu = T_P/2 \]
\[ (ppp) - (ppn) - (pnn) - (nnn) \quad t_\mu = T_P \quad ... \]

Formation of the Output Voltage

\[ \vec{u}_2 = \frac{1}{T_P} \int_0^{T_P} \vec{u}_{2,j} \, dt_\mu \]
\[ = d_{(pnn)} \cdot \vec{u}_{2,(pnn)} + d_{(ppn)} \cdot \vec{u}_{2,(ppn)} \]
\[ = d_{(pnn)} \cdot \frac{2}{3} U + d_{(ppn)} \cdot \frac{2}{3} U e^{j\pi/3} \]
\[ = \vec{u}_2^* \]

Relative On-times

\[ d_{(ppn)} = \frac{\sqrt{3}}{2} M_2 \sin \left( \frac{\varphi_{\vec{u}_2^*}}{3} \right) \]
\[ d_{(pnn)} = \frac{\sqrt{3}}{2} M_2 \sin \left( \frac{\pi}{3} - \varphi_{\vec{u}_2^*} \right) \]
VSI Space Vector Modulation (3)

Freewheeling On-time

\[ d_{(nnn)} + d_{(ppp)} = 1 - (d_{(ppn)} + d_{(pnn)}) \]

Discontinuous Modulation

\[
\begin{align*}
| t_\mu &= 0 (pnn) - (ppn) - (ppp) | \\
| t_\mu &= T_P/2 (ppp) - (ppn) - (pnn) | \\
| t_\mu &= T_P/2 (nnn) - (pnn) - (ppn) | \\
| t_\mu &= T_P \ldots
\end{align*}
\]

Space Vector Orientation

\[
\frac{d_{(ppn)}}{d_{(pnn)}} = \frac{\sin(\varphi_{\bar{u}_2^*})}{\sin\left(\frac{\pi}{3} - \varphi_{\bar{u}_2^*}\right)}
\]

Modulation Limit

\[
M_{2,\text{max}} = \frac{\hat{U}_{2,\text{max}}}{U/2} = \frac{2}{\sqrt{3}}
\]
VSI Space Vector Modulation (4)

**DC-link Current Shape**

\[ i_j = i_{2,j} \]

\[ i_{(nnn)} = 0 \]
\[ i_{(nnp)} = i_C \]
\[ i_{(npp)} = i_B \]
\[ i_{(npp)} = i_B + i_C = -i_A \]
\[ i_{(ppn)} = i_A \]
\[ i_{(ppp)} = i_A + i_C = -i_B \]
\[ i_{(ppp)} = 0 \]

**Local Average Value**

\[ \bar{i} = \frac{1}{T_P} \int_0^{T_P} i_j \, dt \]
\[ \bar{i} = -i_C d_{(ppn)} + i_A d_{(pnn)} \]
VSI Space Vector Modulation (5)

Local DC-link Current Shape

\[ \bar{i} = I = \frac{3}{4} M_2 \hat{I}_2 \cos \Phi_2 \]
VSI DC-link Current Waveform

Influence of Output Voltage Phase Displacement $\Phi_2$ on DC-link Current Waveform

\[ \vec{i} = I \frac{3}{4} M_2 \hat{I}_2 \cos \Phi_2 \]

$M_2 = \frac{2}{\sqrt{3}}$
VSI Functional Equivalent Circuit

**Voltage Conversion**

\[ M_2 = \frac{\hat{U}_2^*}{U/2} \]

\[ \bar{u} = U \]

\[ \bar{i} = \frac{3}{4} \frac{M_2 \hat{i}_2 \cos \Phi_2}{I} \]

**Current Conversion**
I-BBC

Current Space Vectors
Modulation
DC Link Voltage
CSR Commutation & Equivalent Circuit

Forced Commutation

Natural Commutation

Equivalent Circuit

- $3^2 = 9$ Switching States
- Overlapping Switching
CSR Space Vector Modulation (1)

\[ \bar{i}_k = \frac{2}{3} \left( i_{a,k} + a i_{b,k} + a^2 i_{c,k} \right) \quad a = e^{j2\pi/3} \]

Input Current Reference Value

\[ \bar{i}_{1}^* = \tilde{i}_1 e^{j\phi_{1}} = \tilde{i}_1 e^{j(\omega_1 t - \Phi_1^*)} \]

\[ M_1 = \frac{\tilde{i}_1^*}{\tilde{i}_1} \]

\[ M_{1,max} = 1 \]

\[ i_1, (bc) \]

\[ i_1, (ba) \]

\[ i_1, (bb) \]

\[ i_1, (aa) \]

\[ i_1, (cc) \]

\[ i_1, (ca) \]

\[ i_1, (ab) \]

\[ i_1, (cb) \]
CSR Space Vector Modulation (2)

\[ |i_{1,k}| = i_{1,k} = \frac{2}{\sqrt{3}} \cdot I \]

\[ \bar{i}_1 = \frac{1}{T_P} \int_0^{T_P} \bar{i}_{1,k} \, dt = d_{(ac)} \cdot \bar{i}_{1,(ac)} + d_{(ab)} \cdot \bar{i}_{1,(ab)} = \bar{i}_{1}^* \]

**Formation of the Input Current**

**Relative On-times**

\[ d_{(ac)} = M_1 \sin \left( \frac{\pi}{6} + \varphi_{i_1}^* \right) \]

\[ d_{(ab)} = M_1 \sin \left( \frac{\pi}{6} - \varphi_{i_1}^* \right) \]

\[ d_{(aa)} = 1 - (d_{(ac)} + d_{(ab)}) \]

**Space Vector Orientation**

\[ \varphi_{i_1}^* = \varphi_{u_1} - \varphi_{i_1}^* \]

\[ \frac{d_{(ac)}}{d_{(ab)}} = \frac{\sin \left( \frac{\pi}{6} + \varphi_{i_1}^* \right)}{\sin \left( \frac{\pi}{6} - \varphi_{i_1}^* \right)} \]
CSR Space Vector Modulation (3)

Switching State Sequence

\[ \begin{array}{c|c|c|c}
\mu & (ab) \rightarrow (ac) \rightarrow (aa) & \mu = T_P/2 & (aa) \rightarrow (ac) \rightarrow (ab) & \mu = T_P \\
\hline
0 & (ab) \rightarrow (ac) \rightarrow (aa) & \mu = T_P/2 & (aa) \rightarrow (ac) \rightarrow (ab) & \mu = T_P \\
\end{array} \]

DC-link Voltage Formation

\[
\begin{align*}
\bar{u} &= u_{ab}d_{ab} + u_{ac}d_{ac} \\
\end{align*}
\]
CSR Space Vector Modulation (4)

Local DC-link Voltage Shape

\[ \ddot{u} = \frac{3}{2} M_1 \dot{U}_1 \cos \Phi_1^* \]
**CSR DC-link Voltage Waveform**

**Influence of Input Current Phase Displacement \( \Phi_1 \) on DC-link Voltage Waveform**

\[
\begin{align*}
\frac{1}{\sqrt{3}} u_{(ac)} &= \frac{1}{\sqrt{3}} u_{ac} \\
\frac{1}{\sqrt{3}} u_{(ab)} &= \frac{1}{\sqrt{3}} u_{ab}
\end{align*}
\]

\[
M_1 = \frac{j_1}{I}
\]

\[
\bar{u} = \frac{3}{2} M_1 \dot{U}_1 \cos \Phi_1^*
\]
CSR Functional Equivalent Circuit

Voltage Conversion

\[
\bar{u} = \frac{3}{2} M_1 \hat{U}_1 \cos \Phi_1^* 
\]

Current Conversion

\[
M_1 = \frac{i}{I}
\]
Derivation of MC Topologies

Fundamental Frequency Front End

$F^3E$
Classification of Three-Phase AC-AC Converters

- Converter without DC-link Capacitor
F³E Topology / Mains Behavior

\[ u_{\text{min}} = \frac{3}{2} \hat{U}_1 \]

\[ \hat{U}_2^+ < \frac{\sqrt{3}}{2} \cdot \hat{U}_1 \approx 0.86 \hat{U}_1 \]

P. Ziogas [12]
T. Lipo [13, 18, 20]
B. Piepenbreier [15]
**F³E Topology Extension**

- **Sinusoidal Mains Current**

Y. Okuma [34]
Indirect Matrix Converter – IMC

Space Vectors
Modulation
Simulation
Experimental Results
Classification of Three-Phase AC-AC Converters

- **Indirect Matrix Converter**
IMC Topology Derivation

► Extension of $F^3$E-Topology
► Bidirectional CSR Mains Interface

J. Holtz [16]
K. Shinohara [17]
IMC Properties

- Positive DC-link Voltage Required
IMC Voltage and Current Space Vectors

\[ \vec{I}_1,\text{(bc)(ppn)} \]
\[ \vec{I}_1,\text{(bc)(nnn)} \]
\[ \vec{I}_1,\text{(bc)(nnn)} \]
\[ i_{\text{(nnn)}} = i_A \]
\[ i_{\text{(nnn)}} = i_C \]
\[ i_{\text{(nnn)}} = -i_A \]

\[ \vec{u}_2,\text{(ac)(ppn)} \]
\[ \vec{u}_2,\text{(ac)(ppn)} \]
\[ \vec{u}_2,\text{(ac)(ppn)} \]
\[ u_{\text{(ac)}} = u_{\text{ac}} \]
\[ u_{\text{(ab)}} = u_{\text{ab}} \]
\[ u_{\text{(bc)}} = u_{\text{bc}} \]
IMC Space Vector Modulation (1)

\[ \vec{u}_1 = \hat{U}_1 e^{j \varphi_{\vec{u}_1}} = \hat{U}_1 e^{j \omega t} \]

\[ \vec{i}_1 = \hat{I}_1 e^{j \varphi_{\vec{i}_1}} \]

\[ \vec{u}_2 = \hat{U}_2^* e^{j \varphi_{\vec{u}_2}} = \hat{U}_2^* e^{j \omega^* t} \]

\[ \vec{i}_2 = \hat{I}_2 e^{j \varphi_{\vec{i}_2}} = \hat{I}_2 e^{j \left( \varphi_{\vec{i}_2} - \Phi_2 \right)} \]
IMC Space Vector Modulation (2)

- Zero Current Commutation
- Zero Voltage Commutation
IMC Zero DC-link Current Commutation (1)

**DC-link Voltage** \( u = u_{ac} \)

**DC-link Current** \( i = i_A \)
IMC Zero DC-link Current Commutation (2)

DC-link Voltage \( u = u_{qc} \)
DC-link Current \( i = -i_C \)
**IMC Zero DC-link Current Commutation (3)**

**DC-link Voltage** \( u = u_{ac} \)

**DC-link Current** \( i = 0 \)
IMC Zero DC-link Current Commutation (4)

**DC-link Voltage**  \[ u = u_{ab} \]

**DC-link Current**  \[ i = 0 \]
IMC Zero DC-link Current Commutation (5)

**DC-link Voltage**  \( u = u_{qb} \)

**DC-link Current**  \( i = -i_C \)
**IMC Zero DC-link Current Commutation** (6)

**DC-link Voltage**  \( u = u_{ab} \)

**DC-link Current**  \( i = i_A \)

![Diagram showing DC-link Voltage and Current](image)
Summary

- **Simple and Robust** Modulation Scheme Independent of Commutation Voltage Polarity or Current Flow Direction
- **Negligible Rectifier Stage Switching Losses** Due to Zero Current Commutation

**IMC Zero DC-link Current Commutation (7)**
Coffee Break!
**IMC Space Vector Modulation (3)**

**Output Voltage Ref. Value**

\[ \vec{u}_2^* = \hat{U}_2^* e^{j \varphi_{\vec{u}_2}} = \hat{U}_2^* e^{j \omega_2^* t} \]

**Input Current Ref. Angle** \( \varphi_{\vec{i}_1}^* \)

\[ \vec{i}_1 = \hat{I}_1 e^{j \varphi_{\vec{i}_1}^*} \quad \varphi_{\vec{i}_1}^* = \varphi_{\vec{u}_1} - \Phi_1^* \]

**Mains Voltage**

\[ \vec{u}_1 = \hat{U}_1 e^{j \varphi_{\vec{u}_1}} = \hat{U}_1 e^{j \omega_1 t} \]

**Load Behavior**

\[ \vec{i}_2 = \hat{I}_2 e^{j \varphi_{\vec{i}_2}} = \hat{I}_2 e^{j (\varphi_{\vec{u}_2}^* - \Phi_2)} \]

**Assumptions**

\( \varphi_{\vec{u}_1} \in \left[ 0, \frac{\pi}{6} \right] \)

\( \varphi_{\vec{u}_2}^* \in \left[ 0, \frac{\pi}{3} \right] \)

\( \varphi_{\vec{i}_1}^* \in \left[ -\frac{\pi}{6}, \frac{\pi}{6} \right] \)

PWM Pattern is Specific for each Combination of Input Current and Output Voltage Sectors
Freewheeling Limited to Output Stage

\[ d_{(ab)} + d_{(ac)} = 1 \]

Input Current Formation

\[ \bar{i}_a = (d_{(ab)} + d_{(ac)}) \bar{i} = \bar{i} \]
\[ \bar{i}_b = -d_{(ab)} \bar{i} \]
\[ \bar{i}_c = -d_{(ac)} \bar{i} \]

Desired Input Current

\[ \bar{i}_a = \hat{I}_1 \cos \frac{\varphi^e_{i_1}}{i_1} \]
\[ \bar{i}_b = \hat{I}_1 \cos \left( \frac{\varphi^e_{i_1}}{i_1} - \frac{2\pi}{3} \right) \]
\[ \bar{i}_c = \hat{I}_1 \cos \left( \frac{\varphi^e_{i_1}}{i_1} + \frac{2\pi}{3} \right) \]

Resulting Rectifier Stage

Relative On-Times

\[ d_{(ab)} = \sin \left( \frac{\pi}{6} - \frac{\varphi^e_{i_1}}{i_1} \right) \]
\[ d_{(ac)} = \sin \left( \frac{\pi}{6} + \frac{\varphi^e_{i_1}}{i_1} \right) \]

Absolute On-Times

\[ \tau_{(ab)} = d_{(ab)} \frac{T_P}{2} \]
\[ \tau_{(ac)} = d_{(ac)} \frac{T_P}{2} \]
Mains Voltage

\[ u_a = \hat{U}_1 \cos \left( \varphi \frac{\pi}{3} \right) \]

\[ u_b = \hat{U}_1 \cos \left( \varphi \frac{\pi}{3} - \frac{2\pi}{3} \right) \]

\[ u_c = \hat{U}_1 \cos \left( \varphi \frac{\pi}{3} + \frac{2\pi}{3} \right) \]

Available DC Link Voltage Values

\[ u_{(ac)} = u_{ac} = u_a - u_c = \sqrt{3} \cdot \hat{U}_1 \cos \left( \varphi \frac{\pi}{6} \right) \]

\[ u_{(ab)} = u_{ab} = u_a - u_b = \sqrt{3} \cdot \hat{U}_1 \cos \left( \varphi \frac{\pi}{6} \right) \]

Select Identical Duty Cycles of Inverter Switching States (100), (110) in \( \tau_{ac} \) and \( \tau_{ab} \) for Maximum Modulation Range

\[ \delta_{(ac)(pnn)} = \frac{\tau_{(ac)(pnn)}}{\tau_{(ac)}} = \delta_{(ab)(pnn)} = \frac{\tau_{(ab)(pnn)}}{\tau_{(ab)}} = \delta_{(pnn)} \]

\[ \delta_{(ac)(ppn)} = \frac{\tau_{(ac)(ppn)}}{\tau_{(ac)}} = \delta_{(ab)(ppn)} = \frac{\tau_{(ab)(ppn)}}{\tau_{(ab)}} = \delta_{(ppn)} \]
Voltage Space Vectors Related to Active Inverter Switching States

\[ \vec{u}_{2,(pnn)} = \frac{2}{3} u \]

\[ \vec{u}_{2,(ppn)} = \frac{2}{3} u e^{j\pi/3} \]

Output Voltage Formation

\[
\vec{u}_2 = \frac{2/3}{T_P/2} \left( \delta_{(ac)}(pnn) \tau_{(ac)} u_{ac} + \delta_{(ab)}(pnn) \tau_{(ab)} u_{ab} + \delta_{(ac)}(ppn) \tau_{(ac)} u_{ac} e^{j\pi/3} + \delta_{(ab)}(ppn) \tau_{(ab)} u_{ab} e^{j\pi/3} \right)
\]

\[
= \delta_{(pnn)} \frac{2}{3} \left( \frac{\tau_{(ac)}}{T_P/2} u_{ac} + \frac{\tau_{(ab)}}{T_P/2} u_{ab} \right) + \delta_{(ppn)} \frac{2}{3} \left( \frac{\tau_{(ac)}}{T_P/2} u_{ac} + \frac{\tau_{(ab)}}{T_P/2} u_{ab} \right) e^{j\pi/3}
\]

\[
= \delta_{(pnn)} \frac{2}{3} (d_{(ac)} u_{ac} + d_{(ab)} u_{ab}) + \delta_{(ppn)} \frac{2}{3} (d_{(ac)} u_{ac} + d_{(ab)} u_{ab}) e^{j\pi/3}
\]

Local DC-link Voltage Average Value

\[
\bar{u} = d_{(ac)} u_{ac} + d_{(ab)} u_{ab}
\]

\[
\bar{u}_2 = \delta_{(pnn)} \frac{2}{3} \bar{u} + \delta_{(ppn)} \frac{2}{3} \bar{u} e^{j\pi/3}
\]

\[
\vec{u}_2 = \bar{u}_2^*
\]

Calculation of the Inverter Active Switching State On-Times can be directly based on \( \bar{u} \) !
DC-link Voltage Local Average Value

\[ \bar{u} = \frac{3}{2} \cdot \hat{U}_1 \frac{\cos \left( \varphi \bar{u}_1 - \varphi^*_1 \right)}{\cos \left( \varphi^*_1 \right)} = \frac{3}{2} \cdot \hat{U}_1 \frac{\cos (\Phi^*_1)}{\cos (\varphi^*_1)} \]

Minimum of DC-link Voltage Local Average Value

\[ \bar{u}_{\text{min}} = \frac{3}{2} \hat{U}_1 \cos \Phi^*_1 \]

Resulting IMC Output Voltage Limit

\[ \hat{U}_{2,\text{max}} \leq \frac{\sqrt{3}}{2} \cdot \hat{U}_1 \cos \Phi^*_1 \]

Simulation of DC-link Voltage and Current Time Behavior
Resulting Inverter Stage
Relative On-Times

\[ \delta_{(ppn)} = \frac{\sqrt{3}}{2} \cdot \frac{\hat{U}_2^*}{\bar{u}/2} \sin \left( \varphi \bar{u}_2^* \right) \]

\[ \delta_{(pnn)} = \frac{\sqrt{3}}{2} \cdot \frac{\hat{U}_2^*}{\bar{u}/2} \cos \left( \varphi \bar{u}_2^* + \frac{\pi}{6} \right) \]

Resulting Inverter Stage
Absolute On-Times

\[ \tau_{(ac)(pnn)} = \frac{1}{2} T_P d_{(ac)} \delta_{(pnn)} = \frac{1}{2} T_P \frac{2}{\sqrt{3}} \frac{\hat{U}_2^*}{U_1} \frac{1}{\cos \Phi_1^*} \sin \left( \frac{\pi}{6} + \varphi^*_{i_1} \right) \cos \left( \varphi \bar{u}_2^* + \frac{\pi}{6} \right) \]

\[ \tau_{(ac)(ppn)} = \frac{1}{2} T_P d_{(ac)} \delta_{(ppn)} = \frac{1}{2} T_P \frac{2}{\sqrt{3}} \frac{\hat{U}_2^*}{U_1} \frac{1}{\cos \Phi_1^*} \sin \left( \frac{\pi}{6} + \varphi^*_{i_1} \right) \sin \left( \varphi \bar{u}_2^* \right) \]
DC-link Voltage Local Average Value

\[ \bar{i}_{(ac)} = \frac{1}{\tau_{(ac)}} \left( i_A \delta_{(pnn)} \tau_{(ac)} - i_C \delta_{(ppn)} \tau_{(ac)} \right) = i_A \delta_{(pnn)} - i_C \delta_{(ppn)} \]

\[ \bar{i}_{(ab)} = \frac{1}{\tau_{(ab)}} \left( i_A \delta_{(pnn)} \tau_{(ab)} - i_C \delta_{(ppn)} \tau_{(ab)} \right) = i_A \delta_{(pnn)} - i_C \delta_{(ppn)} \]

Equal DC-link Current Local Average Values for Inverter Active Switching States

\[ \bar{i} = \bar{i}_{(ac)} = \bar{i}_{(ab)} = \hat{I}_2 \frac{\hat{U}_2^* \cos \Phi_2}{\hat{U}_1 \cos \Phi_1^*} \cos \frac{\varphi^*}{\bar{i}_1} \]

Local Average Value of Input Current in \( a \)

\[ \bar{i}_a = \bar{i} = \hat{I}_1 \cos \frac{\varphi^*}{\bar{i}_1} \]

Resulting Input Phase Current Amplitude

\[ \hat{I}_1 = \hat{I}_2 \frac{\hat{U}_2^* \cos \Phi_2}{\hat{U}_1 \cos \Phi_1^*} \]

Power Balance of Input and Output Side

\[ \bar{p} = P = \bar{u} \bar{i} = \frac{3}{2} \hat{U}_1 \hat{I}_1 \cos \Phi_1^* = \frac{3}{2} \hat{U}_2^* \hat{I}_2 \cos \Phi_2 \]
IMC Simulation Results
RB-IGBT IMC Experimental Results (1)

Efficiency 95%

Input RMS voltage 400V
Output Power 6.8 kVA
Rectifier Switching Frequency 12.5 kHz
Inverter Switching Frequency 25 kHz

2.9 kW/dm³
48 W/in³
RB-IGBT IMC Experimental Results (2)

\[ U_{12} = 400V \]
\[ P_{out} = 1.5 \text{ kW} \]
\[ f_{out} = 120 \text{ Hz} \]
\[ f_s = 12.5 \text{ kHz} / 25\text{kHz} \]
Alternative Modulation Schemes (1)

**Conventional Modulation (HV)**

- DC-link Voltage: Largest and Medium Line-to-Line Mains Voltage
  \[ \hat{U}_{2,\text{max, I}} = \frac{\sqrt{3}}{2} \hat{U}_1 \approx 0.86 \cdot \hat{U}_1 \]

**Low Output Voltage Modulation (LV)**

- DC-link Voltage: Medium and Smallest Line-to-Line Mains Voltage
  \[ \hat{U}_{2,\text{max, II}} = \frac{1}{2} \hat{U}_1 = 0.5 \cdot \hat{U}_1 \]
Alternative Modulation Schemes (2)

► Low Output Voltage Modulation
Alternative Modulation Schemes (3)

► LV vs. HV Modulation

Output Voltage Generation

Input Current Generation
Alternative Modulation Schemes (4)

► LV vs. HV Modulation

Switching Losses

Output Common Mode Voltage

Reduction of Switching Losses to approx. 58%

Output Common Mode Voltage reduced to approx. 75%
Alternative Modulation Schemes (5)

**LV vs. HV Modulation**

- Input Voltage Ripple Doubles
- Output Current Ripple Slightly Reduced
- For given $\hat{U}_2 (M_{12})$, the Component Current Stress are Increasing (Conduction Losses)
Alternative Modulation Schemes (6)

★ Three-Level Medium Voltage Modulation

High Output Voltage Modulation (HVM)

\[ \hat{U}_2 = 0 \cdots \frac{\sqrt{3}}{2} \cdot \hat{U}_1 \]

Low Output Voltage Modulation (LVM)

\[ \hat{U}_2 = 0 \cdots \frac{1}{2} \cdot \hat{U}_1 \]

Three-Level Modulation

\[ \hat{U}_2 = \frac{1}{2} \cdots \frac{\sqrt{3}}{2} \cdot \hat{U}_1 \]

Weighted Combination of HVM and LVM
Sparse Matrix Converter - SMC

Topology Derivation
Bidirectional / Unidirectional Converter
Experimental Results
Classification of Three-Phase AC-AC Converters

- **Sparse Matrix Converter**

Diagram:

- AC/AC Converter
  - Converter with DC-link
    - AC/DC-DC/AC Converter with Voltage DC-link (U-BBC)
    - AC/DC-DC/AC Converter with Current DC-link (I-BBC)
  - Hybrid Matrix Converter
    - Hybrid Direct Matrix Converter (HMC)
    - Hybrid Indirect Matrix Converter (HIMC)
  - Matrix Converter
    - Direct Matrix Converter
      - Conventional Matrix Converter (CMC)
      - Full Bridge Matrix Converter (Open Motorwindings)
    - Indirect Matrix Converter
      - AC/DC-DC/AC Converter without DC-link Capacitor
      - Indirect Matrix Converter (IMC)
      - Sparse Matrix Converter (SMC) (USMC)
    - Three-level Matrix Converter
Sparse Matrix Converter

ETH Zurich

► 15 Transistors
► 18 Diodes
SiC Sparse Matrix Converter

Switching Frequency 150kHz
Output Power 2.5kW@10kW/dm$^3$
SiC Sparse Matrix Converter

Switching Frequency: 150kHz
Output Power: 2.5kW@10kW/dm³
Ultra Sparse Matrix Converter

ETH Zurich
T. Lipo [13, 20]

- 9 Transistors
- 18 Diodes
Ultra Sparse Matrix Converter

\[ U_{\text{in}} = 3\Phi 400V/50Hz \]
\[ U_{\text{out}} = 3\Phi 0...340V / 0...200Hz \]
\[ P = 5.5\text{kVA} \]
\[ f_s = 25\text{kHz (Rect.)} / 50\text{kHz (Inv.)} \]
Unidirectional 9-Switch AC-AC Converters with PFC Input

VIENNA Rectifier with VSI (VR-VSI)

- With Intermediate Energy Storage
- 3-Level Input Stage
- Impressed Currents at Input Terminals (a,b,c)
- Additional DC-Link Chopper Required

Ultra Sparse Matrix Converter (USMC)

- Without Intermediate Energy Storage
- “Quasi” 3-Level Output
- Impressed Voltages at Input Terminals (a,b,c)
- Additional DC-Link Chopper/Clamp Required
Topologies with LC-Element in DC-Link

Z-Source Converter ZSC
T-Source Converter TSC
Z-Source Converter

$F^3E$-Topology with Z-Source-Element (LC-Element) in DC-Link

F. Z. Peng [45]
L. Sack [46]
T-Source Converters

- Suggested 2-Level T-Source Inverter Topologies by Strzelecki et al. [46], 2009, and Trans-Z-Source Inverter by Quian et al. [48], 2010.

T-Source “Sparse Matrix Related” AC-AC Converter

- IMC-Based Modulation Scheme
- Output Voltage Boost Capability
- Low Input Stage Switching Losses
- High Blocking Voltage Requirements of Output Side Switches
- Need for Low Leakage Transformer
IMC - Extensions

- Three-Level
- Hybrid
Classification of Three-Phase AC-AC Converters

- Three-Level IMC
- Hybrid IMC
Three-Level Matrix Converter

► Bidirectional Converter

► Unidirectional Converter

ETH Zurich
Three-Level Matrix Converter

Ch. Klumpner [23, 24]
Hybrid IMC

Ch. Klumpner [5, 6]
Conventional Matrix Converter - CMC

Modulation
Multi-Step Commutation
Classification of Three-Phase AC-AC Converters

- Conventional Matrix Converter
  - AC/DC-DC/AC Converter with Voltage DC-link (U-BBC)
  - AC/DC-DC/AC Converter with Current DC-link (I-BBC)
  - Hybrid Direct Matrix Converter (HCMC)
  - Hybrid Indirect Matrix Converter (HIDC)
  - Direct Matrix Converter
    - Conventional Matrix Converter (CMC)
    - Full Bridge Matrix Converter (Open Motor-windings)
  - Indirect Matrix Converter
    - AC/DC-DC/AC Converter without DC-link Capacitor
    - Indirect Matrix Converter (IMC)
    - Sparse Matrix Converter (SMC) (VSMC) (USMC)
  - Three-level Matrix Converter
Conventional Matrix Converter – CMC

► Quasi Three-Level Characteristic
CMC Classification of Switching States

**Group I**
Freewheeling States

**Group II**
Generating Stationary Output Voltage and Input Current Space Vectors

\[
\begin{align*}
(\text{aaa}) & \quad (\text{bbb}) & \quad (\text{ccc}) \\
(\text{cca}) & \quad (\text{cbb}) & \quad (\text{aab}) \\
(\text{aac}) & \quad (\text{bbc}) & \quad (\text{bba}) \\
(\text{acc}) & \quad (\text{bcc}) & \quad (\text{baa}) \\
(\text{caa}) & \quad (\text{cbb}) & \quad (\text{abb}) \\
(\text{cac}) & \quad (\text{cbc}) & \quad (\text{aba}) \\
(\text{aca}) & \quad (\text{bcb}) & \quad (\text{bab})
\end{align*}
\]

\[
\begin{align*}
u_{AB} &= 0 \\
u_{BC} &= 0 \\
u_{CA} &= 0
\end{align*}
\]

**Group III**
Generating Rotating Space Vectors

\[
\begin{align*}
(\text{abc}) & \quad (\text{cab}) & \quad (\text{bca}) & \quad \text{Positive Sequence} \\
(\text{acb}) & \quad (\text{cba}) & \quad (\text{bac}) & \quad \text{Negative Sequence}
\end{align*}
\]
CMC Rotating Space Vectors

Positive Sequence Switching States

Negative Sequence Switching States
CMC Stationary Space Vectors

Input Current Space Vectors

Output Voltage Space Vectors
CMC/IMC Relation (1)

Correspondence of Switching States

\[ \vec{u}_{2, (acc)} = \vec{u}_{2, (ac) (pnn)} \]

\[ \vec{i}_{1, (acc)} = \vec{i}_{1, (ac) (pnn)} \]

▶ Indirect Space Vector Modulation

P. Ziogas [12]
L. Huber / D. Borojevic
CMC/IMC Relation (2)

Matrix Representation of Voltage and Current Conversion

**CMC**

\[
\begin{pmatrix}
  u_A \\
  u_B \\
  u_C
\end{pmatrix} =
\begin{pmatrix}
  s_{AA} & s_{AB} & s_{AC} \\
  s_{BA} & s_{BB} & s_{BC} \\
  s_{CA} & s_{CB} & s_{CC}
\end{pmatrix}
\begin{pmatrix}
  u_a \\
  u_b \\
  u_c
\end{pmatrix}
\]

**IMC**

\[
\begin{pmatrix}
  i_A \\
  i_B \\
  i_C
\end{pmatrix} =
\begin{pmatrix}
  s_{pA} & s_{An} \\
  s_{pB} & s_{Bn} \\
  s_{pC} & s_{Cn}
\end{pmatrix}
\begin{pmatrix}
  u_p \\
  u_n
\end{pmatrix}
\]

\[
\begin{pmatrix}
  i_A \\
  i_B \\
  i_C
\end{pmatrix} =
\begin{pmatrix}
  S_{CMC,U} & u_a \\
  u_b \\
  u_c
\end{pmatrix}
\]

\[
S_{CMC,I} = S^T_{CMC,U}
\]

\[
S_{IMC,I} = S^T_{IMC,U}
\]
CMC/IMC Relation (3)

\[
\begin{align*}
\mathbf{S}_{CMC,U} & \equiv \mathbf{S}_{IMC,U} \\
\mathbf{S}_{IMC,U} & = \mathbf{S}_{WR,U} \mathbf{S}_{GR,U} = \\
& = \begin{pmatrix} s_{PA} & s_{AN} \\
 s_{PB} & s_{BN} \\
 s_{PC} & s_{CN} \end{pmatrix} \cdot \\
& \begin{pmatrix} s_{PA} & s_{PB} & s_{PB} \\
 s_{ANA} & s_{BNB} & s_{NBN} \end{pmatrix}
\end{align*}
\]

\[
\begin{pmatrix}
 s_{AA} & s_{Ab} & s_{Ac} \\
 s_{BA} & s_{Bb} & s_{Bc} \\
 s_{Ca} & s_{Cb} & s_{Cc} \\
\end{pmatrix}
\]

\[
\equiv \begin{pmatrix} s_{PA} s_{PA} + s_{ANA} s_{AN} & s_{PB} s_{PA} + s_{BNB} s_{AN} & s_{PC} s_{PA} + s_{NBN} s_{AN} \\
 s_{PA} s_{PB} + s_{ANA} s_{BN} & s_{PB} s_{PB} + s_{BNB} s_{BN} & s_{PC} s_{PB} + s_{NBN} s_{BN} \\
 s_{PA} s_{PC} + s_{ANA} s_{CN} & s_{PB} s_{PC} + s_{BNB} s_{CN} & s_{PC} s_{PC} + s_{NBN} s_{CN} \end{pmatrix}
\]

Example

\[
\begin{pmatrix} \vec{u}_{2,(acc)} \end{pmatrix} = \begin{pmatrix} \vec{u}_{2,(ac)(pnn)} \end{pmatrix}
\]

\[
\begin{pmatrix} \vec{i}_{1,(acc)} \end{pmatrix} = \begin{pmatrix} \vec{i}_{1,(ac)(pnn)} \end{pmatrix}
\]

\[
\begin{align*}
\mathbf{S}_{CMC,U} & = \begin{pmatrix} 1 & 0 \\
 0 & 1 \\
 0 & 0 \end{pmatrix} \cdot \begin{pmatrix} 1 & 0 \\
 0 & 0 \\
 0 & 1 \end{pmatrix} = \begin{pmatrix} 1 & 0 \\
 0 & 1 \\
 0 & 0 \end{pmatrix}
\end{align*}
\]
CMC/IMC Relation (4)

\[ \varphi_{\mu} \in [0, \pi/6] \]

Correspondence of Switching States

\[ \ldots | t_{\mu} = 0 \]

\[ (ac)(ppn) - (ac)(ppn) - (ac)(ppp) \]

\[ - (ab)(ppp) - (ab)(ppn) - (ab)(pnn) | t_{\mu} = T_P / 2 \]

\[ (ab)(pnn) - (ab)(ppn) - (ab)(ppp) \]

\[ - (ac)(ppp) - (ac)(ppn) - (ac)(pnn) | t_{\mu} = T_P \ldots \]

\[ \varphi_{\mu}^{*} \in [\pi/6, \pi/3] \]

\[ \ldots | t_{\mu} = 0 \]

\[ (ac)(ppn) - (ac)(pnn) - (ac)(nnn) \]

\[ - (ab)(nnn) - (ab)(pnn) - (ab)(ppn) | t_{\mu} = T_P / 2 \]

\[ (ab)(ppn) - (ab)(ppn) - (ab)(nnn) \]

\[ - (ac)(nnn) - (ac)(pnn) - (ac)(ppn) | t_{\mu} = T_P \ldots \]

\[ \ldots | t_{\mu} = 0 \]

\[ (aac) - (acc) - (ccc) - (bbb) - (abb) - (aab) | t_{\mu} = T_P / 2 \]

\[ (aab) - (abb) - (bbb) - (ccc) - (acc) - (aac) | t_{\mu} = T_P \ldots \]
CMC/IMC Relation (5)

\[ \varphi_{\mu^*} \in [0, \pi/6] \]

\[ \varphi_{\mu^*} \in [\pi/6, \pi/3] \]

\[ \varphi_{\mu^*} \in [0, \pi/3] \]

\[ \alpha_{\mu^*} \]

... \( t_\mu = 0 \) 

\[ (acc) - (aac) - (aaa) - (aaa) - (aab) - (abb) \]

\[ t_\mu = T_P/2 \]

\[ (abb) - (aab) - (aaa) - (aaa) - (aac) - (acc) \]

\[ t_\mu = T_P \]

...
CMC Multi-Step Commutation

Example: \( u \)-Dependent Commutation

- Four-Step Commutation
- Two-Step Commutation

J. Oyama / T. Lipo
N. Burany
P. Wheeler
W. Hofmann
4-Step Commutation of CMC (1)

Example: $i$-Dependent Commutation

- No Short Circuit of Mains Phases
- No Interruption of Load Current

Assumption: $i > 0, u_{ab} < 0, \ aA \rightarrow bA$
4-Step Commutation of CMC (2)

1\textsuperscript{st} Step: Off

Constraints

- No Short Circuit of Mains Phases
- No Interruption of Load Current

Assumption: \( i > 0, u_{ab} < 0, \ aA \rightarrow bA \)
4-Step Commutation of CMC (3)

1\textsuperscript{st} Step: Off
2\textsuperscript{nd} Step: On

Constraints

- No Short Circuit of Mains Phases
- No Interruption of Load Current

Assumption: \( i > 0, u_{ab} < 0, \quad aA \rightarrow bA \)
4-Step Commutation of CMC (4)

1\textsuperscript{st} Step: Off
2\textsuperscript{nd} Step: On
3\textsuperscript{rd} Step: Off

Constraints

- No Short Circuit of Mains Phases
- No Interruption of Load Current

Assumption: $i > 0, u_{ab} < 0, \ aA \rightarrow bA$
4-Step Commutation of CMC (5)

1\textsuperscript{st} Step: Off
2\textsuperscript{nd} Step: On
3\textsuperscript{rd} Step: Off
4\textsuperscript{th} Step: On

Sequence Depends on Direction of Output Current!

Constraints

- No Short Circuit of Mains Phases
- No Interruption of Load Current

Assumption: \( i > 0, u_{ab} < 0, \quad aA \rightarrow bA \)
All-SiC JFET Conventional direct Matrix Converter

- $P_{out} = 3$ kVA, $\eta = 93.1\%$ (at 200 kHz)
- $f_{S,nom} = 144$ kHz ($f_{S,design} = 200$ kHz)
- 3 kVA/dm$^3$ (50W/in$^3$) with 1200 V/6 A SiC JFET
- $\approx 8$ kVA/dm$^3$ (135W/in$^3$) with 1200 V/20 A SiC JFET
- 273 x 82 x 47mm$^3 = 1.05$ dm$^3$ (64 in$^3$)

Measurements @ $U_{in} = 115$ V RMS, 400 Hz
Control Properties of AC-AC Converters (1)

Voltage DC-Link B2B Conv. (V-BBC)

- Boost-Buck-Type Converter
- Max. Output Voltage can be Maintained during Low Mains Condition

Matrix Converter (CMC/IMC)

- Buck-Type Converter
- Maximum Output Voltage is Limited by Actual Input Voltage $\hat{U}_2 = 0.866 \cdot \hat{U}_1$
Control Properties of AC-AC Converters (2)

DC-DC Equivalent Circuits

- **Uncontrolled Input Filter**

- **IMC**

- **I-BBC**

- **V-BBC**

- **CMC**
Control Properties of AC-AC Converters (3)

- Voltage DC-Link B2B Converter (V-BBC)
- Matrix Converter (CMC / IMC)

- Input Current (in Phase with Input Voltage)
- DC-Link Voltage
- Output Current (Torque and Speed of the Motor)

2 Cascaded Control Loops

- Output Current (Torque and Speed of the Motor)

Optional: Input Current (Formation of Input Current still Depends on the Impressed Output Current)
CMC - Extensions

Multi-Level Full-Bridge
Classification of Three-Phase AC-AC Converters

- Hybrid CMC
- Full-Bridge CMC
Hybrid CMC

B. Erickson

IECON' 2010
Full-Bridge CMC / IMC

M. Braun
N. Mohan
Coffee Break!
Comparative Evaluation

DC Link Converters
Matrix Converters
Application Areas of Three-Phase PWM Converters

Bidirectional Power Flow

Unidirectional Power Flow

- Elevators
- Escalators
- Cranes
- Roller Test Benches
- Automation
- Production Machinery
- Ventilation and AC
- Renewable Energy
- MEA

60% of Worldwide Ind. Energy Used by Electric Motor Drives! [a]

Motivation

Cost Allocation of VFD Converters

- Holistic Converter System Comparisons are (still) Rarely Found
- Comprehensive Comparisons Involves a Multi-Domain Converter Design
- Voltage-Source-Type Converter Topologies are Widely Used

Status Quo ⇒ Motivation

Focus of the Investigation

- Bidirectional Three-Phase AC/DC/AC and AC/AC Converters
- Low Voltage Drives
- Power Level from 1 kVA to few 10 kVA

[b]: Based on “ECPE Roadmap on Power Electronics, 2008”
Comparative Evaluation – Virtual Converter Evaluation Platform

- Define Application / Mission Profile
  - $M-n$ Operating Range
    (Continuous / Overload Requirement)
  - Torque at Standstill
  - Motor Type
  - etc.

- Compare Required Total Silicon Area (e.g. for $T_J < 150^\circ C$, $T_C = 95^\circ C$)
  - Guarantee Optimal Partitioning of Si Area between IGBTs and Diodes

- Virtual Converter Evaluation Platform
  - Semiconductor Type, Data
  - Thermal Properties
  - EMI Specifications
  - Converter Type, Motor Type (Losses)
  - Modulation Scheme
  - etc.
  - $M-n$ Operating Range
  - Mission Profile
  - etc.

- Total Si Area – Figure-Of-Merit
  - Operating Efficiency
  - Average Mission Efficiency
  - Total Mission Energy Losses
  - EMI Filter Volume
  - Costs
Considered Converter Topologies – V-BBC, I-BBC, IMC, and CMC

With Intermediate Energy Storage

Voltage Source Back-to-Back Converter (V-BBC)
“State-of-the-Art” Converter System

Current Source Back-to-Back Converter (I-BBC)

Without Intermediate Energy Storage

Indirect Matrix Converter (IMC)

Conventional (Direct) Matrix Converter (CMC)

\[ U_{2,max} = 0.866 U_1 \]
Converter Comparison Overview

Drive System Specs

Operating Point

Converter Topology

Modulation Scheme

Semiconductor Chip Area ($T_J, T_S$)

Power Module

Heat Sink ($T_A, T_S$)

Gate Driver

Semiconductor and Cooling System Design / Optimization

Semiconductor Losses

Energy Storage

Control

Power Quality

Reactive Power

EMI & Filter Topology

Loading Limits $\rightarrow$ Lifetime

Thermal Properties

Passive Components

4 Topologies

Optimized SPV

Passive Component and EMI Filter Design / Optimization
Comparative Evaluation (1) – Specifications and Operating Points

Main Converter Specifications

- 3 x 400 V / 50 Hz, 15 kVA
  \( f_{sw} = [8 \ldots 72] \text{ kHz} \)
  \( U_{DC} = 700 \text{ V (VSBB)} \)

- PMSM, Matched to Converter
  \( \mathcal{L}_s \text{ in mH range, } \Phi_2 \approx 0^\circ \)

- EMI Standard, CISPR 11
  QP Class B (66 dB at 150 kHz)

- Ambient Temperature \( T_A = 50^\circ \text{C} \)
  Sink Temperature \( T_S = 95^\circ \text{C} \)
  Max. Junction Temperature \( T_{J,max} = 150^\circ \text{C} \)
  (for \( T_A = 20^\circ \text{C} \Rightarrow T_S = 65^\circ \text{C} \), \( T_{J,max} = 20^\circ \text{C} \))

Torque Speed Plane

- OP1/OP5: Nominal Motor/Generator Operation (90% \( U_{2,max} \))
- OP2/OP4: Motor/Generator Operation for \( f_2 = f_1 \)
- OP3: Motor Operation at Stand-still \( f_2 = 0 \)
Comparative Evaluation (2) – Semicond. Area Based Comparison

Minimum Chip Area Required to Fulfill the Junction Temperature Limit $T_{J,max}$ (150°C)

ETH Zurich [49]
Semiconductor and Cooling System Modeling

Semiconductor Database

- 1200 V Si IGBT4 and EmCon4 Diodes (Infineon)
- 1200 V normally-on SiC JFET (SiCED)

Component Level

System Level

Cooling Performance

Simulation with ICEPAK and GECKO
Comp. Evaluation (3) – Semiconductor Chip Areas (OP1 & OP5)

1200 V Si IGBT4 and EmCon4 Diodes

1200 V Normally-On SiC JFETs (SiCED)

Conduction Losses

Switching Losses

Resulting Sensitivities
Comparative Evaluation (4) – Torque Envelope for Equal $A_{\text{chip}}$

For OP1 ($P_{2N} = 15$ kVA) and OP3 (Stand-Still)

8 kHz: $A_{\text{chip}} \approx 6$ cm$^2$, Referenced to IMC

32 kHz: Available Chip Area $A_{\text{chip}} \approx 6$ cm$^2$

Note: Design at Thermal Limit – A More Conservative Design would be Applied for a Product!
Verification by Electro-Thermal Simulation Shown for IMC

Junction Temperatures OP1

► Suggested Algorithm to Optimally Select the Semiconductor Chip Area Matches well at OP1 and OP3

Evaluated for OP1 @ 8 kHz

Torque at OP1 and OP3

► Suggested Algorithm allows for Accurate Torque Estimation at OP1 and OP3

► Torque Limit Line Requires a Thermal Impedance Model of the Module (R-C Network)
Passive Component and EMI Input Filter Modeling

**Component Level**

- **System Level**

  - **EMI Input Filter Topology**
    - **CISPR 11** (Compliant to IEC/EN)
      - EMI Standard for CE
    - Filter Design Margin
      - DM Design Margin: 6 dB
      - CM Design Margin: 8-10 dB

**Design Criteria and Constraints**

- Ripple-Based \( \left( C_{\text{inp}}, L_b \right) \)
- Reactive Power \( \left( C_{\text{inp}}, L_b \right) \)
- Control-Based \( \left( C_{DC}, L_{DC} \right) \)
- Energy-Based \( \left( C_{DC}, L_{DC} \right) \)
Comparative Evaluation (5) – Attenuation, Volume of Passives

Volume of Passive Components

- V-BBC Requ. 15 dB More Attenu.
Comparative Evaluation (6) – Total Efficiency and Volume

Efficiency vs. Switching Frequency

Volume vs. Switching Frequency

► V-BBC: Local Optimum at 35 kHz for SiC JFETs
► MC: Significant Volume Reduction
GECKO Research

Multi-Domain Simulation Software
GECKO RESEARCH

GeckoCIRCUITS

Input
Topology / Device Models / Control Circuit / 3D-Geometry / Materials

GeckoHEAT

3D-Thermal FEM Solver
Thermal Impedance Matrix
HF Magnetics Design Toolbox

Fast Circuit Simulator

3D-Electromagn. Parasitics Extraction
Reduced Order Impedance Matrix
EMC Filter Design Toolbox

Heatsink Design Toolbox

Reliability Analysis Toolbox

Post Processing
Design Metrics, Sensitivity Calculation, Optimization

Device & Material Database
Control Toolbox
Optimization Toolbox

GeckoEMC

IECON' 2010
Overview of Gecko-Software Demonstration

► Gecko-CIRCUITs: Basic Functionality

► Indirect Matrix Converter (IMC)
  - IMC Simulation with Controlled AC Machine
  - Specify Semiconductor Characteristics
  - Simulate Semiconductor Junction Temperature
  - etc.

► Gecko EMC: Basic Functionality
Power Electronics Simulation - Gecko Research

- Specialized Software to meet demands of Power Electronics Engineers
- Easy-to-use
- Three tools working together: GeckoCIRCUITS, GeckoEMC, GeckoHEAT
- Multi-Domain approach and Optimization
- Coupled Circuit-, Thermal-, and Electromagnetic Simulation

Free Trial Version of GeckoCIRCUITS
- Online Simulator in Applet-Mode
- No installation required!

Power Electronic Converter Optimization

Let's assume you want to build a single-phase PFC rectifier with 230V input voltage, 400V output voltage and 3.2kW output power. You can optimize this rectifier for highest efficiency or for highest power density or for minimum cost or...

www.gecko-research.com
Overview of AC-AC Converters

AC/AC-Conversion for Highly Compact Drives - What Options Do I Have?

For operating a Permanent Magnet Synchronous Machine (PMSM), which allows a highly compact design, you have to supply three-phase voltage with controllable output frequency and controllable voltage amplitude. There are many different alternatives for the AC/AC converter. Here you will learn all options.

- Part I - An Overview of AC/AC-Converter Topologies

How to Design a 10kW Three-Phase AC/DC Interface Step by Step

You need a rectifier with sinusoidal input currents (power factor correction) and controlled DC-voltage at the output side? In this report you will learn how to compare the well-known Bidirectional 2-Phase AC/DC PWM Converter with Impressed Output Voltage (VIOR) with a Vienna Rectifier employing a simple but effective strategy.

- Part I - How Can I Compare Topologies?
- Part II - Semiconductor Loss Calculation Demystified
- Part III - Do You Know the Junction Temperatures of Your Design? (coming soon)
Useful Hints for e.g. How to Implement Sector Detection for SV Modulation

► JAVA Code Block

- Integration of Complex Control Code; Enhances Overview and Transparency
- Code can Virtually be Copied to DSP C-Code Generator (Minor Syntax Adaptations)
Power Electronics Converter Optimization

Goal: Optimization Toolbox

- Guided Step-by-Step Converter Design Procedure to Enable Optimal Utilization of Technological Base and Optimal Matching between Design Specifications and Final Performance
Conclusions
Hype Cycle of Technologies
-Gartner Group

2000
- Sparse Matrix Converter
- Three-Level Matrix Converter

1995
- Reverse Blocking IGBTs
- Handling of Unbalanced Mains

1990
- Multi-Step Commutation
- Indirect Space Vector Modulation
- Indirect Matrix Converter

1970’s
- Invention of Matrix Converter Topology

2005 –
- Hybrid Matrix Converter
- More Complicated Topologies
- Refinements
- Holistic Comparisons [51-54]

Through of Disillusionment
Conclusions (1)

- **MC is NOT an All-SiC Solution**
  - Industry Engineers Missing Experience
  - 86% Voltage Limit / Application of Specific Motors / Silicon Area
  - Limited Fault Tolerance
  - Braking in Case of Mains Failure
  - Costs and Complexity Challenge
  - Voltage DC Link Converter could be implemented with Foil Capacitors

- **MC does NOT offer a Specific Advantage without Drawback**

**EMI Filter**

**Clamp Circuit**
Conclusions (2)

- **Research MUST Address Comprehensive System Evaluations**
  - **MC Promising for High Switching Frequency**
  - **Consider Specific Application Areas**
  - **Consider Life Cycle Costs**
  - **etc.**

- **V-BBC is a Tough Competitor**

- **F³E Might Offer a Good Compromise**

- **Most Advantageous Converter Concept Depends on Application and on whether a CUSTOM Drive Design is Possible**

- **Integration of Multiple Functions (as for MC) Nearly ALWAYS Requires a Trade-off**
Thank You!
References (1)


References (2)


References (3)


References (4)


References (5)


References (6)


About the Instructors

Johann W. Kolar (F ’10) received his Ph.D. degree (summa cum laude / promotio sub auspiciis praesidentis rei publicae) from the University of Technology Vienna, Austria. Since 1984 he has been working as an independent international consultant in close collaboration with the University of Technology Vienna, in the fields of power electronics, industrial electronics and high performance drives. He has proposed numerous novel PWM converter topologies, and modulation and control concepts, e.g., the VIENNA Rectifier and the Three-Phase AC-AC Sparse Matrix Converter. Dr. Kolar has published over 350 scientific papers in international journals and conference proceedings and has filed 75 patents. He was appointed Professor and Head of the Power Electronic Systems Laboratory at the Swiss Federal Institute of Technology (ETH) Zurich on Feb. 1, 2001.

The focus of his current research is on AC-AC and AC-DC converter topologies with low effects on the mains, e.g. for power supply of data centers, More-Electric-Aircraft and distributed renewable energy systems. Further main areas of research are the realization of ultra-compact and ultra-efficient converter modules employing latest power semiconductor technology (SiC), novel concepts for cooling and EMI filtering, multi-domain/multi-scale modeling / simulation and multi-objective optimization, physical model based lifetime prediction, pulsed power, bearingless motors, and Power MEMS.

He received the Best Transactions Paper Award of the IEEE Industrial Electronics Society in 2005, the Best Paper Award of the ICPE in 2007, the 1st Prize Paper Award of the IEEE IAS IPCC in 2008, and the IEEE IECON Best Paper Award of the IES PEC in 2009. He also received an Erskine Fellowship from the University of Canterbury, New Zealand, in 2003. He initiated and/or is the founder / co-founder of 4 Spin-off Companies targeting ultra high speed drives, multi-domain/level simulation, ultra-compact/efficient converter systems and pulsed power/electronic energy processing. In 2006, the European Power Supplies Manufacturers Association (EPSMA) awarded the Power Electronics Systems Laboratory of ETH Zurich as the leading academic research institution in Power Electronics in Europe.

Dr. Kolar is a Fellow of the IEEE and a Member of the IEEJ and of International Steering Committees and Technical Program Committees of numerous international conferences in the field (e.g. Director of the Power Quality Branch of the International Conference on Power Conversion and Intelligent Motion). He is the founding Chairman of the IEEE PELS Austria and Switzerland Chapter and Chairman of the Education Chapter of the EPE Association. From 1997 through 2000 he has been serving as an Associate Editor of the IEEE Transactions on Industrial Electronics and since 2001 as an Associate Editor of the IEEE Transactions on Power Electronics. Since 2002 he also is an Associate Editor of the Journal of Power Electronics of the Korean Institute of Power Electronics and a member of the Editorial Advisory Board of the IEEJ Transactions on Electrical and Electronic Engineering.
Thomas Friedli (M’09) received his M.Sc. degree in electrical engineering and information technology (with distinction) and his Ph.D. from the Swiss Federal Institute of Technology (ETH) Zurich, in 2005 and 2010, respectively.

From 2003 to 2004 he worked as a trainee for Power-One in the R&D centre for telecom power supplies. His Ph.D. research from 2006 to 2009 involved the further development of current source and matrix converter topologies in collaboration with industry using silicon carbide JFETs and diodes and a comparative evaluation of three-phase ac-ac converter systems.

He received the 1st Prize Paper Award of the IEEE IAS IPCC in 2008 and the IEEE IAS Transactions Prize Paper Award in 2009.