SiC/GaN
Voltage Source Inverter Motor Drives

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Outline

- Advanced Filter Techniques
- Industrial Inverters w/ Output Filter
- Advanced Inverter Topologies

...“How to Handle the Double-Edged Sword”
Advanced Output Voltage Filter Techniques

dv/dt-Limitation
Active CMV Compensation
“Zero”/Low CMV Modulation
$dv/dt$-Limitation
Passive / Hybrid / Active \( \frac{dv}{dt} \)-Limitation

- **Passive** – Damped LC-Filter \( f_c > f_s \)
- **Hybrid** – Undamped LC-Filter & Multi-Step Sw. Transition
- **Active** – Gate-Drive Based Shaping of Sw. Transients

\[
\begin{align*}
 f_{sw} &= 16 kHz \\
 t_R &= t_F = 130 ns \\
 f_c &= 2.4 MHz
\end{align*}
\]

- Connection to DC- & CM Inductor → Limit CM Curr. Spikes / CM EMI / Bearing Currents
Design of Passive $dv/dt$-Filters

- **Sw. Transient** — Results in DM & CM Voltage Step → Consider DM & CM Properties
- **Influence of Motor Impedance** $Z_M$ & (Long) Motor Cable

- $Z_{F,DM}$ Higher Compared to $Z_{F,CM}$ → More Critical
- Low $Z_F$ / Large Filter Capacitor → High Losses → Select $Z_{F,DM}$ Only Slightly Below $Z_{M,a^*b^*c}$
Comparison of \( \frac{dv}{dt} \)-Filtering Techniques (1)

- **Passive Concept**
  1. LCR-Filter
  2. Clamped LC-Filter

- **Hybrid Concept (3f_s)**
  1. LC-Filter
  2. Multi-Step Switching

- **Active Concept**
  1. Miller Capacitor
  2. Gate Curr. Control

**Output Voltage Waveforms** — \( V_{DC} = 800V \), \( P_{out} = 10kW \), 6kV/us

1200V SiC / 16mΩ
\( C_M = 120pF \)

\[ L = 3.8uH \]
\[ C = 2.7nF \]
\[ R = 19\Omega \]

\[ L = 4.1uH \]
\[ C = 1.3nF \]
Comparison of $dv/dt$-Filtering Techniques (2)

- **Passive Concept**
- **Hybrid Concept ($3f_s$)**
- **Active Concept**

**Losses / Power Density** – $V_{DC} = 800V$, $P_{out} = 10kW$, $f_{sw} = 16kHz$, 1200V SiC-MOSFETs (16mΩ)

- Smaller Opt. Chip Area for Hybrid Concept (32mΩ), Adv. of Active Concept for High $dv/dt$

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**Graphs and Diagrams**

- Part-Loud Efficiency $\eta_{PL}$ vs. Volumetric Power Density $\rho$ (kW/l)
- Inverter Efficiency $\eta_{inv}$ vs. Peak Phase Current $\hat{i}_a$ (A)

**Ethzurich**
Staggered/Resonant Switching

- **2-Step Switching / Resonant Transition (cf. Hybrid dv/dt-Filter)**

- **Staggered Sw. Parallel Bridge-Legs → Non-Resonant Multi-Step Transition**

Active CM-Voltage Compensation &
DM dv/dt-Filtering
**Active CM-Voltage Filters (1)**

- **Series Compensation of CM-Voltage & DM dv/dt-Filtering**

- **Aux. Bridge-Leg → Zero CM-Voltage for Active Inv. Sw. States & DM dv/dt-Filtering**

- **Residual CM-Volt. Due to CM-Transf. & Sw. Imperfections / Complexity & Missing Zero State**

Source: X. Chen et al., 2007

Source: T.A. Lipo et al., 1999
Active CM-Voltage Filters (2)

- Series Compensation of CM-Voltage & DM dv/dt-Filtering

Source: X. Chen et al., 2007

- Aux. Bridge-Leg → Zero CM-Voltage for Active Inv. Sw. States & DM dv/dt-Filtering

Source: T.A. Lipo et al., 1999

- Residual CM-Volt. Due to CM-Transf. & Sw. Imperfections / Complexity & Missing Zero State
„Zero“/Low CM-Voltage Modulation
**Conventional Modulation**

- **Voltage Space Vector Formation** — 2 Active & 2 Zero-States / Pulse-Period

\[ u_N = +\frac{1}{6}U_d \]

\[ u_N = -\frac{1}{6}U_d \]

- **Restriction to Active Vectors Showing Same** \( u_N \) → **No/“Zero” CM-Voltage Transients**

Source: Guzinski/Abu-Rub/Strankowski, Wiley, 2015
“Zero”/Low CM-Voltage Modulation

- Only Active Vectors of Same CM-Voltage / No Zero-States (111)/(000) Used

\[ u_N = -\frac{1}{6} U_d \]

- Replace Zero States by Mutually Compensating Active States

- Limited Modulation Range / Higher Harmonics / Higher Sw. Losses

Source: Guziński/Abu-Rub/Strankowski, Wiley, 2015
Commercial Inverter Systems w/ Full-Sinewave Output Filters

Si-SJ MOSFET TCM Inverter
GaN/Si-MOSFET Cascode Inverters
Si-SJ MOSFET ZVS
Triangular Current Mode (TCM) Inverter

NFO
Sinus
**Full-Sinewave Filtering @ ZVS/TCM Operation**

- **ZVS of Inverter Bridge-Legs** (No Use of the Intrinsic Diodes of Si MOSFETs)
- **High Sw. Frequency & TCM → Low Filter Inductor Volume**

- **Transistor Conduction Losses → Only 33% Increase Compared to CCM (!)**
Remark — **S-TCM**

- Widely Varying Sw. Frequency of Conventional TCM
- Multiple Bridge-Legs for Limiting Sw. Frequency Variation
- Sinusoidal Sw. Boundaries → S-TCM

\[ f_{sw,max} = 140kHz \]

- **TCM → S-TCM** — 10% Further Increase of Transistors Conduction Losses

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**ETH zürich**
650V GaN/ Si-MOSFET Cascode Inverter
YASKAWA
**3-Φ 650V GaN Inverter System (1)**

- Transphorm 650V GaN HEMT/30V Si-MOSFET Cascode Switching Devices
- Measurement of Sw. Properties → Turn-On/Off 10A/400V

- Factor 10 Lower On/Off Delay & Sw. Times Comp. to IGBTs
- Extremely Low Sw. Losses → Inverter Sw. Frequency $f_s = 100$kHz
3-Φ 650V GaN Inverter System (2)  

- **Transphorm 650V Normally-On GaN HEMT/30V Si-MOSFET Cascode 6-in-1 Power Module**
- **Sinewave LC Output Filter — Corner Frequency** $f_c = 34\text{kHz}$ ($f_s = 100\text{kHz}$)
- **No Freewheeling Diodes**

**Source:** YASKAWA

**Diagrams and Notes:**

- **Transphorm GaN Module**
- **Sine wave Filter**
- **Torque Transducer**
- **IM (2.2kW (3hp))**
- **IM (11kW (15hp))**

**Text:**

→ Very Low Filter Volume Compared to Si-IGBT Drive Systems ($f_c = 0.8\text{kHz}$ @ $f_s \approx 3\text{kHz}$)
3-Φ 650V GaN Inverter System (3)

- Transphorm 650V Normally-On GaN HEMT/30V Si-MOSFET Cascode 6-in-1 Power Module
- Sinewave LC Output Filter — Corner Frequency $f_C = 34$ kHz ($f_S = 100$ kHz)
- No Freewheeling Diodes

$L_f = 220 \mu$H
Iron Powder Core Filter Inductors
$C_f = 0.1 \mu$F

$f_C \approx 1/3 f_S$

→ Very Low Filter Volume Compared to Si-IGBT Drive Systems ($f_C = 0.8$ kHz @ $f_S = 3$ kHz)
→ Lower Size of DC Input Capacitor (-75% vs. IGBT) & -8dB Audible Noise @ 6krpm
**3-Φ 650V GaN Inverter System (4)**

- **Comparison of GaN Inverter with LC-Filter to Si-IGBT System (No Filter, $f_S=15kHz$)**
- **Measurement of Inverter Stage & Overall Drive Losses @ 60Hz**

→ 2% Higher Efficiency of GaN System Despite LC-Filter (Saving in Motor Losses)!
3-Φ 650V GaN Inverter System (5)

- Sigma-7F Servo Drive — Motor Integration of DC/AC Stage (TO-220 GaN)
- Distributed DC-Link System — Single AC/DC Converter / Smaller Cabinet
- 0.1 – 0.4kW / 270…324V Nominal DC-Link Voltage

→ Small Size (0.4 kW @ 70 x 70 x 170mm)
→ Massive Saving in Cabling Effort / Simplified Installation
650V GaN HEMT Inverter
2-Stage Full-Sinewave Output Filter (1)

- Sinewave Output & IEC/EN 55011 Class-A
- Low-Loss Active Damping of 1st Filter Stage — Neg. Cap. Current Feedback
- 2kW / 400V DC-Link 3-Φ 650V GaN Inverter \((I_m=5A)\), \(f_{\text{out,max}} = 500\text{Hz}\)
- Sw. Frequency \(f_s = 100\text{kHz}\)

\(f_{C1}=7\text{kHz}\)

\(f_{C2}=20\text{kHz}\)

Evaluation of Optimized Inductors — Soft Sat. Toroidal Iron Powder Cores

\(L_1=200\mu\text{H (OD57S)} / C_1 = 2.5\mu\text{F} / L_2 = 25\mu\text{H (OD20S)} / C_2 = 2.5\mu\text{F} / L_d = 33\mu\text{H} / R_d = 5.6\Omega\)
2-Stage Full-Sinewave Output Filter (2)

- Passive Damping of 2nd Filter Stage
- PI-Type Current Control

→ Transfer Functions & Step Response
2-Stage Full-Sinewave Output Filter (3)

- Nonlinearity of MMLC Caps (X7R, 330nF/500V) → Effect on $i_C$-Feedback
- Symmetric Connection of Filter Capacitors to +/-DC Reduces Nonlinearity
- 1st Resonance of Filter Components @ ≈5MHz

- Impedances of Filter Components & DC-Link Capacitor ($C_{DC} = 120\mu F$)
2-Stage Full-Sinewave Output Filter (4)

- **Exp. Verification** — 650V E-Mode GaN Systems Transistors (50mΩ)
- **Sw. Frequency** $f_s = 100$kHz, Efficiency ≈98%
- **200mm x 250mm**

**Stationary Motor Phase Curr. /Voltage @ 2.5Nm & $f_{\text{out}} = 250$Hz**

**Speed Increase from Standstill to $n = 3000$rpm in 60ms**
2-Stage Full-Sinewave Output Filter (5)

- Modification of Output Filter Structure
- Elimination of Direct Cap. Coupling Between Output and Noisy (!) DC+ (Due to $R_{DC}$)
- For Opt. $i_C$ -Feedback $C_1$ Realized Using ≈Linear Kemet KC-Link

● Modified Filter → Compliance to EMI Standard EN55011 Class-A
900V GaN/\textit{Si}-MOSFET Cascode Inverter

SIEMENS
3-Φ 900V GaN Inverter System (1)

- 900V Normally-Off GaN in TO-220 Package (165mΩ)
- 650V DC-Link Voltage (!) / Sinewave Output Filter
- Filter Corner Freq. $f_C$ — Geom. Mean of $f_s$ & $10f_{out,max}$
- Sw. Frequency $f_s = 128$kHz

Filter Corner Frequency $f_C = 8$kHz ($L=320uH$, $\Delta i_{L,max}=50\% @ 3kW$)
3-Φ 900V GaN Inverter System (2)

- 900V Normally-Off GaN in TO-220 Package (165mΩ)
- 650V DC-Link Voltage (!) / Sinewave Output Filter
- Filter Corner Freq. \( f_C \) — Geom. Mean of \( f_S \) & 10\( f_{out,max} \)
- Sw. Frequency \( f_S = 128kHz \)

- GaN Inverter & Filter \( \rightarrow \) 1% Higher Efficiency Comp. to Si-IGBT System (\( f_S = 16kHz \), No Filter)
Advanced Voltage Source Inverter Topologies

Sparse NPC Inverter
Multi-Level Flying Capacitor Inverter
Quasi-Analog MHz-Switching Inverter
3-Level NPC Inverter / Sparse NPC Inverter
2-Level Inverter

- Open Motor Starpoint → Single Unipolar Bridge Leg / Phase
- AC Phase Voltage $U_{\text{phase}}$ Formation Against DC Midpoint
- DC Voltage / Blocking Voltage $\approx 2U_{\text{phase}}$

3-Level Inverter

- Neutral Point Clamped (NPC) Topology Features Connection to Cap. DC Midpoint
- Larger Number of Sw. States / Higher Output Voltage Quality
- Requires Neutral Point Balancing
- Blocking Voltage $\frac{1}{2}U_{DC} \approx U_{phase}$

- Baker (1979)

$\pm \frac{1}{2}U, 0, -\frac{1}{2}U$

- Rel. High Conduction Losses (T-Type Topology as Alternative)
**Sparse NPC 3-Level Inverter (1)**

- **3-Level Neutral Point Clamped (3L-NPC) Topology Proposed in 1979 (Baker)**
- **Sparse NPC Configuration → Reduced Total # of Switches**
- **Fast/Slow & Low/High Voltage Semiconductors (“Hybrid”)**

- Rojas (1993)

- Realization of the Simplified Concept Using 650V GaN HEMTs & 1200V Si IGBTs
Sparse NPC 3-Level Inverter (2)

- 3L Matrix Stage $\rightarrow$ “Voltage Pre-Conditioning” / 2L Inverter Defines Space Vector Direction
- Redundant Half Voltage States for DC Midpoint Balancing

- Missing Sw. States Comp. to Full 3L-NPC $\rightarrow$ 7 Instead of 9 Phase Voltage Levels
- Diff. Sw. Schemes $\rightarrow$ E.g. Commutation of 2L-Stage @ Full DC Voltage Can be Avoided
Sparse NPC 3-Level Inverter (3)

- Application of Low Sw. & Cond. Loss 650V GaN Technology for 800V DC-Link
- Redundant Voltage Vectors Allow Control of Neutral Point Voltage
- Avg. Sw. Frequency of GaN HEMTs & Si IGBT → Factor 6

Piepenbreier (2018)

- Missing Sw. States Comp. to Full 3L-NPC → 7 Instead of 9 Phase Voltage Levels
- Diff. Sw. Schemes → E.g. Commutation of 2L-Stage @ Full DC Voltage Can be Avoided
**Sparse NPC 3-Level Inverter (4)**

- **Demonstrator Using Top-Cooled 650V SMD GaN Half-Bridges & 1200V Si-IGBT Modules**
- **Minimiz. of Commutation Loop by Close Placement of 2L-Inverter & 3L Matrix Stage**
- **Vertical Commutation Loop of 3L Matrix Stage**

- Piepenbreier (2018)

- **10kHz Sampling Freq. → Avg. Sw. Frequencies: 20kHz (GaN) & 3.33kHz (IGBTs)**
Sparse NPC 3-Level Inverter (5)

- Experimental Results → Phase Currents & Phase Voltages

- Analysis for Different Modulation Depths — M=0.49 & M=0.92
3-Level & Multi-Level
Flying-Capacitor (FC) Inverter
3-Level Flying Capacitor (FC) Inverter

- Requires No Connection to DC-Midpoint
- Involves All Switches in Voltage Generation → Eff. Doubles Device Sw. Frequency
- FC Voltage Balancing Possible also for DC Output (!)

Risk of Transistor Overvoltage for Steep DC-Voltage Changes
Remark

Double-Bridge Inverter (1)

- 3L-Characteristic of Motor Phase Voltages
- Unfolder / 6-Pulse Operation of Bridge #2 \(\rightarrow\) Effectively Doubles DC Link Voltage (!)

- Requires Open-End Motor Windings \(\rightarrow\) Best Suited for Motor Integr. Inverters (!)
Remark

Double-Bridge Inverter (2)

- Comparison to Conv. 2-Level Inverter + Front-End DC/DC Boost-Stage

\[ U_b = 40V...120V \]
\[ P = 1.0kW \]
\[ f_s = 300kHz \text{ (200V EPC GaN)} \]
\[ f_o = 5kHz \]

\[ \frac{1}{2}U \]

\[ U \]

Advantages — Lower Sw. Losses & Lower # of Filter Inductors
Mapping of Switching Device Properties into Converter Performance
SiC/GaN Figure-of-Merit (D-FOM)

- Min. Losses @ Def. $f_{sw}$ & Load Current $\rightarrow$ Opt. Chip Area
- Consideration of 2-Level Topology

$$P_{semi} = I_{rms}^2 \frac{R_{on}'(U_{dc})}{A_{chip}} + A_{chip} C_{oss,Q}(U_{dc}) U_{dc}^2 f_{sw} \bigg|_{2L} \Rightarrow P_{semi,min_{2L}} = 2I_{rms}^2 U_{dc} \sqrt{f_{sw}} \bigg|_{2L} \frac{R_{on}'(U_{dc}) C_{oss,Q}(U_{dc})}{D - FOM_{2L}}$$

$$D - FOM_{2L} = \frac{1}{\sqrt{R_{on}' C_{oss,Q}}}$$

- Higher Device Performance (D-FOM) for Lower Blocking Capability
Multi-Level Converter Scaling

- **1/N Scaling of Blocking Voltage** → Lower $R_{DS(on)}$ Semiconductors ($R_{on} \sim U_B^2$)
- **Eff. Increase of Sw. Frequency** → $f_{sw,eff} = N f_{sw}$ (individual device)
- **Larger Chip Area and/or Smaller $L_0$**

$N = \# \text{ of Levels} - 1$

- **$D$-FOM** for $N+1$ Levels = $D$-FOM ($U_{dc}/N$) → Results in ML-Performance Dependent on $N$ (X-FOM)

# of Levels = 2

- \# = 3
- \# = 5
- \# = 7

\[U_{dc} \rightarrow \frac{U_{dc}}{N} \rightarrow i_L \rightarrow N \rightarrow U_{dc}/N \rightarrow u_{out} \rightarrow f_{sw,eff} = N f_{sw} \rightarrow f_{sw} \text{ individual device} \rightarrow R_{DS(on)} \sim U_B^2 \rightarrow D-FOM \rightarrow \text{ML-Performance Dependent on } N \rightarrow X-FOM \]
**X-FOM of Multi-Level FC Inverters**

- Quantifies Bridge-Leg Performance of (N+1)-Level FC Converters

\[ P_{\text{semi,min,ML}} \approx \frac{1}{N^{1.5}} P_{\text{semi,min,2L}} \]

\[ A_{\text{chip,ML}} \approx N^{1.5} A_{\text{chip,2L}} \]

\[ N = \# \text{ of Levels} - 1 \]

**Compared to 2-Level Benchmark @ Same Filter Ind. Volt-Seconds**

\[ D - \text{FOM}(U_B) = \frac{1}{\sqrt{R_m(U_B)C_m(U_B)}} \]

\[ X - \text{FOM}(U_B,N) = N \cdot D - \text{FOM}(\pm U_B) \]

\[ P_{\text{semi,min}|\text{ML}} = \frac{2f_{\text{sw}} C_{\text{sw}}}{N \cdot D - \text{FOM}\left(\frac{U_B}{N}\right)} \]
7-Level Flying Cap. 200V GaN Inverter (1)

- DC-Link Voltage: 800V
- Rated Power: 2.2 kW / Phase
- 99% Efficiency → Natural Convection Cooling (!)

- High Effective Sw. Frequency (6 x 30kHz = 180kHz) → Small Filter Inductor $L_0$

260 W/in³
7-Level Flying Cap. 200V GaN Inverter (2)

- DC-Link Voltage  800V
- Rated Power  2.2 kW / Phase
- 99% Efficiency → Natural Convection Cooling

- Pareto Optimization Indicates Adv. Over 3L Topology  → “3 Levels are NOT Enough (!)”

Power Density (kW/l)

Efficiency (%)

260 W/in³
Quasi-2L/3L
Flying Capacitor Inverter
Quasi-2L & Quasi-3L Inverters (1)

- **Operation of N-Level Topology in 2-Level or 3-Level Mode**
- **Intermediate Voltage Levels Only Used During Sw. Transients**
- **Applicability to All Types of Multi-Level Converters**

- Schweizer (2017)

**ABB**

- Reduced Average $dv/dt \rightarrow$ Lower EMI / Lower Reflection Overvoltages
- Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors
- Low Voltage/Low $R_{DS(on)}/$Low $\$$ MOSFETs $\rightarrow$ High Efficiency / No Heatsinks / SMD Packages
Quasi-2L & Quasi-3L Inverters (2)

- Operation of 5L Bridge-Leg Topology in Quasi-3L Mode
- Intermediate Voltage Levels Only Used During Sw. Transients
- Applicability to All Types of Multi-Level Converters

- Schweizer (2017)

ABB

3.3kW @ 230V rms/50Hz
Equiv. $f_s = 48$ kHz

3.5kW/dm$^3$
Eff. $\approx 99\%$

SMD 150V Si-MOSFETs

- Reduced Average $dv/dt \rightarrow$ Lower EMI / Lower Reflection Overvoltages
- Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors
- Low Voltage/Low $R_{DS(on)}/$Low $\$$ MOSFETs $\rightarrow$ High Efficiency / No Heatsinks / SMD Packages
**Quasi-2L & Quasi-3L Inverters (3)**

- Operation of 5L Bridge-Leg Topology in Quasi-3L Mode
- Intermediate Voltage Levels Only Used During Sw. Transients
- Applicability to All Types of Multi-Level Converters

- Schweizer (2017)  
  ABB

- Reduced Average $dv/dt \rightarrow$ Lower EMI / Lower Reflection Overvoltages
- Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors
- Low Voltage/Low $R_{DS(on)}$/Low $\$$ MOSFETs $\rightarrow$ High Efficiency / No Heatsinks / SMD Packages

3.3kW @ 230V<sub>rms</sub>/50Hz  
Equiv. $f_S = 48$kHz

3.5kW/dm$^3$  
Eff. $\approx 99\%$
Quasi-2L & Quasi-3L Inverters (4) - Schweizer (2017)

- Operation of 5L Bridge-Leg Topology in Quasi-3L Mode
- Intermediate Voltage Levels Only Used During Sw. Transients
- Applicability to All Types of Multi-Level Converters

Operation @ 3.2kW

- Conv. Output Voltage
- Sw. Stage Output Voltage
- Flying Cap. (FC) Voltage
- Q-FC Voltage (Uncntrl.)
- Output Current
- Conv. Side Current

- Reduced Average dv/dt → Lower EMI / Lower Reflection Overvoltages
- Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors
- Low Voltage/Low $R_{DS(on)}/Low$ MOSFETs → High Efficiency / No Heatsinks / SMD Packages

ETH Zürich
Motor-Integrated Modular Inverter
Motor-Integrated Modular Inverter

- Machine/Inverter Fault-Tolerant VSD
- Motor-Integr. Low-Voltage Inverter Modules
- Very-High Power Density / Efficiency
- Supply of 3-Φ Winding Sets / Low-C Buffer Cap.

- Rated Power 45kW / $f_{out} = 2\text{kHz}$
- DC-Link Voltage 1 kV

$\rightarrow$ Evaluate Machine Concept (PMSM vs. SRM etc.) / Wdg Topologies / Filter Requ. / etc.
Motor-Integrated Inverter Demonstrator

- **Rated Power**: 9kW @ 3700rpm
- **DC-Link Voltage**: 650V...720V
- **3-Φ Power Cells**: 5+1
- **Outer Diameter**: 220mm

Main Challenge — Thermal Coupling/Decoupling of Motor & Inverter

- Axial Stator Mount
- 200V GaN e-FETs
- Low-Capacitance DC-Links
- 45mm x 58mm / Cell
**Ultra-Compact Power Module with Integrated Filter**

650V GaN E-HEMT Technology

\[ f_{S,\text{eff}} = 4.8 \text{MHz} \]

\[ f_{\text{out}} = 100 \text{kHz} \]
Integrated Filter GaN Half-Bridge Module (1)

- Minimization of Filter Volume by Series & Parallel Interleaving & Extreme Sw. Frequency
- Handling of DC Output Requires Flying Capacitor Approach for Series Interleaving

\[ f_{s,\text{eff}} = (M-1) \cdot f_s \]

- \( f_s \) is the switching frequency
- \( M \) is the number of levels
- \( N \) is the number of parallel branches

\[ f_{s,\text{eff}} = N \cdot f_s \]

Target: Best Combination of ML-Level Bridge Legs (M Levels) & Parallel Branches (N)
**Integrated Filter GaN Half-Bridge Module (2)**

- Analysis of Best Combination of Levels \( M \) & Parallel Branches \( N \)
- Application of GaN Semiconductor Technology
- \( U_{DC} = 800V, \ P=10kW, \ \Delta u_{out,pp} = 1\%, \ f_{S,eff} = 4.8MHz \)

\[ @ C_{filt} = 90nF = \text{const.} \]

\[ \rightarrow L_{filt} = 1.26uH \text{ Fixed in Order to Limit Branch Current Ripple for High } N \]

\[ \rightarrow \text{Selection of } M=3 / N=3 \text{ Considering Efficiency / Filter Volume Trade-Off} \]
**Integrated Filter GaN Half-Bridge Module (3)**

- Selection of \( M=3 / N=3 \) Considering Efficiency / Filter Volume Trade-Off
- \( N \cdot L_{\text{filt}}=3.3\mu H \) of Branch Inductance / \( C_{\text{filt}}=90\text{nF} \)
- 650V GaN E-HEMT Technology
- \( f_{S,\text{eff}}=4.8\text{MHz} \)

\[
f_{S,\text{eff}} = N \cdot (M-1) \cdot f_s
\]

- Design for Max. Output Frequency of \( f_{\text{out}} = 100\text{kHz} (!) \) @ Full-Scale Voltage Swing

\( V_L < 15\% \)
\( I_C < 30\% \)
**Integrated Filter GaN Half-Bridge Module (4)**

- **Demonstrator System**
  - 650V GaN Power Semiconductors
  - Volume of ≈180cm³ (incl. Control etc.)
  - H₂O Cooling Through Baseplate

- Operation @ $f_{out}=100$kHz ($f_{s, eff} = 4.8$MHz)

- $≈ 50$kW/dm³
Buck-Boost Inverter Topologies

Z-Source Inverter etc.
Star-Point DC-Source Inverter
Y-Inverter
**Motivation**

- **General / Wide Applicability**
  - Adaption of (Load-Dependent) Supply Voltage & Motor Voltage
  - Wide Speed Range  \(\rightarrow\) Wide Output Voltage Range

- **No Add. Converter for Voltage Adaption**  \(\rightarrow\) Single-Stage Energy Conversion
"Outside-the-Box" Topologies

- **Z-Source Inverter** → Shoot-Through States Utilized for Boost Function
- **Higher Component Stress** Eff. Limits Boost Operation to $\approx 120\% U_{in}$

![Diagram of Z-Source Inverter](source: F.Z. Peng / 2003, J. Rabkowski / 2007)

- **3-Φ Back-End DC/AC Cuk-Converter**


- **Integration** Typ. Results in Higher Comp. Stresses & Complexity / Lower Performance
Boost Converter DC-Link Voltage Adaption

- Inverter-Integr. DC/DC Boost Conv. → Higher DC-Link Voltage / Lower Motor Current
- Access to Motor Star-Point & Specific Motor Design Required
- No Add. Components

Explicit Front-End DC/DC Boost-Stage

Source: J. Pforr et al. / 2009
Source: www.rick-gerber.com
Source: R.W. Erickson et al. / 1986

→ Analyze Coupling of the Control of Both Converter Stages → “Synergetic Control”
Y-Inverter
**General Remarks**

- **Generation of AC-Voltages Using Unipolar Bridge-Legs**
- **Open Machine Starpoint → Allows to Introduce a Voltage Offset Against DC-**

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**Source:** Cuk (1982)

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Fig. 7. New three-phase switching amplifier. Three bidirectional dc-dc converters, with their own modulators, driven by a set of three-phase sine waves, constitute three phase voltages around the differential load.

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Fig. 8. (a) Line-to-ground and (b) line-to-line voltages generated by the new three phase power amplifier. The dc component of the line-to-ground voltages automatically disappears in line-to-line voltages which are pure ac.

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- **3-Φ Inverter → 3 x DC/DC Conv. (Phase) Modules**
Y-Inverter Derivation (1)

- Generation of AC-Voltages Using Unipolar Bridge-Legs
- Open Machine Starpoint → Allows to Introduce Voltage Offset Against Negative DC-Bus

- Replace Conv. Inv. Buck-Type Bridge-Legs → Buck-Boost DC/DC Conv. (Phase) Modules
Y-Inverter Derivation (2)

- **Generation of AC-Voltages Using Unipolar Bridge-Legs**

- Switch-Mode Operation of Buck OR Boost Stage $\rightarrow$ Quasi Single-Stage Energy Conversion (!)
- 3-Φ Continuous Sinusoidal Output / Low EMI $\rightarrow$ No Shielded Cables / No Motor Insul. Stress
- Standard Bridge-Legs / Building Blocks $\rightarrow$ 1.2kV SiC MOSFETs
Sinusoidal Modulation

- **Y-Inverter**

- **Motor Winding Voltages**

- **Const. DC Offset** → **Strictly Positive Output Voltages** $u_{aN}, u_{bN}, u_{cN}$

- **Mutually Exclusive Operation of the Half-Bridges** → **Low Switching Losses**
**Buck-Operation** $u_{an} < U_i$

- **Phase-Module**

- **Motor Winding Voltages**

- **Voltage-Source-Type Operation**
- **Boost Bridge-Leg High-Side Switch Cont. ON** → **Quasi Single-Stage Energy Conversion**
**Boost-Operation** \( u_{an} > U_i \)

- **Phase-Module**

- **Motor Winding Voltages**

- **Current-Source-Type Operation**

- **Buck Bridge-Leg High-Side Switch Cont. ON → Quasi Single-Stage Energy Conversion**
**Discontinuous Modulation**

- **Y-Inverter**

- **Motor Winding Voltages**

- **Clamping of Each Phase for 1/3 of the Fund. Period** → **Low Switching Losses (!)**
- **Non-Sinusoidal Module Output Voltages / Sinusoidal Line-to-Line Voltages**
**Y-Inverter Control**

- Control Structure

```
- (i) Motor dq control
- (ii) Output Voltage Control
- (iii) Inductor Current Control
- (iv) "Democratic" Buck-Boost Modulator
```

"Democratic Control" of $i_L$ → Seamless Transition Between Buck & Boost Operation
Y-Inverter Prototype (1)

- **Demonstrator Specifications**
  - Wide DC Input Voltage Range \(\rightarrow 400...750\text{V}_{\text{DC}}\)
  - Max. Input Current \(\rightarrow \pm 15\text{A}\)

- **Max. Output Power** \(\rightarrow 6...11\text{ kW} \text{ (Dep. on } V_{\text{in}}\text{)}\)
- **Output Frequency Range** \(\rightarrow 0...500\text{Hz}\)
- **Output Voltage Ripple** \(\rightarrow 3.2\text{V Peak @ Output of Add. LC-Filter}\)
**Y-Inverter Prototype (2)**

- DC Voltage Range $400...750\text{V}_{\text{DC}}$
- Max. Input Current $\pm 15\text{A}$
- Output Voltage $0...230\text{V}_{\text{rms}}$ (Phase)
- Output Frequency $0...500\text{Hz}$
- Sw. Frequency $100\text{kHz}$
- $3\times$ SiC $(75\Omega)/1200\text{V}$ per Switch
- IMS Carrying Buck/Boost-Stage Transistors & Commutation Caps & $2^{nd}$ Filter Ind.

**Dimensions** → $160 \times 110 \times 42 \text{mm}^3$ ($15\text{kW}/\text{dm}^3$, $245\text{W}/\text{in}^3$)
**Measurement Results (1)**

- **Stationary Operation**

\[ U_{DC} = 400V \]
\[ U_{AC} = 400V_{rms} \text{ (Motor Line-to-Line Voltage)} \]
\[ f_0 = 50Hz \]
\[ f_S = 100kHz / DPWM \]
\[ P = 6.5kW \]

\[ U_{DC} \]
\[ i_L \]
\[ u_{DC} \]
\[ u_{S,a} \]

\[ u_{ab} \]
\[ \Delta u_{ab} \]

**Line-to-Line Output Voltage Ripple < 3.2V**
Measurement Results (2)

- Transient Operation

\[ U_{DC} = 400V \]
\[ U_{AC} = 400V_{rms} \text{ (Motor Line-to-Line Voltage)} \]
\[ f_0 = 50Hz \]
\[ f_S = 100kHz / \text{DPWM} \]
\[ P = 6.5kW \]

Dynamic Behavior V-f Control & Voltage Ampl. Step
**EMI-Limits (VSD Product Standard)**

- IEC 61800-3 → Product Standard for Variable-Speed Motor Drives
- EMI Emission Limits → Grid Interface (GI) and Power Interface (PI)
- Application → Residential (C1) or Industrial (C2)

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**EMI-Filter Design for Unshielded Cables > 2m and Resid. Applications (Cond. & Rad.)**

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**Conducted EMI Limits**

- **Grid Interface**
  - C1: Residential (CISPR Class B)
  - C2: Industrial (CISPR Class A)

- **Power Interface**
  - C1*: C1 & Unshielded Cables > 2m (CISPR Class A + 1dBμV)

**Radiated EMI Limits**

- **Overall System**
  - C1: Residential (CISPR Class B)
  - C2: Industrial (CISPR Class A)
Conducted EMI-Filter Design (1)

- Calculation of Conducted EMI w/o EMI-Filter (@ $f_{out} = 50$Hz)

$\rightarrow$ >30dB Attenuation @ 200kHz ($2f_s$) Needed

$\rightarrow$ Additional Single-Stage EMI-Filter for Conducted EMI Compliance
**Conducted EMI-Filter Design (2)**

- Separate Cond. DM & CM EMI-Filter on DC-Side & DC-Minus Ref. EMI-Filter on AC-Side

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- **Low Add. EMI Filter Volume** — 74 cm³ for Each Filter (incl. Toroid. Rad. EMI Filter)
- **Total Power Density Reduces** — 15 kW/dm³ (740 cm³) → 12 kW/dm³ (890 cm³)
Experimental Results - Conducted EMI

- Measurements of the Cond. EMI Noise on the AC-Side (QP, with 50Hz AC-LISN)

⇒ Small 80uH CM-Ind. Added on AC-Side - (3cm³ of Add. Volume = 0.5% of Converter Vol.)
⇒ Conducted EMI with Unshielded Motor Cable Fulfilled
**Measurement of Radiated EMI-Noise (1)**

- Equipment Under Test (EUT) Placed on Wooden Table with Specified Arrangement
- CM Absorption Devices (CMAD) Terminate All Cables on AC- & DC-Side (Total $l_{\text{cable}} \approx 1.5m$)
- Measurement of Radiated Noise with Antenna in 3m Distance

Either Open-Area Test Site (OATS) or Special Semi-Anechoic Chamber (SAC) Needed

Alternative Pre-Compliance Measurement Method
Measurement of Radiated EMI-Noise (2)

- CM-Currents NOT Returning IN THE CABLE are Dominant Source of Radiation
- Relation Between Radiated Electric Field and CM-Currents (!)

\[ E = \begin{cases} \frac{\mu_0 \cdot f \cdot l_{\text{cable}} \cdot I_{cm}}{r} & \frac{\lambda}{4} \leq l_{\text{cable}} \\ \frac{\mu_0 \cdot c_0}{4} \cdot I_{cm} & \frac{\lambda}{4} > l_{\text{cable}} \end{cases} \]

[Electromagnetic Compatibility Engineering, H. Ott]

- Max. Allow. El. Field Strength of 40dBuV/m \(\Rightarrow\) Max. CM-Current of 3.5uA (11dBuA)
- Current Probe Impedance of 6.3\(\Omega\) (F-33-1) \(\Rightarrow\) Max. Noise Volt. of 26dBuV @ Test Receiver

[Fischer FCC F-33-1] up to 250MHz
\(Z_{\text{nom}} = 6.3\Omega\)
**Radiated EMI-Filter Design (1)**

- **High Freq. CM-Filter** Needed to Limit Radiated EMI, i.e. CM-Currents < 3.5μA for f > 30MHz
- **Radiated EMI @ 30MHz Still Measureable with LISN**, i.e. 3.5μA @ 50Ω = 45dBμV

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**Assume Worst-Case CM-Noise of 74dBμV @ 30MHz** → **Attenuation of -29dB Needed**

**Considering Additional Attenuation Margin** → **Cut-Off Freq. Below 3MHz**
"Radiated EMI-Filter Design (2)"

- Single-Stage HF CM-Filter on DC-Side and AC-Side
- Plug-On CM-Cores (NiZn-Ferrites) → Low Parasitics & Good HF-Att. up to 1GHz

Additional EMI Filter Volume Already Considered with Conducted EMI Filter

Total Power Density Slightly Reduces — 15kW/dm³ → 12kW/dm³
**Experimental Results - Radiated EMI**

- Y-Inverter Placed in Metallic Enclosure ➔ Emulate Housing, but UNshielded Cables (!)
- Measurement Setup ➔ According IEC 61800-3
- Alternative Measurement Principle ➔ Conducted CM-Current Instead of Radiation

- Already Noticeable Noise Floor
- HF-Emissions Well Below Equivalent EMI-Limit ➔ Next Step: Verification Using Antenna
Efficiency Measurements

- Dependency on Input Voltage & Output Power Level

\[ U_{DC} = 400V / 600V \]
\[ U_{AC} = 230V_{rms} \text{ (Motor Phase-Voltage)} \]
\[ f_S = 100kHz \]

Multi-Level Bridge-Leg Structure for Increase of Power Density @ Same Efficiency
Remark — 3-Φ Buck-Boost Current Source Inverter

- Y-Inverter — Fully Phase Modular (Buck-Stage / Current Link / Boost-Stage)
- 3-Φ Integrated Concept → Buck-Stage & 3-Φ Current DC-Link (Boost) Inverter

● Advantages → Single Inductor & Applicability of Future Monolithic Bidir. GaN Switches
Thank you!