Google/IEEE Little-Box Challenge

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Outline

► The Google Little Box Challenge
► ETH / FH-IZM / Fraza Team
► Converter Topology / Control
► New Component Technologies
► Construction
► Experimental Results
► Evaluation / Optimization
► Concepts of Other Finalists
► Conclusions
The **Google** Little Box Challenge

*Requirements*

*Grand Prize*

*Team*
LiTTLE BOX
CHALLENGE

- Design / Build the 2kW 1-Φ Solar Inverter with the Highest Power Density in the World
- Power Density > 3kW/dm³ (50W/in³)
- Efficiency > 95%
- Case Temp. < 60°C
- EMI FCC Part 15 B

Push the Forefront of New Technologies in R&D of High Power Density Inverters
LiTTLE BOX CHALLENGE

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- Push the Forefront of New Technologies in R&D of High Power Density Inverters
The Grand Prize

- Highest Power Density (> 50W/in$^3$)
- Highest Level of Innovation

$1,000,000

Timeline

- Challenge Announced in Summer 2014
- 2000+ Teams Registered Worldwide
- 100+ Teams Submitted a Technical Description until July 22, 2015
- 18 Finalists (3 No-Shows)
The Grand Prize

- Highest Power Density (> 50W/in³)
- Highest Level of Innovation

* GaN
* MHz
* Ceramic Caps
* HF Inductors
* etc.

Explore New Technologies
Secure Intellectual Property
Publish Key Results

Timeline
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- 2000+ Teams Registered Worldwide
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- 18 Finalists (3 No-Shows)
18 Finalists Invited to NREL / USA
Presentations on Oct. 21, 2015
Winner → Feb. 29, 2016
Inverter

- **Multi-National Team**
  - Germany
  - Switzerland
  - Slovenia

  ![Fraunhofer IZM](image)
  ... Packaging, Embedding, EMI, etc.

  ![ETH Zürich](image)
  ... Topologies, Circuits, Control, Software, System Testing, etc.

  ![Fraza d.o.o.](image)
  ... HF Inductor Technology

- **Acknowledgment**
  - Components
  - Academic Award (10)
  - Donation (6)
Derivation of Converter Topology
Derivation of Output Stage Topology (1)

- DC/AC Buck Converter & Output Frequency “Unfolder”

- Temporary PWM Operation of Unfolder @ \( U < U_{\text{min}} \)
- CM Component of Output Voltage \( v_0 \)
Derivation of Output Stage Topology (2)

- Full-Bridge Output Stage
- Modulation of Both Bridge Legs

- DM Component of $u_1$ and $u_2$ Defines Output $u_0$
- CM Component of $u_1$ and $u_2$ Represents Degree of Freedom of the Modulation (!)
DC-Side Power Pulsation Buffering

- Compensation of 120Hz Output Power AC Component → Constant DC Supply Current

- Parallel or Series / Passive or Active Buffer Concepts
- Parallel Approach for Limiting Voltage Stress on Full-Bridge Semiconductors
**DC-Side Passive Power Pulsation Buffer**

- Electrolytic Capacitor

\[ i_i = i_{C} \]

\[ V_{C,\text{max}} \]

\[ \Delta V_{C} \]

\[ S_0 = 2.0 \text{ kVA} \]

\[ \cos \Phi_0 = 0.7 \]

\[ V_{C,\text{max}} = 450 \text{ V} \]

\[ \frac{\Delta V_{C}}{V_{C,\text{max}}} = 3\% \]

- \( C > 2.2 \text{mF} / 166 \text{ cm}^3 \) → Consumes 1/4 of Allowed Total Allowed Volume!
DC-Side Active Power Pulsation Buffer

- Large Voltage Fluctuation Foil or Ceramic Capacitor
- Buck-Type (Lower Voltage Levels) or Boost-Type DC/DC Interface Converter

Significantly Lower Overall Volume Compared to Electrolytic Capacitor

CeraLink TDK

$108 \times 1.2 \mu F / 400 \, V$

$C_k \approx 140 \mu F$

$V_{Ck} = 23.7 \, cm^3$

ETH zürich
DC-Side Active Power Pulsation Buffer

- Cascaded Control Structure

- P-Type Resonant Controller
- Feedforward of Output Power Fluctuation
- Underlying Input Current ($i_i$) / DC Link Voltage ($u_C$) Control
AC-Side Power Pulsation Buffering

- Compensation of 120Hz Output Power AC Component → Constant DC Supply Current

- CM Reactive Power of Output Filter Capacitors used for Comp. of Load Power Pulsation
- CM Reactive Power prop. 2 C
- DM Reactive Power prop. ½ C
Modulation
ZVS of Output Stage / TCM Operation

- TCM Operation for Resonant Voltage Transition @ Turn-On/Turn-Off

- Requires Only Measurement of Current Zero Crossings, \( i = 0 \)
- Variable Switching Frequency Lowers EMI
4D-Interleaving

- Interleaving of 2 Bridge Legs per Phase - Volume / Filtering / Efficiency Optimum
- Interleaving in Space & Time – Within Output Period
- Alternate Operation of Bridge Legs @ Low Power
- Overlapping Operation @ High Power

Implemented Converter Topology / Output Control
Final Converter Topology

- Interleaving of 2 Bridge Legs per Phase
- Active DC-Side Buck-Type Power Pulsation Buffer
- 2-Stage EMI AC Output Filter

- ZVS of All Bridge Legs @ Turn-On/Turn-Off in Whole Operating Range (4D TCM Interleaving)
- Heatsinks Connected to DC Bus / Shield to Prevent Cap. Coupling to Grounded Enclosure
Technologies

Power Semiconductors
Passives
Cooling

DSP/FPGA
**Selection of Switching Frequency**

- Significant Reduction in EMI Filter Volume for Increasing Sw. Frequency

- Doubling Sw. Fequ. $f_s$ Cuts Filter Volume in Half
- Upper Limit due to Digital Signal Processing Delays / Inductor & Sw. Losses – Heatsink Volume
Power Semiconductors

- 600V IFX Normally-Off GaN GIT - ThinPAK8x8
- 2 Parallel Transistors / Switch
- Antiparallel CREE SiC Schottky Diodes

- 1.2V typ. Gate Threshold Voltage
- 55 mΩ \( R_{DS,\text{on}} \) @ 25°C, 120mΩ @ 150°C
- 5Ω Internal Gate Resistance

\[ \frac{dv}{dt} = 500kV/\mu s \]

- CeraLink Capacitors for DC Voltage Buffering
Advanced Gate Drive (1)

- Fixed Negative Turn-off Gate Voltage Independent of Switch Frequency and Duty Cycle
- Extreme dv/dt Immunity (500 kV/μs) Due to CM Choke at Signal Isolator Input

- Total Prop. Delay < 30ns incl. Signal Isolator, Gate Drive, and Switch Turn-On Delay
Advanced Gate Drive (2)

- Fixed Negative Turn-off Gate Voltage Independent of Sw. Frequency and Duty Cycle
- Extreme dv/dt Immunity (500 kV/μs) Due to CM Choke at Signal Isolator Input

Triangular Current Mode (TCM) Operation at No Load → ZVS and No Free Ringing of $u_{T+}$, $u_{T-}$, or $i_L$
High Frequency Inductors (1)

- Multi-Airgap Inductor with Patented Multi-Layer Foil Winding Minimizing Prox. Effect
- Very High Filling Factor / Low High Frequency Losses
- Magnetically Shielded Construction Minimizing EMI

- \( L = 10.5 \mu \text{H} \)
- 2 x 8 Turns
- 24 x 80\( \mu \text{m} \) Airgaps
- Core Material DMR 51 / Hengdian
- 0.61mm Thick Stacked Plates
- 20 \( \mu \text{m} \) Copper Foil / 4 in Parallel
- 7 \( \mu \text{m} \) Kapton Layer Isolation
- 20m\( \Omega \) Winding Resistance / \( Q = 800 \)
- Terminals in No-Leakage Flux Area

Dimensions - 14.5 x 14.5 x 22mm\(^3\)
High Frequency Inductors (2)

IEEE TRANSACTIONS ON MAGNETICS, VOL. MAG-11, NO. 1, JANUARY 1975

The Origin of the Increase in Magnetic Loss Induced by Machining Ferrites

JOHN E. KNOWLES

- Cutting of Ferrite Introduces Mechanical Stress in the Surface (5μm Layer)
- Significant Increase of the Loss Factor
- Reduction by Polishing / Etching

Comparison of Temp. Increase of a Bulk and a Sliced Sample @ 70mT / 800kHz
Thermal Management (1)

- 30mm Blowers with Axial Air Intake / Radial Outlet
- Full Optimization of the Heatsink Parameters
  - 200um Fin Thickness
  - 500um Fin Spacing
  - 3mm Fin Height
  - 10mm Fin Length
  - CSPI = 37 W/(dm³.K)
  - 1.5mm Baseplate

- CSPI_{eff} = 25 W/(dm³.K) Considering Heat Distribution Elements
- Two-Side Cooling → Heatsink Temperature = 52°C @ 80W (8W by Natural Convection)
Thermal Management (2)

- CSPI = 37 W/(dm\(^3\).K)
- 30mm Blowers with Axial Air Intake / Radial Outlet
- Full Optimization of the Heatsink Parameters
- CSPI\(_{\text{eff}}\) = 25 W/(dm\(^3\).K) incl. Heat Cond. Layers

Two-Side Cooling \(\rightarrow\) Heatsink Temperature = 52°C @ 80W (8W by Natural Convection)
Control Board & i=0 Detection

- Fully Digital Control - Overall Control Sampling Frequency of 25kHz
- TI DSC TMS320F28335 / 150MHz / 179-pin BGA / 12mmx12mm
- Lattice FPGA LFXP2-5E / 200MHz / 86-pin BGA / 8mmx8mm

- TCM Current / Induced Voltage / Comparator Output

- i=0 Detection of TCM Currents Using R4/N30 Saturable Inductors
- Galv. Isolated / Operates up to 2.5MHz Switching Frequency / <10ns Delay
Power Pulsation Buffer Capacitor

- High Energy Density 2\textsuperscript{nd} Gen. 400V\textsubscript{DC} CeraLink Capacitors Utilized as Energy Storage
- Highly Non-Linear Behavior $\rightarrow$ Opt. DC Bias Voltage of 280VDC
- Cap. Losses of 16W @ 2kVA Output Power

- 108 x 1.2\textmu F / 400 V
- 23.7cm\textsuperscript{3} Capacitor Volume

\textbf{ETH zürich}
Auxiliary Supply & Measurements

- ZVS Constant 50% Duty Cycle Half Bridge with Synchr. Rectification
- Compact / Efficient / Low EMI

- 10W Max. Output Power
- 380V...450V Input Operating Range
- 13.6V...16.8V DC Output in Full Inp. Voltage / Output Power Range
- 90% Efficiency @ $P_{\text{max}}$

- 19mm x 24mm x 4.5mm (2cm$^3$ Volume)
Experimental Results

Hardware
Output Voltage/Input Current Quality
Thermal Behavior
Efficiency
EMI
Little-Box Prototype I

- Electrolytic Capacitors as DC-Side Power Pulsation Buffer

- 7.3 kW/dm³
- 9.7cm x 9.1cm x 3.1cm
- 97.5% Efficiency @ 2kW
- $T_c = 58^\circ C @ 2kW$

- $\Delta u_{DC} = 2.85\%$
- $\Delta i_{DC} = 15.4\%$
- $THD+N_U = 2.6\%$
- $THD+N_I = 1.9\%$

- Compliant to All Original Specifications (!)
- No Low-Frequ. CM Output Voltage Component
- No Overstressing of Components
- All Own IP / Patents
Measurement Results I-(1)

- Electrolytic Capacitors as DC-Side Power Pulsation Buffer

■ Compliant to All Original Specifications (!)
Measurement Results I-(2)

- Electrolytic Capacitors as DC-Side Power Pulsation Buffer

Heating of System Lower than Specified Limit ($T_{c,\text{max}} = 60^\circ\text{C}$ @ $T_{\text{amb}} = 30^\circ\text{C}$)

$\eta_w = 96.4\%$ Weighted Efficiency

Heating of System Lower than Specified Limit ($T_{c,\text{max}} = 60^\circ\text{C}$ @ $T_{\text{amb}} = 30^\circ\text{C}$)
Measurement Results I-(3)

- Electrolytic Capacitors as DC-Side Power Pulsation Buffer

P_{out} = 400W

Compliant to All Original Specifications (!)
**Little-Box Prototype II-(1)**

- Active DC-Side Power Pulsation Buffer

- 8.2 kW/dm³
- 8.9cm x 8.8cm x 3.1cm
- 96.3% Efficiency @ 2kW
- $T_c=58^\circ \text{C} @ 2kW$

- $\Delta u_{\text{DC}}=1.1\%$
- $\Delta i_{\text{DC}}=2.8\%$
- $\text{THD}+N_U=2.6\%$
- $\text{THD}+N_I=1.9\%$

- Compliant to All *Original Specifications* (!)
  - No Low-Frequ. CM Output Voltage Component
  - No Overstressing of Components
  - All Own IP / Patents

★ 135 W/in³
Little-Box Prototype II-(2)

- Active DC-Side Power Pulsation Buffer

- 8.2 kW/dm$^3$
- 8.9cm x 8.8cm x 3.1cm
- 96.3% Efficiency @ 2kW
- $T_c=58°C @ 2kW$
- $\Delta u_{DC} = 1.1%$
- $\Delta i_{DC} = 2.8%$
- $THD+N_U = 2.6%$
- $THD+N_I = 1.9%$

Compliant to All Original Specifications (!)
- No Low-Frequ. CM Output Voltage Component
- No Overstressing of Components
- All Own IP / Patents

★ 135 W/in$^3$
Measurement Results II-(1)

- Active DC-Side Power Pulsation Buffer

![Graphs showing measurement results](image)

- Ohmic Load / 2kW

**Output Current**
- Inductor Current Bridge Leg 1-1
- Inductor Current Bridge Leg 1-2

**DC Link Voltage (AC-Coupl., 2V/Div.)**
- Buffer Cap. Voltage
- Buffer Cap. Current
- Output Voltage

- Compliant to All *Original* Specifications (!)
Measurement Results II-(2)

- Active DC-Side Power Pulsation Buffer

- Start-Up and Shut-Down (No Load Operation)
Evaluation

Volume Distribution
Loss Distribution
Evaluation / Optimization Potential

- **Volume Distribution (240cm³)**

  - Power Pulsation Buffer 71.3cm³
  - Inverter Stage 169.1cm³
  - MOSFETs
  - Capacitor
  - Electronics
  - Inductor
  - Inductors
  - Electronics
  - Output Filter
  - Cooling
  - Housing
  - Others
  - MOSFETs

- **Loss Distribution (75W)**

  - Power Pulsation Buffer 28.1W
  - Inverter Stage 46.3W
  - MOSFETs
  - Capacitor
  - Electronics
  - Inductor
  - Output Filter
  - Electronics
  - Inductor

**- Large Heatsink (incl. Heat Conduction Layers)**
**- Large Losses in Power Fluctuation Buffer Capacitor (!)**
**- TCM Causes Relatively High Conduction & Switching Losses @ Low Power**
**- Relatively Low Switching Frequency @ High Power – Determines EMI Filter Volume**
Optimization

Full-Bridge TCM Interleaved
Full-Bridge TCM Not Interleaved
Full-Bridge PWM
Buck-Stage & Unfolder
Multi-Objective Optimization Results

- 135 W/in\(^3\) → 230 W/in\(^3\) (!) @ CSPI = 25 W/(dm\(^3\).K)

- No Interleaving
- PWM / Constant Switching Frequency
- X6S Capacitor Technology Employed in Power Pulsation Buffer
Other Finalists

- Topologies
- Switching Frequencies
- Power Density / Efficiency Comparison

For Detailed Descriptions:
www.LittleBoxChallenge.com
Finalists - Performance Overview

- 18 Finalists (3 No-Shows)
- 7 Groups of Consultants / 7 Companies / 4 Universities

- 70 ... 300 W/in³
- 35 kHz ... 500kHz ... 1 MHz (up to 1MHz: 3 Teams)
- Full-Bridge or DC/AC Buck Converter + Unfolder
- Mostly Buck-Type Active Power Pulsation Filters (Ceramic Caps of Electrolytic Caps)
- GaN (11 Teams) / SiC (2 Teams) / Si (2 Teams)
Finalists - Performance Overview

- 18 Finalists (3 No-Shows)
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- Mostly Buck-Type Active Power Pulsation Filters (Ceramic Caps of Electrolytic Caps)
- GaN (11 Teams) / SiC (2 Teams) / Si (2 Teams)
Category I: 300 – 400 W/in³ (1 Team)

- “Over the Edge”
- Hand-Wound Overstressed & Too Small Electrolytic Capacitors (210uF/400V)
- No Voltage Margin of Power Semiconductors (450V GaN, Hard Switching)
- 50V Voltage Source for Semicond. Voltage Stress Reduction
- Low-Freq. CM AC Output Component

- Alternate Switching of Full-Bridge Legs
- Input Cap. of Full-Bridge Used for Power Pulsation Buffering

- 256 W/in³ (400 W/in³ Claimed) / 1MHz
- Multi-Airgap Toroidal Inductors (3F46, $C_p \approx 1.5pF$)
- Bare Dies Directly Attached to Pin-Fin Heatsink
- High Speed Fan (Mini Drone Motor & Propeller)
Category I: 300 – 400 W/in³ (1 Team)

- “Over the Edge”
- Hand-Wound Overstressed Electrolytic Capacitors (210μF (?) / 400V)
- No Voltage Margin of Power Semiconductors (450V GaN, Hard Switching)
- 50V Voltage Source for Semicond. Voltage Stress Reduction

- Alternate Switching of Full-Bridge Legs
- Input Cap. of Full-Bridge Used for Power Pulsation Buffering

- 256 W/in³ (400 W/in³ Claimed) / 1MHz
- Multi-Airgap Toroidal Inductors (3F46, C_p≈1.5pF)
- Bare Dies Directly Attached to Pin-Fin Heatsink
- High Speed Fan (Mini Drone Motor & Propeller)
Category II: 200 – 300 W/in³ (4 Teams) – Example #1

- “At the Edge”
- High Complexity
- 7-Level Flying Capacitor Converter
- Series-Stacked Active Power Buffer

- 216 W/in³
- 100V GaN
- Integrated Switching Cell
- 720kHz Eff. Sw. Freq. (7 x 120kHz)
Category II: 200 – 300 W/in³ (4 Teams) – Example #2

- “At the Edge”
- Very Well Engineered Assembly (e.g. 3D-Printed Heatsink w. Integr. Fans, 1 PCB Board, etc.)
- No Low-Frequ. Common-Mode AC Output Component

- 201W / in³
- Multi-Airgap (8 Gaps) Inductors
- 900V SiC @ 140kHz (PWM, Soft & Hard Switching)
- Buck-Type Active DC-Side Power Pulsation Filter / Ceramic Capacitors (X6S)
Category III: 100 – 200 W/in³ (8 Teams) – Example

- “Advanced Industrial”
- Sophisticated 3D Sandwich Assembly incl. Cu Honeycomb Heatsink
- Shielded Multi-Stage EMI Filter @ DC Input and AC Output
- No Low-Frequ. Common-Mode AC Output Component

- 143 W/in³
- GaN @ ZVS (35kHz...240kHz)
- 2 x Interleaving for Full-Bridge Legs
- Buck-Type DC-Side Active Power Pulsation Filter (<150μF)
Category III: 100 – 200 W/in³ (8 Teams) – Example

- “Advanced Industrial”
- Sophisticated 3D Sandwich Assembly incl. Cu Honeycomb Heatsink
- Shielded Multi-Stage EMI Filter @ DC Input and AC Output
- No Low-Frequ. Common-Mode AC Output Component

- 143 W/in³
- GaN @ ZVS (35kHz...240kHz)
- 2 x Interleaving for Full-Bridge Legs
- Buck-Type DC-Side Active Power Pulsation Filter (<150μF)
Category IV: 50 – 100 W/in³ (1 Team)

- “Industrial”
- $400V_{\text{max}}$ Full-Bridge Input Voltage
- DC-Link Cap. Used as Power Pulsation Buffer (470uF)
- GaN Transistors / SiC Diodes (400kHz DC/DC, 60kHz DC/AC)
- Multi-Stage EMI Filter @ AC Output and $L_{\text{CM}}$ + Feed-Trough $C_{\text{CM}}$ @ DC Inp. (Not Shown)

- $\approx 70 \text{ W/ in}^3$
- 98% CEC Efficiency
- 4.4% DC Input Current Ripple
- 54°C Surface Temp. / Cooling with 10 Micro-Fans
■ Conclusions
Conclusions

There's NO Silver Bullet

- >200W/in^3 (12kW/dm^3) Achievable
- f_s < 150kHz (Constant) Sufficient
- SiC Can Also Do It
- ZVS (Partial) Helps
- Full-Bridge Output Stage
- Active Power Pulsation Buffer (Buck-Type, X6S Cap.)
- Conv. EMI Filter Structure
- Multi-Airgap Litz Wire Inductors
- DSP Can Do It (No FPGA)
- Careful Heat Management (Adv. Heat Sink, Heat Distrib., 2-Side Integr. Cooling, etc.)
- Careful Mechanical Design (3D-CAD, Single PCB, Avoid Connectors, etc.)

Overall Summary

- No (Fundamentally) New Approach
- Passives & 3D-Packaging are Finally Defining the Power Density → CIPS (!)
- Competition Timeframe Too Short for Advanced Integration
- Building a Full System Not Possible for Many Universities – High Drop Out Rate
Thank You!
Questions