(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
19 July 2001 (19.07.2001)

PCT

(10) International Publication Number
WO 01/52397 A1

(51) International Patent Classification[7]: H02M 3/00, 3/02, 3/155, 7/00, 7/42, 7/44

(21) International Application Number: PCT/IB00/00655

(22) International Filing Date: 16 May 2000 (16.05.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
A 25/2000 10 January 2000 (10.01.2000) AT

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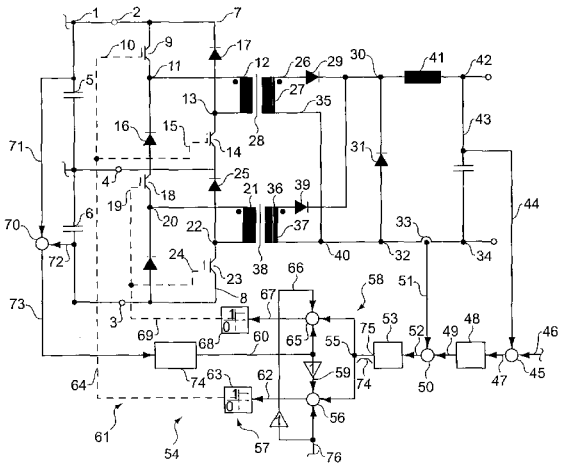
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) **Title:** METHOD AND APPARATUS FOR STABILIZATION AND MINIMIZATION OF LOSSES OF A SERIES CONNECTION OF DC/DC-CONVERTERS CONNECTED TO THE OUTPUT-SIDE PARTIAL VOLTAGES OF A THREE-LEVEL PWM RECTIFIER SYSTEM



(57) **Abstract:** A method and an apparatus for active stabilization of the voltage sharing of a series connection of DC/DC converter stages (7, 8), and a method and an apparatus for minimization of the current stress of the input capacitors (5) of DC/DC converters operating at the output of a three level converter. For each DC/DC converter there is one pulse width modulation-stage (57, 58), where at the input side summing elements get control signal defining the power flow to the secondary power circuit from a supervising output voltage controller and/or an output current controller. The symmetry controller creates a positive and negative offset of this control signal in case of an asymmetry of the partial input voltages of the DC/DC-converters. The offset controls the power flow of the DC/DC converters in a way that the DC/DC converter with higher input voltages takes less power from its input capacitor.

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METHOD AND APPARATUS FOR STABILIZATION AND MINIMIZATION OF LOSSES OF A SERIES CONNECTION OF DC/DC-CONVERTERS CONNECTED TO THE OUTPUT-SIDE PARTIAL VOLTAGES OF A THREE-LEVEL PWM RECTIFIER SYSTEM

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to a method for stabilizing the balance of the input-voltages of a series connection of DC/DC-converters, and a method for minimizing the current-stress of the input-capacitors if the DC/DC converters are connected to the output-side of a three-level Pulse Width Modulation "PWM" rectifier. A method for symmetric sharing of the switching losses between the power transistors of the DC/DC converters if the DC/DC converters are realized as two-transistor forward converters or two-transistor flyback converters is also described.

Description of the Prior Art

According to the current state of technology, DC-voltage-to DC-voltage converters (referred to herein as DC/DC-converters) with high input voltage, output isolation and low output voltage are often configured as a series connection of two partial converter systems at their primary sides. The isolated outputs of these converters are connected in parallel to feed the load. Compared to a single converter stage with high input voltage, this configuration results in the halving of the blocking voltage stress of the primary side power semiconductors, in a transformation ratio of the transformer that is advantageous concerning the coupling, and in a simply realizable high output current.

Such systems have difficulty, however, in symmetrically splitting and balancing the total input voltage lying across the input capacitors of the DC/DC-converters, because the converters show a constant power characteristic (and/or

negative differential input impedance) in the case of high control dynamics. For stable operation of the two DC/DC-converters with symmetric partial input voltages, the output voltage controller determines the same relative on-time of the power transistors of both DC/DC-converters. As a result, the DC/DC-converter connected to the higher partial input voltage takes a higher input current than the DC/DC-converter connected to the lower partial input voltage does. Because the charging current of the input capacitors of both DC/DC-converters is the same, this results in stabilization of the symmetry of the partial input voltages. A disadvantage of this passive scheme is the poor dynamic behavior of the stabilization. A further disadvantage (for example concerning a forward converter) is that the time necessary to reach a symmetric sharing of the partial input voltages is based on the size of the input capacitors and the output inductor.

If the input capacitors are not always charged at the same time, but mostly alternately (as given, for example, in case of operation of the series connection of DC/DC-converters connected to the output side of a three-level converter), and if both partial converters get the identical switching signals and/or both input capacitors are discharged at the same time, then a high current stress on the input capacitors results.

Furthermore, in a case where the DC/DC-converters are two-transistor forward converters or two-transistor flyback converters, without extra measure, the symmetric sharing of the switching losses of the transistors of the DC/DC-converters is not guaranteed. The transistors of one DC/DC-converter are connected in series. Changing into the state of demagnetization, it is possible that the same transistor, driven by the driver-stage showing a smaller delay time, always breaks the load current and/or carries the total switching losses. This results in a thermal overload of the transistor and the failure of the whole converter.

The present invention provides a method of stabilizing the sharing of the input voltage with defined dynamic behavior, and thus minimizes the current stress of the input capacitors of the series connected DC/DC-converters connected to the output side of a three-level PWM rectifier system, such that when the partial converters are two-transistor forward converters or flyback converters, there is a symmetric sharing of the switching losses of the power transistors.

SUMMARY OF THE INVENTION

According to the invention, for an actively controlled symmetric sharing of the partial input voltages, the known (state of technology) pulse-pattern for control of the DC/DC-converters is manipulated in a way that, in the case of higher voltage on the positive input capacitor one-sided connected to the positive potential of the total input voltage (compared to the voltage on the negative input capacitor one-sided connected to the negative potential of the total input voltage), the power removal from the positive capacitor increases by increasing the duration of the time of energy supply to the secondary side. At the same time, the power removal from the negative capacitor is reduced by reducing the time of energy supply to the secondary side. The dynamic of this pulse pattern-change, that is symmetrically opposite between the two DC/DC-converter systems, directly defines the dynamic of the reduction of an asymmetry (given by a difference between charging current and discharge current of the capacitors) of the partial input voltages. Alternatively, the change of the pulse-pattern can also be done in an asymmetric way. This means that only the time of energy supply of the partial DC/DC-converter at the higher potential increases, while the time of energy supply of the partial DC/DC-converter at the lower potential is not changed. Or, alternatively, the time of energy supply of the partial DC/DC-converter at the lower potential is reduced, while the pulse pattern of the partial DC/DC-converter at the higher potential is not changed.

An advantageous realization of the symmetric variant of the method can also be described in form of an electrical circuit. Here, there exists one pulse width modulated (PWM)-stage (according to standard technology) for each partial DC/DC-converter. A supervising controller defines a voltage level (control signal) that is compared to a carrier signal using a comparator. This comparison defines a rectangular shaped signal with the value zero or one. The rectangular shaped signal is the gate-signal of the power transistors of the converters, and the voltage level of the control signal defines the pulse width of the rectangular signal. Furthermore, the difference of the positive and negative partial input voltage is formed, and dynamically weighted by a symmetry-controller. The output signal of the symmetry-controller is added to the control signal input of the PWM-stage of the positive DC/DC-converter, and subtracted from the control signal input of the PWM-stage of

the negative DC/DC-converter. For example, if the positive partial input voltage is higher than the negative one, the PWM-stage of the positive DC/DC-converter increases the on-time of the power transistors of the positive DC/DC-converter, while the PWM-stage of the negative DC/DC-converter reduces the on-time of the power transistors of the negative DC/DC-converter. This results in an increase of the power supply for the positive DC/DC-converter and reduced power supply for the negative DC/DC-converter, where in connection with an equal current recharging the two input capacitors a symmetry of the partial input voltages is achieved.

Another embodiment of the invention provides for an apparatus for the symmetric sharing of the partial input voltages that is not based on control concepts, but on an expansion of the power circuit of the DC/DC-converter. The power transistors of the DC/DC-converter connect the input voltages directly to the according primary transformer winding. In this embodiment, every transformer has an additional winding with the number of turns equal to the primary winding. The additional winding of the positive DC/DC-converter is connected to the input voltage of the negative DC/DC-converter via a positive series diode, and the additional winding of the negative DC/DC-converter is connected to the input voltage of the positive DC/DC-converter via a negative series diode. The series diodes are oriented in such a way that, in case of a two-transistor forward converter for higher partial input voltage of the positive DC/DC-converter for on-state of the transistors of the positive DC/DC-converter, the diode connected in series with the additional winding of the positive converter is in on-state.

For higher partial input voltage of the negative DC/DC-converter for on-state of the transistors the diode of the negative DC/DC-converter is in on-state. As a result, the input capacitor with the lower voltage is charged from the input capacitor with higher voltage automatically and directly. Therefore, the asymmetry of the partial input voltages is eliminated in the initial stage.

In case of a four-transistor and/or full bridge configuration of the DC/DC-converters, the additional winding can also be connected to the opposite partial input voltage via a full diode bridge. This increases the effect causing symmetry, but also increases the realization effort.

Furthermore, according to the invention, it is possible in the case of a two-transistor flyback converter, to orient the series diodes in a way that, during the off-time of the transistors, the lower DC/DC-converter input voltage is charged by the magnetic energy stored in the transformer core of the DC/DC-converter with the higher partial input voltage. An advantage of this concept is the natural limitation of the value of the load current that is determined by the load condition of the system.

Another embodiment of the present invention provides a method of minimizing the current stress on the input capacitors of the series connected DC/DC-converters connected to the output side of a three-level rectifier system. To minimize the current in the capacitor, in a case when the DC/DC-converter is a two-transistor forward or flyback converter, the same transistor switching frequency is selected for the three-level rectifier and the DC/DC-converters. If the DC/DC-converters are used as a complete bridge, then the transistor switching frequency for the three-level rectifier is twice the transistor switching frequency of the DC/DC-converter. The phase displacement between the switching patterns of the two systems is defined in a way that the input currents show a maximum overlap-time concerning the charging current and discharge current-time areas. This means that the positive (negative) DC/DC-converter feeds power to the output side mainly in time intervals where the positive (negative) input capacitor is charged by the three-level rectifier. Therefore, the load current of the input capacitor is mainly (ideally totally) covered by the charging-pulses of the three-level rectifier. This results in a low current Root Mean Square ("RMS")-stress of the input capacitors and a low voltage ripple of the partial input voltages. The doubling of the switching frequency for the full bridge structure of the DC/DC-converter can be explained by the fact that during one switching period, two discharging current pulses are taken from one input capacitor, while there is only one charging current pulse for one input capacitor by the three-level rectifier during one switching period.

Accordingly, another aspect of the invention provides for an apparatus for the practical realization of the above-described method, in which the DC/DC-converter is a two-transistor forward converter with the primary-side power circuit according to the known technology. According to the invention, for each partial DC/DC-converter there is a PWM-stage. The synchronization between the switching frequency of the

three-level rectifier and the correct (optimized) loading and charging of the two input capacitors is achieved. For the PWM-stage of one DC/DC-converter, the triangular carrier signal of the input current control (according to standard technology) of the one- or three-phase three-level rectifier is used, and for the PWM-stage of the other DC/DC-converter the inverted triangular carrier signal of the input current control of the one- or three-phase three-level rectifier is used. A detailed analysis of the pulse width modulation of a three-level converter shows that in the vicinity of the positive maximum value of the triangular carrier signal of the three-level converter, only the positive output capacitor of the three-level converter (and/or the input capacitor of the positive DC/DC-converter) is charged. In the vicinity of the negative maximum value of the triangular carrier signal of the three-level converter, only the negative output capacitor of the three-level converter (and/or the input capacitor of the negative DC/DC-converter) is charged.

The control signal defining the pulse width of the DC/DC-converter is given by an output voltage controller according to standard technology (and/or by an output current controller that is underlying the output voltage controller). According to the invention, this control signal is connected to the input of a summing element, where the second input of the summing element is connected directly to the carrier signal of the three-level rectifier. The output-signal of the summing element is connected to the input of a comparator with switching threshold zero. This results in a pulse width modulated output-signal of the comparator with the values zero and one, that is connected to the gates of the two transistors of the positive DC/DC-converter. A comparator output-signal zero switches the transistors off; a comparator output-signal one switches the transistors into on-state. For the negative DC/DC-converter, there is a PWM-stage of identical structure, but the carrier signal is the inverted carrier signal of the three-level converter. As a result, in the vicinity of the positive maximum value of the carrier signal of the three-level converter, the positive DC/DC-converter takes energy from the positive input capacitor, while in the vicinity of the negative maximum value of the carrier signal of the three-level converter, the negative DC/DC-converter takes energy from the negative input capacitor. This results in synchronization of charging and discharging of an input capacitor. Because of the large compensation of charging and discharging current pulses (covering the same

time-periods) the current stress of the capacitors is minimized and their voltage ripple with switching frequency is also minimized.

In another embodiment, the invented apparatus can be used for control if the DC/DC-converters are two-transistor flyback converters.

Alternatively, according to the invention, using a two-transistor forward converter, the structure of the secondary power circuit can be simplified (and/or the realization effort can be reduced) compared to other standard configurations, because the energy supply to the output-side is done alternately by one of the two partial DC/DC-converters. Instead of separated output inductors and separated free-wheeling diodes of the DC/DC-converters, according to the invention, there is only one common output inductor for both partial systems one-sided connected to the positive potential of the output voltage, and only one free-wheeling diode with the anode connected to the negative potential of the output voltage and the cathode connected to the second terminal of the output inductor. The secondary winding of the transformer of the DC/DC-converters that carry the output current alternately are one-sided connected to the negative output voltage terminal, and each secondary winding is connected via a rectifier diode in flow direction to the cathode of the free-wheeling diode. The orientation of the winding is chosen in a way such that, in case of on-state of the primary power transistors of a DC/DC-converter, the according rectifier diode is forced into conduction.

Another embodiment of the invention provides a method for symmetric sharing of the switching losses between the switching power semiconductors structuring the DC/DC-converter as a two-transistor forward converter or a flyback converter. For both converter-types, the primary winding of the transformer of a DC/DC-converter is connected via two transistors to the according input voltages. Both transistors are gated synchronously, but in practical realization the driver stages of the two transistors show different delay times. Therefore, it is possible that the same transistor always breaks the load current and thus suffers thermal overloading. According to the invention, this overload is avoided by splitting the identical gate-signals (according to known technology) for both transistors into two signals, where the gate-signal of the first transistor (according to the former gate-signal) shows a small delay at every second turn-off instant, while the gate-signal of the second

transistor shows a small delay at every turn-off instant when the first transistor switches without delay. As a result, the two transistors switch the primary current alternately, and a symmetric sharing of the switch-off losses between the two power transistors is guaranteed. The delay time has to be higher than the maximum difference of the delay times of the driver stages and the switching times of the power transistors.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawing, which is incorporated in and constitutes a part of this specification, illustrates an embodiment of the invention and together with the description serves to explain to principles of the invention.

Fig. 1 illustrates a method and apparatus for stabilization and minimization of losses of a series connection of DC/DC-converters connected to the output-side partial voltages of a three-level PWM rectifier system.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

In the following, the invention is explained with examples and simulated results. These examples are illustrative only, and not limiting of the remainder of the disclosure in any way whatsoever.

Fig. 1 exemplifies the invented apparatus for stabilization of the symmetry of the partial input voltages of in series connected two-transistor forward converter with known configurations of the primary power circuit and of the output voltage control and output current control, realizing the invented minimization of the current stress of the input capacitors and/or the output capacitors of the three-level converter, where the two DC/DC-converters are connected.

In Fig. 1, the output circuit (1) of a three-level converter with a positive output terminal (2), a negative output terminal (3) and an output voltage center point (4) are shown, where a positive output capacitor (5) between positive output terminal (2) and center point (4) and a negative output capacitor (6) between center point (4) and negative output terminal (3) is placed. The positive capacitor (5) is the input capacitor of the positive DC/DC-converter (7) and the negative capacitor (6) is the input capacitor of the negative DC/DC-converter (8)

The positive DC/DC-converter (7) is formed at the primary side by a positive power transistor (9) with gate (10), with its collector connected to the positive input voltage terminal (2), and with its emitter (11) connected to the according transformer primary winding (12). A negative power transistor (14) with a gate (15), has its emitter connected to the center point (4), and the collector connected to the terminal (13) of the transformer primary winding (12). Between center point (4) and emitter of the positive transistor (9), there is a negative free-wheeling diode (16) in the direction of conducting. Between the collector of the negative transistor (14) and positive input terminal (2), there is a positive free-wheeling diode (17) in conducting direction. The negative DC/DC-converter (8) shows an identical structure at the primary side of a positive power transistor (18) with gate (19), with its collector connected to the center point (4), and with its emitter (20) connected to the according transformer primary winding (21). A second negative power transistor (23) with gate (24) has its emitter connected to negative input terminal (3), and the collector connected to the terminal (22) of the transformer primary winding (21). Between the negative input terminal (3) and emitter of the positive transistor (18), there is a negative free-wheeling diode (24) in conducting direction. Between the collector of the negative transistor (23) and the center point (4), there is a positive free-wheeling diode (25) in conducting direction.

According to the invention, the beginning of the winding (26) of the secondary winding (27) on the transformer (28) for the positive DC/DC-converter (7), is connected via rectifier diode (29) in conducting direction, to the cathode (30) of the free-wheeling diode (31) which is common to both converters. The anode of the diode (31) is connected via a current sensor (33) to the negative output terminal (34) of the output DC voltage. The end (35) of the secondary winding (27) is connected to the anode (32) of the free-wheeling diode (31). Then, the beginning (36) of the secondary winding (37) of the transformer (38) for the negative converter (8) is connected via rectifier diode (39) in conducting direction to the cathode (30) of the free-wheeling diode (31). The end (40) of the secondary winding (37) is connected to the anode (32) of the free-wheeling diode (31). From the cathode (30) of the free-wheeling diode (31), there is a connection to an output inductor (41) common for both converters (7) and (8). This output inductor (41) is connected to the positive potential

(42) of the output voltage. To smooth the output voltage, there is a capacitor (43) between the positive output terminal (42) and the negative output terminal (34).

The output voltage control shows a known structure, where the output voltage signal on the signal-line (44) is compared with a reference voltage (46) by a comparing element (45). The result of comparison and/or the voltage difference (47) is dynamically weighted by a controller (48), resulting in a reference value (49) for the inner output current control loop. The comparison of this reference value (49) with the signal (51) of the output current sensor (33) by a comparing element (50), gives the current control error (52) that is dynamically weighted by a controller (53). This results in the signal (55) that defines the relative on-times of the power transistors (9), (14), (18), (23) of the positive and negative DC/DC-converters (7) and (8), where signal (55) is at the input side of the invented apparatus for control (54).

The control apparatus (54) has one PWM-stage for each DC/DC-converter, that consists of an input side summing element and a following comparator with the comparison threshold zero. The control signal (55) lies at the input of the summing element (56) of the modulation-stage (57) for the positive DC/DC-converter (7), where at the second input of the summing element (56) the symmetric isosceles triangle-shaped carrier signal (76) of the three-level converter lies. At the third input of the summing element (56) lies the inverted value (59) of the output signal (60) of the control circuit (61), that controls the symmetry of the partial input voltages. The resulting signal (62) lies at the input of a comparator (63), which gives a pulse-width modulated output signal (64) with the value of either zero or one, that is connected to the gates (10) and (15) to control the power transistors (9) and (14) of the positive converter (7).

The control signal (55) lies at the input of the summing element (65) of the modulation-stage (58) for the negative DC/DC-converter (8), where at the second input of the summing element (65), the inverted signal (66) of the symmetric isosceles triangular-shaped carrier signal (76), for the three-level converter lies. At the third input of the summing element (65) lies the output signal (60) of the control circuit (61), that controls the symmetry of the partial input voltages. The resulting signal (67) lies at the input of a comparator (68), which gives a pulse-width modulated

output signal (69) with the value zero or one, that is connected to the gates (19) and (24) to control the power transistors (18) and (23) of the negative converter (8).

At the input of the control circuit (61), for controlling actively the symmetry of the partial input voltages, a signal (73) is formed that is the output signal of the summing element (70) that forms the sum of the partial input voltage (71) of the positive DC/DC-converter (7) and the inverted partial input voltage (72) of the negative DC/DC-converter (8). This signal (73) is different from zero in case of an asymmetry of the partial input voltages. The signal (73) is dynamically weighted by a controller (74) that gives the symmetry-signal (60) as its output signal.

A reduction of the value of the control signal (55) results in an increase of the relative on-times of the power transistors (9), (14), (18) and (23). Because the maximum relative on-time of a two-transistor forward converter has to be limited with 0.5, it is necessary to employ a limitation (74) of the output signal (75) of the current controller (53) to values larger than zero.

According to the basic function of a three-level converter, in the vicinity of the positive maximum value of the carrier signal (76) of the three-level converter, only the positive output capacitor (5) of the three-level converter (and/or the input capacitor of the positive DC/DC-converter (7)) is charged. In the vicinity of the negative maximum value of the carrier signal (76) of the three-level converter, only the negative output capacitor (6) of the three-level converter (and/or the input capacitor of the negative DC/DC-converter (8)) is charged. Because the carrier signal (76) is, as invented, directly used as the carrier signal of the pulse width modulation (57) of the positive DC/DC-converter, with the resulting signal (64) of the comparison (63) between the carrier signal (76) and the control signal (55) the on-times of the transistors (9) and (14) of the positive DC/DC-converter are lying symmetrically around the positive maximum value of the carrier signal (76).

During these on-times, the positive input capacitor (5) is supplying energy to the output side in form of discharging current pulses. Therefore, a synchronization between the mainly charging current pulses of the input capacitor (5) and the discharging current pulses is reached. Because of the mutual compensation of the charging and discharging current pulses the current stress of input capacitor (5) and /or its voltage ripple with switching frequency is minimized. The same is valid also

for the negative input capacitor, where time-intervals of discharging current pulses are lying symmetrically around the negative maximum value of the carrier signal (76) because of the use of the inverted carrier signal (66) of the three-level converter for pulse width modulation.

If there is an asymmetrical sharing of the partial input voltages with higher voltage of the positive input capacitor (5), then there is a positive signal at the output (60) of the symmetry controller (74). This positive signal is fed into the modulation-stage (58) of the negative DC/DC-converter directly and fed as an inverted signal (59) into the modulation-stage (57) of the positive DC/DC-converter. This results in an increase of the relative on-times (defined by control signal (55)) of the transistors (9) and (14) of the positive DC/DC-converter (7), and in a reduction of the relative on-times (defined by control signal (55)) of the transistors (18) and (23) of the negative DC/DC-converter (8). This influences the input power in such a way that the asymmetry of the partial input voltages is eliminated.

We claim:

1. A method for the stabilization of the sharing of the input voltage between two series connected DC/DC-converters (7) and (8) with input capacitors (5) and (6) which is characterized by increasing the power supply into the positive DC/DC-converter by increasing the relative on-time of the according power transistors if the voltage of the positive input capacitor (5) is higher than the voltage of the negative input capacitor (6). At the same time, the power supply from the negative input capacitor (6) into the negative DC/DC-converter is reduced by reducing the on time of the according power transistors. If the negative partial voltage of the negative input capacitor (6) is higher than the positive one, an opposite change of the duration of the power supply from the according input capacitors into the two DC/DC-converters (7) and (8) is performed. Alternatively, only the time-duration of the energy supply into the DC/DC-converter with the higher partial input voltage is increased (compared to the time-duration in case of ideal symmetry of the partial input voltages) and/or only the time-duration of the energy supply into the secondary side of the DC/DC-converter with the lower partial input voltage is reduced (compared to the time-duration in case of ideal symmetry of the partial input voltages).

2. An apparatus for practical realization of the method according to claim 1 that is characterized by pulse width modulation-stages (57) and (58) for each DC/DC-converter (7) and (8), where a known supervising output voltage and/or output current control loop creates a continuous control signal (55) that is added to the input of a summing element (56) of the modulation-stage (57) of the positive DC/DC-converter (7) in a known way. At the second input of the summing element (56) a carrier signal (76) with switching frequency is lying, and at the third input of the summing element (56) the inverted value (59) of the output signal (60) is lying, where the signal (60) is the output of the control circuit (61) to control the symmetry of the partial input voltages. The resulting sum (62) is compared at a comparator (63) with zero, which results in a pulse width modulated output signal (64) of the comparator (63) with the possible values zero or one. This signal (64) controls the gates (10) and

(15) of the power transistors (9) and (14) of the positive DC/DC-converter (7), in a way that for the value zero of the pulse width modulated gate control signal (64) the power transistors (9) and (14) are in off-state and that for the value one of the pulse width modulated gate control signal (64) the power transistors (9) and (14) are in on-state. The continuous control signal (55) is added to the input of a summing element (65) of the modulation-stage (58) of the negative DC/DC-converter (8). At the second input of the summing element (65) a carrier signal (66) with switching frequency is lying, and at the third input of the summing element (65) the output signal (60) is lying, where the signal (60) is the output of the control circuit (61) to control the symmetry of the partial input voltages. The resulting sum (67) is compared at a comparator (68) with zero, which results in a pulse width modulated output signal (69) of the comparator (68) with the possible values zero or one. This signal (69) controls the gates (19) and (24) of the power transistors (18) and (23) of the negative DC/DC-converter (8). At the input of the control circuit (61) for actively controlling the symmetry of the sharing of the partial input voltages the positive partial input voltage (71) of the positive DC/DC-converter (7) is added (70) to the (by a proper measurement) inverted partial input voltage (72) of the negative DC/DC-converter (8), and a signal (73) is formed that is different from zero in case of asymmetry of the partial input voltages. This signal (70) is dynamically weighted by a controller (74) and used as a symmetry-control signal (60). In case of an asymmetric sharing of the partial input voltages in form of higher partial input voltage of the positive input capacitor (5) the output signal (60) of the symmetry-controller (74) is positive, which is fed into the modulation-stage (58) of the negative DC/DC-controller directly and in inverted form (59) into the modulation-stage (57) of the positive DC/DC-controller. This results in an increase of the relative on-times for the power transistors (9) and (14) of the positive DC/DC-converter (7), and in an reduction of the relative on-times for the power transistors (18) and (23) of the negative DC/DC-converter (8), where the relative on-times are generally defined by the continuous control-signal (55). This means that the power supply into the positive DC/DC-converter (7) increases and the power supply into the negative DC/DC-converter (8) is reduced, which results in a reduction of the asymmetry of the partial input voltages of the DC/DC-converters (7) and (8) resulting ideally in total elimination of the asymmetry.

3. An apparatus for creating symmetry of the partial input voltages between two in series connected DC/DC-converters (7) and (8) with transformers (28) and (38) that is characterized by additional winding for each transformer (28) and (29) with the number of turns equal to that of the primary winding. The additional winding of the positive DC/DC-converter (7) is connected via a positive series diode in parallel to the input capacitor (6) of the negative DC/DC-converter (8), and the additional winding of the negative DC/DC-converter (8) is connected via a negative series diode in parallel to the input capacitor (5) of the positive DC/DC-converter (7). These series diodes are oriented in a way that for the known realization of the DC/DC-converters (7) and (8) as two-transistor forward converter in case of higher partial input voltage of the positive DC/DC-converter (7) for on-state of the two according transistors (9) and (14), where the partial input voltage is directly connected to the primary winding of the transformer (28), the positive series diode is in conducting direction. In case of higher partial input voltage of the negative DC/DC-converter (8) for on-state of the two according transistors (18) and (23) the negative series diode is in conducting direction. Therefore, the input capacitor (6) or (5) with lower partial input voltage is charged automatically and directly from the input capacitor (5) or (6) with higher partial input voltage and the according DC/DC-converter (7) or (8). This prevents formation of an asymmetry of the partial input voltages of the DC/DC-converters (7) and (8). For the known full-bridge configuration of the DC/DC-converters (7) and (8), the additional windings are connected via diode full-bridges to the accordingly other partial input voltages, which increases the effect of reducing (eliminating) asymmetry. For the known realization of the DC/DC-converters (7) and (8) as two-transistor flyback converter the orientation of the two series diodes has to be chosen in a way that during the off-state of the according transistors the charging of the capacitor with the lower partial input voltage is done by the magnetic energy stored within the core of the transformer by the DC/DC-converter with the higher partial input voltage. This guarantees a natural limitation of the symmetry-creating compensating currents.

4. Method for minimization of the current stress on the input capacitors of two in series connected DC/DC-converters (7) and (8) where the operation at the output (1) of a three-level rectifier system is characterized by the same switching frequency of the DC/DC-converters (7) and (8) realized as (known) two-transistor DC/DC-forward converters or DC/DC-flyback converters and the three-level converter and/or by halved switching frequency of the DC/DC-converters (7) and (8) if realized as (known) full-bridge system compared to the switching frequency of the three-level converter. Furthermore, a phase-shift between the pulse-pattern controlling the transistors of the three-level converter and the pulse pattern controlling the transistors of the DC/DC-converters (7) and (8) is realized in a way that there results a maximum overlap-time of the pulses from the three-level rectifier charging the input capacitors (5) and (6) and the discharging current pulses feeding energy in DC/DC-converters. Then, the positive (negative) DC/DC-converter supplies energy during the charging of the positive (negative) input capacitor to the load, and the discontinuous pulsed input current of the DC/DC-converters is mainly supplied directly by charging current pulses from the three-level converter. This results in low RMS-current stress on the input capacitors and a reduced voltage ripple of the partial input voltages.

5. An apparatus for minimization of the current stress of the input capacitors of two in series connected DC/DC-converters (7) and (8) operating at the output (1) of a three-level rectifier system and realization of the DC/DC-converter primary sides as two-transistor forward converters and use of pulse width modulation-stages (57) and (58) according to claim 2 for formation of the control signals (64) and (69) of the DC/DC-converters (7) and (8) which is characterized by synchronization to the switching of the three-level converter and proper (optimized) discharging of the two input capacitors. This is realized by feeding the modulation-stage (57) of the positive DC/DC-converter (7) directly with the triangular-shaped carrier signal (76) of the three-level converter and feeding the second modulation-stage (58) of the negative DC/DC-converter (8) with the inverted triangular-shaped carrier signal (66) of the three-level converter. Because in the vicinity of the positive maximum value of the three-level carrier signal (76) only the positive output capacitor (5) of the three-level

converter (and/or the positive input capacitor of the DC/DC-converter (7)) is charged, and in the vicinity of the negative maximum value of the three-level carrier signal (76) only the negative output capacitor (6) of the three-level converter (and/or the negative input capacitor of the DC/DC-converter (8)) is charged, and because in the vicinity of the positive maximum value of the three-level carrier signal (76) only the positive DC/DC-converter (7) discharges the positive input capacitor (5), and in the vicinity of the negative maximum value of the three-level carrier signal (76) only the negative DC/DC-converter (8) discharges the negative input capacitor (6), it is obvious that a synchronization between (mainly) charging and discharging of the input capacitors is given. This results in large compensation of the overlapping charging and discharging current pulses of the capacitors (5) and (6) and/or a minimization of the voltage ripple with switching frequency on the input capacitors. Energy supply to the output side is done alternately (without timely overlapping) by the two DC/DC-converters (7) and (8). At the secondary side of the DC/DC-converters (7) and (8) there is only free-wheeling diode (31) and one output capacitor (41), where the beginning of the winding (26) of the secondary winding (27) of the transformer (28) of the positive DC/DC-converter (7) is connected via a rectifier diode (29) in conducting direction to the cathode (30) of the free-wheeling diode (31). The anode of the free-wheeling diode (31) is connected to the negative terminal (34) of the output DC voltage. The end of the winding (35) of the secondary winding (27) is connected to the anode (32) of the free-wheeling diode (31). The beginning of the winding (36) of the secondary winding (37) of the transformer (38) of the negative DC/DC-converter (8) is connected via a rectifier diode (39) in conducting direction to the cathode (30) of the free-wheeling diode (31). The end of the winding (40) of the secondary winding (37) is connected to the anode (32) of the free-wheeling diode (31). The output inductor (41) connects the cathode (30) of the free-wheeling diode (31) to the positive output voltage terminal (42). To smooth the output voltage an output capacitor (43) is connecting in the known way the positive (42) and negative (34) output voltage terminals.

6. A method for symmetric sharing of the switching losses between the switching power semiconductors for realization of the DC/DC-converters (7) and (8)

as two-transistor forward converter or two-transistor flyback converter that is characterized by splitting the two (normally known as) identical gate-signal (64) and/or (69) into two signals, where the gate-signal of the first transistor (9) and/or (18) shows a small delay time at every second turn-off instant compared to the original gate-signal (64) and/or (69). The second transistor (14) and/or (23) shows a small delay time at the turn-off instant when the first transistor (9) and/or (18) is not delayed. Since this defined delay time is longer than the maximum difference of the delay times of the driver-stages and the switching-times of the according power transistors (9), (14) and/or (18), (23), the transistors (9), (14) and/or (18), (23), switch off alternately the primary current, so that there results a symmetrical sharing of the switch-off losses of the power transistors (9), (14) and/or (18), (23) of each DC/DC-converter (7) and (8).

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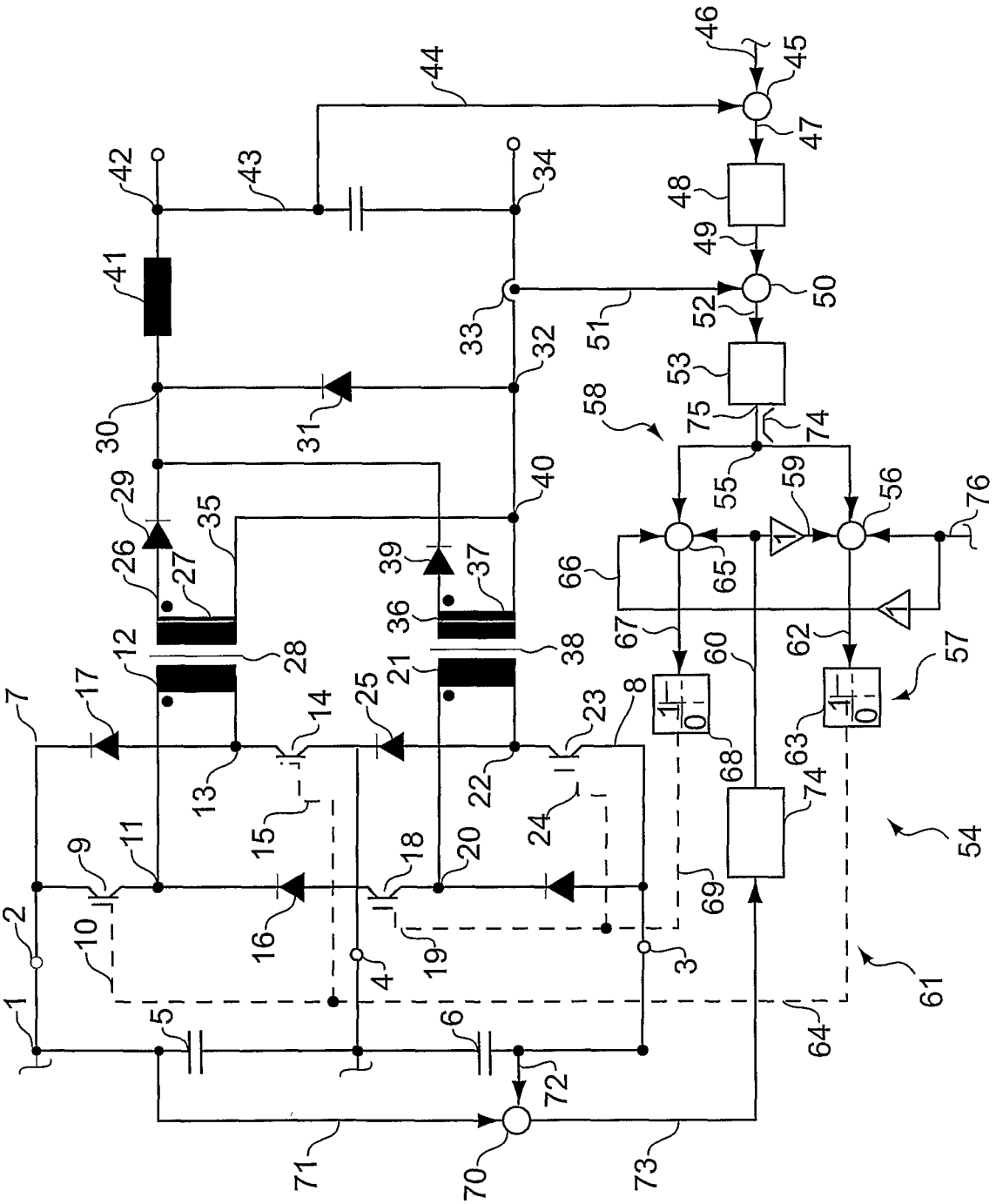

FIG. 1

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB00/00655

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H02M 3/00, 3/02, 3/155, 7/00, 7/42, 7/44
US CL :363/15, 16, 20, 21, 65, 71
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 363/15, 16, 20, 21, 65, 71

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 3,893,015 A (WEIL) 01 July 1975 (01.07.1975), see entire document.	1-6
A	US 5,550,730 A (SEKI) 27 August 1996 (27.08.1996), see entire document.	1-6
A	US 5,088,017 A (YAGINUMA et al) 11 February 1992 (11.02.1992), see entire document.	1-6
A,P	US 6,031,747 A (ILIC et al) 29 February 2000 (29.02.2000), see entire document.	1-6

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
25 JANUARY 2001	19 MAR 2001
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