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4.8 MHz GaN Class-D Power Amplifier and Measurement Systems for Next Generation Power Electronics

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Für meine Freundin Sina,
für meine Eltern Barbara und Beat,
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Abstract

The increasing energy demand of our highly industrialized society requires steady technological advances to ensure sustainable energy supply, and in particular to replace fossil-based with modern renewable energy sources such as wind and solar. Naturally, this leads to a decentralization of energy production, away from a few centralized high-power plants with typically constant energy production independent of external conditions, to several distributed power plants that have fluctuating energy production depending on weather and other environmental influences, which could be buffered with local storage or demand side management. In this context, the number of power conversion and power processing stages will vastly increase, requiring highly efficient and highly compact (power-dense) power electronic systems. This trend is facilitated by emerging technologies like Wide-Bandgap (WBG) power semiconductors that allow a significant reduction of power conversion losses and at the same time render possible extremely power-dense converter systems, i.e., the performance boundaries present with state-of-the-art technologies are shifted. A characteristic property of such *Next Generation Power Electronics (NGPE)* are the higher possible switching frequencies (for the same losses) that facilitate a volume reduction, specifically of passive filter and storage elements. However, the widespread adoption of those new technologies is only slowly progressing, which is mainly explained with various challenges that need to be addressed in order to fully exploit their potential.

This thesis highlights design and implementation challenges arising from the utilization of WBG power semiconductors with considerably higher switching frequencies (up to one order of magnitude higher compared to state-of-the-art technologies) from three perspectives, namely the converter design, the required advanced high-performance measurement technologies and the Electromagnetic Interference (EMI) noise assessment, and then contributes new technological solutions for each considered perspective in order to mitigate those challenges.

An initial contribution analyzes the design of an Ultra-High Bandwidth Power Amplifier (UHBWPA), as typically found in Power-Hardware-in-the-Loop (P-HIL) test environments to characterize and verify the operation of power converters, so-called Systems Under Test (SUTs), under different operating conditions (nominal and critical). It is clear that ever higher performance of the SUTs demands for even higher performing, i.e., ultra-high output dynamics, test equipment, e.g., Power Amplifiers (PAs). A switch-mode realization of such a UHBWPA with a large-signal output Bandwidth (BW) of 100 kHz (at full-power of 10 kVA) and an effective switching frequency of

4.8 MHz is designed and realized, employing topological advantages of series- and parallel-interleaving of multiple Switching Cells (SCs). Finally, it achieves an efficiency of 95.8 % at full output power and maximum output frequency with a power density of 25 kW/dm^3.

Along with faster switching and higher output BW of power converters comes the requirement for ultra-high BW measurement technologies (mainly on-board voltage and current measurements). Not only do they permit the aforementioned fast control dynamics but they also allow ultra-fast reacting protection mechanisms (overvoltage/overcurrent), essential in converters with low-valued capacitive/inductive filtering elements, which is a characteristic property of high BW PAs. This thesis therefore further contributes solutions to extend the BW of commercially available dc-capable Hall-effect current sensors above 50 MHz and to offer at the same time very high Common Mode (CM) robustness, i.e., high immunity to fast $\mathrm{d}v/\mathrm{d}t$ voltage switching transitions. Additionally, galvanically isolated voltage measurement systems with extremely high Common Mode Rejection Ratio (CMRR) are analyzed. They are generally used for measurements on a floating and rapidly changing reference potential, e.g., for High-Side (HS) Gate-Source (GS) voltage measurements in a half-bridge or for voltage balancing in multi-level converters, where the switch-node voltage acts as CM disturbance on the measurement in both cases. A very compact galvanically isolated voltage measurement system with a BW of 130 MHz and a CMRR of > 100 dB at 100 MHz is proposed and its performance is experimentally verified. The performance is on par with the best state-of-the-art solutions but in comparison, the proposed system only needs a host computer where the data can be displayed and processed and does not rely on (typically vendor-specific) additional equipment such as oscilloscopes, which is a huge cost advantage.

To account for the more delicate EMI noise assessment in converters with high switching frequencies and high voltage transition rates ($\mathrm{d}v/\mathrm{d}t$), a further contribution discusses the modal splitting of the conducted EMI noise emissions, i.e., the separation into a CM and a Differential Mode (DM) part for every spectral component in the regulated frequency range (150 kHz to 30 MHz), by means of a three-phase active CM/DM EMI noise separator. An active realization, i.e., with operational amplifiers, has several advantages compared to implementations found in literature using passive components (mainly transformers and CM chokes), namely a much higher separation performance, i.e., very high CMRR and Differential Mode Rejection Ratio (DMRR) (50 dB or better across the entire regulated frequency range) and a very much facilitated manufacturing and trimming process. In addition, the influence

of asymmetries in the standard EMI test setup is thoroughly analyzed analytically and experimentally in order to provide practical guidelines how to properly measure conducted EMI in three-phase systems and therefore, to promote the optimization of the respective CM and DM filter stages for the best-possible cost-, volume- and weight-efficiency.

Finally, the most important findings of this thesis are summarized and an outlook of possible future research topics on each considered perspective is provided, which mainly depend on large-scale functional integration of driving and control circuitry into power semiconductor packages.

Kurzfassung

Der zunehmende Energiebedarf in unserer hochindustrialisierten Gesellschaft bedingt stetige technologische Fortschritte um eine nachhaltige Energieversorgung sicherzustellen, insbesondere mit dem Ziel, fossile Energieträger mit modernen erneuerbaren Energiequellen wie Solar- und Windkraft zu ersetzen. Naturgemäss führt dies zu einer Dezentralisierung der Energiegewinnung, weg von einigen wenigen zentralen Hochleistungskraftwerken mit typischerweise konstanter und von Umwelteinflüssen unabhängiger Produktion, hin zu vielen verteilten Kleinkraftwerken mit oftmals fluktuierender Produktion, abhängig von Wetter- und anderen Umwelteinflüssen. Die fluktuierende Energieproduktion kann durch intelligentes Lastmanagement und durch intermediäre Energiepufferung, beispielsweise mit Batteriesystemen, ausgeglichen werden. Dadurch wird die Anzahl der leistungselektronischen Konversions- und Verarbeitungsstufen jedoch deutlich zunehmen, was den Einsatz von hocheffizienten und extrem kompakten (leistungsdichten) leistungselektronischen Systemen erfordert. Die stetige Weiterentwicklung und Verbreitung von modernen Leistungshalbleitertechnologien mit weitem Bandabstand (*Wide-Bandgap (WBG) Leistungshalbleiter*) begünstigt diesen Trend. Deren Einsatz ermöglicht eine signifikante Reduktion der Konversionsverluste bei gleichzeitig deutlich kompakteren Systemrealisierungen. Das bedeutet in anderen Worten, dass leistungselektronische Systeme der nächsten Generation, sogenannte *Next Generation Power Electronics (NGPE)*, realisiert mit WBG Schaltelementen, die derzeit vorhandenen Grenzen bezüglich erreichbarer Leistungsfähigkeit verschieben. Eine charakteristische Eigenschaft solcher NGPE ist eine höhere mögliche Schaltfrequenz (bei gleichbleibenden Verlusten), was eine Reduktion des Bauvolumens, insbesondere der passiven Filter- und Speicherementen, erlaubt. Trotz den genannten Vorteilen findet die WBG Technologie nach wie vor nur langsam Einsatz in industriellen Systemen, was vor allem auf diverse in einer praktischen Realisierung auftretende Herausforderungen zurückzuführen ist, die zunächst verstanden und gelöst werden müssen, um das volle Potenzial der Technologie auszuschöpfen.

Die vorliegende Dissertation beleuchtet die Herausforderungen, die sich aus der Verwendung von WBG Leistungshalbleitern mit wesentlich höheren Schaltfrequenzen (bis zu einer Grössenordnung höher im Vergleich zu heutigen Technologien) ergeben, aus unterschiedlichen Perspektiven, nämlich dem Konverterdesign, der benötigten Messtechnik und der Einhaltung von Regulierungen bezüglich elektromagnetischer Verträglichkeit. Für jeden betrachteten Blickwinkel werden neue technologische Lösungen vorgeschlagen, um die ermittelten Herausforderungen anzugehen.

Im ersten Beitrag der Dissertation liegt der Fokus auf der Auslegung und Realisierung eines Leistungsverstärkers mit ultrahoher Bandbreite (UHBWPA), wie er typischerweise in Power-Hardware-in-the-Loop (P-HIL)-Testumgebungen Einsatz findet, um den Betrieb von leistungselektronischen Systemen (insbesondere NGPE), in diesem Kontext mit dem englischen Begriff *Systems Under Test (SUTs)* bezeichnet, bei unterschiedlichen Betriebsbedingungen zu charakterisieren und zu verifizieren. Es ist offensichtlich, dass die immer höhere Leistungsfähigkeit der SUTs noch leistungsfähigere Test- und Messsysteme (z.B. besagte Leistungsverstärker), hauptsächlich in Bezug auf ultra-schnelle Dynamik (Bandbreite), erfordert. Eine aus Effizienzsicht vorteilhafte Realisierung des UHBWPA als Schaltverstärker mit einer Grosssignalbandbreite von 100 kHz (bei voller Leistung von 10 kVA pro Phasenausgang) und einer effektiven Schaltfrequenz von 4.8 MHz ist zentraler Teil dieses ersten Beitrages. Dabei werden topologische Vorteile des phasenversetzten Betriebes von mehreren serien- und parallel-geschalteten Schaltzellen genutzt, wobei letztlich bei maximaler Ausgangslast und Ausgangsfrequenz eine Systemeffizienz von 95.8 % und eine Leistungsdichte von 25 $\mathrm{kW/dm^3}$ resultieren.

Als Folge der höheren Schaltfrequenzen und Ausgangsbandbreiten von Leistungsverstärkern resultieren anspruchsvolle Anforderungen and die zu verwendende Messtechnik, namentlich extrem breitbandige, konverterintegrierte Spannungs- und Strommessungen, welche einerseits für die Regelung oben genannter hochdynamischer Leistungsverstärker benötigt werden und andererseits als Überwachung, d.h. als extrem schnell reagierende Überspannungs- und Überstromabschaltung, Einsatz finden. Letzteres ist von besonderer Relevanz, wenn die verwendeten Ausgangsfilterelemente tiefe Werte aufweisen, was im Falle von breitbandigen Leistungsverstärkern ein charakteristisches Merkmal darstellt. Ein weiterer Beitrag dieser Dissertation beschäftigt sich daher mit Lösungsansätzen, um die Bandbreite von kommerziell erhältlichen, DC-fähigen Hall-Effekt Stromsensoren auf über 50 MHz zu erweitern, bei gleichzeitig extrem hoher Robustheit gegenüber Gleichtaktstörungen, wie sie bei schnellen Schaltflanken (hohes $\mathrm{d}v/\mathrm{d}t$) in Leistungskonvertern auftreten. Des Weiteren werden breitbandige, galvanisch getrennte Messsysteme mit extrem hoher Gleichtaktunterdrückung (CMRR) im Detail untersucht, welche bei Messungen an einem sich schnell ändernden/springenden Bezugspotenzial Einsatz finden, beispielsweise zur Messung der Gate-Source Spannung des oberen (high-side) Schalters eines Brückenzweiges oder zur Sicherstellung der gleichmässigen Spannungsaufteilung in Multizellen-Konvertern, wo in beiden Fällen die Schaltknotenspannung als

Gleichtaktstörung wirkt. Es wird ein sehr kompaktes, galvanisch isoliertes Spannungsmesssystem mit einer Bandbreite von 130 MHz und einer CMRR von > 100 dB bei 100 MHz vorgeschlagen und experimentell verifiziert. Die erreichte Performance entspricht den bzw. übertrifft die besten Lösungen nach aktuellem Stand der Technik. Dabei benötigt das vorgeschlagene Messsystem im Vergleich dazu keine zusätzlichen Messinstrumente wie Oszilloskope zur Darstellung und Auswertung der Ergebnisse, sondern lediglich einen Host-Computer, was einen enormen Kostenvorteil darstellt.

Um der in Umrichtern mit hohen Schaltfrequenzen und steilen Spannungsflanken typischerweise schwierigeren Einhaltung der Normen bezüglich elektromagnetischer Interferenz (EMI) Rechnung zu tragen, wird in einem weiteren Beitrag dieser Dissertation die Trennung der leitungsgebundenen EMI-Rauschemissionen in einen Gleichtaktanteil (CM) und Gegentaktanteil (DM) für jede Spektralkomponente im regulierten Frequenzbereich von 150 kHz bis 30 MHz mittels eines dreiphasigen CM/DM-EMI-Rauschseparators untersucht. Eine Realisierung mit aktiven Komponenten, d.h. mit Operationsverstärkern, hat mehrere Vorteile gegenüber in der Literatur typischerweise diskutierten Realisierungen mit passiven Komponenten (hauptsächlich Transformatoren und Gleichtaktdrosseln), nämlich eine massiv verbesserte Trenncharakteristik, namentlich eine höhere Gleichtakt- und Gegentaktunterdrückung (CMRR und DMRR; beide jeweils grösser als 50 dB im gesamten regulierten Frequenzbereich), bei gleichzeitig wesentlich einfacherem Herstellungs- und Abgleichprozess. Darüber hinaus wird der Einfluss von Asymmetrien im Aufbau von typischen EMI-Prüfständen sowohl analytisch als auch experimentell untersucht, um praktische Leitlinien für eine korrekte und von oben genannten Asymmetrien hinreichend unbeeinflusste Messung der leitungsgebundenen EMI-Rauschemissionen in dreiphasigen Umrichtern vorzulegen. Dadurch lassen sich die jeweiligen CM- und DM-Filterstufen optimal ausgelegen, was zu bestmöglicher Gewichts-, Kosten- und Volumeneinsparung führt.

Zum Schluss werden die wichtigsten Forschungsbeiträge der Dissertation zusammengefasst und in einem Ausblick für jedes der betrachteten Teilgebiete mögliche Themen für weiterführende Forschung beleuchtet. Ein gemeinsamer und zentraler Aspekt ist dabei die funktionale Integration von Ansteuer- und Messschaltungen in die Gehäuse der Leistungshalbleiter.

Abbreviations

3L3	Three-Level Triple-Interleaved
AAF	Anti Aliasing Filter
ADC	Analog-to-Digital Converter
AFE	Analog Front-End
BJT	Bipolar Junction Transistor
BNC	Bayonet Neill Concelman
BVDS	Blocking Voltage from Drain to Source
BW	Bandwidth
CE	Conducted Emission
CHB	Cascaded H-Bridge
CM	Common Mode
CMC	Common Mode Choke
CMRR	Common Mode Rejection Ratio
CMTF	Common Mode Transfer Function
CT	Current Transformer
D2S	Differential to Single-Ended
DM	Differential Mode
DMRR	Differential Mode Rejection Ratio
DMTF	Differential Mode Transfer Function
DS	Drain-Source
DSP	Digital Signal Processor
DUT	Device Under Test
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EUT	Equipment Under Test
EV	Electric Vehicle
FB	Full-Bridge
FC	Flying Capacitor
FCC	Flying Capacitor Converter

FEM	Finite Element Method
FOM	Figure-of-Merit
FPGA	Field-Programmable Gate Array
GaN	Gallium-Nitride
GBP	Gain-Bandwidth Product
GD	Gate Driver
GIT	Gate Injection Transistor
GS	Gate-Source
GUI	Graphical User Interface
HEMT	High-Electron-Mobility Transistor
HF	High-Frequency
HPF	High-Pass Filter
HRPWM	High-Resolution PWM
HS	High-Side
HSW	Hard Switching
HV	High-Voltage
IC	Integrated Circuit
IGBT	Insulated-Gate Bipolar Transistor
IVS	Isolated Inductor Voltage Sensing
LF	Low-Frequency
LISN	Line Impedance Stabilization Network
LPF	Low-Pass Filter
LS	Low-Side
LSB	Least Significant Bit
LV	Low-Voltage
MEA	More Electric Aircraft
MMC	Modular Multi-Level Converter
MnZn	Manganese-Zinc
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MRI	Magnetic Resonance Imaging

MSPS	Megasamples Per Second
MV	Medium-Voltage
NGPE	Next Generation Power Electronics
NiZn	Nickel-Zinc
NPC	Neutral-Point Clamped
NTC	Negative Temperature Coefficient
PA	Power Amplifier
PCB	Printed Circuit Board
PE	Protective Earth
P-HIL	Power-Hardware-in-the-Loop
PHSW	Partial-Hard Switching
PoF	Power-over-Fiber
PSPWM	Phase-Shifted PWM
PSRR	Power Supply Rejection Ratio
PSU	Power Supply Unit
PTFE	Polytetrafluoroethylene
PUC	Pickup Coil
PV	Photovoltaic
PWM	Pulse Width Modulation
RE	Radiated Emission
RF	Radio-Frequency
RMS	Root Mean Square
RR	Rejection Ratio
RTS	Real-Time Simulator
SC	Switching Cell
SEPIC	Single-Ended Primary Inductance Converter
Si	Silicon
SiC	Silicon-Carbide
SNR	Signal-to-Noise Ratio
SRF	Self-Resonance Frequency

SST	Solid State Transformer
SSW	Soft Switching
SUT	System Under Test
TF	Transfer Function
TIM	Thermal Interface Material
UHBWPA	Ultra-High Bandwidth Power Amplifier
VGA	Variable Gain Amplifier
VSI	Voltage Source Inverter
WBG	Wide-Bandgap
ZCS	Zero-Current Switching
ZVS	Zero-Voltage Switching

Contents

1 Introduction

In order to sustainably supply the steadily increasing energy demand in the future, modern renewable energy sources such as wind and solar power (sorted according to their share in the global renewable energy mix in 2021 with 23.5 % and 13 %, respectively [1]) inarguably play a pivotal role. In 2019, 11.5 % of the worldwide total final energy consumption was supplied by renewable energy sources (this also includes hydro power with a share of 54 % in the global renewable energy mix in 2021 according to [1]) and with currently in place and planned policies, their share is expected to reach 18 % by 2030, whereas according to the "Net Zero Emissions by 2050 Scenario (NZE)", aiming for net zero CO_2 emissions in the global energy sector by 2050 — equivalent to limiting the global temperature rise to 1.5 °C above pre-industrial level [2]— they should account for 32 % [3, 4]. Therefore, a significant prioritization of those energy sources is needed, which is to a large extent dependent on the available power conversion and power processing technologies. In this context, *Next Generation Power Electronics (NGPE)* such as ultra-fast drive systems, e.g., fuel cell compressor drives [5], highly compact Photovoltaic (PV) inverters, Solid State Transformers (SSTs) (e.g., for next-generation traction vehicles or wind turbine electrical systems) [6] as well as Electric Vehicle (EV) drive systems and on-board/off-board EV chargers, already play an important role today and will play an increasingly central role in the near future in order to use the available primary energy resources as efficient as possible [7].

Ongoing reduction of the functional volume is a further characteristic aspect of NGPE and facilitates highly compact designs that are desirable in virtually all applications, such as for example, in on-board EV chargers to use the freed-up space for additional information/security/entertainment devices, to increase the vehicle payload and/or to install a larger battery. Highly dynamic

drive systems also strongly benefit from compact power electronics designs which allow, e.g., to integrate the motor inverter directly into the machine in order to minimize the cabling effort (complexity, cost, mass, reliability and signal integrity advantages) [5, 8], in particular attractive for electrified transportation [9] and industry automation. At the same time, high conversion efficiencies are all the more important, since miniaturization also implies a smaller overall surface area to dissipate the heat. The use of modern Wide-Bandgap (WBG) semiconductor technologies such as Gallium-Nitride (GaN) and Silicon-Carbide (SiC) allows to design systems with considerably higher efficiencies (compared to traditional Silicon (Si)-based realizations [10]) and/or for the same losses enables an increase in the switching frequency, which is the main enabler for shrinking the volume in switch-mode power electronic converter systems [11]. This thesis particularly focuses on increasing the power density and the thereby resulting opportunities and challenges. In the following, two major advantages for NGPE achievable with an increased switching frequency are listed and explained, namely:

- Higher converter power densities (volumetric and/or gravimetric), and
- faster control/output dynamics.

The former arises from the fundamental inversely proportional relation between the required passive filter element values (capacitance and inductance) and the respective voltage and current ripple frequency. A higher ripple frequency thus allows to use lower valued filter components, which enables a lower filter volume, since for a given voltage and current rating, the volume (and under the assumption of a constant mass density also the weight) of passive elements is proportional to the component value [12]. The output dynamics and/or Bandwidth (BW) of a switch-mode power converter is fundamentally limited by the necessary output filter, which removes the High-Frequency (HF) switching components and ideally solely passes the desired fundamental frequency component (e.g., a sine wave with several hundred Hz to several kHz in case of a high-speed motor drive). To achieve an adequate output voltage and/or current quality, the converter switching frequency must be roughly ten times higher than the output filter corner frequency [13] and therefore, high output dynamics directly demand a high switching frequency.

With the aforementioned technological advances in NGPE, their test and verification is ever more important, yet more challenging. Power-Hardware-in-the-Loop (P-HIL) test environments are a well-known and popular frame-

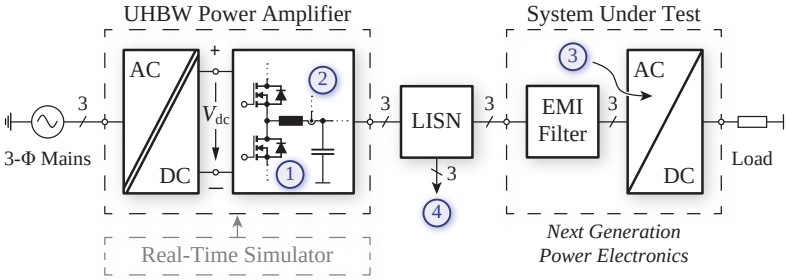


Fig. 1.1: Generalized overview of a P-HIL test environment for a Next Generation Power Electronics (NGPE) System Under Test (SUT), which in this exemplary case could be an ultra-compact single- and/or three-phase on-board Electric Vehicle (EV) charger (incl. EMI filter). A three-phase mains-interfaced Ultra-High Bandwidth Power Amplifier (UHBWPA) emulates, e.g., the three-phase grid under certain operating conditions (fault signatures) in order to test the SUT behavior. Moreover, a Line Impedance Stabilization Network (LISN) allows to measure the conducted electromagnetic noise emissions with help of an EMI test receiver. The highlighted labels ① – ④ indicate major focus areas and/or contributions of this thesis.

work for characterizing and verifying the correct operation of power electronic Systems Under Test (SUTs) and to emulate various nominal and exceptional operating conditions with relatively low cost and time effort [14]. They consist of an Ultra-High Bandwidth Power Amplifier (UHBWPA) that is used in conjunction with a Real-Time Simulator (RTS) to emulate a certain power source and/or sink behavior from the SUT's perspective. An example is shown in **Fig. 1.1** where the operation of an ultra-compact grid-tied single- and/or three-phase EV charger as a NGPE-SUT is analyzed. To verify the SUT's grid compatibility, the three-phase power grid is emulated under normal operating and fault conditions. The testing of the latter is in particular rather challenging and expensive without P-HIL test environments. For maximum testing versatility and fast dynamics, the UHBWPA requires sufficient large-signal or full-power BW of several ten to hundred kHz [14], which, considering power conversion efficiency advantageously is implemented as switch-mode rather than linear-mode system and therefore, implies a very high switching frequency in the multi-MHz range, as will be shown later in this thesis in more detail.

In the following, the general challenges arising from an increased converter switching frequency are presented and the contributions of this thesis aiming at mitigating those are highlighted. In the interest of better readability

and comprehensibility, each chapter of this thesis has a separate detailed introduction, which provides a thorough application overview and presents state-of-the-art solutions.

1.1 Challenges

As generally true in engineering, no benefit comes for free and thus, the advantages and opportunities made possible with an increased switching frequency are accompanied by various challenges, which finally motivate the research presented in this thesis. A categorization in three parts, namely, challenges related to the converter design, challenges arising for the measurement technology and finally, challenges in the assessment of the conducted Electromagnetic Interference (EMI) noise spectrum is done in the following list:

Part A — Converter Design

- Every switching instant in a switch-mode converter dissipates a certain energy E_{sw} due to residual charges on semiconductor internal parasitic capacitances and due to overlap of switch voltage and current resulting from finite switching transition speeds (turn-on and turn-off times). The switching losses P_{sw} are found as product of E_{sw} and the switching frequency f_{sw}, i.e., $P_{sw} = E_{sw} \cdot f_{sw}$. Given the linear scaling of P_{sw} with f_{sw}, high switching frequencies in the MHz range can lead to excessive switching losses, which degrade the converter efficiency and demand to reduce E_{sw} and/or for a sophisticated thermal design.

- The increased power densities result in lower volumes and/or surface areas and thus higher power loss densities, which make it very challenging to extract the heat from the thermal hotspots and again demand for a sophisticated thermal design.

- Even though a high switching frequency generally allows to reduce the filtering element values and accordingly results in low volume input/output filter realizations, in case of inductors this requires suitable core materials and winding arrangements capable to operate at frequencies of several MHz without generating excessive losses.

- An increasing switching frequency f_{sw} results in a coarser time resolution in a digital controller and modulator implementation running

on a Digital Signal Processor (DSP) or Field-Programmable Gate Array (FPGA) with limited clock frequency f_{clk}, because only $n = f_{\mathrm{clk}}/f_{\mathrm{sw}}$ computation cycles are available during each switching period. This can severely impact, e.g., the resolution of the digital Pulse Width Modulation (PWM) generation and therefore, the accuracy of the output voltage, and in addition considerably contributes to the total latency of the digital controller execution.

- The impact of the accumulated time delays of various origin such as Analog-to-Digital Converter (ADC) latency, interlocking delays (dead times), delays in the computation process and Gate Driver (GD) as well as the above mentioned latency of the PWM generation has stronger influence on the converter control, since they correspond to a significant part of one switching period.

- A high switching frequency is typically accompanied by fast switching transients during the turn-on and turn-off transitions of the power semiconductors, mainly for efficiency reasons (reduced $V - I$ overlap and hence reduced switching losses). The layout of the power loop and the GD is extremely critical in order to limit the overvoltage across the power semiconductors (due to high rates of current change $\mathrm{d}i/\mathrm{d}t$) and to prevent undesired oscillations between the semiconductor output capacitances and parasitic Printed Circuit Board (PCB) capacitances and inductances.

Part B — Advanced Measurement Technology

- To achieve increased closed-loop output voltage/current dynamics of power electronic converters — besides an increased switching frequency — very high BW and accurate on-board measurement systems are required, in particular voltage and current measurements. Moreover, ultra-fast reacting protection mechanisms (overvoltage/overcurrent) rely on these high BW measurements to guarantee reliable and safe converter operation.

- In the course of the continuing reduction of the functional volume of power electronic systems, these employed on-board measurement systems must also be realized ever more compact. In highly power-dense converters it is often not anymore possible to physically access the components of interest in order to carry out measurements during commissioning in the laboratory. Therefore, it would be desirable to

have measurement solutions fully integrated in the converter with a generic data interface to read out measurement data. Besides, this level of integration would facilitate online condition monitoring in the field, e.g., of machines and/or drive systems to find early signs of failure and thereby to minimize maintenance effort and to increase the overall available operation time.

- Commissioning and verification of GD circuits in power converters requires accurate measurements of the Gate-Source (GS) voltage on floating and fluctuating reference potentials. This is one prominent example of measurements typically carried out with galvanically isolated voltage probes. There, the fluctuating switch-node voltage (several hundreds of volts to several kilovolts) acts as a Common Mode (CM) disturbance on the desired GS voltage measurement. With the fast voltage transitions ($\mathrm{d}v/\mathrm{d}t$) achieved with WBG power semiconductors, these measurements are extremely challenging, and measurement systems with a very high Common Mode Rejection Ratio (CMRR) are required.

Part C — Conducted EMI Noise Assessment

- Conducted EMI noise emissions measured with an EMI test receiver via a Line Impedance Stabilization Network (LISN) at the SUT mains-interfacing terminals have to be limited in the frequency range of 150 kHz to 30 MHz to comply with various regulatory standards on Electromagnetic Compatibility (EMC), such as *CISPR 11* (EN 55011) [15], and *CISPR 14* (EN 55014) [16]. With faster switching converters where the switching frequency lies close to or even within the regulated frequency band, adequate and efficient noise filtering with carefully designed and optimized filter stages is of paramount importance. Moreover, the faster switching transitions ($\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$) of WBG power semiconductors generate significant HF (above few MHz) noise contributions, which make EMI filtering more challenging, since in this frequency range, the filter behavior is to a great extent defined by parasitic elements and (intentional or unintentional) coupling effects, e.g., due to component placement and/or the PCB layout.

- Current EMI compliance measurement procedures allow the assessment of the total conducted emissions but do typically not provide a modal split, i.e., do not distinguish between CM and Differential

Mode (DM) noise components. At a given frequency there can be significant differences between the two noise components and in case of non-compliance with the limits, in particular at high frequencies, it is currently not possible to determine whether the CM or DM noise is responsible.

1.2 Aims and Contributions

This thesis provides numerous new concepts and analyses to address the above mentioned challenges. The content is grouped into three parts and divided into five main chapters, whereas chapter interdependencies have been reduced to the absolute minimum. Hence, each chapter can largely be read as a standalone text.

Part A — Converter Design

- The aforementioned challenges related to the converter design equally affect NGPE converter systems as well as systems for their test and verification like UHBWPAs. In **Chapter 2**, using the example of such a UHBWPA as part of a P-HIL test environment shown in **Fig. 1.1**, the challenges related to the design of high-performance systems with latest WBG power semiconductors and with the goal of pushing the switching frequency to the maximum feasible (in terms of converter efficiency) limit are highlighted and addressed. A switch-mode realization of a 100 kHz large-signal BW GaN-based 10 kVA Class-D Power Amplifier (PA) with a switching frequency of 4.8 MHz and significantly higher efficiency and power density compared to state-of-the-art switch-mode realizations and in particular compared to realizations operating in linear-mode, is proposed. Two key concepts, namely series- and parallel-interleaving of multiple switching and/or converter cells to decouple the *effective* switching frequency relevant to output filtering and therefore, related to the output BW, from the individual device switching frequency relevant to the switching losses in each device, are instrumental to achieve the high-performance specifications. Designs and eligible devices are evaluated based on a trade-off between efficiency, realization volume (power density), thermal performance and realization complexity. A liquid-cooled hardware demonstrator of a single-phase module of a three-phase UHBWPA with an output power of 10 kVA (per phase), a Root Mean Square (RMS) output voltage

of 230 V, a full-power (large-signal) BW of 100 kHz, very high output voltage quality (fundamental frequency harmonic content < 2.5 V and < 1.2 V for the 3rd and 5th harmonic, respectively), an efficiency of > 95 %, a power density of 25 kW/dm^3, and a switching frequency of 4.8 MHz is realized.

Part B — Advanced Measurement Technology

- Having designed and realized a switch-mode PA with the capability to reach a very high large-signal output BW, **Chapter 3** focuses on dc-coupled HF current sensors, which are required for its highly-dynamic closed-loop operation, e.g., as part of the inner current control loop in case of a cascaded control structure as proposed in [17]. To facilitate large-signal control BWs of 100 kHz (or more) and ultra-fast responding supervision/fault detection circuits for operation with switching frequencies in excess of several MHz, on-board current measurements must offer > 10 MHz BW. Different concepts to extend the BW of commercially available off-the-shelf dc-coupled Low-Frequency (LF) Hall-effect current sensors (BW < 1 MHz) above several tens of MHz are presented. Thereby, various HF current measurement principles such as Rogowski coils, PCB-integrated Pickup Coils (PUCs) as well as Current Transformers (CTs) are investigated and compared with the aim to maximize the measurement BW, to minimize the influence of CM disturbances originating from fast $\mathrm{d}v/\mathrm{d}t$ voltage transitions and to realize the overall sensor (LF sensor plus HF extension) as compact as possible to conveniently embed it into power-dense converter systems. With the proposed concepts, a measurement BW greater than 50 MHz and a CMRR of almost 100 dB is achieved. The active circuit required for the BW extension is realized with a footprint of 22 mm × 25 mm, however, chip integration of the measurement circuit together with the LF Hall sensor would allow for a substantially more compact solution in future systems.

- Complementary to current measurements, **Chapter 4** focuses on high BW galvanically isolated (floating) voltage measurements with superior CM robustness, quantified with a very high CMRR, i.e., high immunity to fast $\mathrm{d}v/\mathrm{d}t$ transients of the measurement reference potential. The required CMRR at different frequencies to limit the maximum time-domain measurement error below a certain value is analytically derived and with the identified very simple relation, it can easily be obtained in

any practical application scenario, only requiring the switched bus voltages and expected voltage transition rates. Moreover, a very compact galvanically isolated measurement system with a measurement BW of 130 MHz and a CMRR of > 100 dB at 100 MHz is proposed (performance on par with the best commercially available probing solutions, however, realized in a much more compact form), highlighting critical design aspects that are paramount to achieve this performance. In contrast to currently existing (commercial) solutions, the proposed system directly digitizes the measured voltage and transmits the data wireless to a host interface and therefore eliminates the need for an oscilloscope to evaluate the measurements. With an overall volume of $\approx 60\,\mathrm{cm}^3$ the proposed solution can be directly integrated in various Medium-Voltage (MV) and/or high-power converter systems, where direct access with conventional measurement probes during commissioning and/or operation is often impossible. Further miniaturization of the presented measurement system is possible, e.g., by integrating the analog measurement circuit including digitization into a single chip and therefore, enabling online/continuous measurement and monitoring capabilities in highly compact systems, which otherwise are impossible with current state-of-the-art isolated voltage probes.

Part C — Conducted EMI Noise Assessment

- **Chapter 5** proposes a three-phase active conducted EMI noise separator, which extends the testing capabilities compared to the standard EMI pre-compliance test procedure that only measures the total emitted noise, by enabling accurate determination and quantification of the CM and the DM portion in the total emitted noise at every frequency. The knowledge of the CM/DM shares of the total EMI noise is very beneficial to optimize the respective filter stages in a way to be compliant with the regulatory standards with minimal effort (e.g., cost, volume and weight). The proposed active realization of a three-phase noise separator shows unprecedented separation capabilities, i.e., a CM component at the input is attenuated by > 50 dB at the DM output over the full considered frequency range from 150 kHz to 30 MHz (and equally, a DM component at the input is attenuated by > 50 dB at the CM output), which is one of the numerous achieved advantages compared to state-of-the-art passive realizations relying mostly on magnetic components. Having realized such a high-performance noise separator, the whole Conducted Emission (CE) EMI test setup is investigated more in

depth and it is thoroughly analyzed and experimentally proven that all elements in such a test setup (e.g., connection cables, LISNs, layout of the SUTs' EMI filter) cause asymmetries, which manifest themselves as unwanted conversion from CM to DM (and reciprocal conversion from DM to CM) and therefore, the initial goal to accurately determine the origin (CM or DM) of each noise spectral component is thwarted. Experimental results show around 20 dB degradation of the initial noise separator separation capabilities, whereas the actual EMI filters (component tolerances, self-parasitic elements, parasitic coupling effects and the layout) are identified to have the most severe impact. The proposed three-phase active CM/DM noise separator successfully helps to identify those setup imperfections, improves the overall filter design process and optimization and further facilitates the EMI noise source modeling in circuit simulators based on real-world measurement data.

Finally, **Chapter 6** concludes the findings of this thesis and provides an outlook for future research topics in the covered fields.

1.3 List of Publications

Key research results presented in this thesis have been published in leading international scientific journals and conference proceedings, or have been presented at workshops. The publications created as part of this thesis, and also in the scope of other related research projects, are listed below.

1.3.1 Journal Papers

⑥ **P. S. Niklaus**, J. W. Kolar, and D. Bortis, "100 kHz Large-Signal Bandwidth GaN-Based 10 kVA Class-D Power Amplifier with 4.8 MHz Switching Frequency," *IEEE Transactions on Power Electronics*, vol. 38, no. 2, pp. 2307-2326, February 2023. DOI: 10.1109/TPEL.2022.3213930.

⑤ **P. S. Niklaus**, R. Bonetti, C. Stäger, J. W. Kolar, and D. Bortis, "High-Bandwidth Isolated Voltage Measurements with Very High Common Mode Rejection Ratio for WBG Power Converters," *IEEE Open Journal of Power Electronics*, vol. 3, pp. 651-664, September 2022. DOI: 10.1109/OJPEL.2022.3208693.

④ **P. S. Niklaus**, D. Bortis, and J. W. Kolar, "Beyond 50 MHz Bandwidth Extension of Commercial DC-Current Measurement Sensors

with Ultra-Compact PCB Integrated Pickup Coils," *IEEE Transactions on Industry Applications*, vol. 58, no. 4, pp. 5026-5041, August 2022. DOI: 10.1109/TIA.2022.3164865.

③ **P. S. Niklaus**, M. M. Antivachis, D. Bortis, and J. W. Kolar, "Analysis of the Influence of Measurement Circuit Asymmetries on Three-Phase CM/DM Conducted EMI Separation," *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 4066-4080, April 2021. DOI: 10.1109/TPEL.2020.3025122.

② **P. S. Niklaus**, D. Bortis, and J. W. Kolar, "Design and Experimental Analysis of a Three-Phase Active CM/DM Conducted EMI Noise Separator," *CPSS Transactions on Power Electronics and Applications*, vol. 5, no. 3, pp. 273-288, September 2020. DOI: 10.24295/CPSSTPEA.2020.00023.

Moreover, the author had the pleasure to contribute to the following journal paper:

① M. Antivachis, **P. S. Niklaus**, D. Bortis, and J. W. Kolar, 'Input/Output EMI Filter Design for Three-Phase Ultra-High Speed Motor Drive GaN Inverter Stage," *CPSS Transactions on Power Electronics and Applications*, vol. 6, no. 1, pp. 74-92, March 2021. DOI: 10.24295/CPSSTPEA.2021.00007.

1.3.2 Conference Papers

⑤ **P. S. Niklaus**, D. Bortis, and J. W. Kolar, "High-Bandwidth High-CMRR Current Measurement for a 4.8 MHz Multi-Level GaN Inverter AC Power Source," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Phoenix, AZ, USA, July 2021. DOI: 10.1109/APEC42165.2021.9487044.

④ **P. S. Niklaus**, J. Azurza Anderson, D. Bortis, and J. W. Kolar, "Ultra-High Bandwidth GaN-Based Class-D Power Amplifier for Testing of Three-Phase Mains Interfaces for Renewable Energy Systems," in *Proc. of the International Conference on Renewable Energy Research and Applications (ICRERA)*, Brasov, Romania, November 2019. DOI: 10.1109/ICRERA47325.2019.8996585. *Best Paper Award*

③ **P. S. Niklaus**, D. Bortis, and J. W. Kolar, "Next Generation Measurement Systems with High Common-Mode Rejection," in *Proc. of the IEEE*

Workshop on Control and Modeling for Power Electronics (COMPEL), Padua, Italy, June 2018. DOI: 10.1109/COMPEL.2018.8460026.

Furthermore, the author had the pleasure to contribute to the following conference publications:

② J. W. Kolar, J. Azurza Anderson, S. Mirić, M. Haider, M. Guacci, M. Antivachis, G. Zulauf, D. Menzi, **P. S. Niklaus**, J. Miniböck, P. Papamanolis, G. Rohner, N. Nain, D. Cittanti, and D. Bortis, "Application of WBG Power Devices in Future 3-Φ Variable Speed Drive Inverter Systems - How to Handle a Double-Edged Sword," in *Proc. of the IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, December 2020. DOI: 10.1109/IEDM13553.2020.9372022.

① F. Krismer, V. N. Behrunani, **P. S. Niklaus**, and J. W. Kolar, "Optimized Cascaded Controller Design for a 10 kW / 100 kHz Large Signal Bandwidth AC Power Source," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Detroit, MI, USA, October 2020. DOI: 10.1109/ECCE44975.2020.9236149.

1.3.3 Workshops and Seminars

② **P. S. Niklaus**, D. Bortis, and J. W. Kolar, "100 kHz Large-Signal Bandwidth GaN-Based 10 kVA Class-D Power Amplifier with 4.8 MHz Switching Frequency and Measurement Techniques," presented at the *Real-Time Simulation Workshop*, Karlsruhe, Germany, November 2022. DOI: not available.

① **P. S. Niklaus**, M. Antivachis, and J. W. Kolar, "Measurement of Conducted EMI using a Three-Phase Active CM/DM Noise Separator," presented at the *IEEE Applied Power Electronics Conference and Exposition (APEC)* (virtual conference), New Orleans, LA, USA, March 2020. DOI: not available.

1.3.4 Patent

① **P. S. Niklaus**, D. Bortis, and J. W. Kolar, "Galvanisch getrenntes Messsystem (in German)," CH Patent CH716494A2, 2019. DOI: not available.

Part A

Converter Design

2

100 kHz Large-Signal Bandwidth GaN-Based 10 kVA Class-D Power Amplifier

This chapter summarizes the most relevant findings regarding the analysis, design and evaluation of a 100 kHz large-signal Bandwidth (BW) 10 kVA Power Amplifier (PA), which are also published in:

- **P. S. Niklaus**, J. W. Kolar, and D. Bortis, "100 kHz Large-Signal Bandwidth GaN-Based 10 kVA Class-D Power Amplifier with 4.8 MHz Switching Frequency," *IEEE Transactions on Power Electronics,* vol. 38, no. 2, pp. 2307-2326, February 2023.

Chapter Abstract

Power Amplifiers (PAs) are widely used, for example, to emulate the behavior of the power grid or electric machines under critical operating conditions, to measure the impedance of the power grid, or to generate specific power source/sink and impedance profiles in Power-Hardware-in-the-Loop (P-HIL) test environments. To accurately emulate dynamic effects and to characterize power electronic systems featuring Wide-Bandgap (WBG) power semiconductors, PAs with very high output voltage quality and ever higher Bandwidth (BW) at full output power are required, motivating the development of Ultra-High Bandwidth Power Amplifiers (UHBWPAs). While linear UHBWPAs achieve very high signal fidelity and BW, they suffer from a tremendously bad efficiency, demanding large cooling effort and resulting in uneconomical low-efficiency operation, particular at high power levels and/or during long-term tests. Therefore, this chapter investigates possibilities for a switch-mode realization of UHBWPAs with significantly higher efficiencies and power densities compared to existing solutions. There are two key concepts, namely series- and parallel-interleaving of multiple switching and/or converter cells, that allow to increase the *effective* switching frequency relevant to output filtering without increasing the individual device switching frequency that determines the per device switching losses. This chapter analyzes comprehensively the advantages and disadvantages of a combination of series- and parallel-interleaving in terms of loss, volume and complexity scaling. Finally, a UHBWPA with 10 kVA output power (single-phase), a nominal Root Mean Square (RMS) output voltage of 230 V, a full-power BW of 100 kHz, very high output voltage quality (3^{rd} and 5^{th} harmonic < 2.5 V and < 1.2 V, respectively), an efficiency > 95 %, a power density of 25 kW/dm^3 (410 W/in^3), and a switching frequency of 4.8 MHz is presented. A hardware demonstrator is built and extensive measurements verify the system performance and confirm the initial analyses based on loss models.

2.1 Introduction

Testing and characterization of power electronic systems is of great importance for their stable and reliable operation in the field. In industrial practice, Power-Hardware-in-the-Loop (P-HIL) test environments are mostly used for this purpose, since they offer a cost-effective way to test various operating modes, difficult to achieve with fully implemented hardware setups [18]. Here,

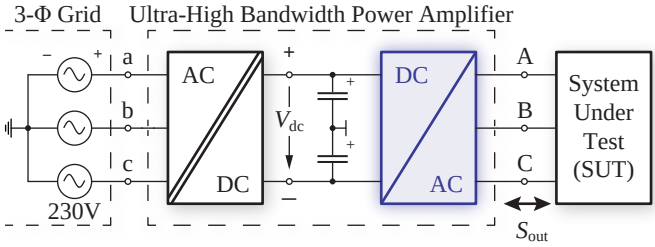


Fig. 2.1: System overview of the 100 kHz large-signal bandwidth Power Amplifier.

the behavior of a system model is emulated by means of a Real-Time Simulator (RTS) and a Power Amplifier (PA), where the latter is connected to a power electronic System Under Test (SUT) [19, 20]. Examples are the emulation of the power grid for testing grid-tied inverter stages (e.g. Photovoltaic (PV) inverters) or rectifiers with regard to grid compatibility (voltage imbalances, transient phenomena and/or frequency deviations) [21], the emulation of a certain virtual grid impedance [22, 23], or any dc or ac load, e.g., an electrical machine [24], for analyzing drive systems and/or their control loops. A further application scenario is the measurement of the grid impedance [25], which has a significant impact on the stability of grid-tied converters [26]. As shown, e.g., in [19], the Bandwidth (BW) of such PAs is the ultimate limiting factor for the achievable accuracy when emulating dynamic effects like voltage and/or load transients. Furthermore, maximum output voltage quality, i.e., minimum distortion and minimum noise, must be ensured while simultaneously offering the ability to source and/or sink multiple kVAs of output power (bidirectional power flow, arbitrary load phase angle φ). This clearly motivates the use of Ultra-High Bandwidth Power Amplifiers (UHBWPAs) as an interface to the SUTs. **Fig. 2.1** shows a very simplified block diagram of such a three-phase UHBWPA that is composed of a (typically isolated) three-phase grid interfacing rectifier stage to provide a (galvanically isolated) dc link voltage V_{dc} for the subsequent ultra-high BW inverter stage (dc/ac stage, highlighted in blue). The design of one single-phase module of the latter is the focus of this chapter. A full three-phase system can then easily be assembled with three such modules. Note that within this chapter the terms UHBWPA and PA (used interchangeably) refer to a single-phase module of the highlighted dc/ac stage from **Fig. 2.1** with the specifications listed in **Table 2.1**. In the nominal operating point, the full 10 kVA output power (per phase) is delivered for a nominal Root Mean Square (RMS) output

Tab. 2.1: Main system specifications for one single-phase of the investigated Power Amplifier (PA).

Parameter		Value
Peak Output Voltage per Phase	$V_{\text{out,pk}}$	0 . . . 350 V
Output Frequency	f_{out}	dc. . . 100 kHz
Output Power per Phase	S_{out}	0 . . . 10 kVA
DC Link Voltage	V_{dc}	800 V
Effective Switching Frequency	$f_{\text{sw,eff}}$	4.8 MHz
System Efficiency (Nom. Op. Pt.)	η	95 %

voltage of 230 V at a fundamental frequency of 100 kHz into an ohmic load ($S_{\text{out}} = P_{\text{out}} = 10\,\text{kW}$). Note that the term "large-signal BW" refers to the frequency at which the amplifier can provide its full-scale output power (at nominal output voltage and current) according to **Table 2.1**, as defined in [27].

Traditionally, such PAs are implemented as linear amplifiers, especially those with very high BW requirements [28, 29]. While they offer a very high output voltage quality, a major disadvantage of such solutions is their low efficiency (in particular for non-resistive loads and for power *sinking*), which is especially concerning for high output powers and/or long-term tests. Besides the inefficient operation, the high losses demand a large cooling effort and consequently lead to a low power density. For high output powers, switch-mode amplifiers (Class-D amplifiers) are therefore clearly preferred and are also increasingly found in commercial implementations [30, 31]. However, as explained later, to reach the desired output BW in a switch-mode PA, very high switching frequencies in the multi-MHz range are required.

In [27], different implementation options for such switch-mode PAs are presented and their advantages and disadvantages are compared with those of linear and hybrid PAs. Furthermore, a comprehensive review of currently available and developed PAs in industry and academia is given and a switch-mode realization composed of multiple cascaded (series-connected) Full-Bridges (FBs) that achieves the same full-power BW of 100 kHz and same single-phase output power of 10 kW is presented. The cascade/series-connection of complete converter cells (FBs), denoted Cascaded H-Bridge (CHB) converter, enables an increased *effective* switching frequency and reduced switch-node voltage steps, which is advantageous for output filtering. There are other PA designs realized as CHB converter that achieve remarkable performance, such as [32], a Magnetic Resonance Imaging (MRI) high-power

gradient PA with 7 kHz large-signal BW, an output capability of 1000 V/500 A, extremely low noise and high precision resulting from a sophisticated control method, or [33], a 41 level pulsed-sine generator with an output fundamental frequency of up to 1 MHz at an output voltage of up to 2 kV peak-to-peak used for cancer treatment in biomedical applications (output power and output signal quality unspecified). Similarly, [34] demonstrates a CHB based converter with a 1 MHz, 200 V amplitude sinusoidal output with a maximum power of 1.35 kW. The downside common to all CHB realizations, despite their very promising dynamic performance especially under aggressive load conditions and their full modularity (limited output voltage/power might still be available in case of failure of one CHB cell), is, however, the need for a galvanically isolated dc supply for each converter cell and the resulting relatively large coupling capacitances towards Protective Earth (PE), which cause significant Common Mode (CM) currents. These CM currents must be adequately filtered in order to not impair the converter operation.

A further interesting concept are hybrid analog/digital PA realizations that combine a high power, high efficiency switch-mode PA (main amplifier) with a relatively low power (yet high output voltage or high output current capability) linear PA (correction amplifier) to achieve maximum output BW and/or maximum signal fidelity/precision and yet moderate system efficiency. They can be seen as compromise between purely analog and fully digital implementations. There are three possible configurations, namely series- and parallel-connection and envelope tracking, which are comprehensively reviewed in [35]. In [36, 37], a CHB based main amplifier is connected in series to a linear correction amplifier in a way that the closed-loop dynamics are determined solely by the latter. Thereby, a BW of 105 kHz of the linear amplifier is achieved, which, e.g., allows to generate full-scale test signals of up to 60 kHz with the hybrid PA. An example of a parallel hybrid PA is shown in [38], where the linear amplifier defines the output voltage and the via a single filter inductor coupled switch-mode amplifier delivers the bulk load current. In that sense, the linear amplifier can be seen as active filter of the switch-mode main amplifier. Similarly, the linear amplifier could be replaced by a low power, fast switching (and therefore, high BW) digital converter, shown, e.g., in [39, 40]. Envelope tracking is a technique where a switch-mode converter forms a varying supply voltage for the linear PA based on the desired output voltage envelope, in order to minimize the voltage drop across and hence the conduction losses in the linear power transistors [41]. A particularly interesting application field are Radio-Frequency (RF) PAs where an RF signal with varying amplitude envelope has to be amplified.

Realizations of such an envelope tracking PA based on a three-level buck converter are presented in [42, 43] where experimental results verify accurate tracking of a 10 kHz rectified sine wave with an amplitude of 4 V. A boost type solution for higher operating voltages (up to 130 V rms) and power levels (up to 1.5 kW) and a tracking BW of 1 kHz is shown in [44].

In contrast to CHB converter cells and/or hybrid analog/digital and digital/digital approaches, which typically are more complex in realization, this chapter discusses the realization of an entirely switch-mode PA with multiple Switching Cells (SCs) connected in parallel and series, which, in addition to reducing the switch-node voltage steps, also allows an increase in the *effective* switching frequency [45]. Within this chapter we use the term *Switching Cell* for one half-bridge with corresponding dc link capacitor, unlike CHB *Converter Cells*, which are composed of one FB with dedicated dc link capacitor. The aim is to explore the performance limitations by pushing the (effective) switching frequency to very high values, while still keeping circuit complexity at a reasonable level. In [46], the optimal number of parallel- and series-connected SCs for the specifications given in **Table 2.1** has already been discussed. In this chapter, this analysis is extended and verified using a hardware demonstrator.

2.1.1 Overview of this Chapter

Section 2.2 derives the circuit topology, focusing on semiconductor loss scaling depending on the number of series- and parallel-interleaved SCs and ultimately a suitable topology is selected. **Section 2.3** then shows a detailed design procedure for the High-Frequency (HF) output filter inductors before **Section 2.4** presents the realized hardware demonstrator of the UHBWPA including a liquid cooling system and highlights important design aspects. The performance of the hardware demonstrator is experimentally verified in **Section 2.5**. Finally, **Section 2.6** concludes this chapter.

2.2 Converter Topology

2.2.1 Switch-Mode Power Amplifier

The BW of switch-mode PAs is limited by the necessary output filter (typically a $k-$stage second-order LC filter with corner frequency f_c and an attenuation of $-k \cdot 40$ dB/dec), which attenuates the HF spectral content in the switched output voltage, such that the local average (averaged over one switching pe-

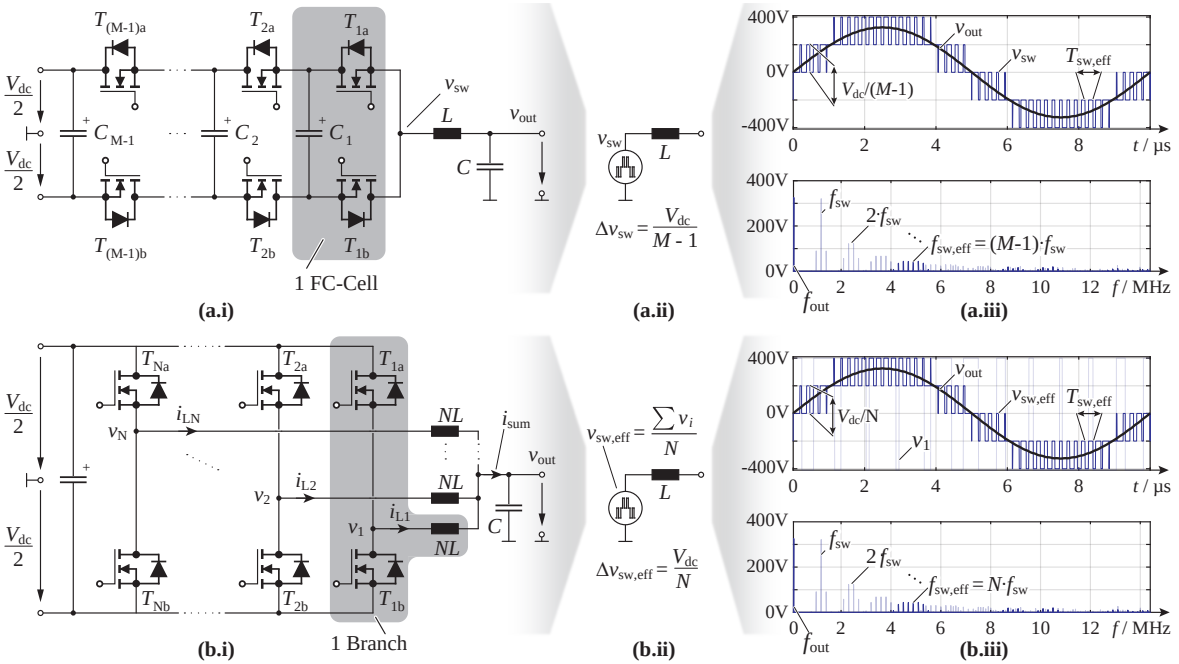


Fig. 2.2: (a.i) Circuit diagram of an M-level Flying Capacitor Converter (FCC) with one FC-cell highlighted, **(a.ii)** resulting equivalent circuit for the switch-node voltage v_{sw} and **(a.iii)** corresponding time- and frequency-domain representations of v_{sw} for $M = 5$, i.e., a 5-level converter (4 FC cells), clearly indicating the multi-level nature of the output voltage with the first occurring frequency component (above f_{out}) in the spectrum at the effective switching frequency $f_{sw,eff} = (M-1) \cdot f_{sw}$. **(b.i)** Parallel interleaving of multiple (N) two-level (2L) branches leading to **(b.ii)** the equivalent circuit with the effective switch-node voltage $v_{sw,eff}$ formed with the inductive voltage divider. The same multi-level waveform **(b.iii)** as for (a.iii) is achieved by taking the mean of all individual switch-node voltages and thus the first frequency component (above f_{out}) in the spectrum is located at $f_{sw,eff} = N \cdot f_{sw}$ (here shown for 4 interleaved 2L branches).

riod T_{sw}) remains [38]. This local average is tracking a programmed reference voltage/waveform v_{ref} given by the desired application scenario (e.g., defined by the RTS in P-HIL test environments). Within this chapter the discussion is restricted to single-stage *LC* output filters. Assuming a naturally sampled (continuous) Pulse Width Modulation (PWM) with a triangular carrier and a purely sinusoidal v_{ref} with frequency f_{out}, the switched voltage v_{sw} contains spectral components at multiples of the switching frequency $n \cdot f_{sw}$ and the respective sidebands $n \cdot f_{sw} \pm k \cdot f_{out}$ with $n \in \mathbb{N}$ and $k \in \{2, 4, \ldots\}$ if n is odd or $k \in \{1, 3, \ldots\}$ if n is even [47]. To attenuate sidebands at frequencies below f_{sw}, the filter corner frequency f_c must be substantially lower than f_{sw}. To account for effects such as finite filter slopes (e.g., −40 dB/dec) and component tolerances, in practice, $f_c < f_{sw} / 10$ is typically chosen [13]. At the same time, f_c must be higher than the maximum anticipated output frequency $f_{out,max}$ to avoid exciting the filter resonance ($f_c \geq k_f \cdot f_{out,max}$). Thereby, to reach the desired BW of 100 kHz, switching frequencies in the range of several MHz are required ($f_{sw} \geq 10 \cdot k_f \cdot f_{out,max}$).

The authors of [27] derived the minimum required f_{sw} to reach a certain output voltage quality (quantified by means of the peak-to-peak output voltage ripple $\Delta v_{out,pp}$) for a certain maximum capacitive current and maximum inductive voltage drop in the respective filter elements. For a practical case of $\Delta v_{out,pp} = 2\,\% \cdot V_{dc}$, 30 % capacitive current and 15 % inductive voltage drop a standard 2L Voltage Source Inverter (VSI) requires $f_{sw} = 5\,\text{MHz}$. Even with the ever more widespread availability of Wide-Bandgap (WBG) power semiconductors with significant reduction of switching losses compared to their traditional Silicon (Si) counterparts, f_{sw} in normal 2L operation is still limited by the (hard) switching losses, particularly if a certain efficiency (95 % in the case at hand) is targeted. Therefore, alternative circuit topologies to the 2L-VSI are required, which allow to increase the *effective* switching frequency $f_{sw,eff}$ of the switched voltage seen by the output filter without the penalty of high switching losses per device (switching losses distributed between multiple devices), i.e., the individual devices switch at a much lower frequency f_{sw}.

Based on results of a previous study on this topic in [46], the basic idea of series- and parallel-interleaving is briefly repeated to ultimately find the most suitable combination of both approaches, i.e., a series-parallel-interleaved multi-level converter topology, which best fulfills the design goals (cf. **Table 2.1**).

Series Interleaving

Multi-level converters are used to increase the number of voltage levels of v_{sw} applied to the output filter inductor by phase-shifting the operation of $(M-1)$ series-connected SCs or full converter cells. Each cell is operated with f_{sw}, generating M distinct voltage levels at the switch-node as depicted in **Fig. 2.2 (a.ii)-(a.iii)**. The HF harmonics of v_{sw} are shifted to higher frequencies, i.e., to $f_{sw,eff} = (M-1) \cdot f_{sw}$. Furthermore, the blocking voltage stress of the switches is reduced to $V_{dc} / (M-1)$, which on the one hand renders certain semiconductor technologies usable in application scenarios where they normally cannot be used (e.g., 600 V Gallium-Nitride (GaN) devices with an 800 V dc link) and on the other hand offers the possibility to use lower voltage devices with a potentially better Figure-of-Merit (FOM) [48]. From the various multi-level topologies described in literature, such as Modular Multi-Level Converters (MMCs) [49] (which need active control of the individual submodule capacitor voltages [50]), CHB [51] and Neutral-Point Clamped (NPC) converters [52, 53], the Flying Capacitor Converter (FCC) initially proposed in [54] and depicted in **Fig. 2.2 (a.i)** has the fundamental advantage that it can generate a high number of voltage levels with reasonable semiconductor effort, lower circuit complexity compared to other multi-level approaches and is capable of generating a dc output without auxiliary circuits for active voltage balancing of the stacked dc link capacitors. It has to be mentioned, however, that under certain operating and load conditions (e.g., low inductor current ripple and dc output voltage component), active balancing of the Flying Capacitor (FC) voltages can be required and can be implemented with relatively simple control algorithms, such as the one presented in [42]. As mentioned in the chapter introduction, there are several application scenarios where CHB converters are very well suited but due to circuit complexity and overall system efficiency considerations (an isolated dc link voltage needs to be provided to each individual CHB cell), the FCC is identified as most-promising converter candidate for the given application. The operation of the M-level FCC has been widely discussed in literature [55–57] and a further explanation is omitted here.

Parallel Interleaving

High current ratings demand an increased semiconductor area, which can either be realized with large devices or by paralleling N small devices. In the latter case, phase-shifted operation of N parallel-interleaved 2L SCs as shown in **Fig. 2.2 (b.i)**, hereinafter called branches, can favorably be used (commonly

also referred to as multi-phase operation in literature) [58]. Not only does this lead to a (partial) cancellation of the current ripple between the individual branches, and hence a reduction of the ripple in the summed output current i_{sum} seen by the filter capacitance C, but at the same time, an increased effective switching frequency $f_{\text{sw,eff}} = N \cdot f_{\text{sw}}$ is obtained at the output capacitor as illustrated in **Fig. 2.2 (b.ii)-(b.iii)** [59]. There, f_{sw} denotes the switching frequency of each individual 2L SC and N the number of interleaved branches. The *effective* (or virtual) switch-node voltage $v_{\text{sw,eff}}$ results from the inductive voltage divider and shows a multi-level nature that is equal for both, one single series-interleaved M-level bridge leg and $N = M - 1$ times parallel-interleaved two-level half-bridges (cf. **Fig. 2.2 (a.iii)** and **(b.iii)** for $M = 5$ and $N = 4$, respectively). In both cases the voltage spectrum contains no components between f_{out} and $f_{\text{sw,eff}}$ (assuming natural sampling PWM), and therefore, the filtering effort can be drastically reduced while keeping a moderate switching frequency f_{sw} of each half-bridge, which is beneficial in terms of switching losses per device. Note, that coupled inductors can be used to symmetrize the individual branch currents $i_{\text{L}i}$ and to further reduce the current ripple, while achieving the same or even better transient response [60,61]. Uncoupled filter inductors, however, are offering the desired flexibility to operate UHBWPAs either as single-phase high current sources or three-phase lower current sources, which extends the possible application scenarios as mentioned earlier.

Series-Parallel Interleaving

Since series-interleaving distributes the voltage stress among several devices and parallel interleaved operation distributes the current stress among the parallel branches, a combination of the two approaches gives additional degrees of freedom in terms of loss and stress distribution. For a parallel-interleaved multi-level converter, the effective switching frequency of the current ripple seen by the filter capacitor C is given as

$$f_{\text{sw,eff}} = N \cdot (M - 1) \cdot f_{\text{sw}} = n_{\text{SC}} \cdot f_{\text{sw}}, \tag{2.1}$$

where $n_{\text{SC}} = N \cdot (M - 1)$ denotes the total number of utilized SCs. At the same time, the effective (or virtual) switch-node voltage is composed of $n_{\text{SC}} + 1$ distinct voltage levels, i.e., the voltage steps applied to the output filter are $\Delta v_{\text{sw,eff}} = V_{\text{dc}}/n_{\text{SC}}$. Considering a required $f_{\text{sw,eff}}$ in the range of 5 MHz, a combination of both approaches allows for a low individual device switching frequency f_{sw} and offers both, voltage and current stress sharing.

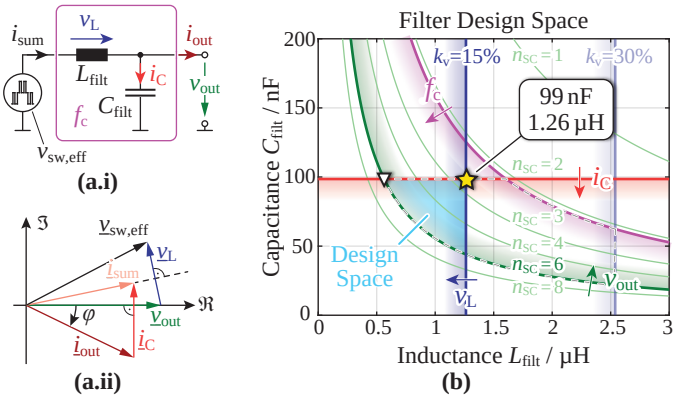


Fig. 2.3: (a.i) Equivalent circuit of N parallel-interleaved M-level series-interleaved branches indicating the effective switch-node voltage $v_{sw,eff}$, the effective filter inductance L_{filt} and the filter capacitance C_{filt} for a single-stage output filter. **(a.ii)** Fundamental frequency phasor diagram showing the impact of a load phase angle φ (here: ohmic-inductive load) and the reactive current and voltage in the filter elements. **(b)** Representation of four design criteria that define the valid range for the filter components in the filter design space according to [62], displayed for different number of switching cells $n_{SC} = N \cdot (M-1)$. The valid design space for $n_{SC} = 6$ (realizable, e.g., with $M = N = 3$) is highlighted and the preferred solution is marked with ★.

2.2.2 Output Filter Design

To design the single-stage LC output filter, four different constraints are derived based on the general HF equivalent circuit of a switching stage depicted in **Fig. 2.3 (a.i)**, where $v_{sw,eff}$ denotes the unfiltered $(n_{SC}+1)$−level switched voltage with switching frequency $f_{sw,eff}$ that is generated with the series- and parallel-interleaved converter (with an arbitrary M and N).

In the resultant filter design space proposed in [62], the criteria are graphically visualized on an L_{filt} vs. C_{filt} plane (cf. **Fig. 2.3 (b)** for different n_{SC} and highlighted for $n_{SC} = 6$). Note that for the output filter operation it is irrelevant by which combination of M and N a certain n_{SC} is obtained.

The primary goal of UHBWPAs is to achieve maximum BW. This criterion is formulated with a minimum ratio k_f between filter corner frequency $f_c = 1/(2\pi \cdot \sqrt{L_{filt} C_{filt}})$ and maximum output frequency $f_{out,max}$, i.e.,

$$L_{filt} \cdot C_{filt} \leq \frac{1}{(2\pi)^2 \cdot k_f^2 \cdot f_{out,max}^2}, \tag{2.2}$$

which corresponds to a minimum required f_c to prevent peaking of v_{out} at the maximum output frequency. (2.2) embodies a hyperbola in the design space and is illustrated with the pink line in **Fig. 2.3 (b)** for $f_{out,max} = 100\,\text{kHz}$ and $k_f = 4$ (empirical value).

To maximize the output voltage quality (besides the BW the main goal in PAs) a certain maximum peak-to-peak output voltage ripple $\Delta v_{out,pp}$ has to be defined. Assuming a *fixed* $f_{sw,eff}$ (e.g., 4.8 MHz to be in the range of the required $\approx 5\,\text{MHz}$ to achieve the desired output dynamics; $f_{sw,eff}$ can be achieved with any desired number n_{SC} of SCs, each switching at $f_{sw,eff}/n_{SC}$), the *relative* output voltage ripple $\Delta v_{out,pp}/V_{dc}$ is found as

$$\Delta v_{out,pp}/V_{dc} = \frac{1}{32 \cdot n_{SC} \cdot L_{filt} \cdot C_{filt} \cdot f_{sw,eff}^2} \tag{2.3}$$

and corresponds to a hyperbola in the filter design space (green curves in **Fig. 2.3 (b)** for different n_{SC} and for $\Delta v_{out,pp}/V_{dc} = 0.4\,\%$ that corresponds to 1 % peak-to-peak ripple with respect to the output voltage amplitude in the nominal operating point, i.e., $\Delta v_{out,pp} = 3.25\,\text{V}$). There, V_{dc} is the full dc link voltage, even though in practice, a split dc link with $2 \times V_{dc}/2$ is used. With $f_c = 1/(2\pi \cdot \sqrt{L_{filt}C_{filt}})$, (2.3) can be rearranged to

$$f_c = \sqrt{\frac{8}{\pi^2} \cdot n_{SC} \cdot f_{sw,eff}^2 \cdot \frac{\Delta v_{out,pp}}{V_{dc}}} \tag{2.4}$$

and shows that with increasing M and/or N (that is, with increasing n_{SC}) the same output voltage quality (e.g., $\Delta v_{out,pp}/V_{dc} = 0.4\,\%$) is achieved with a higher filter corner frequency. In fact, (2.4) gives the maximum allowed f_c to still achieve the desired output voltage quality. This clearly motivates the series- and parallel-interleaved circuit topology, because for a given effective switching frequency $f_{sw,eff} = n_{SC} \cdot f_{sw}$ a realization with series- and parallel-interleaving ($n_{SC} > 1$), thanks to the increased maximum possible f_c, therefore reduces the filtering effort. In any case, a higher f_c allows to use smaller filter components and thereby advantageously helps to minimize the system volume.

Additional design constraints result from the maximum voltage drop v_L and maximum current i_C in the filter elements at the nominal operating point with $V_{out} = 230\,\text{V rms}$, $P_{out} = 10\,\text{kW}$ (ohmic load) and the maximum output frequency $f_{out,max} = 100\,\text{kHz}$, i.e., as already calculated in [27],

$$2\pi \cdot f_{out,max} \cdot L_{filt} \cdot I_{out} \leq k_v \cdot V_{out} \tag{2.5}$$

$$2\pi \cdot f_{out,max} \cdot C_{filt} \cdot V_{out} \leq k_i \cdot I_{out} \tag{2.6}$$

with the nominal RMS output current $I_{out} = P_{out}/V_{out}$ (for an ohmic load). k_v and k_i are the maximum allowed fractions of V_{out} and I_{out} to appear across L_{filt} and flow through C_{filt}, respectively. (2.5) and (2.6) correspond to the vertical blue and horizontal red line in the design space in **Fig. 2.3 (b)** and result in $L_{filt} \leq 1.26\,\mu H$ and $C_{filt} \leq 99\,nF$ with $k_v = 15\,\%$ and $k_i = 33\,\%$. The intersection of the two lines gives the minimum possible f_c. As can be seen with the highlighted valid design space (cyan) for $n_{SC} = 6$, the maximum inductor voltage drop and maximum capacitor current constraints overrule the minimum f_c criterion from (2.2) for the given values of k_f, k_v and k_i. If, for example, $k_v = 30\,\%$ would be chosen (semi-transparent blue line), the design space would be limited by the maximum f_c according to (2.2) for $L_{filt} > 1.6\,\mu H$ (cf. dashed gray outline in **Fig. 2.3 (b)**). Note that only the output voltage quality criterion depends on n_{SC}. In the interest of maximum output voltage quality, the minimum possible filter corner frequency $f_{c,min} = 1/(2\pi\sqrt{L_{filt,max}C_{filt,max}}) = 472\,kHz$ (marked with ★ in **Fig. 2.3 (b)**) with $L_{filt,max} = 1.26\,\mu H$ and $C_{filt,max} = 99\,nF$ is selected. If the smallest possible filter volume is favored, the design with $C_{filt} = C_{filt,max}$ and the minimum required L_{filt} should be selected from the design space (marked with ▼ in **Fig. 2.3 (b)** for $n_{SC} = 6$). Generally, a low filter inductance and high filter capacitance facilitates a low converter output impedance to prevent load dependence of the output voltage. Note that depending on the load phase angle φ, the inductive voltage drop across L_{filt} and the capacitive current through C_{filt} lead to an increase or a decrease of $v_{sw,eff}$ and i_{sum} as illustrated with the fundamental frequency phasor diagram in **Fig. 2.3 (a.ii)**. In the nominal operating point with an ohmic load, the chosen k_v and k_i increase the required $v_{sw,eff}$ by $\approx 1\,\%$ and i_{sum} by $\approx 4.5\,\%$.

From **Fig. 2.3 (b)** follows that a valid design space only results for $n_{SC} \geq 3$, which again proves that for a given $f_{sw,eff}$ a higher n_{SC} is beneficial in terms of filtering, i.e., that for $f_{sw,eff} = 4.8\,MHz$, a single 2L ($n_{SC} = 1$) or three-level ($n_{SC} = 2$) SC could not achieve sufficient output voltage quality. As will be shown later, for the given specifications and the available power semiconductors, only designs with $M \geq 3$ and $N \geq 2$ ($n_{SC} \geq 4$) are feasible.

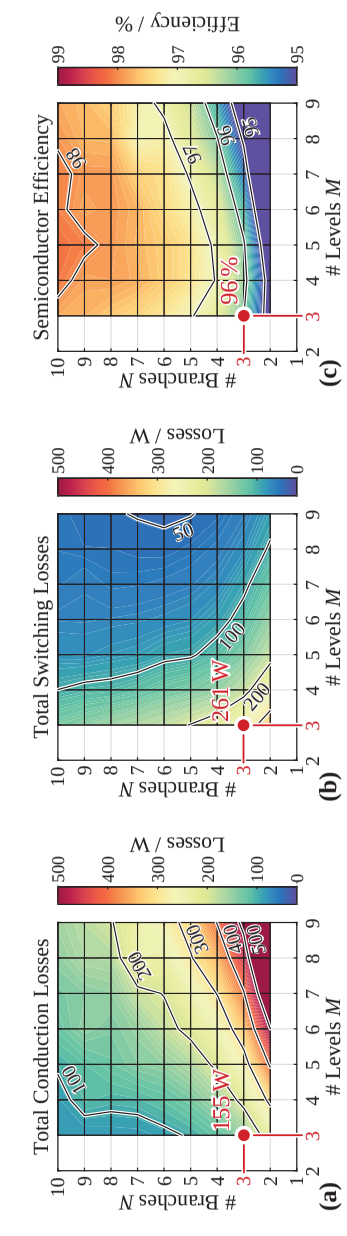


Fig. 2.4: Characteristics of a class-D amplifier inverter stage realization with N parallel-interleaved M-level Flying Capacitor Converter (FCC) branches. **(a)-(b)** Total power semiconductor conduction and switching losses and **(c)** resulting efficiency considering only the total semiconductor losses. For the calculation, 70 mΩ 600 V GaN High-Electron-Mobility Transistors (HEMTs) are considered [63].

2.2.3 Quantitative Performance Evaluation

To ultimately determine the best-suited combination of N parallel-interleaved $M-$level series-interleaved branches, a comprehensive simulation model is used to estimate the occurring converter losses. Due to the arbitrary output voltage and current waveform, generally, Hard Switching (HSW) losses occur. Given the at the same time relatively high expected device switching frequency f_{sw}, only GaN power semiconductors can be reasonably utilized in this application, since both, Silicon-Carbide (SiC) and Si devices have too high specific switching losses (either due to the output charge Q_{oss} and/or the reverse recovery charge Q_{rr}). Generally, GaN devices with a small die area and therefore low Q_{oss} are preferred as they have lower Zero-Current Switching (ZCS) and HSW losses. Furthermore, the device must be available in a package that allows adequate heat dissipation, since despite the series- and parallel-interleaved operation, substantial losses per device are expected. To avoid heat dissipation through the Printed Circuit Board (PCB), e.g., by means of thermal vias [64] or advanced PCB technologies such as copper inlays or PCB integrated power devices [65], only top-side cooled devices are considered. GaN High-Electron-Mobility Transistors (HEMTs) are available either as High-Voltage (HV) devices with blocking voltage capabilities of $600 - 650\,\mathrm{V}$ or as Low-Voltage (LV) devices with blocking voltages of $100 - 200\,\mathrm{V}$. The latter are only applicable for $M \geq 7$ voltage levels and therefore, $600\,\mathrm{V}$ devices are better suited for the analysis under the given specifications. $70\,\mathrm{m\Omega}$ $600\,\mathrm{V}$ GaN Gate Injection Transistors (GITs) (a special realization of GaN HEMTs [66]) turned out to be best-suited from the currently available devices on the market in terms of switching performance and particularly regarding heat dissipation capabilities. As will be shown later in more detail, the overall losses are prominently dominated by the HSW losses. This again motivates that in general a low die area and therefore, a low output charge Q_{oss} of the semiconductor is preferred. Moreover, top-side cooled devices allow to decouple the electrical layout of the power commutation loop from the thermal design. Thereby, no thermal vias and/or copper inlays are required, which on the one hand would limit the possibilities to design a power commutation loop with as low an inductance as possible and on the other hand would also limit the heat dissipation capabilities because the heat has to flow through the PCB. From the available top-side cooled $600\,\mathrm{V}/650\,\mathrm{V}$ devices, many are intended for high current applications, i.e., feature a low $R_{ds,on}$ and thus a relatively large Q_{oss}, and are therefore not well suited for this application. The selected $70\,\mathrm{m\Omega}$ devices have a Q_{oss} of only $41\,\mathrm{nC}$ (at $400\,\mathrm{V}$) and at the same time offer a large metallic cooling pad (area

of $\approx$ 0.8 cm^2). A similar device would be [67] with $R_{\mathrm{ds,on}} = 67\,\mathrm{m\Omega}$ but it has a higher Q_{oss} of 47 nC (14 % more than [63]) and a smaller cooling pad of only $\approx$ 0.16 cm^2 (80 % less than [63]). With estimated losses of $\approx$ 35 W per semiconductor (cf. **Fig. 2.4**) the power loss density is the limiting factor for the thermal design and therefore, a large cooling surface is preferred. There are other devices with larger cooling surface, e.g., [68] with $\approx$ 0.47 cm^2 (still 40 % less compared to [63]) but they have a Q_{oss} of 134 nC (3 $\times$ more compared to [63]), which would significantly increase the already high switching losses (cf. loss breakdown in **Fig. 2.11**) and are thus not favored. The selected 70 mΩ devices are therefore a reasonable trade-off between the considered aspects. In addition, these particular devices by means of a so-called hybrid drain prevent the phenomenon of increased dynamic on-state resistance (dynamic $R_{\mathrm{ds,on}}$) after application of a large drain-source voltage (current collapse) reported to occur in GaN switches [69]. An additional p-GaN region electrically connected to the drain injects holes during the off-state, which completely release the trapped electrons and thus eliminates the effect of the dynamic on-state resistance [70, 71]. This is a significant advantage for operation with high switching frequencies. Therefore, these devices are used for the loss evaluation [63]. It has to be mentioned, however, that there is still a significant temperature dependence of $R_{\mathrm{ds,on}}$, which is considered in the loss model by utilizing the worst-case $R_{\mathrm{ds,on}}$, i.e., the value at a junction temperature of 125°C.

Fig. 2.4 shows the result of a detailed loss analysis for different possible converter realizations with N parallel-interleaved M−level series-interleaved branches. **Fig. 2.4 (a)** shows the conduction losses, **Fig. 2.4 (b)** the switching losses and **Fig. 2.4 (c)** the resultant semiconductor efficiency for different combinations of M and N in the nominal operating point. In all cases, the output filter with $L_{\mathrm{filt,max}}$ and $C_{\mathrm{filt,max}}$ is considered. The reverse conduction losses during the dead time are included in the total conduction losses of **Fig. 2.4 (a)** assuming a fixed dead time of $t_{\mathrm{d}} = 24$ ns (a more detailed explanation regarding the selection follows just below). Note that at least $M_{\mathrm{min}} = 3$ voltage levels are required in each bridge leg for $V_{\mathrm{dc}} = 800$ V when using 600 V switches. Similarly, at least $N_{\mathrm{min}} = 2$ parallel-interleaved branches are required to not exceed the maximum current rating of the utilized switches (if paralleling of multiple devices is not considered). Moreover, the efficiency target can only be achieved with $N > 2$.

Conduction Losses

From **Fig. 2.4 (a)**, it can be deduced that for any given N, the conduction losses increase linearly with increasing M, since at any time $(M-1)$ series-connected transistors conduct the branch current. Similarly, for a given M, they scale with $1/N^{\alpha}$ whereas ideally, $\alpha = 1$, meaning that the current perfectly distributes among the N branches. In practice, $0 < \alpha < 1$ because only the fundamental component of the total inductor current (i_{sum}) splits equally among the N branches but the current ripple does not scale with $1/N$ for a fixed $f_{\text{sw,eff}}$ and a fixed L_{filt}. It does, however, reduce with increasing M, because the voltage difference (and hence the voltage-time area) applied to the inductor reduces.

Switching Losses

The switching losses in **Fig. 2.4 (b)** include calorimetrically measured HSW and Soft Switching (SSW) (Zero-Voltage Switching (ZVS)) losses [46]. Depending on the switched current, full ZVS may not be possible within the given dead time ($t_{\text{d}} = 24\,\text{ns}$ in all cases — a minimum t_{d} is favorable to minimize Low-Frequency (LF) harmonics in v_{out} as will be seen in **Section 2.5.2**), so Partial-Hard Switching (PHSW) occurs where a certain residual charge on the output capacitor is shorted inside the transistor. PHSW losses are modeled based on the approach presented in [72] and are included in the calculation. Note that generally, the selection of the dead time is subject to an optimization process to minimize the overall losses. A large dead time enables full ZVS for lower switched currents but at the same time has the disadvantage of increasing the reverse conduction (3^{rd} quadrant) losses due to the increased voltage drop between source and drain. This is in particular a concern with GaN semiconductors, which do not have a physical body diode but are inherently symmetrical devices such that during reverse conduction the voltage between source and drain equals the threshold voltage plus the absolute value of the negative gate to source voltage to keep the transistor safely in the off-state [73]. Ideally, the dead time is adapted based on the switched current in order to always achieve full ZVS without the disadvantage of keeping the complementary device in the off-state for an unnecessary long time with increased reverse conduction losses [72]. A low fixed dead time on the other hand has the advantage of giving the lowest output voltage distortion (cf. **Section 2.5.2**) but achieves full ZVS only for higher switched currents ($\approx$ 4 A in the given case), i.e., PHSW is more likely to occur. In the

interest of maximum output voltage quality, a value as low as possible (but fixed) is selected for the dead time ($t_\mathrm{d} = 24\,\mathrm{ns}$) in the following analysis.

The HSW losses per device can be modeled as

$$P_\mathrm{HSW} = f_\mathrm{sw}\left(Q_\mathrm{oss}V_\mathrm{sw} + \frac{1}{2}\frac{V_\mathrm{sw}^2}{\mathrm{d}v/\mathrm{d}t}I_\mathrm{sw} + \frac{1}{2}\frac{I_\mathrm{sw}^2}{\mathrm{d}i/\mathrm{d}t}V_\mathrm{sw}\right) \tag{2.7}$$

with the transistor output charge Q_oss (which is in fact voltage dependent, i.e., $Q_\mathrm{oss}(V_\mathrm{sw})$), the switched voltage V_sw, the switched current I_sw and the voltage and current transition slopes $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$. Only the effect of charging and discharging of the output capacitance C_oss as well as $V-I$ overlap during the turn-on transition (turn-off transition assumed lossless) is considered in (2.7) [74]. According to [46], the term in (2.7) that changes quadratically with I_sw can be neglected unless very high currents are switched ($\mathrm{d}i/\mathrm{d}t \to \infty$). In the considered device, $Q_\mathrm{oss}(V_\mathrm{sw})$ scales approximately linearly with V_sw and therefore, for a given I_sw the HSW losses are expected to scale quadratically with V_sw under the simplified assumption of a constant $\mathrm{d}v/\mathrm{d}t$ independent of the switched voltage and current. For a given V_sw, however, a linear relation between the HSW losses and I_sw is expected on top of a certain loss offset (ZCS losses, $Q_\mathrm{oss}V_\mathrm{sw}$ term). In a series- and parallel-interleaved converter, V_sw reduces linearly with M and similarly, the fundamental component of I_sw reduces linearly with N. For a fixed $f_\mathrm{sw,eff}$ and a fixed L_filt the current ripple, however, does not scale with N. Therefore, with increasing N (and fixed M), i.e., decreasing fundamental component of I_sw but constant current ripple, the HSW losses are expected to scale with $1/N^\beta$ ($\beta > 1$). For low switched currents, that is for high N, e.g., $N > 6$, the ZCS and/or PHSW and/or SSW losses dominate and the simplified scaling with $1/N^\beta$ is not valid anymore as seen in **Fig. 2.4 (b)**.

With increasing M (and fixed N) and therefore decreasing V_sw, a loss scaling with $1/(M-1)^\gamma$ and $\gamma = 2$ would be forecasted using (2.7). Yet, **Fig. 2.4 (b)** rather indicates a linear relation, i.e., $\gamma = 1$, which has two reasons:

i) Calorimetric HSW loss measurements confirm the quadratic dependence on V_sw only for low currents ($I_\mathrm{sw} < 8\,\mathrm{A}$), but for higher I_sw the losses scale linearly with V_sw.

ii) For a given N, the hard switched current I_sw increases with increasing M due to the accompanying lower current ripple. This accordingly leads to larger HSW losses and counteracts the expected quadratic decrease.

Semiconductor Efficiency

Finally, **Fig. 2.4 (c)** shows the resultant expected semiconductor efficiency η_{semi} considering the total forward and reverse conduction, HSW, PHSW and SSW losses, i.e.,

$$\eta_{\text{semi}} = \frac{P_{\text{out}}}{P_{\text{out}} + \underbrace{P_{\text{cond,tot}}}_{\text{Fig. 2.4 (a)}} + \underbrace{P_{\text{sw,tot}}}_{\text{Fig. 2.4 (b)}}} \tag{2.8}$$

in the nominal operating point ($P_{\text{out}} = 10\,\text{kW}$). As expected from the loss scaling, η_{semi} improves with increasing N, whereas for a given N it generally decreases with increasing M as the conduction losses start to dominate. With very high M and N, efficiencies up to 98 % are theoretically possible, but come at the expense of a very complex design. Fortunately, the efficiency target is reached already with lower M and N. It has to be kept in mind that the presented calculation only considers one specific switch. For $M \geq 7$, LV 200 V GaN HEMTs could be used, however, as shown in [48], the area-specific on-state resistance $r^*_{\text{ds,on}}$ (in $\Omega{\cdot}\text{m}^2$ or $\text{m}\Omega{\cdot}\text{mm}^2$) of GaN devices roughly scales linearly with the required Blocking Voltage from Drain to Source (BVDS). Therefore, the penalty of utilizing a high BVDS GaN device at a lower voltage is not as high compared to Si devices, which scale roughly with $\text{BVDS}^{2\ldots2.5}$.

2.2.4 Design Selection

To choose a suitable design, not only the losses but also the volume, particularly of the FCs and the branch inductors, as well as the overall design complexity (e.g. placement of Gate Drivers (GDs) for each of the $2 \cdot n_{\text{SC}}$ switches, layout of the commutation loop in each SC, routing of the signals, etc.) must be considered.

Flying Capacitor Volume

The FC volume is approximated using a polynomial fit of the capacitance density vs. rated voltage from commercially available ceramic capacitors. As shown, e.g., in [56], the required capacitance is found as a function of the peak switched current and the desired *absolute* voltage ripple Δv_{FC} (5 V peak-to-peak in this case) as well as the frequency $f_{\text{iLpp}} = f_{\text{sw,eff}}/N$ at which the FCs are charged and discharged (equal to the current ripple frequency in each branch). The peak switched current reduces slightly with increasing M for a given N thanks to the smaller current ripple and therefore, the required capacitance

per FC reduces. Nevertheless, by adding an additional voltage level with series-interleaving ($M' = M + 1$), the FC volume automatically increases, since on top of the already present FCs of the $M-$level series-interleaved bridge leg now an additional FC is placed. While the voltage rating of each additional capacitor is smaller, the overall FC volume still scales linearly with M. However, with increasing N, for a given M, the volume scales even nearly quadratically for three reasons:

i) Every branch needs the same number of FCs at the same voltage levels (volume scaling linear with N).

ii) Due to the fixed $f_{\mathrm{sw,eff}}$, f_{iLpp} reduces with $1/N$. Thus the required capacitance and therefore the required FC volume increases linearly with N.

iii) The peak switched current, however, does not linearly reduce with increasing N, which would lead to a scaling of the required capacitance and FC volume with $1/N$, but due to the constant current ripple shows a less pronounced dependence on N, as explained earlier.

Branch Inductor Volume

The volume of each individual branch inductor L_{br} scales roughly with $k_{\mathrm{VL}} = L_{\mathrm{br}} \cdot i_{\mathrm{L,pk}} \cdot I_{\mathrm{L,rms}}$, where k_{VL} is an indicator for the stored energy in L_{br}. With a fixed value for L_{filt}, the branch inductance scales linearly with N and is independent of M. The branch inductor RMS current $I_{\mathrm{L,rms}}$ does not significantly reduce with increasing M (i.e., lower current ripple), but reduces approximately with $1/N$, since it is almost entirely defined by the fundamental component, which scales with $1/N$. The branch inductor peak current $i_{\mathrm{L,pk}}$ reduces with increasing M due to the smaller current ripple (more pronounced for high N) and as explained above, scales with $1/N^{\alpha}$, $0 < \alpha < 1$ (only the fundamental component scales with $1/N$, whereas the ripple remains constant, hence there is a more pronounced reduction with increasing N for high M where the current ripple is low). All in all, the total volume of all N required branch inductors reduces with increasing M (more pronounced for high N) and increases with increasing N (less pronounced for high M).

Three-Level Triple-Interleaved (3L3) Converter

From the $\eta_{\mathrm{semi}} = 95\,\%$ contour in **Fig. 2.4 (c)** can be seen that almost all designs with $N > 2$ (exception $M = 9/N = 3$) are fulfilling the efficiency

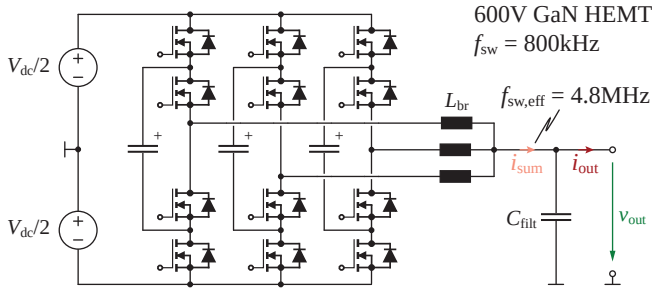


Fig. 2.5: Topology of the selected Three-Level Triple-Interleaved (3L3) Flying Capacitor Converter (FCC) realized with 70 mΩ 600 V GaN power switches switching at 800 kHz, resulting in an effective switching frequency $f_{sw,eff}$ of 4.8 MHz.

criterion. It should be noted, however, that additional losses in the converter, e.g., in the inductors, cause the system efficiency η to be smaller than η_{semi}. Therefore, a design with $\eta_{semi} > 95\,\%$ has to be chosen. After a comprehensive efficiency, volume and design complexity trade-off consideration, finally the solution with $M = N = 3$, i.e., a Three-Level Triple-Interleaved (3L3) converter topology is selected (highlighted in **Fig. 2.4**), which is expected to achieve 96 % semiconductor efficiency, allows for a very power dense system realization and has manageable design complexity. The topology is depicted in **Fig. 2.5**. With $n_{SC} = 6$ switching cells, each transistor has a device switching frequency of $f_{sw} = 800\,\text{kHz}$ to finally achieve $f_{sw,eff} = 4.8\,\text{MHz}$ at the summation node. The triple-interleaved design advantageously offers the flexibility to reconfigure the converter for a three-phase output (with 1/3 power rating in each phase compared to the total single-phase output power) by placing three individual filter capacitors with a capacitance of $C_{filt}/3$ after each branch inductor. Therefore, the converter can also be used, for example, as high BW three-phase motor drive system with sine filter. Please note that a three-level FCC has also been identified in [43] as best-suited for a tracking power supply of a linear RF PA.

2.3 Branch Inductor Design

2.3.1 Core Material and Geometry

A vital part of the system are the branch inductors $L_{br1...3}$ that give the effective filter inductance $L_{filt} = 1.26\,\mu\text{H}$ (cf. **Fig. 2.3**). With $N = 3$ branches, each

of the three inductors has an inductance of 3.8 µH and sees a triangular current ripple with a frequency $f_{\mathrm{iLpp}} = f_{\mathrm{sw,eff}}/N = 1.6\,\mathrm{MHz}$. Since both, the fundamental and the ripple components of the inductor current are relatively HF, a suitable core material with good HF properties, such as those offered by Manganese-Zinc (MnZn) and Nickel-Zinc (NiZn) ferrites, is required. It should further have a sufficient magnetic permeability μ_{r} at frequencies in the MHz range without generating excessive core losses. A comprehensive analysis of various available materials has shown that the 3F46 ferrite from Ferroxcube [75] designed for a maximum operating frequency of $1-3\,\mathrm{MHz}$ is the most suitable.

A pot core geometry that covers the whole winding minimizes the external magnetic stray field around the inductor (magnetic shielding) provided the air gap is only in the center pillar. This is a very important benefit, since it allows to encapsulate the inductor in a metallic housing to facilitate the heat dissipation without generating excessive ac losses due to the proximity effect, as it would be the case for other core shapes, e.g., E-cores, where the winding heads are not covered by the magnetic material. The required core cross-sectional area A_{Fe} is selected based on the maximum allowed peak magnetic flux density B_{pk} (single-sided amplitude), which necessarily needs to be below the saturation flux density $B_{\mathrm{sat,3F46}} \approx 430\,\mathrm{mT}$ at a temperature of 100°C, but typically is selected considerably smaller to limit core losses. An empirically determined value $B_{\mathrm{pk}} = 250\,\mathrm{mT} < B_{\mathrm{sat,3F46}}$ is used in this case. In a simplified assumption, B can be thought of as being composed of two components:

i) a *current-impressed* fundamental component B_0 and

ii) a *voltage-impressed* ripple component B_{HF}.

Their respective single-sided amplitudes $\hat{B}_0$ and $\hat{B}_{\mathrm{HF}}$ (peak values) are expressed as

$$\hat{B}_0 = L_{\mathrm{br}} \cdot \hat{i}_{\mathrm{L},0}/(N_{\mathrm{t}} \cdot A_{\mathrm{Fe}}) \tag{2.9}$$

$$\hat{B}_{\mathrm{HF}} = V_{\mathrm{dc}}/(8 \cdot (M-1) \cdot N_{\mathrm{t}} \cdot f_{\mathrm{iLpp}} \cdot A_{\mathrm{Fe}}) \tag{2.10}$$

with the peak fundamental branch inductor current $\hat{i}_{\mathrm{L},0}$ (equal distribution of the sum of the output current i_{out} and the filter capacitor current i_{C} between the N branches; $\hat{i}_{\mathrm{L},0} = 21\,\mathrm{A}$ in the nominal operating point for $N = 3$) and the number of turns N_{t}. The worst-case current ripple occurring for duty-cycles $D = 0.5\,/\,(M-1)$ (and odd multiples thereof) [45] is assumed in (2.10). The remaining two degrees of freedom are N_{t} and A_{Fe}, which must be chosen to limit

the peak value of the total flux density $B_{\mathrm{pk}} \in \left[\max\left\{\hat{B}_0,\ \hat{B}_{\mathrm{HF}}\right\},\ \hat{B}_0 + \hat{B}_{\mathrm{HF}}\right]$, i.e., the superposition of the fundamental and ripple component, accordingly. The worst-case $B_{\mathrm{pk}} = \hat{B}_0 + \hat{B}_{\mathrm{HF}}$ arises when the maximum current ripple occurs at the same time as the peak fundamental current. Due to the arbitrary load phase angle φ, no a priori statement regarding the location of the worst-case current ripple with respect to the peak fundamental current can be made, hence the worst-case $B_{\mathrm{pk}} = \hat{B}_0 + \hat{B}_{\mathrm{HF}}$ has to be considered.

Using the well-known area product $A_{\mathrm{Fe}}A_{\mathrm{w}}$ (winding window area A_{w}) [76], a P26/16 core with $A_{\mathrm{Fe}} = 87\,\mathrm{mm}^2$ is chosen from all cores of the selected material and shape (core dimensions indicated in **Fig. 2.6 (a.i)-(a.ii)**) [77]. With (2.9) and (2.10) together with the now known A_{Fe}, the minimum required number of turns is found as

$$N_{\mathrm{t,min}} = \left\lceil \frac{1}{B_{\mathrm{max}}A_{\mathrm{Fe}}} \left(L_{\mathrm{br}}\hat{i}_{\mathrm{L},0} + \frac{V_{\mathrm{dc}}}{8(M-1)f_{\mathrm{iLpp}}} \right) \right\rceil = 6. \tag{2.11}$$

This finally results in $\hat{B}_0 = 155\,\mathrm{mT}$ and $\hat{B}_{\mathrm{HF}} = 60\,\mathrm{mT}$ and therefore, a worst-case $B_{\mathrm{pk}} = 215\,\mathrm{mT}$.

2.3.2 Winding Arrangement

It was already shown in [46] that HF litz wire results in minimum losses for the given inductor current profile. In particular, the losses at fundamental frequency f_{out} are substantially lower compared to, e.g., solid round or flat wire. The above mentioned encapsulation of the inductor in the metallic housing has the disadvantage that it is more difficult to extract heat from the winding. While heat extraction is improved by potting the winding in the core with a thermally conductive compound (Bergquist TGF 3500LVO [78]), still a relatively conservative maximum LF RMS current density $S_{\mathrm{rms}} = 7\,\mathrm{A/mm}^2$ is selected to prevent substantial self-heating. With $I_{\mathrm{L,rms}} = 17\,\mathrm{A}$ (obtained from circuit simulation at the nominal operating point), a copper cross section $A_{\mathrm{Cu}} \approx 2.5\,\mathrm{mm}^2$ is required. A HF litz wire with $625 \times 71\,\mu\mathrm{m}$ strands is selected (twisted with $5 \times 5 \times 25$ bundles/strands).

2.3.3 AC Winding Losses

The air gap is calculated to obtain the required inductance ($\delta = 1.6\,\mathrm{mm}$ in this case) and as mentioned earlier, is realized only in the center pillar of the pot core to avoid external stray fields. Inside the winding window, however, there is a strong magnetic field near the gap. Consequently, this region

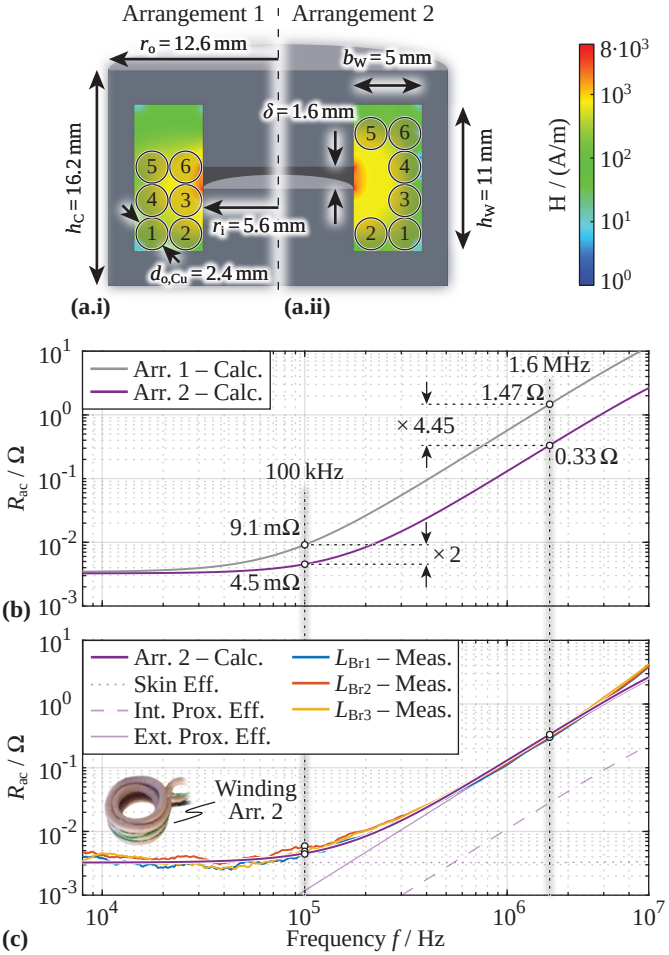


Fig. 2.6: (a.i) - (a.ii) Comparison of two winding arrangements and the resulting magnetic field H in the winding window assuming an impressed current of 1 A in each turn (obtained with Finite Element Method (FEM) simulations). The dimensions of the utilized pot core are further indicated. **(b)** Calculated ac winding resistance considering the skin effect and the internal and external proximity effect of both investigated winding arrangements. Thereby, the magnetic field determined with FEM simulations is used for the calculation. **(c)** Comparison of the measured inductor ac winding resistance (Arr. 2 — picture of the winding included) with the calculation.

Tab. 2.2: Calculated (italic) and measured (upright) ac resistance at $f = 100\,\text{kHz}$ and $f = 1.6\,\text{MHz}$ with resulting ac winding losses. In all cases, the losses are calculated with the simulated inductor current spectrum at the nominal operating point.

	R_{dc}	$R_{\text{ac,100k}}$	$R_{\text{ac,1.6M}}$	P_{100k}	P_{HF}	P_{tot}
	mΩ	mΩ	Ω	W	W	W
Arr. 1	*3.40*	*9.14*	*1.47*	2.10	29.21	31.31
Arr. 2	*3.20*	*4.53*	*0.33*	1.04	6.63	7.67
L_{br1}	3.15	4.41	0.28	1.02	6.59	7.61
L_{br2}	3.46	5.84	0.30	1.28	6.84	8.12
L_{br3}	3.25	4.83	0.33	1.18	7.59	8.77

must not be filled with turns. **Fig. 2.6** motivates this by comparing two winding arrangements in the P26/16 core that both lead to the desired L_{br}. In **Fig. 2.6 (a.i)**, the $N_{\text{t}} = 6$ turns are placed uniformly distributed starting from the bottom (Arrangement 1), whereas in **Fig. 2.6 (a.ii)** the area in the vicinity of the air gap is kept empty (Arrangement 2). In both cases, the magnetic field H in the winding window is obtained with Finite Element Method (FEM) simulations (also indicated in **Fig. 2.6 (a.i)-(a.ii)**). Thereby, a homogeneous current density in each turn is assumed (ideal HF litz wire). The ac resistance $R_{\text{ac}}(f)$ versus frequency with contributions from the skin effect and proximity effect (internal and external) is then analytically calculated as proposed in [79] using the mean H^2_{rms} in each of the turns. Of particular interest are the values $R_{\text{ac,100k}}$ at $f_{\text{out,max}} = 100\,\text{kHz}$ and $R_{\text{ac,1.6M}}$ at $f_{\text{iLpp}} = 1.6\,\text{MHz}$. As visualized in **Fig. 2.6 (b)**, compared to arrangement 1, arrangement 2 reduces $R_{\text{ac,100k}}$ by a factor of 2 and $R_{\text{ac,1.6M}}$ by almost a factor of 4.5 for the same dc resistance and is therefore clearly preferred.

Finally, **Fig. 2.6 (c)** compares the measured R_{ac} of the three constructed prototypes according to winding arrangement 2 with the analytically calculated value and reveals very close matching. The measurements are obtained with a precision impedance analyzer (Agilent Technologies 4294A [80]). Moreover, **Fig. 2.6 (c)** includes a picture of one inductor winding (Arrangement 2) where the empty space on the inner side is visible.

The resulting ac winding losses are estimated with the simulated inductor current spectrum for the nominal operating point and with $R_{\text{ac}}(f)$ (calculated and/or measured). **Table 2.2** summarizes the results for the calculated R_{ac} (italic) of arrangements 1 and 2 and the measured R_{ac} (upright) of the three inductors and the resulting ac winding losses. The total losses P_{tot} are split

into a fundamental component P_{100k} and a HF component P_{HF}. The latter contains everything except the fundamental component, i.e., all frequency components above 100 kHz. There are slight variations between the three inductors due to tolerances in the manufacturing, but in general the measured R_{ac} conforms very well with the model. It can be seen that the ac winding losses are mainly determined by the HF components of the current ripple. The calculated R_{ac} in **Fig. 2.6 (c)** is further decomposed into contributions from the skin-, internal and external proximity effect. The latter clearly dominates R_{ac} for frequencies above several hundred kilohertz and could be reduced by using a litz wire with a smaller strand diameter, e.g., 40 µm instead of 71 µm, and more strands to achieve a similar copper cross section area. This would lower P_{HF} (approximately by a factor of $3-4$ predicted with calculations, i.e., by around $16-18$ W for all three inductors combined), however, the filling factor is also reduced and the placement of the winding according to arrangement 2 is potentially not possible anymore. In addition, the combined ac winding losses of all three branch inductors are below 25 W, which is a very insignificant part of the total converter losses, as will be shown later.

2.3.4 Core Losses and Properties of the Realized Inductors

The realized inductor prototypes are potted in metallic cooling enclosures with the same compound used to pot the winding in the core. The final prototypes have a Self-Resonance Frequency (SRF) of approximately 23 MHz, which is significantly above f_{iLpp}. The saturation current is determined with measurements and exceeds 60 A. The worst-case core losses in the final inductors are roughly estimated with electrical loss measurements with sinusoidal excitation in a series-resonant configuration as proposed in [81]. Due to the highly non-uniform flux distribution in pot cores, the P26/16 core is also used for the loss measurements in order to have conditions as similar as possible to those in the final operation. Pure ac excitation with 100 kHz and $\hat{B}_0 = 155$ mT results in losses of ≈ 1.1 W. Similarly, a HF excitation with a sinusoidal flux density profile with $f_{iLpp} = 1.6$ MHz and $\hat{B}_{HF,\sim} = 49$ mT (amplitude of the first harmonic in the triangular flux density profile with $\hat{B}_{HF} = 60$ mT, cf. (2.10)) on top of a dc bias $B_{dc} = \{0, 77, 100, 125, 155\}$ mT results in losses of $\{1.53, 2.45, 3.01, 4.17, 4.34\}$ W. Therefore, the worst-case weighted core losses over one fundamental period are ≈ 4.2 W (sum of the 100 kHz loss component and the weighted HF ripple components for different dc bias flux densities occurring over one fundamental period). Here, always the maximum HF flux

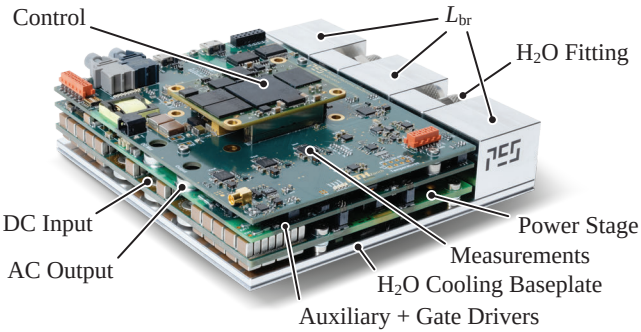


Fig. 2.7: Picture of the realized hardware demonstrator of the single-phase 10 kVA PA with the most important building blocks labeled. The overall dimensions of 123 mm × 123 mm × 26.5 mm give a power density of 25 kW/dm^3 (410 W/in^3).

density ripple is assumed. In practice, depending on the duty-cycle, the HF flux density ripple and therefore the associated core losses are smaller, so core losses of ≈ 4.2 W per inductor are a worst-case approximation. Due to the large surface and very good thermal connection of the core to the cooling housing, the core losses can anyway be dissipated very well. Furthermore, similar to the ac winding losses, compared to the semiconductor losses, the core losses do not significantly influence the system efficiency.

2.4 Hardware Demonstrator

This section describes the development of a 3L3 converter hardware prototype, which is used to demonstrate the full functionality of the system, i.e., operation with high $f_{\text{sw,eff}}$ and the high output voltage quality, and to verify the predicted system efficiency. **Fig. 2.7** shows a picture of the realized prototype and highlights the very compact realization (overall dimensions of 123 mm × 123 mm × 26.5 mm, Field-Programmable Gate Array (FPGA) board not included, since this could be soldered directly on the top PCB) with a boxed volume of only 400 cm^3 (24.4 in^3), which results in a power density of 25 kW/dm^3 (410 W/in^3). The most relevant system building blocks and the dc input/ac output interfaces are labeled. The converter consists of three PCBs, starting with the power section (power transistors, GDs, dc link and FCs) at the bottom, the GD supply, the HV auxiliary supply and part of the measurement circuits in the middle and at the top the Analog-to-Digital Con-

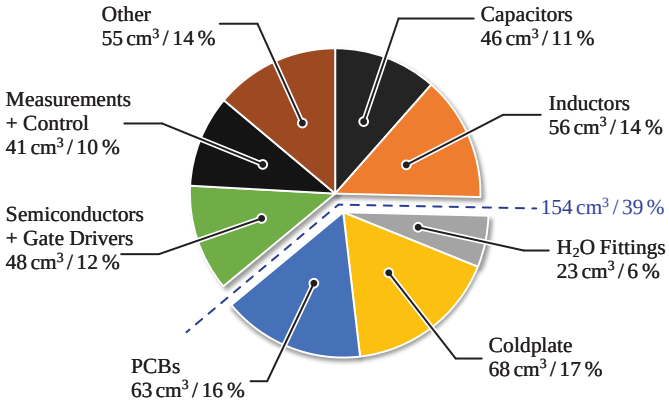


Fig. 2.8: Volume breakdown of the hardware demonstrator indicating the absolute and relative contribution of the individual building blocks/components.

verters (ADCs) and the FPGA to control the system. Furthermore, the top PCB features several communication interfaces to connect the converter with a host computer. The whole system is mounted on a custom manufactured coldplate as part of a liquid cooling system (cf. **Section 2.4.2**). The cubes in the background contain the three branch inductors L_{br} (cf. **Section 2.3**) and the connection (fittings) for the liquid cooling system.

The volume breakdown of the 3L3 converter shown in **Fig. 2.8** indicates a very uniform distribution between the different components. Remarkable is that the PCBs, the fittings for the liquid cooling system and the coldplate already account for almost 40 % of the total volume. The capacitor share is composed of the dc link capacitors ($\approx$ 14 µF effective capacitance between DC+ and DC- at $V_{\mathrm{dc}} = 800$ V, split as 2×28 µF at 400 V at the split dc link), the FCs ($\approx$ 6 µF effective capacitance at $V_{\mathrm{FC}} = 400$ V) and the output filter capacitor (realized with 3×33 nF C0G).

2.4.1 Power Stage Layout Considerations

To minimize the $V - I$ overlap losses, the switching transitions must be as fast as possible (high $\mathrm{d}v/\mathrm{d}t$, cf. (2.7)), demanding careful layout of the GDs and the power commutation loop. **Fig. 2.9 (a)** shows the bottom view of the power stage PCB with the top-side cooled switches. The layout of the three branches is fully modular and could easily be extended for any M and/or N. **Fig. 2.9 (b)** exemplary highlights the coplanar commutation loop layout for

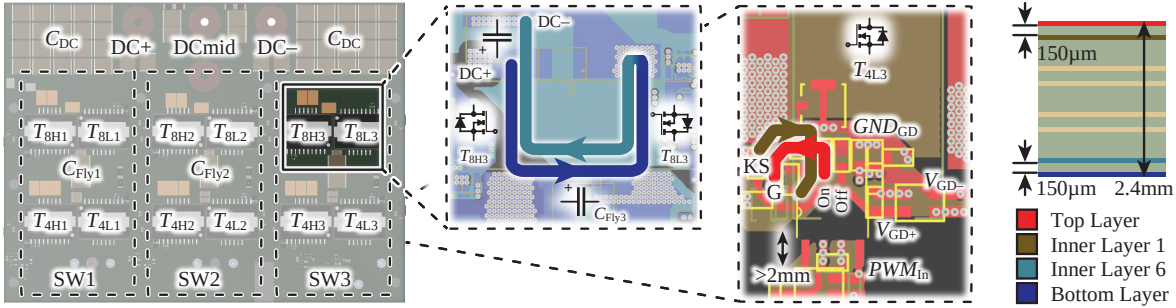


Fig. 2.9: (a) Power stage of the 3L3 converter with highlighted individual branches and corresponding components. **(b)** Detailed view of the coplanar power commutation loop (drain to source) in the outer FC cell of branch 3. **(c)** Detailed view of the coplanar Gate (G) to Kelvin Source (KS; equal to GND_{GD} potential) commutation loop of one switch (T_{4L3}) (turn-on path highlighted; equivalent for the turn-off path). **(d)** Layer stack of the 2.4 mm thick power PCB. Each copper layer has a thickness of 70 µm (2 oz.).

the outer SC of the third branch (T_{8H3} and T_{8L3}). The layout is identical for all six SCs. The copper plane on the inner layer 6 (distance of 150 µm to the bottom layer where the switches are mounted, cf. **Fig. 2.9 (d)**) is on "DC-" potential and provides a coplanar return path for the commutation current (indicated with the blue and cyan arrow for current flow on the bottom and the inner layer 6, respectively). Measurements reveal a contribution of the PCB layout to the power loop inductance of < 2.2 nH for the outer switching cells and of < 1.5 nH for the inner switching cells (copper plates that cover the entire semiconductor footprint are used instead of the transistors to account solely the PCB contribution). In the latter case, the inductance is lower because the source of T_{4Hi} and the drain of T_{4Li} are directly connected at the respective switch-nodes "SWi" ($i \in \{1, 2, 3\}$). Related to the device internal inductance of 3.5 nH between drain and source, the layout does not significantly contribute to the overall power loop inductance.

Fig. 2.9 (c) shows the GD layout of T_{4L3} (identical layout for all 12 switches). In contrast to Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) with an isolated gate, the utilized GaN GITs have a diode between gate and source, which after turn-on requires a small steady-state gate current $I_{g,ss}$ to flow [73]. Therefore, a GD circuit featuring an ac-coupled high current turn-on path and in parallel a dc-coupled path for the small $I_{g,ss}$ based on the one proposed in [82] is utilized. In this case, the GD has a bipolar supply to ensure a constant negative bias $V_{GD-} = -5$ V in the off-state to prevent parasitic turn-on. Similar to the power loop, the gate loop is realized coplanar to minimize the loop inductance (return path on inner layer 1). Measurements reveal a turn-on and turn-off gate loop inductance of $L_{g,on} \approx 3$ nH and $L_{g,off} \approx 4$ nH. Since the GD Integrated Circuit (IC) sink pin (for the turn-off) is located further away from the GaN transistor, it makes sense that $L_{g,off} > L_{g,on}$. Compared to the measured device internal gate to source loop inductance of $L_{G,int} \approx 7$ nH, the external contribution is minor. Strict care was taken to prevent overlapping copper of jumping potentials (e.g., the source nodes) and logic nets (e.g., PWM, enable or measurement signals coming from/going to the FPGA), which would introduce significant CM currents over the parasitic capacitance due to the high $\mathrm{d}v/\mathrm{d}t$ and potentially lead to distortions and/or malfunction of the digital circuit.

2.4.2 Cooling System

An anticipated semiconductor efficiency of $\eta_{semi} = 96\,\%$ at a power level of $P_{out} = 10$ kW (nominal ohmic load) results in power losses of roughly

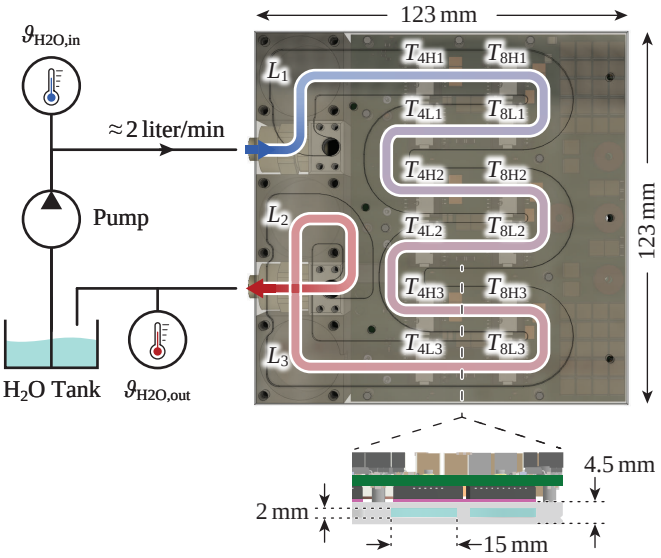


Fig. 2.10: Simplified setup of the liquid cooling solution for the 3L3 converter with indicated dimensions of the overall system (123 mm × 123 mm), the thickness of the coldplate (4.5 mm) and the dimensions of the liquid cooling channel (15 mm × 2 mm). From the measured coolant inlet and outlet temperature and the volume flow of approximately 2 l/min, the total losses can be estimated.

$P_{\text{loss,device}} = 35\,\text{W}$ in each switching transistor of the 3L3 design (total semiconductor losses ≈ 420 W). The resultant semiconductor power loss density of ≈ 42 W/cm^2 demands for liquid cooling to efficiently dissipate the heat without excessive temperature rise [83]. Along with reliability concerns, a too high junction temperature ϑ_j of the GaN transistor substantially increases the conduction losses because of the very pronounced temperature dependence of the on-state resistance $R_{\text{ds,on}}$ [69]. A custom-milled aluminum liquid cooling coldplate to cool the 12 power transistors and the three branch inductors is designed. **Fig. 2.10** shows a semi-transparent bottom view of the coldplate and the power PCB. The path for the coolant (H_2O in this case) from the inlet (cold side, blue) to the output (hot side, red) through the single meandering channel as well as the positions of the components to be cooled are highlighted. A detailed side view of the assembly is shown at the bottom of **Fig. 2.10**. The rectangular water channel is 15 mm wide to match the width of the power transistor's heat pad. Due to the coldplate's low profile of only

3 mm (2 mm channel height), the 1.5 mm thick cover plate is glued to the coldplate to ensure a fully sealed assembly. An electrically insulating thermal gap pad (T-Global TG6050, indicated with pink color) attaches the transistors to the coldplate.

With the resulting volume flow of roughly $\dot{V} = 2\,\mathrm{l/min}$ and the measured water inlet and outlet temperatures $\vartheta_{\mathrm{H2O,in}}$ and $\vartheta_{\mathrm{H2O,out}}$, the losses can be estimated from the basic heat transfer equation with

$$P_{\mathrm{loss,tot}} \approx \dot{Q} = \rho_{\mathrm{H2O}} \cdot \dot{V} \cdot c_{\mathrm{H2O}} \cdot (\vartheta_{\mathrm{H2O,out}} - \vartheta_{\mathrm{H2O,in}}) \tag{2.12}$$

where $c_{\mathrm{H2O}} = 4181\,\mathrm{J/(kg{\cdot}K)}$ is the specific heat capacity and $\rho_{\mathrm{H2O}} = 997\,\mathrm{kg/m^3}$ the mass density of water at a temperature of 25°C, respectively. Note that (2.12) neglects heat dissipation from the surface of the coldplate, e.g., through natural convection or radiation. Therefore, the actual total losses are slightly higher than the estimated ones. With (2.12), the calculated total losses of ≈ 420 W would only lead to a temperature difference of 3 K, which is difficult to measure accurately. Nevertheless, the simple estimation is a good sanity check for the precision electrical loss measurements presented later (cf. **Section 2.5.1**). Note that the coolant (H_2O) heats up while flowing from the inlet towards the outlet such that, e.g., underneath T_{8L3} and T_{4L3} the temperature is already higher than the inlet temperature $\vartheta_{\mathrm{H2O,in}}$. This could in principle lead to unequal semiconductor temperatures and therefore, to unbalanced losses (e.g., due to the strongly temperature-dependent on-state resistance in GaN devices). However, thanks to the relatively high volume flow and short channel length, with the given cooling solution the overall temperature difference between inlet and outlet is only roughly 3 K (at maximum losses of ≈ 420 W) and therefore, there is no significant uneven temperature distribution that could have an influence on the loss sharing and the symmetric current handling, as verified in **Fig. 2.15**. There are alternative cooling channel geometries, which do ensure a more symmetrical temperature distribution, i.e., multiple parallel channels, which is of particular importance for large heat sinks. There, it must be ensured that the volume flow is equal in all parallel channels as otherwise the temperature distribution can be significantly non-uniform [83]. The geometry in **Fig. 2.10** is mainly selected because it inherently ensures equal volume flow throughout the channel, allows for a straight-forward channel design and still gives a small overall temperature difference thanks to the relatively small dimensions and the high volume flow.

Tab. 2.3: Available measurements on the 3L3 converter with their sampling rate f_s, resolution B and Bandwidth (BW).

Signal	f_s	B	BW
Output Voltage v_{out}	125 MSPS	14 Bit	$\approx$ 30 MHz
Load Voltage v_{load}	125 MSPS	14 Bit	$\approx$ 30 MHz
Output Current i_{out}	125 MSPS	14 Bit	$>$ 30 MHz
Summed Ind. Current i_{sum}	125 MSPS	14 Bit	$>$ 30 MHz
Branch Currents $i_{Lbr1...3}$	3.125 MSPS	14 Bit	$\approx$ 1 MHz
FC Voltages $v_{FC1...3}$	3.125 MSPS	14 Bit	$\approx$ 100 kHz
DC Link Voltages v_{dcp}, v_{dcn}	3.125 MSPS	14 Bit	$\approx$ 800 kHz

2.4.3 Measurement Circuits and Control

An FPGA is responsible for the PWM pattern generation, the processing of measurement signals, the supervision of voltages and currents and for the communication with a host computer. In this chapter, the 3L3 is operated without closed-loop control but in a next step, suitable control schemes such as the ones proposed in [17] are implemented. This has to be done directly in hardware on the FPGA for maximum controller update rate, i.e., to minimize execution time. As shown in [17], a crucial part to achieve a high control BW is to minimize the overall loop delay, which includes the measurements (latency of the ADC), the execution time inside the FPGA (pipeline latency) and the signal isolator and GD delays. An ADC with a sampling rate of 125 MHz and a latency of 5 clock cycles (Analog Devices LTC2255 [84]) is used to sample the summed inductor current i_{sum}, the output voltage v_{out} and the output current i_{out}. The transistors are driven with an isolated GD IC featuring a low propagation delay and a very tightly specified jitter (Silicon Labs/Skyworks Si8271 [85]). Apart from a small loop delay, very high BW voltage and current measurements are required. The latter have been extensively analyzed in [86, 87] and finally, an off-the-shelf Hall-effect current sensor has been extended with a Current Transformer (CT) to achieve a BW $>$ 30 MHz and is integrated into the 3L3. **Table 2.3** summarizes all available measurements with their sampling rate and resolution that can be performed with the converter. Note that the v_{load} measurement can be used for ac load sensing to compensate, e.g., the voltage drop across the inductor connecting the output of the 3L3 with the load or to impress a certain output impedance as shown in [23].

All measurements from **Table 2.3** are additionally used for overvoltage and overcurrent protection with ultra-fast response, i.e., within few tens of nanoseconds.

2.5 Performance Verification

This section presents experimental measurement results to verify the performance of the 3L3 hardware prototype. As mentioned above, the converter is operated in open-loop configuration.

2.5.1 Efficiency and Losses

The system efficiency η is electrically measured for sinusoidal output voltages with a constant RMS value $V_{\text{out}} = 230\,\text{V}$ at different output power levels $P_{\text{out}} \in \{3.3\,\text{kW}, 5\,\text{kW}, 7.3\,\text{kW}, 8\,\text{kW}, 9\,\text{kW}, 10\,\text{kW}\}$ (purely ohmic load) and for different output frequencies $f_{\text{out}} \in \{10\,\text{kHz}, 20\,\text{kHz}, 50\,\text{kHz}, 100\,\text{kHz}\}$.

In all cases, the system is supplied with a split dc link composed of two 400 V dc voltage sources and a fixed dead time $t_{\text{d}} = 24\,\text{ns}$ is set. The load resistor R_{L} is realized with multiple parallel-connected low-inductance planar resistors (Ohmite TAP800 [88]). To minimize the parasitic inductance L_{L} from the connection between converter output and load, depending on P_{out}, multiple separate load resistor assemblies are connected directly to the converter output. At maximum f_{out} and P_{out}, the influence of L_{L} is the strongest, since at this operating point simultaneously the inductive voltage drop becomes maximum and the load resistance minimum. This worst-case corresponds to the nominal operating point, where $L_{\text{L}} \approx 1.4\,\mu\text{H}$, and results in a phase-shift of roughly $10\,^{\circ}$ between v_{out} and i_{out} ($\cos(\varphi) = 0.985$). **Appendix A** derives the maximum possible output power for different load phase angles φ. An output power derating of maximum 27.5 % is required for purely capacitive loads.

The efficiency measurements are performed with a precision power analyzer (Yokogawa WT3000 [89]) and are depicted in **Fig. 2.11 (a)**. The measured efficiency (dots) is compared with calculations (continuous lines) resulting from the loss model introduced in **Section 2.2.3**, additionally including the branch inductor ac winding losses according to **Section 2.3.3**. The target efficiency of 95 % is achieved over a very wide range of P_{out} and f_{out}. In the nominal operating point (marked with ★) the efficiency is 95.8 %. The partial load efficiency is worse for higher f_{out} because of the capacitive current i_{c} in C_{filt}, which depends solely on f_{out} and v_{out} and not on P_{out} (for a fixed output

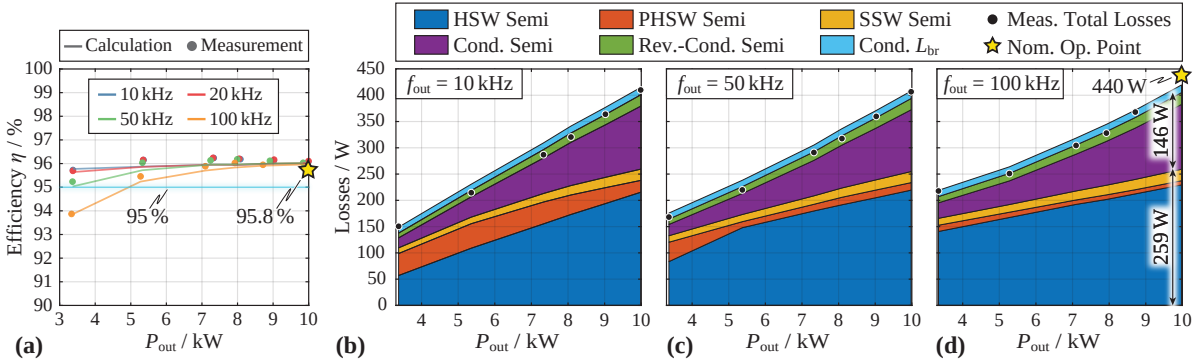


Fig. 2.11: (a) Measured (dots) and calculated (lines) system efficiency for different output frequencies (10 kHz - blue, 20 kHz - red, 50 kHz - green and 100 kHz - orange) vs. output power P_{out} with an ohmic load, an output RMS voltage of $V_{\text{out}} = 230\,\text{V}$ and a fixed dead time (interlocking delay) of $t_{\text{d}} = 24\,\text{ns}$. **(b) - (d)** Calculated loss breakdown indicating Hard Switching (HSW, blue), Partial-Hard Switching (PHSW, orange), Soft Switching (SSW, yellow) losses, semiconductor conduction losses (purple), semiconductor reverse conduction losses (green) and inductor conduction losses (cyan) for an output frequency of **(b)** 10 kHz, **(c)** 50 kHz and **(d)** 100 kHz. Further included are the measured total losses (black dots) in comparison with the loss model. The nominal operating point (10 kW ohmic/100 kHz) is marked with ★.

voltage). This current generates switching and conduction losses in the power stage. Furthermore, **Fig. 2.11** shows detailed calculated loss breakdowns for **(b)** $f_{\mathrm{out}} = 10\,\mathrm{kHz}$, **(c)** $f_{\mathrm{out}} = 50\,\mathrm{kHz}$ and **(d)** $f_{\mathrm{out}} = 100\,\mathrm{kHz}$. In general, the measurements conform very well with the calculations and the absolute difference between the measured and calculated losses is $< 25\,\mathrm{W}$. Because measurements give a better efficiency at low P_{out} than the calculations but a lower efficiency at high P_{out}, it can be concluded that the model underestimates ohmic losses and slightly overestimates constant losses (independent of P_{out}) and/or losses scaling linear with P_{out}. More specifically, since the effect is more pronounced for high f_{out}, the real system has more ac resistance in the power path than modeled. Potential sources for the ac resistance are, e.g., the primary conductor of the CTs (two in total), PCB tracks carrying the load current (in particular the return connection from the summing node to the filter capacitor located next to the dc link) and contact resistance of soldering joints. With an rms output current of 43.5 A (10 kW at an rms output voltage of 230 V), a resistance of $1\,\mathrm{m\Omega}$ in the current path contributes 1.9 W of additional losses. **Fig. 2.11 (d)** nicely shows the loss "offset" for $f_{\mathrm{out}} = 100\,\mathrm{kHz}$ compared to $f_{\mathrm{out}} = 10\,\mathrm{kHz}$, even at low P_{out}, due to the higher switching losses given by the aforementioned capacitive current in C_{filt}. The semiconductor loss distribution in the nominal operating point (marked with ★) is practically identical to the one in **Fig. 2.4** for the $M = N = 3$ design.

Furthermore, **Fig. 2.11 (b)** and **(c)** reveal that for $f_{\mathrm{out}} = 10\,\mathrm{kHz}$ and 50 kHz a better partial load efficiency (lower losses) could be achieved by implementing an adaptive dead time, which enables full ZVS also for lower switched currents. Since this would require an increase of t_{d} from its minimum value of 24 ns and in turn would lead to a distortion of the output voltage, further measures would need to be implemented to compensate this effect (cf. **Section 2.5.2**).

Fig. 2.12 depicts the efficiency and a breakdown of the calculated losses (obtained with the extended loss model also used in **Fig. 2.11**) for operation with $f_{\mathrm{out}} = 100\,\mathrm{kHz}$ and full-scale output current, i.e., an RMS output current $I_{\mathrm{out}} = P_{\mathrm{out,max}}/V_{\mathrm{out,nom}} = 43.5\,\mathrm{A}$ into a purely ohmic load, for different RMS output voltages V_{out} between 40 V and 230 V (nominal operating point). This corresponds to the worst-case operating mode, since the output power decreases linearly with output voltage and the output current is always maximum. The efficiency drops from 96 % in the nominal operating point ($V_{\mathrm{out}} = 230\,\mathrm{V}$ and $P_{\mathrm{out}} = 10\,\mathrm{kW}$) to 80 % for $V_{\mathrm{out}} = 40\,\mathrm{V}$ and $P_{\mathrm{out}} = 1.74\,\mathrm{kW}$. This is expected, since the total losses do not reduce with lower output voltage (they are more or less constant and show a slight bathtub shape),

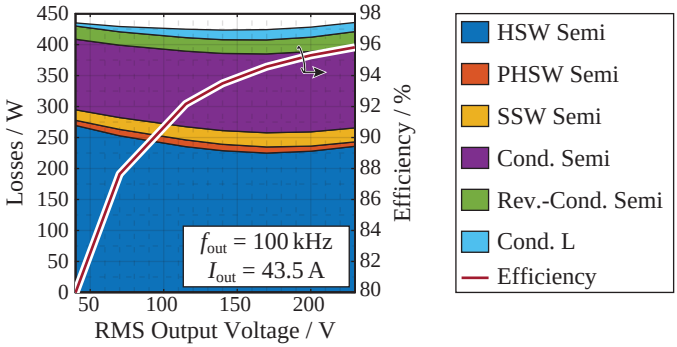


Fig. 2.12: Calculated efficiency and loss breakdown for operation with $f_{out} = 100\,\text{kHz}$ at maximum RMS output current $I_{out} = P_{out,max}/V_{out,nom} = 43.5\,\text{A}$ and varying RMS output voltage V_{out} into a purely ohmic load.

whereas the output power does (linear decrease with decreasing V_{out}). The bathtub shape of the losses can be explained with the current ripple, which depends on the modulation depth (and therefore on V_{out}). Reducing the output voltage from the nominal value of 230 V initially increases the current ripple (duty-cycle more often close to 0.25 and 0.75, which gives maximum current ripple in a three-level FCC [42]) and therefore, leads to reduced HSW losses (lower current switched hard) and more PHSW and SSW transitions. With further output voltage reduction (below approximately 170 V rms), the ripple is reduced because the duty-cycle is always close to 0.5, which in a three-level FCC gives minimum current ripple [42]. Opposite to the case of large ripple, this leads to more HSW losses (higher current switched hard) and less PHSW and SSW transitions. The conduction losses, however, slightly decrease thanks to the lower ripple but this decrease has negligible impact on the total losses. The reduced current ripple also explains the lower inductor conduction losses for low output voltages, which according to **Table 2.2** are predominated by the HF losses (current ripple) at f_{iLpp} due to the substantially higher ac resistance at f_{iLpp} compared to f_{out} (approximately a factor of 50). Despite the efficiency degradation with reduced output voltage in this worst-case operation mode it is still substantially higher compared to linear PAs (best-case efficiency of 78.5 % for a full-scale output into a purely ohmic load [27]).

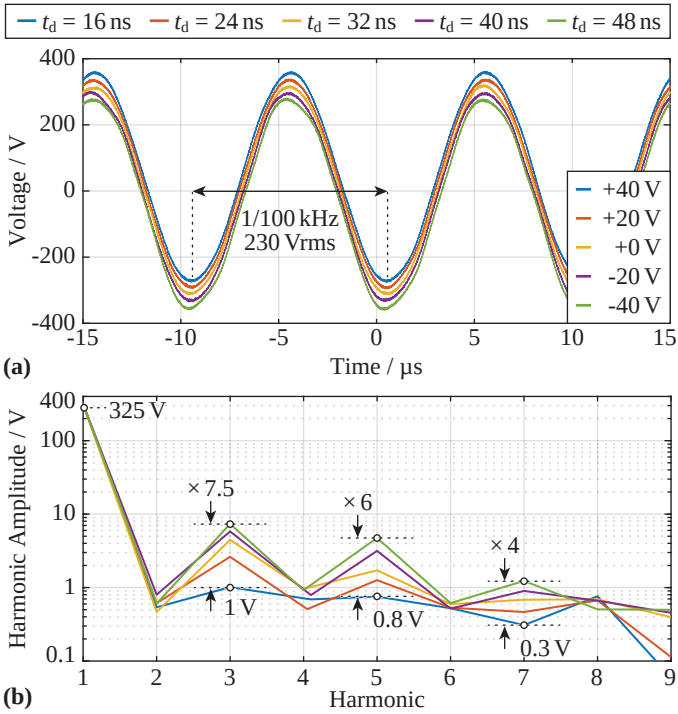


Fig. 2.13: Influence of the dead time t_d on the output voltage quality with a quasi-analog PWM modulator (125 MHz update rate). **(a)** Measured output voltage (f_{out} = 100 kHz, V_{out} = 230 V rms, P_{out} = 3.3 kW, ohmic load). The measurements are offset by multiples of 20 V to visualize the differences in the waveforms. **(b)** Corresponding output voltage amplitude spectra with the 9 lowest harmonics of f_{out}.

2.5.2 Output Voltage Quality

Phase-Shifted PWM (PSPWM), where one reference signal v_{ref} is compared with n_{SC} phase-shifted carrier signals, each with a frequency f_{sw} (device switching frequency) is one possible modulation strategy for series- and/or parallel-interleaved converters [90]. This strategy is used in the presented 3L3 converter. Digital implementation of the PWM offers maximum flexibility, but has the disadvantage of finite horizontal (time) and vertical (amplitude) resolution. It was shown in [17] that a regularly sampled PWM (also called synchronous PWM), where the compare values/duty-cycles are updated at

the top and bottom of a triangular carrier signal introduces a time delay T_d of $3/(2f_{sw,eff}) = 312.5\,ns$ (with $f_{sw,eff} = 4.8\,MHz$), which can substantially limit the maximum achievable controller BW. Therefore, a quasi-continuous operation of the PWM unit is favorable, i.e., the duty-cycles are updated in every FPGA clock period, resulting in an update rate of $f_{PWM} = f_{clk} = 125\,MHz$, where 125 MHz is the maximum achievable FPGA clock frequency. This implementation is comparable to a naturally sampling PWM [47] and is used in the 3L3 to virtually eliminate the PWM delay [91]. The vertical resolution is limited by the ratio of FPGA clock frequency to the symmetric (triangular) carrier signal frequency f_{sw}. The number of possible duty-cycles equals $\lfloor f_{clk}/(2 \cdot f_{sw}) \rfloor = 78$. The 3L3 can set the local average of the switch-node voltage $\langle v_{sw} \rangle$ (mean over one switching period) with a resolution of $\Delta\langle v_{sw} \rangle = V_{dc}/78 = 10.25\,V$ in each branch. Effectively, this corresponds to a voltage resolution $\Delta\langle v_{sw,eff} \rangle = \Delta v_{sw}/N = 3.42\,V$ (local average of the effective switch-node voltage $v_{sw,eff}$) thanks to the parallel-interleaved topology. A further reduction of $\Delta\langle v_{sw,eff} \rangle$ would be possible with a High-Resolution PWM (HRPWM), which is currently being investigated as part of ongoing research on this topic.

Fig. 2.13 (a) shows measured output voltages at $f_{out} = 100\,kHz$, $V_{out} = 230\,V$ rms and $P_{out} = 3.3\,kW$ (ohmic load) for different dead times t_d (interlocking delays). Note that the different waveforms are offset by multiples of 20 V to better visualize the distortions. The resulting output voltage spectra are depicted in **Fig. 2.13 (b)** and indicate the presence of odd harmonics of the output voltage. With a higher t_d, the amplitudes of the odd harmonics are increasing, which is also visible in **Fig. 2.13 (a)** as distorted waveform around the minima and maxima of the sine. Compared to $t_d = 48\,ns$, for $t_d = 16\,ns$, the 3rd and 5th harmonic are substantially reduced from 7.5 V to 1 V and from 4.8 V to 0.8 V, respectively. During the dead time, depending on the direction of the switched current, either a resonant ZVS transition starts, which directly after the turn-off signal from the FPGA (neglecting the delay of the GD) changes the switch-node voltage (SSW), or the switch to be turned off goes into reverse conduction and only after the signal to turn on the complementary switch, i.e., after t_d, the switch-node voltage changes (HSW). This is a fundamental cause of non-linearities, in particular the source of odd harmonics [92], because depending on the direction and magnitude of the switched current, a voltage-time area is applied to the inductor, which is different from the one calculated in the controller [93]. Nevertheless, **Fig. 2.13** indicates a very high output voltage quality for low t_d. A further improvement, however, could be desired, e.g., to reduce the error voltage applied to

the output voltage controller. A common strategy to mitigate the dead time nonlinearities is to delay the switching pulses in the FPGA depending on the current direction and magnitude to effectively apply the correct voltage-time area to the inductor. This acts as feed-forward term to correct the dead time induced non-linearities. Alternatively, the actual pulses at the switch-node can be measured and compared with the ideal PWM pulses (without the dead time), which does not need output current sign and/or magnitude measurements. Noise-shaping is then applied to shift the dead time induced non-linearities to higher frequencies [94]. While the accurate measurement of the fast pulses at the switch-node can be difficult because of HF noise coming from the extremely fast $\mathrm{d}v/\mathrm{d}t$ and/or switching of GaN transistors, the noise-shaping approach further requires that f_{sw} (and not $f_{\mathrm{sw,eff}}$ because the dead time is present for every SC, i.e., occurs in every switching period $1/f_{\mathrm{sw}}$) is significantly greater than f_{out} (typically, $f_{\mathrm{sw}}/f_{\mathrm{out}} > 10$ [94]), which is not given for the realization at hand. In the current implementation, no dead time correction is used and therefore, a minimum t_{d} should be selected in the interest of maximum output voltage quality. Because efficiency measurements showed that $t_{\mathrm{d}} = 24\,\mathrm{ns}$ has the lowest losses, this value is finally selected. The amplitudes of the 3$^{\mathrm{rd}}$ and 5$^{\mathrm{th}}$ harmonic are 2.5 V and 1.2 V, respectively in this case, which is still lower than the effective switch-node voltage resolution $\Delta\langle v_{\mathrm{sw,eff}}\rangle = V_{\mathrm{dc}}/(N \cdot \lfloor f_{\mathrm{clk}}/(2 \cdot f_{\mathrm{sw}})\rfloor) = 3.42\,\mathrm{V}$ (cf. derivation above).

2.5.3 Exemplary Waveforms at Nominal Operating Point

Fig. 2.14 shows the measured output voltage v_{out} (green; 100 V/div) and output current i_{out} (red; 15 A/div) in the nominal operating point ($f_{\mathrm{out}} = 100\,\mathrm{kHz}$, $P_{\mathrm{out}} = 10\,\mathrm{kW}$ (ohmic load), $V_{\mathrm{out}} = 230\,\mathrm{V}$ rms). The output represents a clean sine wave without harmonic distortion. In **Fig. 2.15**, the measured individual branch inductor currents i_{L1} (blue; 6 A/div), i_{L2} (red; 6 A/div) and i_{L3} (green; 6 A/div) and the calculated summed current i_{sum} (orange; 18 A/div) are depicted for the same operating point. It can be seen that the three currents are symmetrically distributed and correctly phase-shifted by 120 ° between the branches. The ripple on the resulting summed current i_{sum} is therefore significantly reduced (note the different vertical scale in **Fig. 2.15**). As no active (closed-loop) current balancing is employed, the current sharing is established purely by the application of the same reference signal to the PWM modulator in each branch (nominally identical voltage-time areas applied to each L_{br}) and by the parasitic resistances ($R_{\mathrm{ds,on}}$ of the transistors and the winding resistance of L_{br}). The FC voltages are naturally balanced with an

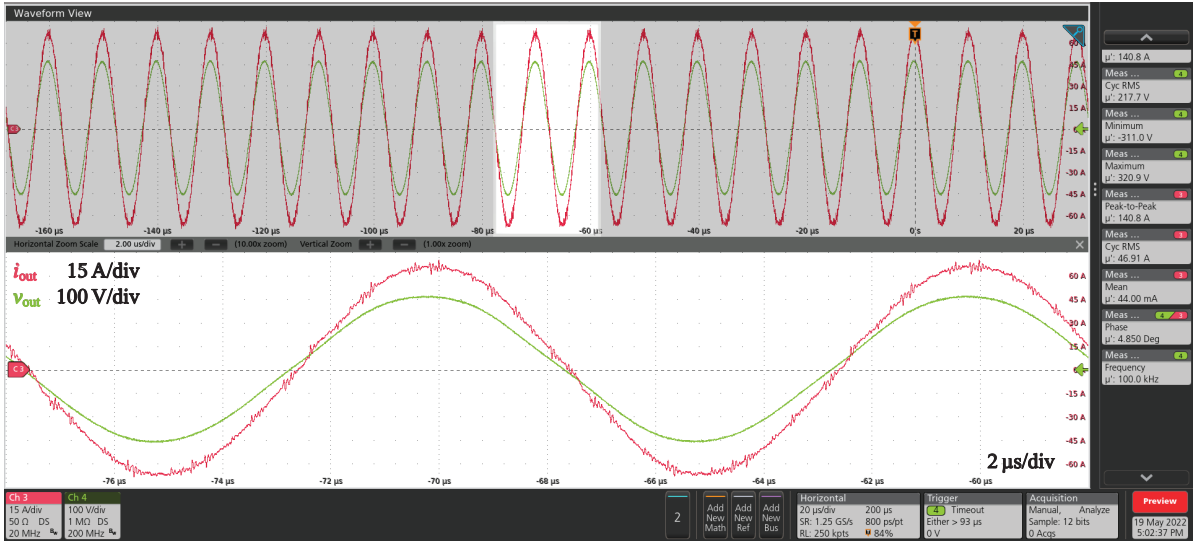


Fig. 2.14: Measured waveforms of the output voltage (green; 100 V/div) and output current (red; 15 A/div) for a 100 kHz large-signal (230 V rms) sinusoidal reference and an output power P_{out} of 10 kW (ohmic load). Time scale of the zoomed view is 2 µs/div.

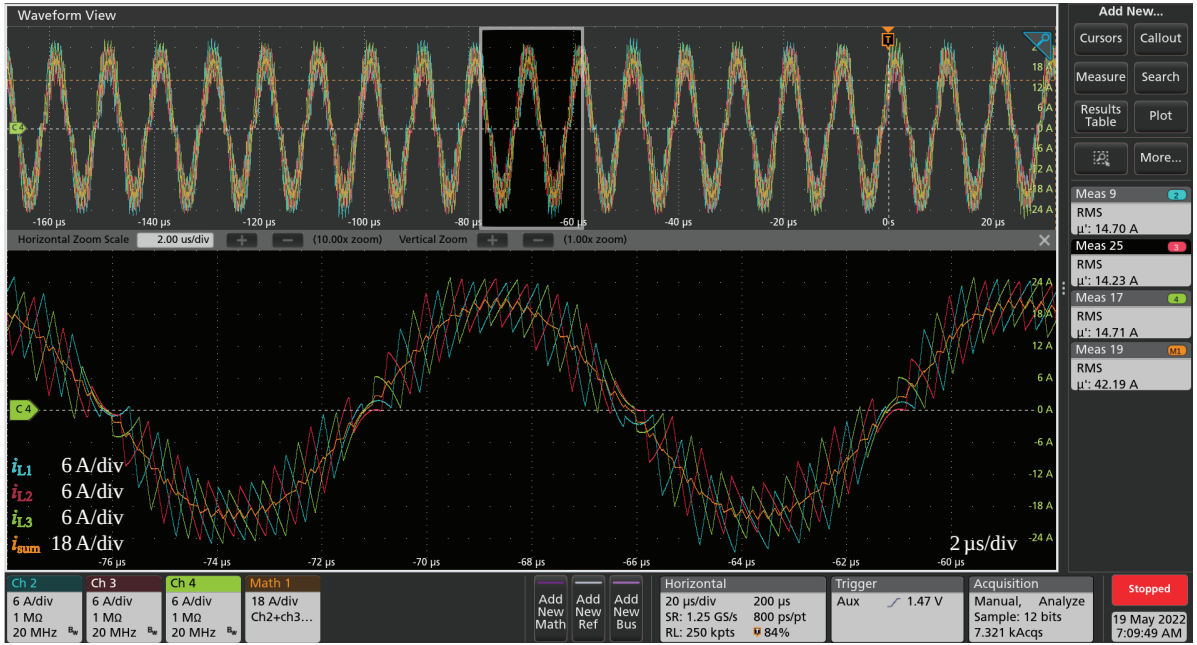


Fig. 2.15: Measured branch inductor currents i_{L1} (blue), i_{L2} (red) and i_{L3} (green) on a scale of 6 A/div indicating balanced current sharing between the three branches. Additionally, i_{sum} (orange; 18 A/div) indicates the reduced current ripple thanks to the parallel interleaving.

error $< \pm 2\,\%$ of the nominal voltage thanks to the inherent losses in the power stage. Active balancing would be possible with the currently implemented modulation to further improve the steady-state FC balancing but is not used at this stage.

Due to the compact realization and the mounting of the top-side cooled switches on the coldplate, the temperature distribution of the switches could not be measured during operation, e.g., with a thermal camera. The switch case temperatures as well as the branch inductor winding temperatures are measured with Negative Temperature Coefficient (NTC) temperature sensors. For a H_2O inlet temperature of $\vartheta_{H2O,in} = 30\,°C$ the semiconductor case temperatures are all below 60 °C. With a datasheet specified thermal resistance from junction to case of $R_{th,j-c} = 1\,K/W$ and with approximately 35 W losses per switch this leads to a junction temperature $\vartheta_j \approx 95\,°C$, which is well below the maximum allowed value. The inductor winding temperatures are all below 40 °C.

2.6 Conclusion

The growing prevalence of power electronic converter systems featuring Wide-Bandgap (WBG) semiconductors with ever higher switching frequencies motivates research on Ultra-High Bandwidth Power Amplifiers (UHBWPAs) for characterization and testing purposes. In this chapter, circuit topologies for a switch-mode (Class-D) realization of such Power Amplifiers (PAs) are analyzed. A switch-mode realization is generally desired because it features a significantly higher efficiency compared to traditional analog realizations. However, the achievable Bandwidth (BW) in switch-mode amplifiers is ultimately limited by the maximum possible switching frequency. This frequency has to be chosen sufficiently higher than the corner frequency of the output filter. Therefore, series- and parallel-interleaving concepts are investigated to allow an effective switching frequency $f_{sw,eff}$ (relevant for filtering) in the MHz range despite a moderate switching frequency f_{sw} of the individual switches. Series-interleaving distributes the blocking voltage stress and parallel interleaving the current stress between multiple devices. Therefore, the combination of both approaches, i.e., the parallel-interleaved operation of several series-interleaved (multi-level) bridge legs, is comprehensively analyzed in terms of loss, volume and design complexity scaling and eventually a Three-Level Triple-Interleaved (3L3) Flying Capacitor Converter (FCC) is selected. A highly compact hardware demonstrator (power density of $25\,kW/dm^3$ / $410\,W/in^3$) of a single-phase module is realized for performance verification.

Important design aspects are described in detail. Experimental results verify the operation with 10 kVA output power (per phase) at 230 V rms output voltage with an output frequency of 100 kHz (nominal operating point), where a system efficiency of 95.8 % and excellent output voltage quality (3^{rd} and 5^{th} harmonic of 2.5 V and 1.2 V, respectively) is achieved. A three-phase output can be realized with three individual single-phase modules of the presented converter or alternatively, the three parallel-interleaved branches of a 3L3 converter can be reconfigured for a three-phase output.

The presented versatile UHBWPA module serves as a solid basis for testing and characterization of Next Generation Power Electronics (NGPE) featuring WBG semiconductors. Further work on this topic includes the implementation of highly dynamic closed-loop controllers for different application scenarios, e.g., general amplification, virtual impedance emulation, machine emulation and so on. Important characterization parameters are then dynamic specifications such as the responses to a reference voltage step and to a load step (disturbance). Thereby, also a High-Resolution Pulse Width Modulation (HRPWM) and dead time correction are advantageously implemented to additionally improve the output voltage quality and/or to achieve high precision reference tracking.

Part B

Advanced Measurement Technology

3

High-Frequency DC-Coupled Current Measurement Sensors

This chapter summarizes the most relevant findings regarding High-Frequency (HF) current measurements with dc capability, which are also published in:

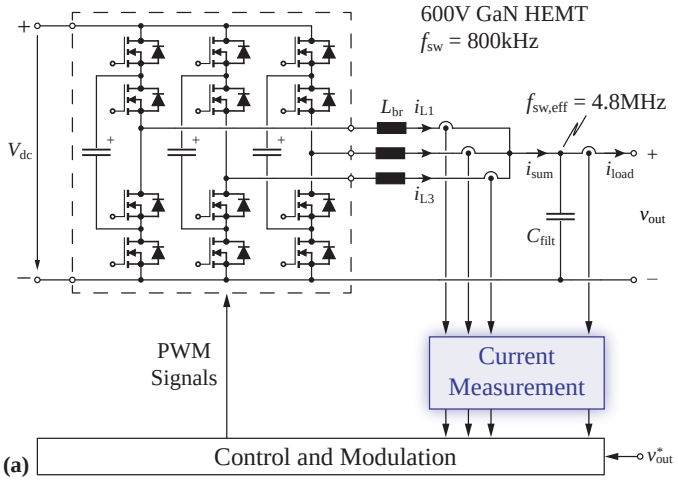
- **P. S. Niklaus**, D. Bortis, and J. W. Kolar, "Beyond 50 MHz Bandwidth Extension of Commercial DC-Current Measurement Sensors with Ultra-Compact PCB Integrated Pickup Coils," *IEEE Transactions on Industry Applications,* vol. 58, no. 4, pp. 5026-5041, August 2022.

Chapter Abstract

The control of very high switching frequency power electronic converter systems featuring latest generation Wide-Bandgap (WBG) devices requires current measurements with a very high Bandwidth (BW) to achieve high closed-loop control dynamics. One example is the previously described ultra-high BW 4.8 MHz parallel-interleaved multi-level Gallium-Nitride (GaN) inverter ac power amplifier with a target large-signal output BW of 100 kHz. This chapter investigates the combination of commercially available Low-Frequency (LF) Hall-effect current sensors (BW $\approx$ 1 MHz) with suitable HF sensors to extend the BW above 10 MHz, i.e., enough to measure the HF inductor current. Based on a conventional Printed Circuit Board (PCB) integrated Rogowski coil, for the HF sensor three improved Pickup Coil (PUC) geometries based on proposals in the literature are investigated. The LF and HF sensor signals are combined with a precision fully-differential combiner circuit. Design guidelines for the HF sensors as well as the combiner circuit are presented and thereby the influence of mismatches and tolerances is examined. The performance of the proposed HF sensors is experimentally verified and compared to further proposed solutions based on Isolated Inductor Voltage Sensing (IVS) and a Current Transformer (CT). The PUCs reach a BW $>$ 50 MHz, which is an improvement by more than a factor of 50 compared to the fastest available Hall sensor. Furthermore, it is proven that all investigated sensors are capable to accurately measure the triangular inductor current ripple in a hardware prototype of the aforementioned ac power amplifier. In a final step, the influence of Common Mode (CM) disturbances originating from fast $\mathrm{d}v/\mathrm{d}t$ switching transients on the sensor performance is analyzed. The presented current sensors achieve a Common Mode Rejection Ratio (CMRR) of almost 100 dB.

3.1 Introduction

Modern power electronic converter systems (Next Generation Power Electronics (NGPE)) typically use latest Wide-Bandgap (WBG) power semiconductors to allow higher switching frequencies (in the MHz-range), which in turn results in very power-dense system realizations. Besides a higher power density, MHz-range switching frequencies enable the realization of highly dynamic converter systems such as the Gallium-Nitride (GaN)-based phase-modular 10 kW (per phase) ac power amplifier with 100 kHz large-signal out-



(a)

(b)

Parameter		Value
Peak Output Voltage per Phase	$V_{out,pk}$	0 ... 350 V
Output Frequency	f_{out}	DC ... 100 kHz
Output Power per Phase	S_{out}	0 ... 10 kVA
DC Link Voltage	V_{dc}	800 V
Effective Switching Frequency	$f_{sw,eff}$	4.8 MHz

Fig. 3.1: (a) System overview of the 100 kHz large-signal output voltage control Bandwidth (BW) Power Amplifier (PA) realized as *Three-Level Triple-Interleaved (3L3)* converter with Gallium-Nitride (GaN) switches. **(b)** The main system specifications.

put Bandwidth (BW) and an effective switching frequency of $f_{sw,eff} = 4.8$ MHz described previously in **Chapter 2**. As a recap, **Fig. 3.1 (a)** shows again the proposed converter topology, a *Three-Level Triple-Interleaved (3L3) Flying Capacitor Converter (FCC)* with the main specifications listed in **Fig. 3.1 (b)**. Each switching cell (two switches plus a Flying Capacitor (FC)) switches with 800 kHz, which results in a current ripple with a frequency of $f_{iLpp} = 1.6$ MHz in each of the three branch inductors L_{br}. The parallel-interleaved operation and the subsequent summation of the three inductor currents $i_{L,1...3}$ at the output filter capacitor node results in the effective switching frequency of 4.8 MHz. For closed-loop operation with up to 100 kHz large-signal output BW a cascaded control scheme with a very fast inner current controller and outer voltage controller including several feed-forward paths turned out to

be the most promising approach [17]. Wideband current and voltage measurements are required for proper operation of these fast controllers. The former is depicted in **Fig. 3.1 (a)** and is typically more challenging to realize in practice compared to voltage measurements, since most state-of-the-art current measurement principles are covering either dc and Low-Frequencys (LFs) ($< 1\,\mathrm{MHz}$) or High-Frequency (HF) components but not dc. The following requirements are considered for the target current measurement:

- dc-capable and $> 10\,\mathrm{MHz}$ BW to capture at least six harmonics (even and/or odd) of the 1.6 MHz triangular inductor currents,
- galvanic isolation to allow current measurements on a floating potential,
- no or very low added losses,
- measurement range of $\pm 40\,\mathrm{A}$ for the inductor current and $\pm 65\,\mathrm{A}$ for the output current with a sensitivity in the range of $15 - 30\,\mathrm{mV/A}$ to maximally utilize the full-scale voltage range of typical Analog-to-Digital Converters (ADCs),
- high immunity to Common Mode (CM) disturbances resulting from the high $\mathrm{d}v/\mathrm{d}t$ of WBG semiconductors,
- small form factor.
- Deviation of $< \pm 3\,\%$ over the frequency range (corresponds to $\pm 0.25\,\mathrm{dB}$ variation).

Generally, an accuracy in the range of several percent is considered sufficient for the current measurement, since it is part of the inner current control loop. The outer voltage control loop, which typically has integrating behavior [17], can still correct residual errors from the inner loop that are within the voltage controller BW.

Most state-of-the-art commercial current sensors either rely on the Hall-effect [95, 96], feature a magneto-resistive element [97] or work based on the flux-gate principle [98]. They offer very high precision, adequate sensitivity, high CM immunity, galvanic isolation and they are dc-capable. Common to all is, however, the fundamental disadvantage of limited BW in the range of only 500 kHz to 1 MHz, which is at least one order of magnitude too low for the given application.

Although a commercial off-the-shelf solution would be desirable due to the ease of use and small form factor, unfortunately, no device that meets all the above requirements, particularly the BW, exists. To benefit from the aforementioned advantages of commercial sensors, an extension of the

frequency range of a readily available commercial current sensor to make it suitable for the given application is required.

The combination of a LF and HF current sensor has been comprehensively studied in literature. A typical approach is to use a Hall element in an open-loop [99–101] or a closed-loop [102–104] configuration to measure the remaining magnetic flux density in the core of a gapped Current Transformer (CT). In the former case, the LF Hall element voltage is directly added to the output of the CT, whereas in the latter case a compensator injects a current into the CT secondary winding to nullify the magnetic flux in the core. The closed-loop approach has the advantage of linearizing the Hall element's response but is fairly complex to realize. The common disadvantage of both approaches is the required air gap in the magnetic core to fit the Hall element, which complicates the manufacturing. Furthermore, there is a pronounced stray field in the vicinity of the air gap, which particularly for the open-loop configurations could distort the Hall element measurements due to parasitic voltage induction in the connecting leads [100, 102]. In [105], a Hall sensor and CT are operated independently of each other and combined using a dedicated combiner network. An alternative approach is presented in [106] where a Hall element in open-loop configuration is combined with a Rogowski coil [107]. The Rogowski coil measures the change in current and therefore needs a subsequent integration stage to obtain a signal that is proportional to the current [103, 108, 109]. This inherently limits the dc and LF response, which is added by the Hall element.

3.1.1 Overview of this Chapter

Different possibilities to combine a LF Hall-effect and a HF current sensor have been previously analyzed and compared in [86] by the author of this thesis, aiming for a BW extension of commercially available LF current sensors. This chapter briefly summarizes the findings of [86] in **Section 3.2** and extends them with an alternative approach for the combination presented in **Section 3.3**, which simplifies the HF current sensor design. Thereby, very compact and highly linear Printed Circuit Board (PCB) integrated Rogowski coils can be used. Then, **Section 3.4** presents three favorable PCB integrated realizations for the HF Rogowski coil to achieve the desired coupling with very compact sensors and compares them to the classical toroidal Rogowski coil realization. Afterwards, the performance is verified experimentally in **Section 3.5** and in **Section 3.6** the immunity with respect to CM disturbances is analyzed. Finally, **Section 3.7** discusses the findings and compares them to results in literature before **Section 3.8** concludes the chapter.

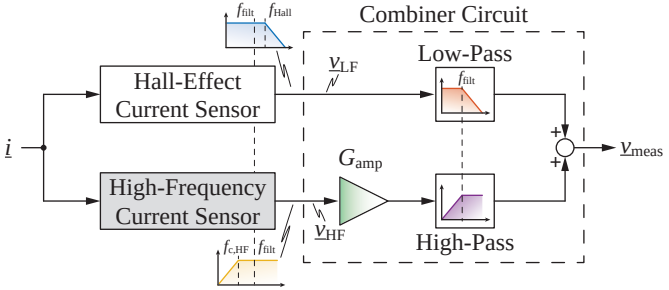


Fig. 3.2: Block diagram of the current measurement system including the combiner circuit proposed in [86].

3.2 HF Extension of LF Hall-Effect Sensor

This section briefly summarizes the findings of [86] where a commercial fully integrated Hall-effect current sensor is combined with a suitable HF sensor using an analog combiner circuit.

3.2.1 Measurement System

Fig. 3.2 shows the block diagram of the initially proposed measurement system including the combiner circuit to combine the signal $\underline{v}_{LF}$ of the LF Hall-effect sensor (Allegro ACS733 [96]) with its inherent low-pass characteristic (corner frequency f_{Hall}) with the signal $\underline{v}_{HF}$ of the HF extension (cf. **Section 3.2.2**), which has an intrinsic high-pass characteristic (corner frequency $f_{c,HF}$). Please note that $\underline{v}_x$ indicates a complex quantity with a magnitude and phase information. If both, the LF and HF sensor show an ideal first-order low-pass and high-pass response with $f_{Hall} = f_{c,HF}$, ideally, no combiner circuit would be required for a flat frequency response but the two signals could just be added. In practice, this is unfortunately not the case — particularly the Hall sensor frequency response deviates from a first-order low-pass response [96] — resulting in magnitude and phase errors. The combiner network therefore introduces an additional low-pass characteristic with corner frequency $f_{filt} = \omega_{filt}/(2\pi)$ for $\underline{v}_{LF}$ and a high-pass characteristic with the same corner frequency f_{filt} for $\underline{v}_{HF}$ such that the summation of the two voltages equals

$$\underline{v}_{meas} = \underline{v}_{LF} \cdot \frac{1}{1 + s/\omega_{filt}} + \underline{v}_{HF} \cdot G_{amp} \cdot \frac{s/\omega_{filt}}{1 + s/\omega_{filt}}. \tag{3.1}$$

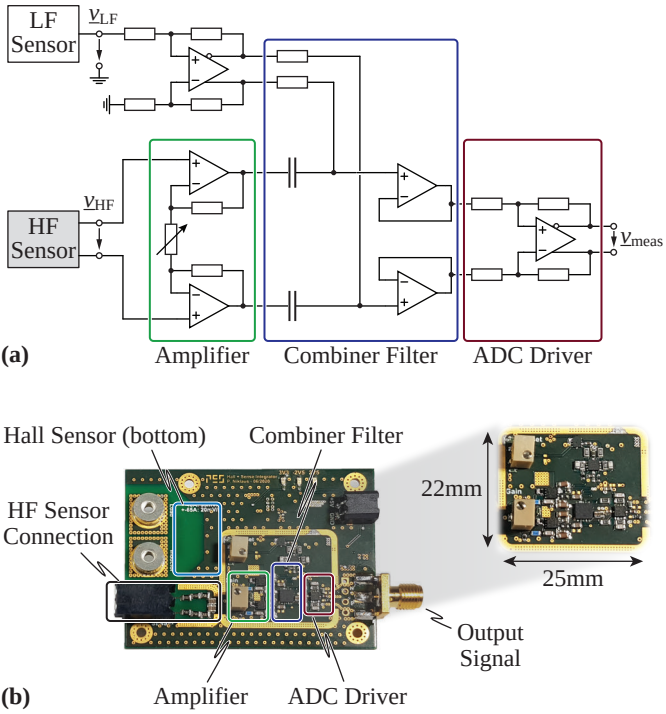


Fig. 3.3: (a) Simplified schematic of the fully differential combiner circuit of [86] and **(b)** picture of the realized hardware demonstrator for the performance evaluation. The individual circuit blocks are highlighted.

For a flat frequency response in the transition range around f_{filt} a large overlap in the LF and HF sensor frequency response is therefore required ($f_{\text{c,HF}} < f_{\text{filt}} < f_{\text{Hall}}$). This vanishes the influence of the inherent LF sensor low-pass and HF sensor high-pass characteristic and the transition is solely defined by the combiner network. With the Hall sensor frequency response taken from the datasheet [96] the HF sensor corner frequency and the combiner frequency have to be chosen lower than $f_{\text{c,HF}} < 500\,\text{Hz}$ and $f_{\text{filt}} < 19\,\text{kHz}$, respectively, to keep the magnitude error below 0.25 dB (cf. Fig. 4 in [86]). The resulting phase deviation is in this case below 1°.

The Low-Pass Filters (LPFs) and High-Pass Filters (HPFs) are realized as first-order passive filters with the components connected between the LF and HF signal buffers/amplifiers (cf. **Fig. 3.3 (a)**), which inherently sets the

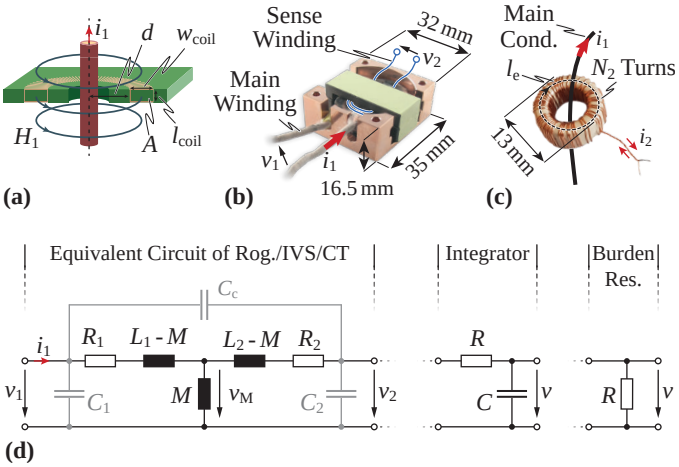


Fig. 3.4: Considered HF measurement sensors in [86]. **(a)** PCB integrated circular Rogowski coil, **(b)** Isolated Inductor Voltage Sensing (IVS) realized on the existing output filter inductor and **(c)** Current Transformer (CT) realized on a small iron powder toroidal core. **(d)** General equivalent circuit with a passive integrator to terminate the Rogowski coil and/or the IVS or a low ohmic burden resistor to terminate the CT.

corner frequency of the two filters to the same value, regardless of component tolerances. This mitigates a further source of magnitude and phase deviation. To increase immunity against CM disturbances, e.g., from nearby switching actions, the combiner circuit is realized fully differentially and a simplified schematic is shown in **Fig. 3.3 (a)**. The finalized hardware prototype of the combiner circuit is shown in **Fig. 3.3 (b)**. Apart from the bulky connectors required for testing purposes, a very compact realization is possible with dimensions of only 22 mm × 25 mm. The final design includes PCB mounted shields for improved immunity against external disturbances, for example magnetic fields emerging from the loop formed by the connection of the main current to the Hall sensor.

3.2.2 HF Measurement Sensors

The Hall sensor with the highest specified BW, i.e., $f_{\text{Hall}} > 1\,\text{MHz}$ [96], is chosen as a starting point in [86]. Three concepts to extend the BW of this LF sensor are investigated: 1) the conventional circular Rogowski coil, 2) the Isolated Inductor Voltage Sensing (IVS) and 3) the CT. The three solutions

are shown in **Fig. 3.4** including a general equivalent circuit and the required termination circuits.

Conventional Rogowski Coil

Rogowski coils generate a voltage v_2 that is proportional to the change in primary current ($\mathrm{d}i_1/\mathrm{d}t$), where the proportionality factor is the mutual inductance M. To get a signal proportional to the primary current i_1 the coil is loaded with a high impedance integrator, here realized with a passive RC network, with corner frequency $f_{\mathrm{int}} = 1/(2\pi \cdot RC)$. The coil is either realized as helical winding wrapped around the conductor to be measured or as PCB integrated solution. The latter is illustrated in **Fig. 3.4 (a)**. Due to the absence of a magnetic core, the sensor behaves very linear but has a low mutual inductance M (in the order of tens of nH). Its measurement sensitivity is directly proportional to M and the integrator corner frequency f_{int}. The latter is equal to the HF sensor's corner frequency $f_{\mathrm{c,HF}}$. Using a combiner circuit as shown in **Fig. 3.3** with $f_{\mathrm{c,HF}} < f_{\mathrm{filt}}$, the low M and the low required $f_{\mathrm{c,HF}}$ lead to an extremely small measurement sensitivity and thus dispose the classical Rogowski unsuitable as a HF sensor. As will be shown later, there are alternative approaches to combine the LF and HF signal where Rogowski coils become feasible.

Galvanically Isolated Inductor Voltage Sensing

A considerably higher measurement sensitivity is achieved when the inductor voltage is measured with an additional sense winding composed of a small number of turns on an already present output filter inductor L_{br} as shown in **Fig. 3.4 (b)**. The sense winding is terminated with a high impedance integrator circuit with $f_{\mathrm{int}} = f_{\mathrm{c,HF}} = 350\,\mathrm{Hz}$. Due to the galvanic isolation this concept is denoted *Isolated Inductor Voltage Sensing (IVS)*. The underlying principle is identical to a Rogowski coil but thanks to the magnetic core with its relative permeability μ_{r} a significantly higher mutual inductance M ($M \approx 2.1\,\mu\mathrm{H}$) and thus a higher measurement sensitivity is achieved. In other words, for a given measurement sensitivity a lower corner frequency $f_{\mathrm{c,HF}}$ can be chosen. Furthermore, no additional volume for a dedicated coil is required, since the sense winding is directly placed on the inductor. However, a variation of μ_{r}, e.g., due to temperature variations or the nonlinear $B - H$ characteristic of the magnetic material directly influences the measurement sensitivity. In practice, the effect is relatively small, since the air gap in the inductor linearizes the effective permeability. Same as the conventional Rogowski coil the BW of the IVS is implicitly limited by the Self-Resonance Frequency (SRF) of the coil or sense winding [110]. The SRF

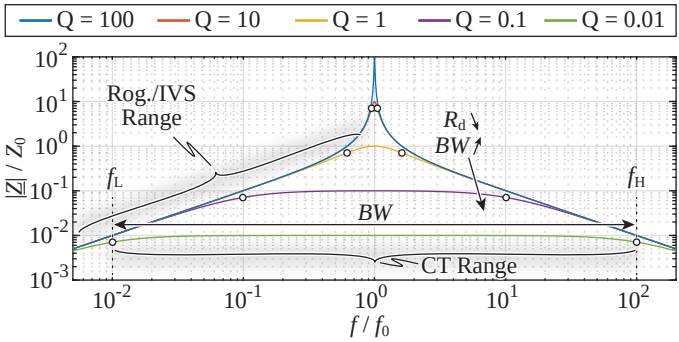


Fig. 3.5: Impedance of a Rogowski coil and/or IVS winding and/or CT secondary winding for different quality factors $Q = R_d / Z_0$. For a given resonance frequency f_0 the peaking reduces with lower Q (lower R_d). Highlighted are the operation range of the Rogoswki coil and the IVS (range where $|\underline{Z}|$ increases with f) as well as the operation range of the CT (range where $|\underline{Z}|$ is constant).

$f_0 = 17.2\,\text{MHz}$ is determined by the parallel resonance between the self-inductance L_2 and the equivalent parasitic capacitance $C_p = C_2 \,||\, \frac{C_c C_1}{C_c + C_1}$ of the sense winding (cf. **Fig. 3.4 (d)**). Above the typically very weakly damped SRF the coil behaves capacitively and therefore does not measure the current anymore. A damping resistor R_d is often connected in parallel to the output of conventional Rogowski coils to damp the SRF, i.e., to flatten the peak. This prevents oscillations in the output signal in case the SRF is excited during operation. **Fig. 3.5** shows the effect of the added damping resistor R_d that effectively lowers the quality factor $Q = R_d / Z_0$ of the coil. For $Q = 1 / 2$, i.e., $R_d = Z_0 / 2 = 1 / 2 \cdot \sqrt{L_2 / C_p}$ there is no peaking (critical damping). For the IVS, thanks to the high coupling, several hundred volts appear at the sense winding. Therefore, damping is not practically possible in this case because the required R_d is usually in the few hundred ohm range, which would cause significant losses.

Current Transformer

A CT typically features one single primary turn N_1 and a high number of secondary turns N_2. **Fig. 3.4 (c)** shows a realization with $N_2 = 50$ turns on a small iron powder toroidal core. The high turns ratio allows the CT to be loaded with a small burden resistance R, which inherently damps the SRF by lowering Q to very small values without contributing high losses. From **Fig. 3.5** follows that the impedance is flat over a very wide frequency

region for a low Q. Consequently, the CT requires no integration stage, since the output voltage v is directly proportional to the primary current i_1. The CT has to be able to carry the full dc current without saturation, thus a low-μ iron powder toroidal core is chosen (Micrometals T50-70B with a $\mu_r = 100$). Its magnetic length l_e is selected such that the maximum expected current of 65 A leads to a decrease of the initial permeability by $< 25\,\%$. The corner frequency $f_{c,HF}$ of the CT is determined by the self inductance L_2, the winding resistance R_2 and the burden resistance R and is selected $f_{c,HF} = 1\,\text{kHz}$ in the presented realization. It has to be emphasized, that the material non-linearities do influence L_2, which has no impact on the measurement sensitivity but only on the corner frequency $f_{c,HF}$. If $f_{c,HF}$ is sufficiently lower than f_{filt}, then the possible fluctuation of $f_{c,HF}$ due to changes in μ_r do not alter the flatness of the overall Transfer Function (TF).

3.2.3 Experimental Verification

The IVS and the CT have been realized as hardware prototypes to experimentally verify the performance. TF measurements in the frequency domain and converter waveform measurements in the time domain reveal satisfactory performance. A BW of 10 MHz for the IVS and 35 MHz for the CT are achieved. Furthermore, a 1.6 MHz triangular current ripple could be accurately followed as a comparison with a reference measurement using a commercial current probe revealed. For detailed measurement results please refer to **Section 3.5**.

3.3 Alternative Measurement System and Combiner Circuit

The advantage of the sensor combination presented in [86] is the inherently matched combiner LPF and HPF, independent of filter element component tolerances. This property comes at the expense of a large required overlap of the LF Hall-effect sensor and the HF current sensor in the frequency response (approximately three to four decades). Clearly, this is not optimal in terms of form factor (functional volume) and/or sensitivity of the individual sensors, particularly for a Rogowski coil, whose sensitivity is directly proportional to its lower corner frequency for a given mutual inductance M. Therefore, alternative approaches of the combination without the required overlap have been proposed, e.g., in [99, 101, 104] and [106]. [99] and [101] present a gapped CT with a Hall element placed inside the air gap. This arrangement allows a combination of LF and HF signals without any processing electronics but requires custom magnetic components and careful placement of the Hall

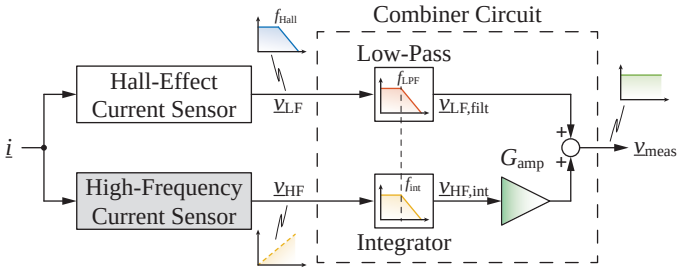


Fig. 3.6: Block diagram of the alternative current measurement system without the need for a large overlap between the LF and HF sensors. The HF sensor is assumed to react to the change in current ($\mathrm{d}i/\mathrm{d}t$), i.e., shows a differentiating behavior.

element to avoid measurement errors due to the magnetic stray field in the vicinity of the air gap.

The aim of this chapter is to realize an optimized high-BW current sensor based on the concept of [104] and [106], which will be explained in the following, and compare the results with the findings of [86]. A major advantage thereby is that for a given measurement sensitivity compact Rogowski coils with a much lower mutual inductance can be used.

3.3.1 General Operation

Fig. 3.6 shows the block diagram of the alternative realization of the measurement system and combiner circuit as shown in [104] and [106]. The LF path is composed of the commercial fully integrated Hall-effect sensor with sensitivity $G_{0,\mathrm{Hall}}$ that shows a low-pass characteristic approximated with corner frequency f_{Hall}, and an additional LPF with corner frequency f_{LPF} sufficiently lower than f_{Hall}. The condition $f_{\mathrm{LPF}} \ll f_{\mathrm{Hall}}$ (at least one decade lower [99]) ensures that the filtered Hall sensor signal $\underline{v}_{\mathrm{LF,filt}}$ behaves like a first-order low-pass response despite the typically very complex frequency response of the Hall sensor itself [96]. The HF path consists of a HF sensor with a high-pass characteristic and an amplifier with gain G_{amp} (assumed constant over frequency and without phase-shift as explained later). The HF sensor is in this case assumed to react proportional to a change in current ($\mathrm{d}i/\mathrm{d}t$), i.e., $\underline{v}_{\mathrm{HF}} = sM \cdot \underline{i}$ in frequency domain. Thus, a subsequent integration stage realized as first-order RC low-pass filter with corner frequency f_{int} introduces a high-pass characteristic for the HF sensor and results in a signal $\underline{v}_{\mathrm{HF,int}}$ proportional to the current $\underline{i}$ above f_{int}. In frequency domain, the output

voltage $\underline{v}_{\text{meas}}$ of the measurement system is

$$\underline{v}_{\text{meas}} = \underbrace{\underline{v}_{\text{LF}} \cdot \frac{1}{1+s/\omega_{\text{LPF}}}}_{\underline{v}_{\text{LF,filt}}} + G_{\text{amp}} \cdot \underbrace{\underline{v}_{\text{HF}} \cdot \frac{1}{1+s/\omega_{\text{int}}}}_{\underline{v}_{\text{HF,int}}} \tag{3.2}$$

with $\omega = 2\pi \cdot f$. Substitution of the LF and HF sensor TF results in a total TF $\underline{G}_{\text{tot}} = \underline{v}_{\text{meas}}/\underline{i}$ of

$$\begin{aligned}\underline{G}_{\text{tot}} = \underline{v}_{\text{meas}}/\underline{i} = &\underbrace{G_{0,\text{Hall}} \cdot \frac{1}{1+s/\omega_{\text{Hall}}}}_{\underline{G}_{\text{Hall}}} \cdot \underbrace{\frac{1}{1+s/\omega_{\text{LPF}}}}_{\underline{G}_{\text{LPF}}} \\ &+ G_{\text{amp}} \cdot \underbrace{sM \cdot \frac{1}{1+s/\omega_{\text{int}}}}_{\underline{G}_{\text{HF-Sensor,int}}}.\end{aligned} \tag{3.3}$$

Assuming $f_{\text{Hall}} \gg f_{\text{LPF}}$, (3.3) simplifies to

$$\underline{G}_{\text{tot}} = G_{0,\text{Hall}} \cdot \frac{1}{1+s/\omega_{\text{LPF}}} + \underbrace{G_{\text{amp}} \cdot M \cdot \omega_{\text{int}}}_{\equiv G_{0,\text{HF}}} \cdot \frac{s/\omega_{\text{int}}}{1+s/\omega_{\text{int}}}. \tag{3.4}$$

Two conditions have to be fulfilled for a flat $\underline{G}_{\text{tot}}$:

i) The sensitivities of the Hall sensor and the HF sensor have to be matched, i.e., $G_{0,\text{Hall}} = G_{\text{amp}} \cdot M \cdot \omega_{\text{int}}$.

ii) The LPF in the LF path and the integrator in the HF path must be set to the same corner frequency, i.e., $f_{\text{LPF}} = f_{\text{int}}$.

With i) and ii), (3.4) simplifies to

$$\underline{G}_{\text{tot}} = G_{0,\text{Hall}} \cdot \left(\frac{s/\omega_{\text{LPF}}}{1+s/\omega_{\text{LPF}}} + \frac{1}{1+s/\omega_{\text{LPF}}} \right) = G_{0,\text{Hall}}, \tag{3.5}$$

which is the summation of a low-pass and high-pass response with the same corner frequency $f_{\text{LPF}} = f_{\text{int}}$. $\underline{G}_{\text{tot}}$ is thus constant over the full frequency range, limited in BW only by the HF sensor itself. In contrast to the combiner circuit in [86], the HF sensor corner frequency f_{int} is identical to the combiner frequency (denoted f_{filt} in [86]), i.e., the frequency of the transition from LF to HF sensor. For a given required measurement sensitivity the HF sensor

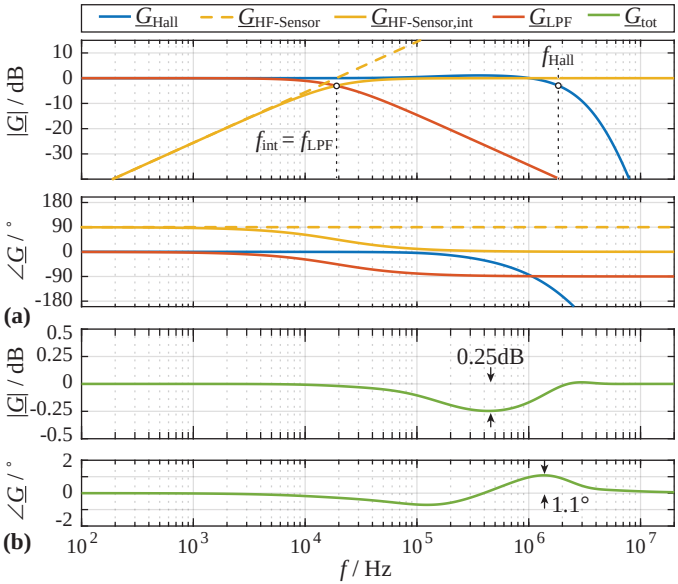


Fig. 3.7: Exemplary Transfer Functions (TFs) for the alternative combiner circuit with **(a)** normalized magnitude and phase response of the LF Hall sensor ($\underline{G}_{\text{Hall}}$, taken from the datasheet [96]) with $f_{\text{Hall}} \approx 1.8\,\text{MHz}$, a HF current sensor ($\underline{G}_{\text{HF-Sensor}}$) with $f_{\text{c,HF}} = f_{\text{int}} = 19\,\text{kHz}$ and the accordingly matched Low-Pass Filter (LPF) ($\underline{G}_{\text{LPF}}$). **(b)** Resulting normalized total TF $\underline{G}_{\text{tot}}$ with a maximum magnitude and phase deviation of 0.25 dB and 1.1°, respectively.

corner frequency can be chosen approximately two decades higher compared to [86] (in the range of tens of kHz instead of hundreds of Hz), which allows to use Rogowski coils with a mutual inductance approximately 100 times lower than the $M \approx 2\,\mu\text{H}$ of the IVS. This will be further elaborated in **Section 3.4**.

Fig. 3.7 shows exemplary normalized TFs to illustrate the operation of the measurement system. Please note that the Hall sensor response $\underline{G}_{\text{Hall}}$ is taken from the datasheet [96]. Despite the perfectly matched LF and HF sensor sensitivities and identical frequencies f_{LPF} and f_{int} ($f_{\text{LPF}} = f_{\text{int}} = 19\,\text{kHz}$) in **Fig. 3.7 (a)**, the total TF $\underline{G}_{\text{tot}}$ in **Fig. 3.7 (b)** shows an amplitude and phase mismatch of 0.25 dB and 1.1°, respectively. This is due to the impact of the Hall sensor's frequency response on the LPF, resulting in a deviation of the behavior of $v_{\text{LF,filt}}$ from an ideal first-order system.

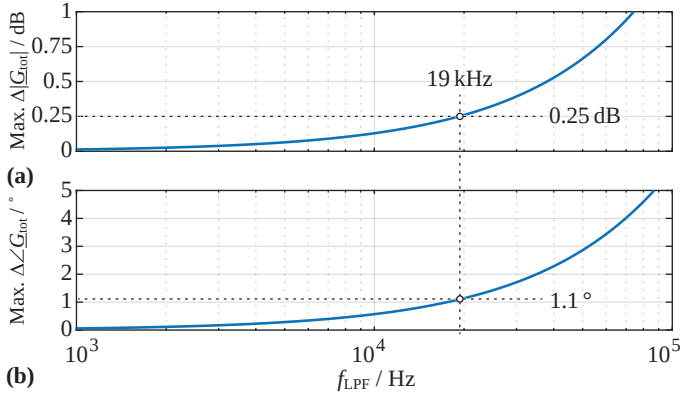


Fig. 3.8: Maximum magnitude deviation $\Delta|\underline{G}_{\text{tot}}|$ and maximum phase deviation $\Delta\angle\underline{G}_{\text{tot}}$ of the total TF $\underline{G}_{\text{tot}}$ for different LPF corner frequencies f_{LPF}. Perfect matching, i.e., $f_{\text{LPF}} = f_{\text{int}}$ is assumed.

3.3.2 Impact of Nonidealities

Selection of the Combiner Frequency

The selection of f_{LPF} and thus the combiner frequency is the remaining degree of freedom in the LF path for the given Hall sensor frequency response. **Fig. 3.8 (a)** indicates the maximum magnitude deviation $\Delta|\underline{G}_{\text{tot}}|$ of the total TF based on the selection of f_{LPF} under the assumption of ideal matching ($f_{\text{LPF}} = f_{\text{int}}$). Similarly, **Fig. 3.8 (b)** shows the maximum phase deviation $\angle\underline{G}_{\text{tot}}$. It is intuitively clear that a lower f_{LPF} results in a smaller magnitude and phase deviation, since the overall behavior is more accurately determined solely by the LPF and is not influenced by the Hall sensor's frequency response ($f_{\text{LPF}} \ll f_{\text{Hall}}$). As already shown, for $\Delta|\underline{G}_{\text{tot}}| < 0.25\,\text{dB}$ (around 3 % error), $f_{\text{LPF}} < 19\,\text{kHz}$ must be chosen. At the same time this implies $\angle\underline{G}_{\text{tot}} < 1.1°$ (cf. **Fig. 3.7**).

Mismatch Between LF and HF Path

A mismatch between f_{int} and f_{LPF} violates condition ii) mentioned above and results in a deviation from the ideally flat behavior in the magnitude and phase response. **Fig. 3.9** depicts the maximum magnitude and phase deviation for a relative mismatch between f_{int} and f_{LPF}. In order to keep $\Delta|\underline{G}_{\text{tot}}| < 0.25\,\text{dB}$ the mismatch between the two corner frequencies needs to be lower than −5.7/+5.8 %. At the same time this results in a $\Delta\angle\underline{G}_{\text{tot}}$ of 0.82°. Both corner

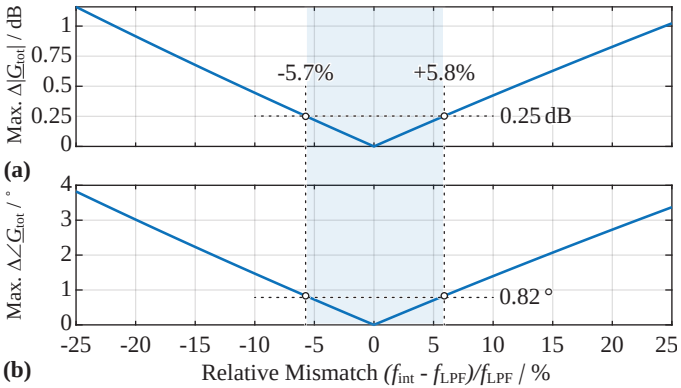


Fig. 3.9: Impact of a relative mismatch of f_{int} with respect to f_{LPF} on the maximum magnitude deviation $\Delta|\underline{G}_{\text{tot}}|$ and maximum phase deviation $\Delta\angle\underline{G}_{\text{tot}}$ of the total TF $\underline{G}_{\text{tot}}$.

frequencies are realized with passive *RC* networks, and tolerances $< 5\,\%$ are easily achieved with readily available components. Manual trimming of the filter elements could improve this even further. Hence, the influence of component tolerances on the flatness of $\underline{G}_{\text{tot}}$ is negligible.

A mismatch between the LF and HF sensor sensitivity (condition i) from above) similarly leads to a magnitude and phase deviation. To keep $\Delta|\underline{G}_{\text{tot}}|$ below 0.25 dB the mismatch must be smaller than $\pm 3\,\%$. Adjustment of the amplifier gain G_{amp} allows to precisely match the sensitivities and therefore, this error contribution is negligible.

Remark: Instead of a sensor that reacts proportional to a current change $\mathrm{d}i/\mathrm{d}t$ and a subsequent integration stage, the HF current measurement could alternatively be realized with a CT as shown in [99], [101] and [86]. In this case, $f_{\text{c,HF}}$ is determined by L_2, R_2 and R (cf. (5) in [86] and **Fig. 3.4**). For a variation of the flux density in the CT, the relative permeability μ_{r} changes based on the non-linear $B - H$ characteristic. Similarly, temperature variations influence μ_{r}. Consequently, L_2 and therefore $f_{\text{c,HF}}$ are not necessarily constant during operation, which violates the matching of the LF and HF sensor corner frequencies. Therefore, it is advisable to use a HF sensor with a subsequent passive *RC* integrator stage, to prevent a variation of $f_{\text{c,HF}}$.

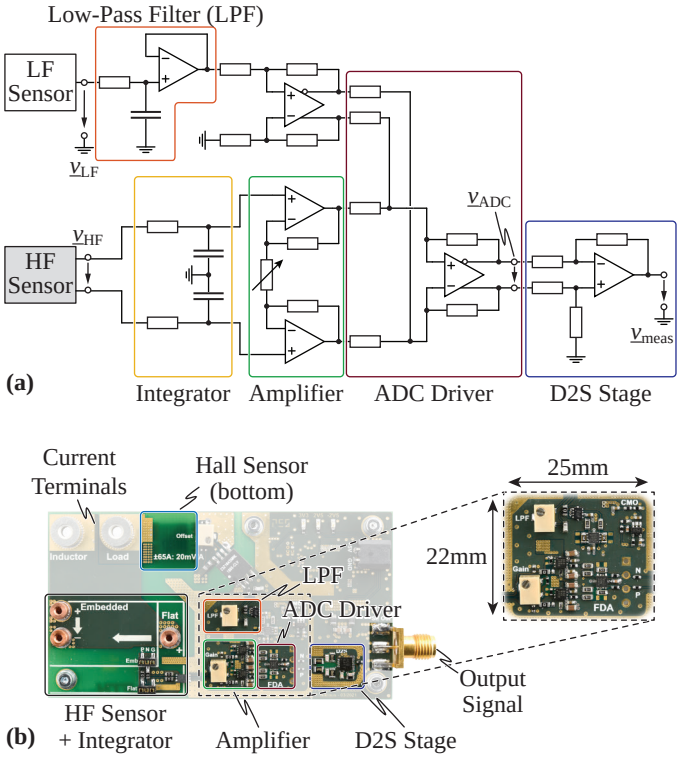


Fig. 3.10: (a) Simplified schematic of the fully differential combiner circuit and **(b)** picture of the realized hardware prototype for the performance verifications. Relevant circuit blocks are highlighted.

3.3.3 Practical Realization

A simplified circuit diagram of the combiner circuit is presented in **Fig. 3.10 (a)** together with a picture of the realized hardware prototype in **Fig. 3.10 (b)**. All the relevant building blocks are highlighted. The circuit is realized fully differentially to improve the robustness against CM disturbances. Both, the differentially implemented integrator (yellow) as well as the LPF after the Hall sensor (orange) are realized as passive *RC* circuits. After the HF sensor amplifier stage (green) with adjustable gain the signals are summed up and the ADC driver (dark red) is the interface to a high-speed fully differential ADC. For the performance verification, however, a single-ended output signal

is required (cf. **Section 3.5**). Therefore, the final stage is a high Common Mode Rejection Ratio (CMRR) Differential to Single-Ended (D2S) conversion (dark blue). The circuit from **Fig. 3.10 (a)** without the D2S conversion is realized extremely compact with an area of only 22 mm × 25 mm. The hardware prototype further includes connectors to mount different HF sensors (cf. **Section 3.4**).

3.4 PCB Integrated Pickup Coils

3.4.1 HF Sensor Sensitivity

The alternative combiner circuit from the previous section requires a significantly smaller overlap between the LF and HF sensor. Consequently, for a given Hall sensor BW, a HF sensor with higher corner frequency f_{int} can be used. In case of a conventional Rogowski coil (cf. **Fig. 3.4 (a)**) the required mutual inductance M can be calculated based on f_{int} and the required sensor sensitivity. Assuming an ADC full-scale range of 2 V peak-to-peak and a maximum current measurement range of ±65 A, the measurement sensitivity is 15.4 mV/A. The HF sensor's sensitivity $G_{0,\text{HF}}$ is increased with G_{amp}, which is typically constrained to values below 10, due to the finite Gain-Bandwidth Product (GBP). As a conservative estimate $G_{\text{amp}} = 5$ is assumed in the following, which gives a large-signal (2 V peak-to-peak) BW of around 200 MHz with a typical high-speed operational amplifier [111]. Therefore, the amplifier's frequency response can be neglected for the considered measurement frequency range (G_{amp} in (3.2) is constant over frequency and has no phase-shift). According to (3.4), the HF sensor's sensitivity is

$$G_{0,\text{HF}} = G_{\text{amp}} \cdot M \cdot \omega_{\text{int}} = G_{\text{amp}} \cdot \frac{M}{RC}, \tag{3.6}$$

where $\omega_{\text{int}} = 1/(RC)$ is the RC-integrator corner frequency (cf. **Fig. 3.6**). While the combiner circuit in **Section 3.2** requires $f_{\text{int}} < 500\,\text{Hz}$ for $\Delta|\underline{G}_{\text{tot}}| < 0.25\,\text{dB}$, with the alternative approach $f_{\text{int}} < 19\,\text{kHz}$ is sufficient. Therefore, the required mutual inductance M for $G_{0,\text{HF}} = 15.4\,\text{mV/A}$ is only 25.8 nH for the combiner circuit according to **Section 3.3**. That is almost 100 times lower compared to the $M \approx 2\,\mu\text{H}$ in case of the IVS with a circuit according to **Section 3.2**. A mutual inductance in the range of tens of nH is feasible with Rogowski coils with the added benefit of high linearity due to the absence of a magnetic core material (no saturation, no material dependent M, etc.). A PCB integrated realization is beneficial not only in terms of accurate, economical and reproducible manufacturing but also in terms of tightly controlled parasitic elements.

3.4.2 Investigated Coil Geometries

PCB integrated Rogowski coils have been comprehensively studied in literature. Within this chapter it is differentiated between the conventional circular Rogowski coil geometry shown in **Fig. 3.11 (a)** and several improved arrangements in **Fig. 3.11 (b)-(d)**, which hereinafter are denoted as *Pickup Coils (PUCs)*. The investigated PUC geometries are based on previously studied designs in the literature [112–116]. Those are, however, mainly focusing on switch current measurements in power semiconductors during the typically very fast switching transitions for characterization, diagnostic and protection purposes, and therefore have a rather low M (typically around 1 nH or less). Furthermore, no dc and LF component is provided, which, however, is mandatory for current control in converter systems. In this chapter, the conventional Rogowski coil geometry as well as three improved PUC arrangements are investigated for suitability as HF BW extension for a Hall-effect current sensor. Thereby, not only a small form factor but also a large enough M ($\approx$ 25 nH) and a low variation of M versus frequency is important.

The geometry for each PUC arrangement is selected with a design procedure that considers the following performance criteria:

i) nominal mutual inductance of $M = 25\,\text{nH}$,

ii) minimum variation of M versus frequency,

iii) maximum BW,

iv) minimum occupied area.

Table 3.1 summarizes the properties of the four investigated geometries as a result of the detailed analysis in the following paragraphs. $\mathrm{d}M_\mathrm{f}$ denotes the relative variation of M in the frequency range $f \in [20\,\text{kHz} \ldots 20\,\text{MHz}]$ with respect to M at $f = 20\,\text{kHz}$ ($\approx f_\text{int}$) and is defined as

$$\mathrm{d}M_\mathrm{f} = \frac{\max\{M(f)\} - \min\{M(f)\}}{M(f = 20\,\text{kHz})} \cdot 100\,\%. \tag{3.7}$$

Conventional Rogowski Coil

The conventional PCB integrated Rogowski coil geometry directly follows from the helical coil wrapped around a conductor. The main current carrying conductor is inserted in the center of the circular PCB (cf. **Fig. 3.11 (a)**) with a radially symmetrically arranged coil of width w_coil and length l_coil. For a distance d between the center of the main current conductor and the inner

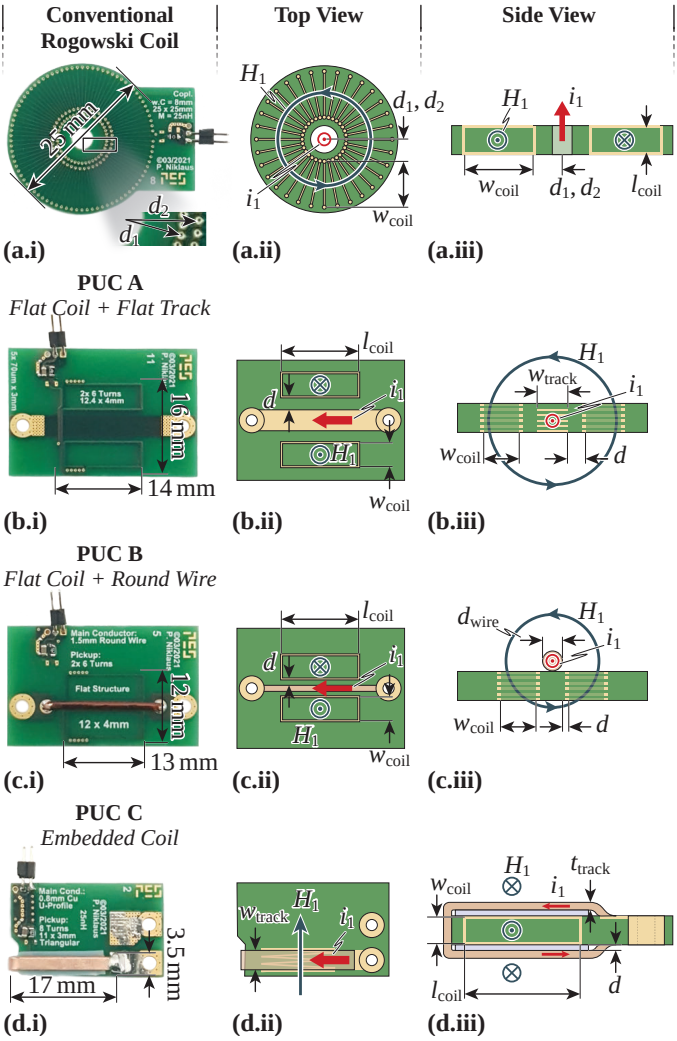


Fig. 3.11: Investigated Pickup Coil (PUC) geometries. **(a.i)** Picture of the conventional circular Rogowski coil with **(a.ii)** schematic top and **(a.iii)** side view with indicated directions of the main current i_1 and the magnetic field H_1 as well as the coil dimensions. **(b)**, **(c)** and **(d)** show the same for PUC arrangements A, B and C, respectively.

Tab. 3.1: Parameters of the four selected geometries of the investigated Rogowski coil/PUC arrangements for a nominal $M = 25\,\mathrm{nH}$ resulting from 2D FEM simulations and the considered design process.

Sensor	N	w_{coil}	l_{coil}	d	w_{track} d_{wire}	Total Area	$\mathrm{d}M_{\mathrm{f}}$
		mm	mm	mm	mm	mm^2	%
Rogowski	86	8.0	1.5	4.2 (d_1) 5.1 (d_2)	n.a.	490	0.1
PUC A	12	4.0	12.4	1.2	3.3	224	3.9
PUC B	12	4.0	12.0	0.25	1.25	156	0.0
PUC C	8	1.5	11.8	0.4	2.5	60	0.9

edge of the coil, the mutual inductance M of a coil with N turns is found as [108]

$$M = \frac{\mu_0 \cdot N \cdot l_{\mathrm{coil}}}{2\pi} \cdot \ln\left(1 + \frac{w_{\mathrm{coil}}}{d}\right). \tag{3.8}$$

M scales proportionally with N and l_{coil} but only logarithmically with increasing w_{coil} because the magnetic field decreases with $1/r$ in radial direction r. Unfortunately, w_{coil} and N are the only design parameters to choose, since l_{coil} is limited by the PCB thickness to around 1.5 mm. Clearly, increasing w_{coil} only marginally increases M given the logarithmic scaling. The self-inductance L_2 (cf. equivalent circuit in **Fig. 3.4 (d)**), which together with C_{p} defines the coil's SRF and ultimately its BW (cf. **Fig. 3.5**) [110], however, scales linearly with w_{coil}. The number of turns is limited by the maximum number of vias that can be placed on the inner edge of the coil (distance d from the center) while meeting the PCB manufacturing process clearances. On the one hand, d should be kept low to increase M but on the other hand the maximum N is a function of d. While M scales linearly with N, L_2 scales quadratically and thus the ratio M/L_2, which is a measure for the coupling coefficient, decreases with $1/N$. To achieve a certain M, comparably large coils with a high N are required, which is detrimental for the SRF and for the coupling coefficient.

With a second layer of vias on the inner edge of the coil, N and thus M can be increased. Under the assumption that $N/2$ of the turns are formed with the first layer of vias on the inner coil edge (distance d_1 from the center, cf. **Fig. 3.11 (a.i)**) and the remaining $N/2$ turns with the second layer of vias (distance d_2 from the center, cf. **Fig. 3.11 (a.i)**), the mutual inductance is

analytically calculated as

$$M = \frac{N}{2} \cdot \frac{\mu_0 \cdot l_{\text{coil}}}{2\pi} \cdot \ln\left(\frac{(d_1 + w_{\text{coil}})^2}{d_1 \cdot d_2}\right) \tag{3.9}$$

based on (3.8). The coil geometry with minimal occupied area (overall diameter of 25 mm) is found by iterating through all possible geometries that achieve the required $M = 25\,\text{nH}$ using (3.9). The resulting coil occupies an area of $490\,\text{mm}^2$ and features $N = 86$ turns (cf. **Table 3.1**).

Pickup Coil A - Flat Coil + Flat Conductor

Compared to the conventional geometry the coupling and hence the mutual inductance can be improved if the coil is in parallel to the main conductor, since M scales proportionally with the coil length. **Fig. 3.11 (b)** shows a picture and top and side view of such an arrangement where the main conductor is realized directly on the PCB with tracks of width w_{track} on multiple layers (5 of totally 6 layers in this case). In fact, the side view of the conventional Rogowski coil now becomes the top view with l_{coil} and w_{coil} as design parameters. This arrangement is based on realizations shown [112], [113] and [114]. The N turns of the PUC are not anymore symmetrically placed around the main track but lie equally distributed on the left and right side of the main conductor in the same plane ($N/2$ on each side). In the following, this arrangement is called *PUC A*. Compared to the simple case of the conventional Rogowski coil, analytical formulas are not easily derived due to the rectangular cross section of the main conductor distributed among multiple layers. In addition, HF effects such as the skin and proximity effect lead to an inhomogeneous current distribution within the main conductor at elevated frequencies with a significant increase of the current density on the outer edges. This results in a relatively large $\mathrm{d}M_{\text{f}}$ as indicated in **Table 3.1**. This effect is particularly detrimental for wide tracks compared to their thickness. At the same time, w_{track} has to be several millimeters wide to constrain the dc current density to values in the range of $40\,\text{A/mm}^2$ for sufficient heat extraction (empirical value).

The magnetic field distribution is obtained for different frequencies up to 20 MHz with help of a 2D Finite Element Method (FEM) simulation for different w_{track}. With the known magnetic field distribution the remaining parameters of the coil, namely the distance d between main track and coil edge, the coil width w_{coil} and the coil length l_{coil} could be varied in post processing to select a suitable geometry for the given performance criteria. At the same time, side conditions such as maximum current density (thermal limit) and minimum isolation distances (safety limit) have to be considered.

The latter condition implies a lower bound of 1.2 mm for d. Please note that for the utilized 6-layer PCB the number of turns is always fixed to $N = 2 \cdot 6 = 12$ under the assumption of one winding per layer. The parameters of the selected geometry of PUC A are listed in **Table 3.1**. As expected, the frequency variation $\mathrm{d}M_\mathrm{f}$ is rather large, however the required total area of 224 mm^2 is more than halved compared to the conventional Rogowski coil. Please note that the parameters refer to the physical realization of the coil, where $l_\mathrm{coil} = 12.4$ mm is selected slightly higher than the strictly required value of 10 mm for $M = 25$ nH. Generally, M is linearly dependent on l_coil, hence a variation of l_coil has no impact on $\mathrm{d}M_\mathrm{f}$.

Pickup Coil B - Flat Coil + Round Conductor

The variation of M versus frequency is virtually eliminated if the main conductor from PUC A is replaced with a solid round wire (diameter d_wire) that is soldered directly on the PCB like a through hole component. This arrangement is denoted as *PUC B* and is depicted in **Fig. 3.11 (c)**. Further advantages are that the copper cross section compared to its diameter is much higher than it is for a PCB track and in addition, d can be reduced, provided the round wire features adequate isolation, e.g., enameled copper wire. The coil dimensions are found with the same design procedure as described for PUC A. The parameters of the selected design are listed in **Table 3.1**. Thanks to the much smaller d, the total area is only 156 mm^2. Similar to PUC A, $l_\mathrm{coil} = 12.0$ mm is chosen slightly larger than the strictly required value of 11.6 mm for $M = 25$ nH.

Remark: For PUC A and PUC B the rectangular turns are placed on the different PCB layers on top of each other as illustrated in **Fig. 3.11 (b.iii) and (c.iii)**. Measurements with modified arrangements where the turns on adjacent layers are offset by the track width to minimize the parasitic capacitance showed a slight increase of the SRF, although the effect is minor.

Pickup Coil C - Embedded Coil

An increased coupling is achieved with a coplanar arrangement (*PUC C*) as shown in **Fig. 3.11 (d)**. This arrangement has been shown in [114], [115] and [116]. Here, the coil is embedded between the main conductor, which is wrapped around the PCB. If the main current conductor should be realized on the same PCB, the small thickness of the copper foil (70 µm on a typical power PCB) implies wide tracks to meet the current density requirement. As already explained for PUC A, this results in a relatively large variation of M over frequency. Furthermore, an expensive PCB technology with buried vias would be needed to realize the embedded coil on the inner layers with

the additional drawback of a smaller w_{coil} (cf. **Fig. 3.11 (d.iii)**). Therefore, it is advisable to use an external copper bar of thickness $t_{\text{track}} > 70\mu\text{m}$ to simultaneously lower w_{track}. The coplanar arrangement has several distinct advantages:

i) The magnetic field sensed by the coil is doubled compared to a single track, since the current passes around the coil on both sides with opposite sign.

ii) The current distribution along the width of the tracks is more uniform compared to a single track, hence the frequency dependency of M is lower (but not eliminated).

iii) As mentioned in [115], the copper bar additionally shields the coil from external magnetic fields.

iv) The sensor can be very easily connected in power electronic systems because the main current terminals lie next to each other.

A disadvantage is the somewhat higher parasitic coupling capacitance C_{c} between main current track and coil.

A suitable geometry for PUC C is found based on the magnetic field distribution simulated with 2D FEM using the same procedure as for PUC A and PUC B. The number of turns N is now an additional degree of freedom, since the turns are formed with tracks on the top and bottom layer connected with vias. The isolation between PUC and main conductor is realized with a Polytetrafluoroethylene (PTFE) foil of thickness $d = 0.4\,\text{mm}$. The value is selected based on a trade-off between parasitic coupling capacitance between PUC and main conductor, and the achievable mutual inductance. The copper bar thickness is selected as $t_{\text{track}} = 0.5\,\text{mm}$. The results in **Table 3.1** reveal that with an area of only $60\,\text{mm}^2$, PUC C is by far the smallest realization (area reduction by a factor of 8 compared to the conventional Rogowski coil), while the $\text{d}M_{\text{f}}$ is below 1 %.

3.4.3 Mutual Inductance and Coil Impedance

The conventional Rogowski coil and the three PUCs are built based on the results listed in **Table 3.1**. To verify the value of the mutual inductance at different frequencies, a current is injected in the main conductor while simultaneously the output voltage of the coil is measured. It has to be ensured that the loop of the injected current is large enough, such that the measurement is not influenced by additional magnetic field components, e.g., from the return conductor. **Table 3.2** summarizes the measurements at

Tab. 3.2: Simulated and measured mutual inductance of the four hardware prototypes including the results from the coil impedance measurements.

Sensor	M_{FEM} nH			M_{meas} nH			ε_{M} %			SRF MHz	L_2 µH	R_2 Ω	C_{c} pF	M/L_2
	100k	1M	5M	100k	1M	5M	100k	1M	5M					@ 100 k
Rog.	25.0	25.0	25.0	23.8	23.2	25.2	-4.9	-7.2	0.8	58	2.32	8.6	1.0	0.010
PUC A	27.3	27.8	27.9	31.6	31.1	33.2	15.7	11.7	19.2	105	1.06	0.7	3.9	0.030
PUC B	30.1	30.1	30.1	36.1	35.2	37.1	19.7	16.9	23.2	105	1.07	1.3	2.3	0.034
PUC C	28.6	28.8	28.9	30.2	29.7	30.1	5.7	2.9	4.4	202	0.32	0.8	5.3	0.094

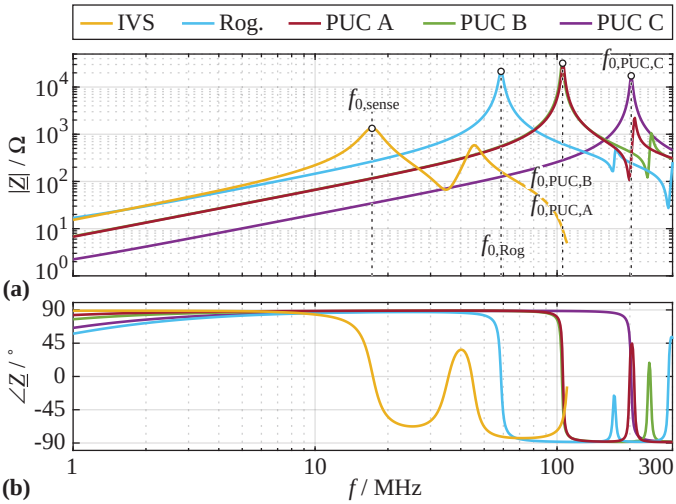


Fig. 3.12: Impedance measurements of the investigated PUCs as well as the IVS. **(a)** Magnitude and **(b)** phase response with highlighted SRF for each coil.

$f = \{100\,\mathrm{kHz}, 1\,\mathrm{MHz}, 5\,\mathrm{MHz}\}$ and compares them with the results from the FEM simulation.

There, the relative error ε_M between the simulated and measured value of M is defined as

$$\varepsilon_\mathrm{M} = (M_\mathrm{meas} - M_\mathrm{FEM})/M_\mathrm{FEM} \cdot 100\,\%. \tag{3.10}$$

Generally, the measurement results agree very well with the FEM simulation with an error of less than 25 %. The deviations can be explained with the slightly larger effective coil cross-sections in the hardware prototypes. The reason for this is the placement of the vias to connect the different layers as well as the return conductor from the last turn back to the first. The layout ensures that each turn has the minimum width and length of w_coil and l_coil as listed in **Table 3.1**, respectively.

The parameter $\mathrm{d}M_\mathrm{f}$ could not be evaluated with this direct measurement method, since the additional capacitive loading of the coil voltage measurement drastically decreases the SRF to values around or even below 20 MHz. The flatness of M vs. frequency will be discussed in **Section 3.5.1**.

As illustrated in **Fig. 3.5** the BW of the HF sensors is limited to values below their SRF. Therefore, the impedance of the coils is measured with a precision impedance analyzer (Keysight E4991B [117]) to determine the SRF and the self-inductance L_2 of each prototype. **Fig. 3.12** shows the self-

impedance measurements of the PUCs in comparison with the sense winding of the IVS described in **Section 3.2** and **Table 3.2** lists the numerical values for the SRF and L_2. Clearly, the conventional Rogowski coil has the highest $L_2 = 2.32\,\mu\text{H}$ due to its high number of turns. PUC C has the lowest number of turns and the lowest area per turn ($w_{\text{coil}} \cdot l_{\text{coil}}$) and hence has the lowest $L_2 = 320\,\text{nH}$. Additionally, numerical results for the coupling capacitance C_c between primary and secondary side are given. As expected, the coplanar arrangement (PUC C) has the highest C_c. Compared to the IVS with a SRF of around $f_{0,\text{sense}} = 17\,\text{MHz}$, an improvement up to a factor 12 is achieved with the PUCs. In alignment with L_2, the conventional Rogowski coil has the lowest SRF of $f_{0,\text{Rog}} = 58\,\text{MHz}$ whereas PUC C achieves the highest SRF of $f_{0,\text{PUC,C}} = 202\,\text{MHz}$. Given the similar dimensions and the similarity of their structures, PUC A and B have almost identical coil impedances and an SRF of $f_{0,\text{PUC,A}} = f_{0,\text{PUC,B}} = 105\,\text{MHz}$. However, thanks to the smaller surface of the main track C_c is lower for PUC B. **Table 3.2** further lists the ratio M/L_2, which is a measure for the magnetic coupling coefficient of each arrangement. A higher value thereby means, that the desired quantity M (an indicator for the measurement sensitivity) is large compared to the undesired quantity L_2 (an indicator for the SRF). For PUC C this ratio is almost a factor of 10 better compared to the conventional Rogowski coil, which results in a much higher SRF for the same sensitivity (better coupling).

3.5 Experimental Verification

The extension of the BW of a commercial Hall-effect current sensor by means of a PCB integrated Rogowski coil/PUC using the combiner circuit presented in **Section 3.3** is experimentally verified in frequency and time domain. Furthermore, the results are compared with measurements using the IVS and the CT from [86] with the combiner circuit summarized in **Section 3.2**. To maximize the BW of the conventional Rogowski coil and the PUCs, the two integrator resistors R are placed directly at the coil terminals [110]. In this way, the additional capacitance of the connection to the combiner circuit does not lower the SRF.

3.5.1 Frequency Response

The small-signal frequency response is measured using a network analyzer (Omicron Lab Bode 100 [118]) with the setup shown in **Fig. 3.13**. A stimulus current $i = 1\,\text{A}$ (peak-to-peak) is injected into the sensor under test with the help of a Power Amplifier (PA) to boost the network analyzer's output signal. The network analyzer determines the sensor TF by comparing the

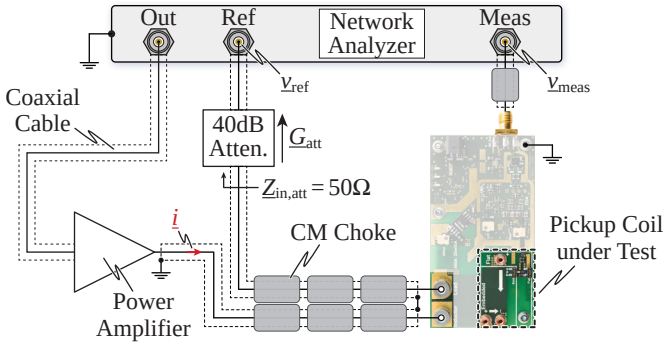


Fig. 3.13: Setup for the frequency response measurements.

sensor output $\underline{v}_{meas}$ with a reference measure $\underline{v}_{ref}$ obtained with a precision 50 Ω 40 dB high-power Radio-Frequency (RF) attenuator (apitech/Weinschel 58-40-33 [119]). In fact, the RF attenuator behaves like a coaxial shunt, which provides a fixed load impedance of 50 Ω for the PA. The measured TF $\underline{G}_{meas}$ is then

$$\underline{G}_{meas} = \frac{\underline{v}_{meas}}{\underline{v}_{ref}} = \frac{\underline{v}_{meas}}{\underline{i} \cdot \underline{Z}_{in,att} \cdot \underline{G}_{att}} = \frac{\underline{G}_{tot}}{\underline{Z}_{in,att} \cdot \underline{G}_{att}} \tag{3.11}$$

from which the total sensor TF $\underline{G}_{tot} = \underline{v}_{meas}/\underline{i}$ can be calculated if the attenuator's input impedance $\underline{Z}_{in,att}$ and attenuation factor $\underline{G}_{att}$ are known. All connections are made using coaxial cables with Common Mode Chokes (CMCs) placed around to prevent circulating ground currents at high frequencies.

Tab. 3.3: Key performance parameters of the frequency response of all compared sensors. n.a. = not applicable.

Sensor	f_x	$f_{45°,x}$	f_{int}	f_{filt}
Hall only	1.4 MHz	490 kHz	n.a.	n.a.
Hall + Sense	10 MHz	8.2MHz	350 Hz	15.2 kHz
Hall + CT	35 MHz	16.5 MHz	1 kHz	24.5 kHz
Hall + Rog.	28 MHz	47 MHz	19 kHz	n.a.
Hall + PUC A	> 50 MHz	30.5 MHz	19 kHz	n.a.
Hall + PUC B	> 50 MHz	33 MHz	19 kHz	n.a.
Hall + PUC C	> 50 MHz	39 MHz	19 kHz	n.a.

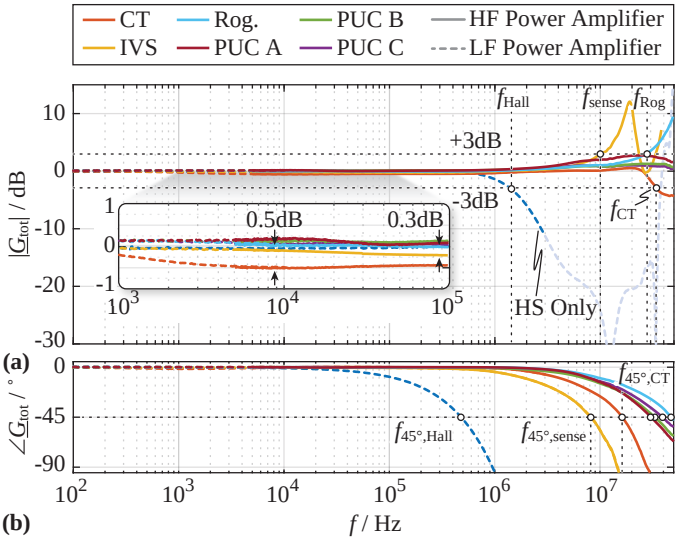


Fig. 3.14: Frequency response measurements of the Hall sensor alone (blue), the BW extension with IVS and CT investigated in [86] (yellow and red) and the conventional Rogowski coil + the proposed PUCs (cyan, dark red, green and purple). Measurements are performed with a LF PA for the lower frequency range (dashed lines) and a RF PA for the higher frequency range (continuous lines).

Fig. 3.14 shows the measured normalized TFs of the Hall sensor alone (blue), the Hall sensor extended with the CT (orange), the IVS (yellow), a conventional Rogowski coil (cyan), PUC A (dark red), PUC B (green) and PUC C (purple). A LF PA (Iwatsu IE-1125B [120]) for frequencies up to 3 MHz (dashed lines) and a RF PA (AR 150A100D [121]) for frequencies between 5 kHz and 50 MHz (continuous lines) are used. **Table 3.3** lists the exact configuration of the HF sensors and the achieved BW, where f_x denotes the −3 dB point and $f_{45°,x}$ the frequency at which the phase is shifted by −45°. It has to be noted that the frequency response includes the phase-shift of the utilized cables and the RF attenuator, hence the displayed phase-shift is larger than the one of the current sensor alone. A manual correction is not performed here, since in a practical application this is usually not possible as well. Therefore, the $f_{-45°}$ values listed in **Table 3.3** are conservative estimates.

Due to the low SRF, the conventional Rogowski coil as well as the IVS have the lowest BW, which is in accordance with the impedance measurements (cf. **Fig. 3.12**). The peaking due to the SRF is already visible in both cases,

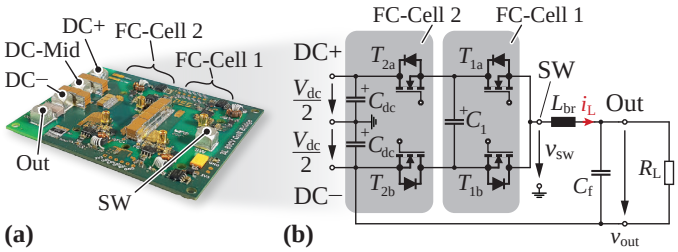


Fig. 3.15: (a) Hardware demonstrator of a single three-level branch of the GaN *3L3* AC power source and **(b)** the corresponding schematic diagram of the configuration for dc/dc operation with $V_{dc} = 600\,V$ (split dc link) and an output load referred to the negative dc rail.

since no damping is provided. Hence, f_x in those cases denotes the frequency at which the amplitude is +3 dB above the nominal value. The placement of a damping resistor R_d would reduce the peaking (cf. **Fig. 3.5**) but would at the same time lead to a larger phase-shift already below the SRF. The PCB integrated PUCs achieve a significantly higher BW compared to the IVS and CT, in fact the −3 dB point could not be identified with the available measurement equipment, that allows to measure up to 50 MHz. The SRF measurements in **Fig. 3.12** indicate an even higher BW (100 − 200 MHz). This proves that the compact PUCs are a very convenient solution to extend the BW of an existing LF current sensor.

With help of frequency response measurements the sensitivities of the LF and HF path can be trimmed by manually adjusting the gain G_{amp} until the sensitivity at very low frequencies ($f \ll f_{c,HF}$) equals the sensitivity at high frequencies ($f \gg f_{c,HF}$). The flatness around the combiner frequency $f_{c,HF}$ is improved by trimming the LPF. A zoomed view in **Fig. 3.14 (a)** reveals excellent flatness of the TF (< 0.3 dB, i.e., < 3.5 % for all sensors except the CT). Therefore, the variation of M versus frequency in the PUCs (dM_f) is generally very low. It is, however, visible that PUC A in accordance with the calculations from **Table 3.1** shows the highest dM_f.

3.5.2 Time-Domain Behavior

To verify the time-domain behavior, a hardware demonstrator of one three-level branch of the GaN 3L3 ac power amplifier with $V_{dc} = 600\,V$ is used in dc/dc operation to generate a reference inductor current i_L. **Fig. 3.15 (a)** and **(b)** show a picture and the circuit of the hardware demonstrator, which is supplied with a split dc link $V_{dc}/2 = 300\,V$. The converter operates with a

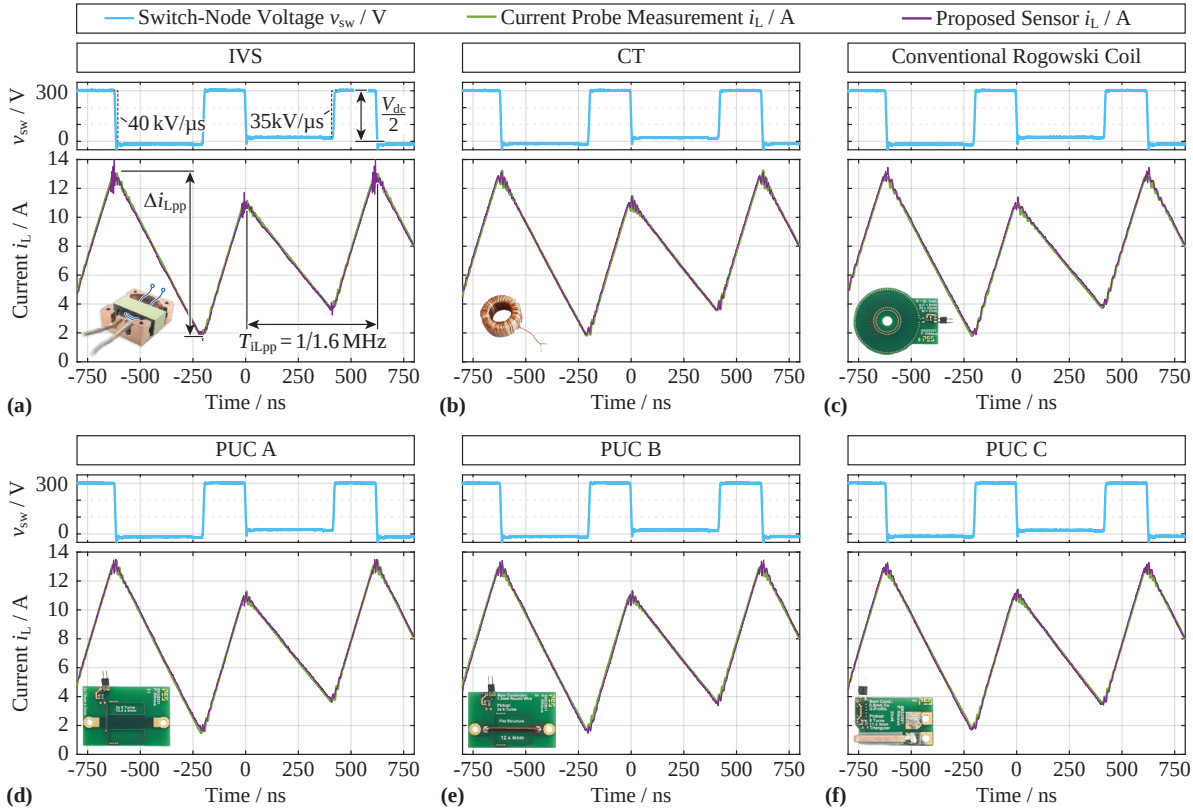


Fig. 3.16: Time-domain measurements of the switch-node voltage (cyan) and inductor current measured with a current probe (green) and the proposed sensors (purple) in one three-level branch of the *3L3*. Hall sensor extended with **(a)** the IVS, **(b)** the CT, **(c)** the conventional Rogowski coil, **(d)** the PUC A, **(e)** the PUC B and **(f)** the PUC C. The current measurements are placed *after* the output filter inductor at the converter output, hence the fast dv/dt transients have no impact.

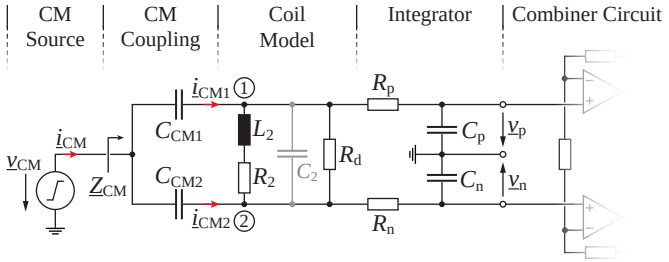


Fig. 3.17: CM equivalent circuit of the PUC with asymmetric coupling ($C_{CM1} \neq C_{CM2}$) of the CM current $\underline{i}_{CM}$ into the coil and integrator.

fixed duty-cycle of $D = 0.7$ and a switching frequency of $f_{sw} = 800\,\text{kHz}$. This results in a current ripple of $\approx 11.5\,\text{A}$ peak-to-peak at $f_{iLpp} = 1.6\,\text{MHz}$. The load resistor R_L is chosen to ensure a strictly positive i_L to obtain one Hard Switching (HSW) and one Soft Switching (SSW) transition per effective switching period T_{iLpp}. **Fig. 3.16** depicts waveforms of the resulting switch-node voltage v_{sw} (cyan) and inductor current i_L over 2.5 effective switching periods. i_L is measured with a 120 MHz BW current probe [122] (reference measurement; green) and the Hall sensor extended with **(a)** the IVS, **(b)** the CT, **(c)** the conventional Rogowski coil, **(d)** PUC A, **(e)** PUC B and **(f)** PUC C (purple curves). Both, the proposed sensor and the current probe are placed after the output filter inductor L_{br}, i.e., at the converter output, to reduce the effect of fast voltage transients at the switch-node. Evidently, all sensor concepts accurately replicate the 1.6 MHz triangular current ripple. Therefore, the BW is in all cases enough to capture the relevant harmonic content. The conventional Rogowski coil and the PUCs are in this case critically damped with a damping resistor and therefore, even for the conventional Rogowski coil with the lowest SRF, no oscillations are visible. Please note that the asymmetry in the zero-voltage of v_{sw} arises from a slight deviation of the FC voltage from the ideal value of $V_{dc}/2$.

It was verified in [86] that the Hall sensor alone is not enough to get an adequate representation of the inductor current as it shows a quasi-sinusoidal shape instead of a triangular one, too small amplitude and a large phase-shift compared to the current probe reference measurement.

3.6 Common Mode Rejection Ratio

To show the influence of CM disturbances occurring from fast switching transients ($\mathrm{d}v/\mathrm{d}t$) on the current sensor performance the measurements

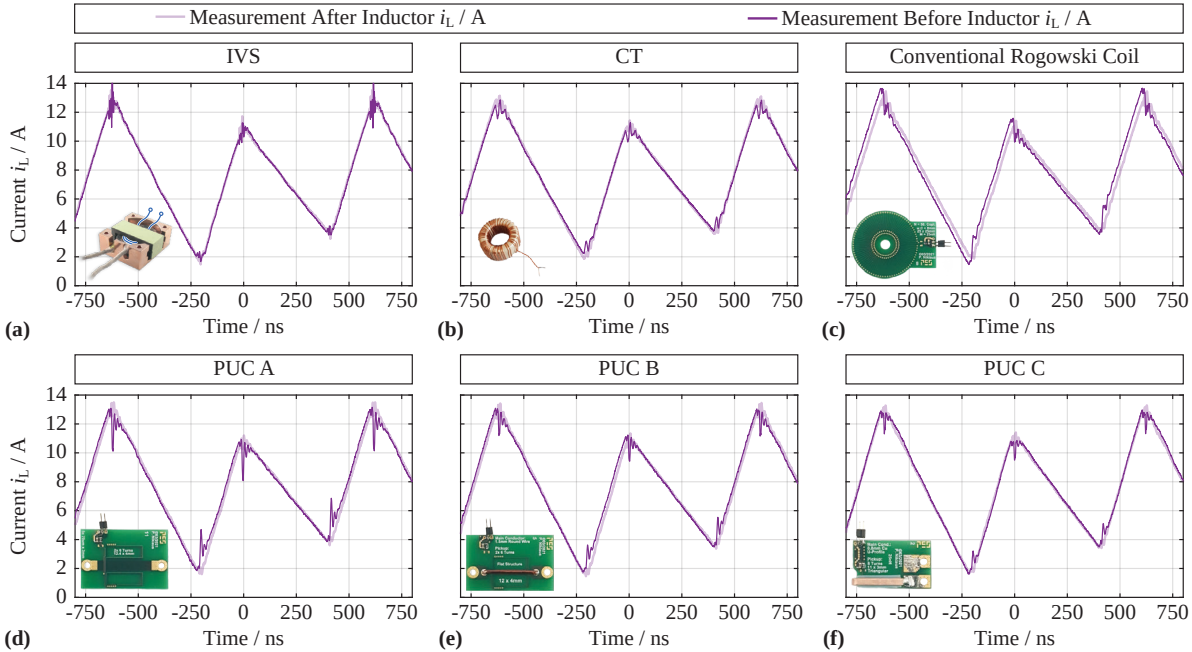


Fig. 3.18: Comparison between measurement before the inductor directly at the switch-node (purple) vs. measurement after the inductor as shown in Fig. 3.16 (light purple) for a $d\upsilon/dt$ between 35 and 40 kV/µs. Hall sensor extended with **(a)** the IVS, **(b)** the CT, **(c)** a conventional Rogowski coil, **(d)** the PUC A, **(e)** the PUC B and **(f)** the PUC C.

of **Fig. 3.16** are repeated in **Fig. 3.18**, this time with the current sensor placed *before* the output filter inductor, i.e., at the switch-node. Thereby, the current measurement is exposed to the full $\mathrm{d}v/\mathrm{d}t$ of $35 - 40\,\mathrm{kV/\mu s}$ at the switch-node. Additionally, the measurements with the sensor placed after the inductor are included in light color for easier comparison. The measurements with the PUCs show distinct error peaks during the switching transitions (≈ 3 A for PUC A, $\approx$ 2 A for PUC B and ≈ 1.5 A for PUC C) as well as a small error during the rising and falling current slopes. The conventional Rogowski coil does not have distinct error peaks during the switching transitions but an increased error during the current slopes ($\approx$ 1 A). The IVS and CT measurements remain almost unaffected.

To understand the impact of CM disturbances on the measured currents, **Fig. 3.17** shows a simplified CM equivalent circuit of the measurement system. The CM voltage v_{CM} from the switching transitions is represented with a CM voltage source. The coil is modeled with L_2, R_2 and C_2 based on the lumped element equivalent circuit (cf. **Fig. 3.4 (d)**). Additionally, the damping resistor R_{d} is included. The differential integrator giving the voltages $\underline{v}_{\mathrm{p}}$ and $\underline{v}_{\mathrm{n}}$ is formed with two *RC* low-pass filters (R_{p}, C_{p} and R_{n}, C_{n}), which are nominally identical. Given the fully differential realization a superior CMRR would be expected. However, four effects with a detrimental impact on the rejection of such CM disturbances are identified:

i) The CM impedance $\underline{Z}_{\mathrm{CM}}$ that determines the total CM current $\underline{i}_{\mathrm{CM}}$ for a given $\underline{v}_{\mathrm{CM}}$. A high $\underline{Z}_{\mathrm{CM}}$ results in a low $\underline{i}_{\mathrm{CM}}$ and therefore in lower distortions. Assuming a perfectly matched integrator, i.e., $R_{\mathrm{p}} = R_{\mathrm{n}} = R$ and $C_{\mathrm{p}} = C_{\mathrm{n}} = C$, $\underline{Z}_{\mathrm{CM}}$ is given by

$$\underline{Z}_{\mathrm{CM}} = \frac{s \cdot \frac{R}{2} \cdot \frac{C_{\mathrm{c}} \cdot 2C}{C_{\mathrm{c}} + 2C} + 1}{s \cdot \frac{C_{\mathrm{c}} \cdot 2C}{C_{\mathrm{c}} + 2C}} \overset{2C \gg C_{\mathrm{c}}}{\approx} \frac{R}{2} + \frac{1}{s \cdot C_{\mathrm{c}}}, \tag{3.12}$$

with the coupling capacitance C_{c} between primary and secondary side (cf. **Fig. 3.4**). The values of C_{c} for the Rogowski coil/PUCs are listed in **Table 3.2**. For the IVS it corresponds to 6.5 pF.

ii) As an approximation the coupling capacitance C_{c} can be split into two capacitances C_{CM1} and C_{CM2} that couple the CM disturbance into both coil terminals ① and ②. The ratio $C_{\mathrm{CM1}}/C_{\mathrm{CM2}}$ depends on the layout. Consequently, the total CM current $\underline{i}_{\mathrm{CM}} = \underline{v}_{\mathrm{CM}}/\underline{Z}_{\mathrm{CM}}$ divides in two parts $\underline{i}_{\mathrm{CM1}}$ and $\underline{i}_{\mathrm{CM2}}$, which leads to an inherent asymmetry if $C_{\mathrm{CM1}} \neq C_{\mathrm{CM2}}$.

iii) The differential integrator is not perfectly matched, hence even for symmetrical distribution of the CM current the two voltages $\underline{v}_\mathrm{p}$ and $\underline{v}_\mathrm{n}$ are not equal. Thus a CM to Differential Mode (DM) conversion occurs.

iv) $\underline{v}_\mathrm{p}$ and $\underline{v}_\mathrm{n}$ are composed of a CM and a DM component. They lead to a CM excitation of the subsequent differential combiner circuit. The operational amplifiers only have a finite CMRR, mainly limited by the matching of the feedback network [123], hence there is a CM-to-DM conversion.

A distortion of 1 A corresponds to only 3.6 mV after the integrator for $f_\mathrm{int} = 19\,\mathrm{kHz}$ and $M = 30\,\mathrm{nH}$. With a CM voltage of 300 V this results in a CMRR of almost 100 dB, i.e., $1:100'000$. With error voltages that low, the distortions visible in **Fig. 3.18** for the conventional Rogowski coil and the PUCs cannot be broken down any further to assign certain error components to one of the above listed effects. Nevertheless, the different approaches can be compared qualitatively. Of particular interest is the comparison between the IVS and the Rogowski coil/PUCs because they rely on the same operational principle. The distortions are caused by the flowing $\underline{i}_\mathrm{CM}$ and are independent of the selected coil arrangement. Assuming equal $\underline{Z}_\mathrm{CM}$ in all cases, the CM distortions should be identical. For the IVS, however, there is a significantly improved Signal-to-Noise Ratio (SNR) due to the higher mutual inductance M ($\approx 2.1\,\mu\mathrm{H}$ compared to $\approx 30\,\mathrm{nH}$). Please note that noise in this context refers to the adverse CM distortion. Therefore, the same absolute CM distortion naturally has a lower effect. A further consequence of the high coupling is the lower integrator corner frequency f_int that can be selected for the same measurement sensitivity (cf. (3.6)). To maximize $\underline{Z}_\mathrm{CM}$ for a given C_c, i.e., minimize $\underline{i}_\mathrm{CM}$, R is ideally chosen as large as possible (cf. (3.12)). Consequently, for a given f_int, C reduces to small values. The lower limit for C is obtained by the CM voltage excitation of the amplifier inputs. Assuming a perfectly matched integrator, the CM excitation of the operational amplifiers is

$$\underline{v}_\mathrm{CM,amp} = \underline{v}_\mathrm{CM} \cdot \frac{C_\mathrm{c}}{C_\mathrm{c}+2C} \cdot \frac{1}{1+s\cdot\frac{R}{2}\cdot\frac{C_\mathrm{c}\cdot 2C}{C_\mathrm{c}+2C}}. \tag{3.13}$$

The step response of (3.13) has a steady-state value of $v_\mathrm{CM,amp,0} = v_\mathrm{CM} \cdot \frac{C_\mathrm{c}}{C_\mathrm{c}+2C}$. To prevent saturation of the amplifiers, $v_\mathrm{CM,amp,0}$ must be below the maximum allowed amplifier input voltage. With the worst-case value $C_\mathrm{c} = 6.5\,\mathrm{pF}$ (IVS) and a CM voltage of 400 V, C must be larger than 1.5 nF to confine $v_\mathrm{CM,amp,0}$ to values below 0.9 V (limit for the considered amplifier with ±2.5 V supply [111]). Given the minimum required C it is obvious that a lower f_int results in a higher R and thus a lower CM current i_CM. Eventually, this means a lower CM error

due to effects ii) to iv) as listed above. Currently, the integrator is realized with $R = 75\,\mathrm{k\Omega}$ and $C = 6\,\mathrm{nF}$ for the IVS and with $R = 5.6\,\mathrm{k\Omega}$ and $C = 1.5\,\mathrm{nF}$ for the Rogowski coil/PUCs. With the C_c values listed in **Table 3.2**, C could be slightly reduced to achieve a better CMRR without exceeding the maximum amplifier input voltage.

As a conclusion, the IVS, despite having the largest coupling capacitance C_c, has a significantly better CMRR thanks to the higher SNR and thanks to the lower f_int due to its substantially higher mutual inductance. The differences between the Rogowski coil/PUCs are very small and can be qualitatively explained with the effects ii) to iv) as listed above.

The CT is terminated with a very low-ohmic burden resistor R placed symmetrically to ground ($R/2$ from each terminal to ground). Given the very close matching of the two burden resistors, there is almost no CM-to-DM conversion occurring and the CM voltage at the amplifier inputs is very low. Furthermore, the CT can be shielded very effectively, which provides a very low impedance path for the CM current that is independent of the evaluation circuit input stage.

As a final remark it has to be mentioned that inductor current measurements are normally placed after the inductor exactly to prevent disturbing the signal with high $\mathrm{d}v/\mathrm{d}t$ transients. In this case all presented sensors are suitable for the high-BW current measurements.

3.7 Comparative Evaluation and Discussion

Table 3.4 shows a comparative evaluation of different designs presented in the literature and the investigated designs in this chapter. Only the best performing PUC (PUC C) is included. Different criteria such as BW, dc capability, mutual inductance M (for Rogowski based sensors), size, $\mathrm{d}v/\mathrm{d}t$-immunity and realization effort are considered. The size includes only the sensor part without processing electronics. In industrial applications more and more functionalities are fully integrated and thus the processing electronics can be realized very compact. PUC C has the highest BW of all dc-capable sensors and particularly outperforms the similarly operating sensor in [106] (higher BW, smaller size thanks to the PCB realization). The CT based design of this chapter outperforms [99] and [101] in terms of BW and realization effort (the latter are more complex in realization due to the gapped magnetic core) with a similar size. The CT realization in [105] utilizes only commercial components and has a low realization effort. However, it has the lowest BW and the compact size is only possible due to the small current range of max. ±20 A. Therefore, this solution is not applicable for the target application. As shown before, CT based designs generally have better $\mathrm{d}v/\mathrm{d}t$-immunity compared to

Tab. 3.4: Comparative evaluation of the investigated designs in this chapter (bold) and solutions presented in literature regarding BW, dc capability, mutual inductance M, sensor size (including the Hall element or the commercial Hall-effect Current Sensor (CS) in case of dc-capable solutions), dv/dt-immunity (qualitative; with voltage step and slope, if specified) and realization effort (qualitative). The results are grouped by dc capability and sorted by descending BW. Please note that a BW determined by simulation or calculation is indicated with † and a BW determined from the ringing in the measured waveform is indicated with ‡. n.a. = not applicable.

Ref.	BW (MHz)	dc capable	M (nH)	Coil Size / Sensor Volume (mm^2 / mm^3)	dv/dt-Immunity	Realization Effort
PUC C	**> 50**	**yes**	**30**	**11 × 11 × 3 (Hall CS)** **17 × 4 × 3 (PUC)**	**– (300V@40kV/µs)**	**++**
CT	**35**	**yes**	**n.a.**	**11 × 11 × 3 (Hall CS)** **13 × 13 × 7 (CT)**	**+ (300V@40kV/µs)**	**–**
IVS	**10**	**yes**	**≈ 2100**	**11 × 11 × 3 (Hall CS)**	**++ (300V@40kV/µs)**	**+**
[106]	≈ 30†	yes	≈ 10	≈ 3 × 2 × 1 (Hall element) ≈ 40 × 40 × 2 (coil)	not specified	+
[99]	30	yes	n.a.	18 × 10 × 8 (incl. Hall element)	+ (100V@16kV/µs)	– –
[101]	20	yes	n.a.	20 × 20 × 7 (incl. Hall element)	+ (350V@16kV/µs)	– –
[105]	5	yes	n.a.	≈ 6 × 5 × 2 (Hall CS) ≈ 9 × 8 × 6 (CT)	not specified	++
[114]	355†	no	2.3	≈ 4 × 4	not specified	++
[112]	333‡	no	0.1	≈ 6 × 0.1	not specified	++
[113]	225†	no	0.1	≈ 10 × 3	not specified	++
[116]	100†	no	10.7	≈ 8 × 8	not specified	++
[112]	93‡	no	0.9	≈ 6 × 0.8	not specified	++

Rogowski based designs. One exception is the IVS, which thanks to its very high coupling and low corner frequency has the best immunity, requires no additional volume for the sensor but at the same time has the lowest BW. The IVS proposed in this chapter is only applicable if a dedicated custom-made filter inductor with accessible core to place the sense winding is used.

Rogowski based pickup coil sensors without dc capability are not feasible for the desired application but are still included in **Table 3.4** (lower part), since they serve as basis for the investigated PUCs. On the one hand, they achieve a very high BW and are highly compact with minimal realization effort (no magnetic elements, no Hall sensor) but on the other hand they typically have low values of M (a factor of 3 to 300 lower than the PUCs in this chapter). This is expected, since a high BW means low self-impedance and therefore small dimensions and/or a low number of turns. For a given measurement sensitivity in V/A a low M requires a high ω_{int}, which is problematic in case of desired dc capability, since eventually the condition $f_{\text{Hall}} \gg f_{\text{int}}$ is violated, which leads to deviations in the frequency response. Moreover, the BW of these designs is not measured directly but determined with FEM simulations or calculated based on self-impedance measurements. As summarized in **Table 3.2** the PUC designs presented in this chapter have SRFs between 100 and 200 MHz (extracted from self-impedance measurements), which indicates a BW > 50 MHz while having a much higher M.

In summary, the presented concepts exceed the performance of previously shown solutions in the literature especially concerning BW and manufacturability. A HF extension with PUC C is recommended if maximum BW and lowest realization effort is desired. The CT is advantageously used if a high $\mathrm{d}v/\mathrm{d}t$-immunity is required. In case of a physically present filter inductor with the possibility to add the sense winding the IVS is suggested, since it requires the lowest volume and has a superior $\mathrm{d}v/\mathrm{d}t$-immunity.

3.8 Conclusion

This chapter analyzes approaches to extend the Bandwidth (BW) of a commercially available Low-Frequency (LF) Hall-effect current sensor beyond 10 MHz. The aim is to implement a wideband current measurement for closed-loop control of an Ultra-High Bandwidth Power Amplifier (UHBWPA) with an effective switching frequency $f_{\text{sw,eff}} = 4.8$ MHz realized as Three-Level Triple-Interleaved (3L3) Flying Capacitor Converter (FCC) employing Wide-Bandgap Gallium-Nitride (GaN) power semiconductors.

In [86], two High-Frequency (HF) current sensors to be used in combination with a Hall-effect current sensor are presented. First, an already present output filter inductor is equipped with an additional sense winding to obtain

the inductor current by integration of the inductive voltage drop (*Isolated Inductor Voltage Sensing (IVS)*). No additional volume for the HF sensor is required in this case. Second, a small Current Transformer (CT) with an ungapped toroidal iron powder core is used to measure the HF current, while at the same time it can handle the dc/LF bias due to the LF current. It contributes a volume of approximately 1.2 cm^3. In both cases, the secondary windings have to be manually wound, which complicates the manufacturing and makes it difficult to achieve reproducible results in practice, since the parasitic elements, which mainly define the HF performance, are difficult to control. This chapter furthermore presents highly compact Printed Circuit Board (PCB) integrated HF sensors based on a conventional circular PCB integrated Rogowski coil as alternative BW extension concepts. Compared to the IVS and CT and advantageous in industrial applications, the manufacturability of PCB integrated components is significantly improved and the parasitics are tightly controlled.

Based on previous research in the literature, three Pickup Coil (PUC) geometries that offer a high magnetic coupling per area and low self parasitics are built and compared to the conventional Rogowski coil. A coil size as low as 17 mm × 3.5 mm (HF sensor volume ≈ 0.2 cm^3) is achieved. The transition between LF and HF current sensors is realized with a fully-differential combiner circuit whose signal processing electronics occupies only 22 mm × 25 mm.

Comprehensive experimental verification with a hardware demonstrator of a single bridge leg of the *3L3* proves that all investigated concepts accurately represent the 1.6 MHz triangular current ripple. The BW of the three PUC geometries exceeds 50 MHz whereas the conventional Rogowski coil achieves 28 MHz due to its low Self-Resonance Frequency (SRF). Compared to the IVS and CT, which reach a BW of 10 MHz and 35 MHz respectively, a substantial improvement is possible with the PUCs.

In a final step, the immunity of all six investigated concepts to Common Mode (CM) disturbances (Common Mode Rejection Ratio (CMRR)) resulting from fast dv/dt transients is analyzed. Compared to the Rogowski coil and the PUCs, the IVS shows superior CMRR. It has to be emphasized, however, that the occurring error in the Rogowski coil/PUC current measurement signals corresponds to an error voltage in the mV range. With several hundred volts of CM voltage, still a CMRR of almost 100 dB is achieved. With the obtained results, the IVS is suggested for current measurements in a dedicated output filter inductor if there is the possibility to access the core to place the sense winding and if the BW of 10 MHz is acceptable because it requires no additional volume for the sensor and it offers a high CMRR. In other cases, either the CT or the PUCs are suitable and the choice depends on a trade-off between required BW, space requirements, CMRR, manufacturability and

realization effort. If maximum BW is desired, the PUCs are preferably selected. Comparing the three PUC designs, PUC C outperforms PUC A and PUC B in all considered performance criteria (BW, volume, CMRR) and should therefore be preferred.

4

High-Bandwidth Isolated Voltage Measurements with Very High Common Mode Rejection Ratio

This chapter summarizes the most relevant findings regarding high-bandwidth galvanically isolated (floating) voltage measurements with very high Common Mode Rejection Ratio (CMRR), which are also published in:

- **P. S. Niklaus**, R. Bonetti, C. Stäger, J. W. Kolar, and D. Bortis, "High-Bandwidth Isolated Voltage Measurements with Very High Common Mode Rejection Ratio for WBG Power Converters," *IEEE Open Journal of Power Electronics,* vol. 3, pp. 651-664, September 2022.

Chapter Abstract

Galvanically isolated voltage measurements are becoming increasingly important in the characterization of converter systems with fast switching Wide-Bandgap (WBG) semiconductors. A very high Common Mode Rejection Ratio (CMRR) of > 80 dB for frequencies up to several tens of MHz is required to accurately measure, e.g., the high-side gate-source or drain-source voltage in a half-bridge, or voltages on floating potentials as, e.g., found in multi-level converters. Common to all listed measurement scenarios is the fast changing reference potential, which acts as Common Mode (CM) disturbance. This chapter derives the minimum necessary CMRR at different frequencies to constrain the time-domain measurement error below a certain limit. Thereby, only the switched voltage and the transition rate ($\mathrm{d}v/\mathrm{d}t$) of the CM disturbance are to be considered and not the actual converter switching frequency f_{sw}. Afterwards, a galvanically isolated measurement system with a CMRR > 100 dB up to 100 MHz and an analog measurement Bandwidth (BW) of 130 MHz is presented. Critical design aspects to achieve this performance are investigated. Compared to commercially available isolated voltage probes, the presented system does not require any additional equipment like an oscilloscope to perform and visualize measurements, since the data is already digitized/sampled and thus can be transmitted directly to a host device (e.g., computer or monitoring system) with corresponding graphical user interface software. Experimental verification in the frequency- and the time-domain confirms that the performance is on par with or even exceeds the best commercially available isolated voltage probes.

4.1 Introduction

Power electronic converter systems with Wide-Bandgap (WBG) semiconductors are key to achieve ever higher efficiencies and power densities, enabling cost-, volume- and weight-efficient conversion of energy within the electrical and/or between electrical and mechanical domain. The very fast switching transitions (high $\mathrm{d}v/\mathrm{d}t$) associated with the use of WBG semiconductors help to minimize the semiconductor losses occurring during Hard Switching (HSW) [48, 74]. As shown, e.g., in [124], the fast switching transitions demand a significantly increased measurement Bandwidth (BW) up to several hundred MHz to measure the signals of interest, e.g., the Drain-Source (DS) and/or Gate-Source (GS) voltages. Therefore, high-performance measurement tools are required to accurately characterize and verify correct operation. In

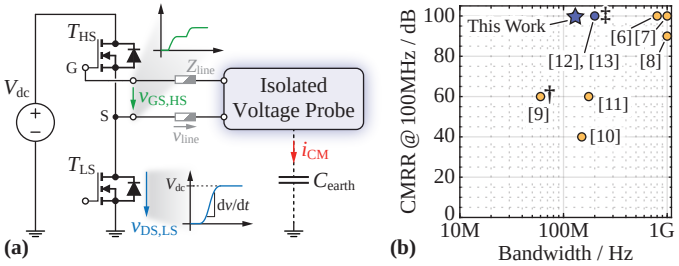


Fig. 4.1: (a) High-Side (HS) Gate-Source (GS) voltage ($v_{GS,HS}$) measurement in a half-bridge with a galvanically isolated voltage probe/measurement system. Indicated is the fluctuating/jumping Common Mode (CM) voltage $v_{DS,LS}$ and the parasitic coupling capacitance C_{earth} towards Protective Earth (PE). **(b)** Different commercially available isolated voltage probes (yellow dots; require an additional, typically vendor-specific oscilloscope) and measurement systems (blue dots; no additional measurement equipment needed) with their reported Bandwidth (BW) and Common Mode Rejection Ratio (CMRR) at 100 MHz. The solution presented in this chapter is marked with ★. Please note that the probes/systems marked with ‡ and † report the CMRR at only 50 MHz and 60 MHz, respectively.

addition, certain measurements have to be performed on floating reference potential, e.g., in multi-level/multi-cell converters [27], that is, the reference potential of the voltage to be measured differs from the reference potential of the measurement equipment (e.g., the oscilloscope), which is typically referred to Protective Earth (PE). Furthermore, isolation between different measurement channels is required when various measurements, all with different reference potential, are performed simultaneously. The scaling of the area-specific on-state resistance with device blocking voltage renders series connection of multiple Low-Voltage (LV) transistors attractive to achieve a certain overall blocking voltage [48]. Thereby, the knowledge of static and/or dynamic device DS voltage sharing, which due to the series connection requires floating low parasitic capacitance measurements, is very important to prevent failures due to overvoltage [125].

From the above listed measurement scenarios, the most critical example is the floating measurement of the High-Side (HS) switch GS voltage $v_{GS,HS}$ between 'G' and 'S', shown in **Fig. 4.1 (a)**, characterized by a relatively small desired *Differential Mode (DM)* voltage (range of several volts to tens of volts) that is measured referred to a floating reference potential in the range of several hundred volts to kilovolts, which acts as *Common Mode (CM)* voltage. This type of measurement is essential to fully characterize the Gate Driver (GD) circuits and the switching transitions, e.g., to verify

the correct dead time, the absence of any cross-conduction (both devices simultaneously turned on during a short period of time, e.g., due to parasitic turn-on during high $\mathrm{d}v/\mathrm{d}t$ transitions in combination with low threshold voltage devices), correct current and voltage commutation, overshoot below certain limits and sufficient damping of potential ringing after the switching transitions [124, 134].

In general, the floating measurement reference potential is not steady but fluctuating, i.e., (abruptly) changes its value over time. In the example of the $v_{\mathrm{GS,HS}}$ measurement, the fluctuating reference potential (CM voltage) is the DS voltage $v_{\mathrm{DS,LS}}$ of the Low-Side (LS) transistor. $v_{\mathrm{DS,LS}}$ is referred to PE and transitions between 0 V and V_{dc} with a certain voltage transition rate $\mathrm{d}v/\mathrm{d}t$, which in case of WBG semiconductors can easily exceed 100 kV/µs. It is of utmost importance to minimize (or ideally eliminate) the influence of this CM *disturbance* on the measurement. The ability of a floating measurement system to attenuate/eliminate the impact of unwanted CM disturbances relative to transferring the desired DM measurement signal ($v_{\mathrm{GS,HS}}$ in this case) is characterized with the *Common Mode Rejection Ratio (CMRR)*, i.e., the ratio of DM attenuation/gain $\underline{A}_{\mathrm{DM}}$ to CM attenuation/gain $\underline{A}_{\mathrm{CM}}$, defined as

$$\mathrm{CMRR} = \left| \frac{\underline{A}_{\mathrm{DM}}}{\underline{A}_{\mathrm{CM}}} \right| . \tag{4.1}$$

Thereby, $\underline{A}_{\mathrm{x}}$ denotes a complex quantity (phasor) with amplitude and phase information and $|\underline{A}_{\mathrm{x}}|$ the absolute value thereof. As will be explained in more detail later, the CMRR typically shows a pronounced frequency dependency, i.e., becomes worse at elevated frequencies above some MHz. In combination with fast CM transients, which generate CM disturbances in the High-Frequency (HF) range, this represents a major challenge for measurement systems.

With the emergence of Insulated-Gate Bipolar Transistors (IGBTs) in the 1990s with comparably faster and larger amplitude switching transitions (multiple kV/µs) compared to back then state-of-the-art Bipolar Junction Transistors (BJTs) and Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), accurate characterization of the GD circuits became ever more important. Thereby, it is necessary to use probes with a high CMRR over a wide frequency range (up to several MHz), as shown, e.g., in [135], where a CMRR of 60 dB at 10 MHz is achieved with an optically isolated measurement system. It will be thoroughly analyzed in this chapter that the requirements on measurement equipment are much more stringent with today's WBG semiconductor technologies. With a $\mathrm{d}v/\mathrm{d}t$ of several tens to hundreds of

kV/µs, measurement BWs of several hundred MHz and a CMRR of > 60 dB above 100 MHz are required [124].

Traditionally, High-Voltage (HV) differential probes are used to perform floating measurements on steady and/or fluctuating reference potentials, since they provide a high impedance from both measurement terminals towards PE. A fundamental disadvantage thereby is the equal attenuation of CM and DM signals by a very high ratio (100 to 1000 or even more) and the resulting low Signal-to-Noise Ratio (SNR) and measurement resolution. The desired measurement signal is essentially obtained by subtracting two large voltages, each divided down individually. A further disadvantage of HV differential probes is the typically very poor CMRR at elevated frequencies (above several MHz), limited by the amplitude and phase matching of the differential signal paths [136], which inadmissibly deteriorates the measurement in WBG converter systems as, e.g., shown in [137]. Different solutions to overcome these limitations have been proposed in literature, e.g., online or offline compensation of the CM influence on the measurement by subtraction of the resulting error in the measurement signal [138] or indirect characterization of the switching transient by integrating the measured switch current [134]. While these methods can help to improve the performance, they are complex to use and do not fully eliminate the measurement error.

Measurements with HV differential probes can be compared to electrical efficiency/loss measurements, where the occurring losses are calculated by subtraction of input and output power. A measurement error of few percent in the individual input and output power measurement can easily lead to errors of ± 100 % in the calculated losses, especially for ultra-high efficiency systems [139]. With a calorimetric measurement setup the occurring losses are directly measured with much higher precision and without information about input and/or output power. In case of floating electrical voltage measurements, a similar measurement setup/system is desired.

In contrast to HV differential probes, the usage of galvanically isolated probes offers inherent isolation of the measurement and decouples the CM and DM signal portions, thus allows to directly measure the DM signal without subtracting large CM signals (which corresponds to calorimetric efficiency measurements where independent from input/output power directly the losses are measured). A single-ended realization is feasible and therefore, the CMRR does not depend on close matching of differential signal paths. Thereby, all limitations of HV differential probes in the presented measurement scenarios are mitigated. Galvanically isolated measurements are widely used in Medium-Voltage (MV) applications and harsh environments, exposed to high noise, switching surges and interferences [140], demanding for robust measurement systems, e.g., in plasma physics experiments [141], in HV electric substations

to quantify the electromagnetic compatibility [142] or to assess the quality of the power distribution grid [143]. An optical link (analog or digital) is mostly used as isolated transmission channel [140, 141, 143] but also wireless communication channels have been investigated [144, 145].

The trend of ever higher required CMRR at elevated frequencies has been recognized by different test and measurement equipment manufacturers and there is a variety of isolated probes/measurement systems commercially available that achieve these requirements. The most important of which are shown in **Fig. 4.1 (b)**, plotted in a plane of their measurement BW and achieved CMRR at 100 MHz. The yellow dots [126–131] thereby denote *isolated voltage probes*, which require an additional, often vendor-specific (except [131]) oscilloscope to perform measurements, whereas the blue dots [132, 133] designate *isolated measurement systems*, which only require a host computer with respective Graphical User Interface (GUI) software to display the measurements. This important difference between a measurement probe and a measurement system has to be kept in mind when evaluating possible solutions from various points of view such as flexibility, ease of use and cost. Further indicated is the measurement system presented in this chapter (★).

Please note that [132] and [133] have a BW of 200 MHz but specify the CMRR only up to 50 MHz (marked with ‡ in **Fig. 4.1 (b)**), which means that at 100 MHz, approximately 10 dB less can be expected. Similarly, [129] has a BW of only 60 MHz and the indicated CMRR value is valid at 60 MHz (marked with † in **Fig. 4.1 (b)**).

4.1.1 Overview of this Chapter

The devices listed in **Fig. 4.1 (b)** all show a very high CMRR and BW performance. An important question is therefore, how much CMRR at which frequency is really required to successfully perform the desired measurements, i.e., which of the listed devices suit the task. With help of the analyses carried out in **Section 4.2**, the minimum required CMRR at different frequencies is derived to limit the time-domain measurement error below a certain threshold. It is shown that the required CMRR reduces above a frequency defined solely by the voltage transition time. Even though isolated probes/measurement systems are fully isolated from PE, their CMRR also degrades at higher frequencies. The origin of this effect is thoroughly explained and in combination with the discussion of different key aspects to design an isolated measurement system with superior HF CMRR, a possible realization is presented in **Section 4.3**. In contrast to commercially available *probes*, the presented *system* is independent of any specific oscilloscope and can directly be used to perform measurements. Influences of different external factors such as connection

to Devices Under Test (DUTs) and the usage of an auxiliary isolated Power Supply Unit (PSU) are experimentally investigated and the performance of the presented system is verified and compared with the best currently available commercial isolated probe in **Section 4.4**. Finally, **Section 4.5** concludes the chapter.

4.2 Derivation of CMRR Requirements

4.2.1 Modeling of Disturbance and Measurement Error

In power electronic converter systems, the modeling of the CM excitation is typically simplified and given by a trapezoidal switched voltage v_{sw}, e.g., the DS voltage $v_{\mathrm{DS,LS}}$ of the LS switch in a half-bridge (cf. **Fig. 4.1 (a)**). Thereby, a constant voltage transition rate $\mathrm{d}v/\mathrm{d}t$ is assumed, mainly determined by the utilized semiconductor technology, e.g., 100 kV/µs for Gallium-Nitride (GaN) power semiconductors. The transition time t_{s} then results from the amplitude V_{dc} of the switched voltage v_{sw}.

Fig. 4.2 (a) shows the trapezoidal CM switch-node voltage $v_{\mathrm{sw}}(t)$ with pulse width t_{p} and switching frequency $f_{\mathrm{sw}} = 1/T_{\mathrm{sw}}$, transitioning between 0 V and V_{dc} (and vice versa) with a transition time $t_{\mathrm{s}} = \frac{V_{\mathrm{dc}}}{\mathrm{d}v/\mathrm{d}t}$. Its spectral representation with the spectral components $\underline{\hat{V}}_{\mathrm{sw}}(n \cdot f_{\mathrm{sw}})$ is shown in **Fig. 4.2 (c)** for two cases with equal V_{dc}, t_{p} and t_{s} but two different switching frequencies $f_{\mathrm{sw,I}}$ (case I, blue) and $f_{\mathrm{sw,II}} = 10 \cdot f_{\mathrm{sw,I}}$ (case II, orange). The spectral envelope (dashed lines) of this *disturbance voltage* has two corner frequencies f_{c1} and f_{c2}, defined as [146]

$$f_{\mathrm{c1}} = \frac{1}{\pi \cdot t_{\mathrm{p}}} = \frac{f_{\mathrm{sw}}}{\pi \cdot D} \tag{4.2}$$

$$f_{\mathrm{c2}} = \frac{1}{\pi \cdot t_{\mathrm{s}}} = \frac{\mathrm{d}v/\mathrm{d}t}{\pi \cdot V_{\mathrm{dc}}} \tag{4.3}$$

with the duty-cycle $D = t_{\mathrm{p}}/T_{\mathrm{sw}}$. The spectral envelope can be divided in three regions:

i) Constant value of V_{dc} for $f < f_{\mathrm{c1}}$,

ii) Decay with -20 dB/dec for $f_{\mathrm{c1}} \leq f < f_{\mathrm{c2}}$,

iii) Decay with -40 dB/dec for $f \geq f_{\mathrm{c2}}$.

In a practical measurement situation, the maximum tolerable peak-to-peak voltage error $\Delta v_{\varepsilon,\mathrm{pp}}$ of the actual DM measurement is typically quantified in

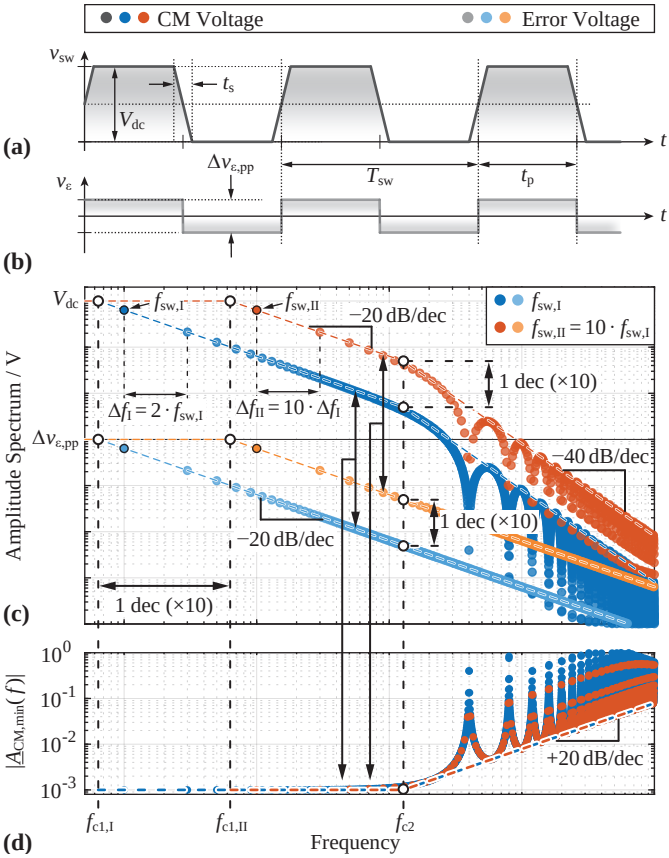


Fig. 4.2: Exemplary time-domain view of **(a)** the trapezoidal CM voltage (switch-node voltage) v_{sw} with pulse width t_p, occurring at switching frequency $f_{sw} = 1/T_{sw}$ with rise/fall times t_s and **(b)** the resulting worst-case square-shaped error voltage v_ε with peak-to-peak value $\Delta v_{\varepsilon,pp}$. **(c)** Frequency-domain representation of v_{sw} and v_ε for two switching frequencies, $f_{sw,II} = 10 \cdot f_{sw,I}$ with indicated corner frequencies $f_{c1,I}$, $f_{c1,II}$ and f_{c2}. **(d)** Resulting minimum required CM attenuation to limit the time-domain error below a certain peak-to-peak limit $\Delta v_{\varepsilon,pp}$ (1/1000 of V_{dc} in this exemplary case).

time-domain and depends on the application. In the exemplary case of the $v_{GS,HS}$ measurement, the voltage measurement range can be between several volts (e.g., ranging from −6 V to +6 V for GaN switches) up to several tens of volts (e.g., −5 V to +20 V for Silicon-Carbide (SiC) switches). Assuming, for

example, a full-scale DM measurement range of 25 V and a desired accuracy of 1 %, $\Delta v_{\varepsilon,\mathrm{pp}}$ must be below 250 mV. The worst-case *error voltage* $v_\varepsilon(t)$ that fulfills $(\max\{v_\varepsilon(t)\} - \min\{v_\varepsilon(t)\}) \leq \Delta v_{\varepsilon,\mathrm{pp}}$ is a square-shaped voltage with pulse width t_p, period T_sw and peak-to-peak value $\Delta v_{\varepsilon,\mathrm{pp}}$, i.e., the measured voltage always deviates $\pm\Delta v_{\varepsilon,\mathrm{pp}}/2$ (e.g., ±125 mV) from the real signal. Generally, this is assumed to be much worse than having the measured voltage disturbed just during the voltage transitions. It must be noted, however, that an alternative error voltage requirement allowing, e.g., only pulse-shaped errors during the switching transitions would require significantly higher Low-Frequency (LF) CM attenuation. In reality, as will be seen later (cf. **Fig. 4.9**), a high LF attenuation is typically inherently present in an isolated voltage measurement system. The square-shaped (worst-case) error voltage is shown in **Fig. 4.2 (b)** (time-domain) and **Fig. 4.2 (c)** (frequency-domain; again for two switching frequencies $f_\mathrm{sw,I}$ in light blue and $f_\mathrm{sw,II} = 10 \cdot f_\mathrm{sw,I}$ in light orange) with spectral components $\underline{\hat{V}}_\varepsilon(n \cdot f_\mathrm{sw})$. The spectral envelope is in this case composed of only two regions:

i) Constant value of $\Delta v_{\varepsilon,\mathrm{pp}}$ for $f < f_\mathrm{c1}$,

ii) Decay with −20 dB/dec for $f \geq f_\mathrm{c1}$.

The required CM attenuation of a measurement system/probe can be thought of as a filter with Transfer Function (TF) $\underline{A}_\mathrm{CM}(f)$, which attenuates the CM disturbance voltage v_sw to the error voltage v_ε [135]. Each spectral component $\underline{\hat{V}}_\varepsilon(n \cdot f_\mathrm{sw})$ of v_ε can be written as

$$\underline{\hat{V}}_\varepsilon(n \cdot f_\mathrm{sw}) = \underline{A}_\mathrm{CM}(f) \cdot \underline{\hat{V}}_\mathrm{sw}(n \cdot f_\mathrm{sw}) \tag{4.4}$$

where n is the harmonic order ($n \in \mathbb{N}$). Here, it is assumed that $\underline{A}_\mathrm{CM}$ has no phase-shift, i.e., the components $\underline{\hat{V}}_\mathrm{sw}(n \cdot f_\mathrm{sw})$ are scaled only in amplitude ($\underline{A}_\mathrm{CM} = \left|\underline{A}_\mathrm{CM}\right|$). This is a first-order approximation, since in reality there is indeed a certain phase-shift between CM disturbance and resulting error voltage. From the spectral envelopes of v_sw and v_ε, the minimum required CM attenuation $\left|\underline{A}_\mathrm{CM,min}(f)\right|$ shown in **Fig. 4.2 (d)** can be graphically determined and it shows for both exemplary disturbance signals of **Fig. 4.2 (a)** equally a constant value $A_\mathrm{CM,min,0} = \Delta v_{\varepsilon,\mathrm{pp}}/V_\mathrm{dc}$ for $f < f_\mathrm{c2}$ and rises with +20 dB/dec for $f \geq f_\mathrm{c2}$. This leads to the very important conclusion that *the minimum required CM attenuation is independent of the converter switching frequency* f_sw and depends only on f_c2, i.e., on the amplitude V_dc of the switch-node voltage v_sw and the voltage transition rates $\mathrm{d}v/\mathrm{d}t$ (cf. (4.3)).

The spectrum of v_sw of case I compared to case II starts to decay one decade earlier ($f_\mathrm{sw,I} = f_\mathrm{sw,II}/10$). Hence, for $f \geq f_\mathrm{sw,II}$ the spectral envelope of case I

is by a factor 10 lower than the envelope of case II, which could lead to the assumption that $\left|\underline{A}_{\mathrm{CM,min}}(f)\right|$ in case I compared to case II is correspondingly lower by a factor of 10. This is, however, not true because in case I, also the envelope of the maximum allowed v_ε starts to decay one decade earlier and therefore, the ratio between $\left|\underline{\hat{V}}_\varepsilon\right|$ and $\left|\underline{\hat{V}}_{\mathrm{sw}}\right|$ is the same for each occurring frequency component in both cases. An intuitive explanation is that the maximum level of distortion caused by a switching transition is independent of how often this transition repeats. An alternative way of looking at this is that in case I the spectral components of $\underline{\hat{V}}_{\mathrm{sw}}(n \cdot f_{\mathrm{sw}})$ and $\underline{\hat{V}}_\varepsilon(n \cdot f_{\mathrm{sw}})$ are indeed ten times lower than in case II but at the same time also ten times denser, i.e., $\Delta f_{\mathrm{I}} = 2 \cdot f_{\mathrm{sw,I}} = \Delta f_{\mathrm{II}} / 10$ [136]. Please note that the factor of two equals the distance between two peaks in the spectrum of the switch-node voltage for a duty-cycle of $D = 0.5$. In general, the spectral components are repeating with the respective switching frequency $f_{\mathrm{sw,\{I,II\}}}$, i.e., $\Delta f = f_{\mathrm{sw}}$, which however, does not change the previous considerations. The signal *energy* (related to the Root Mean Square (RMS) value) is the same in both cases, which intuitively explains that $\left|\underline{A}_{\mathrm{CM,min}}\right|$ has to be identical in both cases.

4.2.2 Practical Cases and Required CMRR

Knowing the operating voltage V_{dc} and the voltage transition rates $\mathrm{d}v/\mathrm{d}t$, the minimum required CM attenuation $\left|\underline{A}_{\mathrm{CM,min}}(f)\right|$ can directly be determined for a given maximum tolerable peak-to-peak time-domain measurement error $\Delta v_{\varepsilon,\mathrm{pp}}$ and therefore, a suitable measurement probe/system can be selected. Datasheets typically specify the frequency response of the CMRR referred to the input, i.e., any attenuation and/or amplification in the DM signal path is already corrected. This means, $\underline{A}_{\mathrm{DM}}$ in (4.1) is unity and the minimum required CMRR directly corresponds to the inverse of $\left|\underline{A}_{\mathrm{CM,min}}\right|$.

The minimum required CM attenuation $\left|\underline{A}_{\mathrm{CM,min}}(f)\right| = 1/\mathrm{CMRR}_{\mathrm{min}}(f)$ (expressed in dB, i.e., $\mathrm{CMRR}_{\mathrm{min,dB}} = -A_{\mathrm{CM,min,dB}}$) is shown in **Fig. 4.3** for different values of V_{dc} and $\mathrm{d}v/\mathrm{d}t$ that leads to $\Delta v_{\varepsilon,\mathrm{pp}} = 1\,\mathrm{V}$. For lower/higher admissible $\Delta v_{\varepsilon,\mathrm{pp}}$, $\left|\underline{A}_{\mathrm{CM,min}}\right|$ is simply shifted down/up. A reduction/increase of $\Delta v_{\varepsilon,\mathrm{pp}}$ by a factor of ten, for example, leads to a $-20\,\mathrm{dB}/+20\,\mathrm{dB}$ shift of $\left|\underline{A}_{\mathrm{CM,min}}\right|$. Some combinations of V_{dc} and $\mathrm{d}v/\mathrm{d}t$ found worst-case in practical converter realizations are highlighted with different colors in **Fig. 4.3**. For example, a converter with SiC semiconductors with a $\mathrm{d}v/\mathrm{d}t = 100\,\mathrm{kV/\mu s}$ and a dc link voltage $V_{\mathrm{dc}} = 800\,\mathrm{V}$, $|\underline{A}_{\mathrm{CM}}| < -70\,\mathrm{dB}$ (CMRR $> 70\,\mathrm{dB}$)

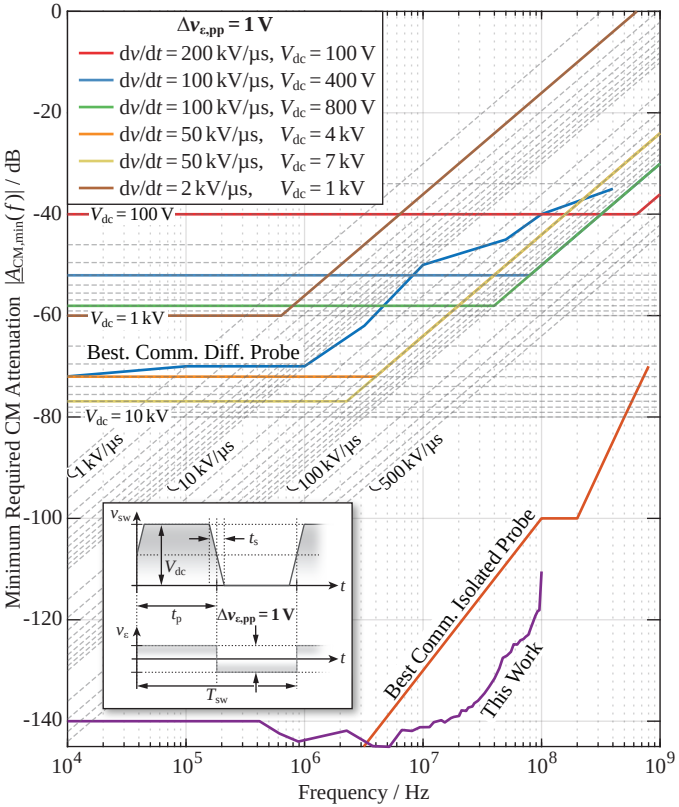


Fig. 4.3: Minimum required CM attenuation based on Fig. 4.2 to constrain $\Delta v_{\varepsilon,\mathrm{pp}}$ to 1 V peak-to-peak for different values of the dc link voltage V_{dc} and different switching transition rates $\mathrm{d}v/\mathrm{d}t$. Some typical combinations of V_{dc} and $\mathrm{d}v/\mathrm{d}t$ are highlighted with colors. For a lower/higher allowed $\Delta v_{\varepsilon,\mathrm{pp}}$ the plot can simply be shifted down/up along the y-axis (e.g., for 100 mV, 20 dB more CM attenuation is required). Further indicated are the CMRR frequency responses for the best-performing commercially available high-voltage differential probe (blue, [147]) and optically isolated probe (orange, [127]) together with the achieved CMRR of this chapter (purple).

at 100 MHz is required to constrain the time-domain measurement error below 100 mV (green line shifted down by 20 dB). Furthermore, the datasheet values for the best-performing commercially available HV differential probe (blue) and optically isolated probe (orange) as well as the solution presented in this chapter (purple) are indicated (up to their respective measurement

BW). **Fig. 4.3** clearly shows that HV differential probes are insufficient for measurements on fluctuating reference potential in WBG converters with high $\mathrm{d}v/\mathrm{d}t$ above several tens of kV/µs, even for a relatively large allowed error voltage of 1 V peak-to-peak. They are, however, sufficient in applications with lower switching transition rates, e.g., in IGBT converters with $V_{\mathrm{dc}} = 1\,\mathrm{kV}$ and $\mathrm{d}v/\mathrm{d}t = 2\,\mathrm{kV/\mu s}$ (brown curve in **Fig. 4.3**).

It has to be noted that **Fig. 4.3** indicates the absolute minimum required $\left|\underline{A}_{\mathrm{CM}}\right|$ in order to achieve the said square-shaped error voltage. In practice, galvanically isolated voltage probes achieve quasi-infinite CMRR at low frequencies, which means that the LF components are much stronger attenuated and only error pulses around the transitions of v_{sw} remain (cf. green curves in **Fig. 4.4**).

4.2.3 Reasons for Decreasing CMRR at Elevated Frequencies

A certain geometry-dependent parasitic capacitance C_{earth} is inherently formed between any galvanically isolated probe/measurement system and the steady reference potential, usually PE. Typical values are in the range of $5 - 20\,\mathrm{pF}$. A CM excitation with a certain $\mathrm{d}v_{\mathrm{sw}}/\mathrm{d}t$ results in a CM current/charging current

$$i_{\mathrm{CM}} = C_{\mathrm{earth}} \cdot \frac{\mathrm{d}v_{\mathrm{sw}}}{\mathrm{d}t}, \tag{4.5}$$

which for exemplary values of $C_{\mathrm{earth}} = 10\,\mathrm{pF}$ and $\mathrm{d}v_{\mathrm{sw}}/\mathrm{d}t = 100\,\mathrm{kV/\mu s}$ equals 1 A. This current has to flow through the connection between DUT and probe and thereby deteriorates the measurement, e.g., by generating a voltage drop v_{line} across the typically ohmic-inductive connection impedance Z_{line} (cf. **Fig. 4.1 (a)**), which without further measures translates into a measurement error. Thus, i_{CM} ultimately defines the CMRR.

Representing (4.5) in the frequency-domain means that i_{CM} increases linearly with frequency (capacitive impedance of C_{earth} is inversely proportional to f), i.e., with +20 dB/dec. In combination with the said ohmic-inductive impedance Z_{line} of the connection between DUT and probe (indicated in **Fig. 4.1 (a)**), which due to its inductive part increases with +20 dB/dec, the voltage drop v_{line} across this connection rises with +40 dB/dec. Therefore, $\left|\underline{A}_{\mathrm{CM}}(f)\right|$ of isolated measurement systems typically increases with +40 dB/dec (equivalently, the CMRR decreases with −40 dB/dec), corresponding to a second-order system.

Because the minimum required CM attenuation $\left|\underline{A}_{\mathrm{CM,min}}\right|$ rises with +20 dB/dec but the actual $\left|\underline{A}_{\mathrm{CM}}\right|$ of real isolated measurement systems rises

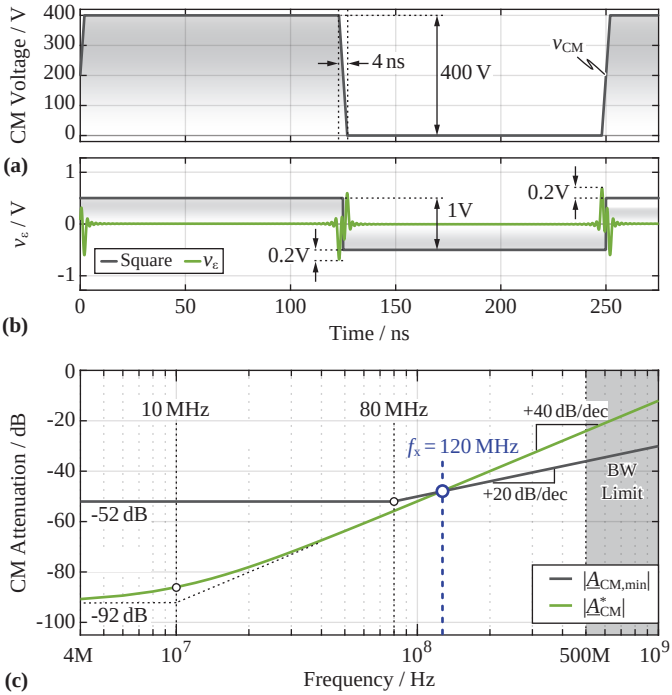


Fig. 4.4: (a) Exemplary CM disturbance with $V_{dc} = 400\,V$ and $dv/dt = 100\,kV/\mu s$. **(b)** Time-domain measurement error voltage v_ε resulting from a violation of the minimum required CM attenuation, which would result in the square-shaped error voltage (gray). **(c)** Exemplary CM attenuation frequency response that leads to v_ε in **(b)** (green), rising with +40 dB/dec after a certain corner frequency to more realistically represent the behavior of a galvanically isolated probe/measurement system.

with +40 dB/dec, there exists a certain intersection frequency f_x, above which $\left|\underline{A}_{CM}\right|$ is above $\left|\underline{A}_{CM,min}\right|$. This is exemplary shown in **Fig. 4.4** for a CM disturbance with $V_{dc} = 400\,V$, a $dv/dt = 100\,kV/\mu s$ and a maximum allowed $\Delta v_{\varepsilon,pp} = 1\,V$. The square-shaped error signal in **Fig. 4.4 (b)** is achieved with the minimum required CM attenuation $\left|\underline{A}_{CM,min}\right| = -52\,dB$ up to 80 MHz, then rising with +20 dB/dec, depicted with the gray curve in **Fig. 4.4 (c)**. Further depicted is an arbitrarily selected CM attenuation frequency response $\left|\underline{A}^*_{CM}\right|$ with a dc value of −92 dB (40 dB better than required) and a +40 dB/dec increase starting at $f = 10\,MHz$, which more accurately represents the

behavior of real isolated probes/measurement systems. The intersection of the two attenuation curves is at $f_x = 120\,\text{MHz}$. This means that spectral components below/above f_x are stronger/weaker attenuated than required, which leads to a reduction (or quasi elimination) of the steady-state value in the square-shaped time-domain error voltage but due to the weaker attenuated HF components to an increase of $\approx 0.2\,\text{V}$ during the CM voltage transitions, as indicated in **Fig. 4.4 (b)**. Therefore, in real isolated measurement systems, the time-domain error voltage v_ε due to a CM disturbance is composed of HF pulses/oscillations around the transitions of the CM voltage. If f_x lies above the desired measurement BW f_{BW} (indicated with a BW limit of 500 MHz in **Fig. 4.4 (c)**), there would be no increase of the HF components, since every spectral signal component above f_{BW} would anyway be attenuated by a filter, i.e., a too low CMRR in this frequency range is not a concern.

4.3 Practical Realization of a Galvanically Isolated Voltage Measurement System

4.3.1 Operating Principle of Existing Solutions

Having defined the required CMRR at different frequencies, this section presents a possible realization of a galvanically isolated measurement system, which in contrast to an isolated probe does not need a connection to an oscilloscope but allows to visualize and evaluate measurements directly on a host device (computer, laptop, tablet, etc.) with corresponding GUI software. Besides maximum flexibility, this is advantageous regarding total measurement equipment cost, since no oscilloscope (often vendor-specific) has to be utilized. To the author's knowledge, all commercially available isolated measurement probes and systems are realized either with a real-time analog [126–131] or digital [132, 133] optical link with a transmitter (probe head) and a receiver (part connected to the oscilloscope, usually referred to PE). Comprehensive experimental investigation has shown that any system that converts the measured signal back into the analog domain, e.g., to connect to an oscilloscope, is prone to distortions that couple into the typically PE-referred receiver side. This can be mitigated with very careful placement (long distance of ideally several meters between the probe transmitter and its receiving unit) and extensive shielding of the probe, its receiver and the oscilloscope. Only with such a *Golden Setup*, clearly unsuitable in everyday laboratory applications, it is possible to even measure/verify the indicated CMRR of $> 100\,\text{dB}$ at $f > 100\,\text{MHz}$ of some commercial probes (cf. **Fig. 4.1 (b)**).

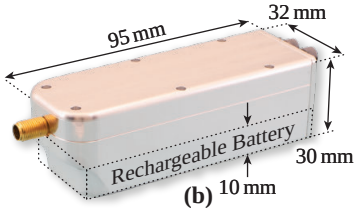
As alternative realization option it is therefore advisable to directly digitize the measurement signal with an Analog-to-Digital Converter (ADC) as close as possible to the measurement point and process/visualize the data solely in digital form in order to be less sensitive to distortions (in the analog domain, every millivolt of distortion directly impairs the measurement, whereas in the digital domain, the distortion must be several volts to cause one or multiple bits to flip and thus, to distort the measurement). The digitized data is then transmitted via an isolated channel to a host unit for visualization and processing. This can be done either in real-time or only the relevant subset of the acquired data (e.g., after a specified trigger condition) can be transmitted over a narrow-band wireless transmission channel, e.g., Bluetooth, with much lower throughput compared to a real-time link [144]. With a sampling rate of 500 Megasamples Per Second (MSPS) and a vertical resolution of 8 Bit, a real-time transmission channel would need a minimum throughput of 4 GBit/s (without any encoding scheme). Besides the more complex realization on the transmitter side and the relatively high power consumption of such high-throughput channels, additional hardware on the receiver side would be required as interface to a host device. A direct interface to the digital signal processing unit in standard oscilloscopes to directly visualize and synchronize the captured data from the isolated system together with other measurements would be a promising solution. Unfortunately, such a port is not provided on most oscilloscopes. Therefore, the *WiScope*, a battery-powered isolated oscilloscope presented in [145], uses a Bluetooth wireless data channel to connect to a host device. Thanks to the Bluetooth interface, basically any device with corresponding GUI software (computer, laptop, tablet, etc.) can act as host. It achieves an analog BW of 100 MHz and a CMRR of 100 dB up to roughly $5 - 6$ MHz, which is suitable for slow switching transitions, e.g., found in power converters featuring IGBTs. At 100 MHz, however, the CMRR reduces to $\approx$ 50 dB, which according to previously conducted analyses of **Section 4.2** is not enough for measurements with WBG converters (cf. **Fig. 4.3**).

4.3.2 Improved Measurement System

The numerous advantages regarding handling and flexibility offered by the WiScope motivate to use it as basis for the design of an improved isolated measurement system with significantly higher HF CMRR, mainly achieved with a carefully designed and very compact Analog Front-End (AFE) and with a sophisticated connection between the measurement point of the DUT and the AFE. The system specifications are listed in **Fig. 4.5 (a)** and **Fig. 4.5 (b)** shows a photo of the finalized prototype and its dimensions (further indicated is the

Parameter	Value
Input Voltage Range	±1 ... ±75 V
Bandwidth	130 MHz
Sampling Rate	400 MSPS
Vertical Resolution	8 Bit
CMRR @ 100 MHz	>108 dB

(a)



(b)

Fig. 4.5: (a) Specifications and **(b)** photo of the presented high BW isolated measurement system with superior HF CMRR, including the overall dimensions (incl. shielding enclosure + rechargeable battery).

volume occupied by the rechargeable battery accounting for approximately 1/3 of the total volume). While the BW, input voltage range, sampling rate and vertical resolution are identical to the WiScope, a CMRR of more than 100 dB at 100 MHz is achieved (improvement by several orders of magnitude).

Fig. 4.6 (a) shows a simplified circuit of the galvanically isolated voltage measurement system and **Fig. 4.6 (b)** the top-side view of the Printed Circuit Board (PCB) with the relevant building blocks highlighted. The measurement system is connected to a DUT (e.g., a half-bridge as shown in **Fig. 4.1 (a)**) with a coaxial connection cable (hereinafter denoted tip cable). A picture of the triaxial tip cable equipped with CM cores is depicted in **Fig. 4.6 (c)** (details follow below). The DM signal path is composed of a single-ended, frequency compensated input voltage divider (1 : 50 division ratio with $R_1C_1 = R_2C_2$, $R_1 = 910\,\text{kOhm}$ and $C_1 = 1\,\text{pF}$), followed by a high-impedance unity-gain buffer (Analog Devices ADA4817) acting as impedance transformer. The gain is adjusted with a Variable Gain Amplifier (VGA) (Texas Instruments LMH6574) and the signal is low-pass filtered with an Anti Aliasing Filter (AAF) (5^{th} order Butterworth filter with corner frequency $f_{\text{AAF}} \approx 130\,\text{MHz}$) before it is digitized by an ADC with a sampling rate of 400 MSPS and a vertical resolution of 8 Bit (two interleaved Texas Instruments ADC08200 with 200 MSPS each). To maximize the conversion resolution for various desired full-scale input voltage ranges, the AFE overall gain is reconfigurable with the VGA and with adjustable voltage references for the ADC. Overall, the full-scale input voltage range can be adjusted between ±0.8 V and ±50 V. A Field-Programmable Gate Array (FPGA) is the interface to a 100 kilosamples ring buffer (memory) that continuously stores the incoming sampled measurement points until at a specific trigger condition (configured on the host GUI software) the acquisition is stopped and the content of the memory is sent to the host via the Bluetooth wireless data link. With the maximum sampling rate of 400 MSPS,

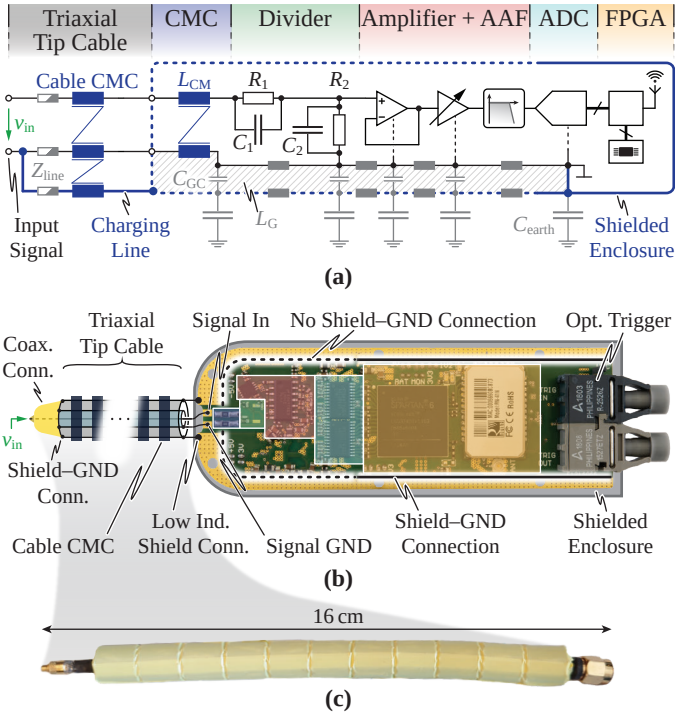


Fig. 4.6: (a) Schematic overview of the single-ended galvanically isolated voltage measurement system. The relevant parts to achieve superior CMRR at high frequencies are highlighted in blue. **(b)** Layout representation of the system with important parts highlighted and labeled. **(c)** Picture of the 16 cm long triaxial tip cable equipped with cable CM cores (cable CMCs).

measurements up to 250 µs duration can be stored. Longer measurement records can be stored with a reduced sampling rate of the ADC.

Recalling from above, the only limiting factor for the (HF) CMRR in an isolated voltage probe/measurement system is the charging current i_{CM} of C_{earth} (cf. (4.5)), leading to erroneous voltage drops across any parasitic (typically ohmic-inductive) impedances along its path (tip cable impedance Z_{line} indicated in **Fig. 4.6 (a)** or ground loop inductance on the PCB). Therefore, there are two obvious measures to improve the CMRR, i.e., minimize i_{CM}:

i) C_{earth} has to be as small as possible – according to $C_{\text{earth}} \propto A/d$, this is achieved with a very compact overall system (small surface A) and by placing the system with a certain distance d away from PE.

ii) C_{earth} has to be decoupled from the fast CM voltage transition, i.e., a certain CM impedance (e.g., Common Mode Chokes (CMCs)) must be inserted between the CM disturbance and C_{earth}.

However, i_{CM} cannot be vanished completely, hence further measures (highlighted in dark blue in **Fig. 4.6 (a)**) ensure that it flows separated from the small DM current that builds the voltage across R_2 and C_2 (desired measurement signal), and therefore, does not alter the measurement:

i) Lossy ferrite suppression cores (CM cores) placed on the tip cable form a single-turn cable CMC that provides a high CM impedance to decouple C_{earth} from the fast voltage transients (switch-node of the half-bridge), as proposed in [148, 149]. Multiple cores stacked on the full length of the cable minimize the parasitic capacitance, i.e., ensure maximum CM impedance up to HF. For fast CM transients (f_{c2} above the resonance frequency $f_{0,\text{line}}$ formed by the inductive part of Z_{line} and C_{earth}, typically in the range of a few tens to hundreds of MHz), the full CM voltage initially appears across the tip cable (and thereby across the CM cores), which could saturate the cores and vanish the CM impedance. A higher number of cores maximizes the core cross-section area and helps to minimize the risk of saturation for a given voltage. Simulation with the utilized tip cable (16 cm long and with 11 cores of type 2643480102 from Fair-Rite, depicted in **Fig. 4.6 (c)**), an assumed $C_{\text{earth}} = 10\,\text{pF}$ and a CM excitation with 10 kV reveals a worst-case peak flux-density $< 100\,\text{mT}$, which is sufficiently below the saturation flux density of the magnetic material. The occurring peak flux density is independent of the repetition rate, i.e., switching frequency, of the CM excitation. A further benefit of the CM cores is the damping of the aforementioned resonance between Z_{line} and C_{earth} by the resistive component of the resulting CM cable impedance, which otherwise could cause significant peaking in the CMRR. Note that instead of ferrite materials, the cores could also be made of nanocrystalline materials such as, e.g., Vitroperm 500F from Vacuumschmelze. The latter offer a significantly higher dc permeability ($\approx 40'000$) compared to ferrites and also give enough resistive contribution at HF to damp occurring resonances. At HF ($> 10\,\text{MHz}$), however, they show a very similar permeability to the utilized ferrite cores (both a few hundred to 1000). A benefit, however, is the higher saturation flux density ($1-2\,\text{T}$ compared to several 100 mT), which, however, in this case is not strictly required as

shown above (peak flux-density < 100 mT). Moreover, nanocrystalline cores are considerably more expensive than ferrites due to the more complex manufacturing process.

ii) The decoupling of C_{earth} from the CM source by means of the tip cable CM impedance from i) is not perfect, hence, there is still a certain i_{CM} flowing. To let this current flow independent of the DM measurement current, instead of just two connection lines between DUT and measurement system, one high-impedance signal line and one ground line, the proposed system uses a *three-wire* tip cable in triaxial configuration (cf. **Fig. 4.6 (b)** on the left side and photo in **Fig. 4.6 (c)**). The center wire is the high-impedance signal line and the two outer conductors are connected together at the DUT side (labeled with 'Shield-GND Conn.' in **Fig. 4.6 (b)**) but are separately connected to the measurement system. The middle connector is the low-impedance ground line (return path for the small measurement signal DM current) whereas the outer connector acts as a separate *charging line* that carries ideally the full i_{CM} and is connected directly to a metallic enclosure with as low an impedance as possible (labeled 'Low Ind. Shield Conn.' in **Fig. 4.6 (b)**). This enclosure effectively shields the sensitive measurement circuit on the PCB by defining C_{earth} with its outer surface and realizing an equipotential, ideally distortion-free zone inside. The finalized measurement system in **Fig. 4.5 (b)** has a C_{earth} of approximately 7 pF (including tip cable) when placed in a defined environment (metallic box connected to PE) at a distance of $\approx$ 15 cm to each side on a non-conductive distance holder (cf. **Section 4.4.1**).

iii) Theoretically, C_{earth} would be charged solely via the charging line according to ii) and no CM current would flow through the signal and ground lines. In practice, this is unfortunately not the case due to nonzero impedance of the charging line. To prevent CM current flow in the signal and ground lines, an additional CM choke L_{CM} (TDK Corporation ACM2510-102) is placed in these two lines, which takes the residual CM voltage appearing across the nonzero impedance of the charging line. Clearly, L_{CM} must provide maximum CM impedance but at the same time must be realized as compact as possible, in order to keep the overall size of the distortion-sensitive AFE small. Moreover, it must feature very high coupling as otherwise the residual DM inductance (leakage inductance) causes inadmissibly high peaking in the DM frequency response due to resonance with the tip cable capacitance and inductance as well as the AFE input capacitance. Due to the compact layout, the circuit ground on the PCB and the shield are capacitively

coupled (indicated in **Fig. 4.6 (a)**), which for HF prevents saturation of L_{CM}. To avoid significant fluctuations between the circuit ground and the shield potential, which particularly at LF could lead to a saturation of L_{CM}, the circuit ground is connected to the shielding enclosure *after* the ADC (labeled 'Shield-GND Connection' in **Fig. 4.6 (b)**). A connection after the ADC is less critical, because there, all signals are digital and less sensitive to small voltage errors (voltage drops across PCB tracks) in case a small CM current would flow on this part of the PCB. The loop inductance L_G between ground and shield (indicated in **Fig. 4.6 (a)**), formed by the physical layout, in addition to L_{CM} helps to drive i_{CM} solely through the charging line.

The very compact AFE depicted in **Fig. 4.6 (a)** is possible thanks to the single-ended realization and is a general advantage to minimize the overall system size and thereby C_{earth}. Furthermore, since it is the most critical part due to its high distortion-susceptibility, the short signal and ground return paths between the analog input and the ADC help to minimize parasitic voltage drops due to residual CM currents. In contrast to the single-ended realization of the AFE depicted in **Fig. 4.6 (a)**, a fully differential variant would also be possible. Two high-impedance signal lines (positive and negative), each connected to an input voltage divider, would lead to i_{CM} almost entirely flowing though the low-impedance charging line (current divider). The fully-differential approach could potentially further improve the CMRR, since any residual voltage drops along the circuit ground act as CM to the subsequent differential amplifier and compared to the single-ended approach do not directly deteriorate the DM measurements. The downside is, however, the requirement of precise matching between the differential signal paths (similar to HV differential probes) [123] and increased complexity and size of the AFE. With full integration of the AFE circuit into one single chip, the matching as well as the circuit size could be significantly optimized. As will be seen in **Section 4.4**, however, the single-ended approach presented in this section achieves more than sufficient performance and is preferably used.

The remaining components on the measurement system are responsible for signal processing, signal transmission and to provide all required auxiliary supply voltages for the components. Furthermore, there are two optical connections, which act as trigger input and output to synchronize the system with other isolated measurement systems or even to synchronize with an oscilloscope using the (external) trigger input/output. As seen in **Fig. 4.5 (b)**, the finalized measurement system is realized very compact with overall dimensions of 95 mm × 32 mm × 30 mm including the rechargeable battery (indicated with a dashed box; accounts for roughly 1/3 of the total volume),

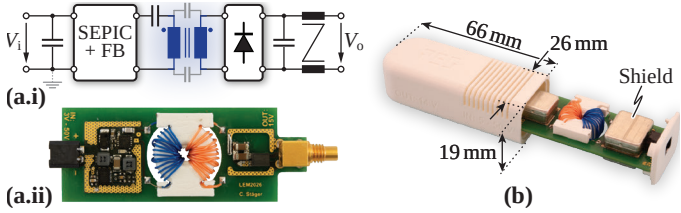


Fig. 4.7: (a.i) Block diagram of the developed wide input voltage range (5 – 50 V) 5 W output power isolated auxiliary PSU composed of a Single-Ended Primary Inductance Converter (SEPIC) plus series resonance operated full-bridge transformer driver, featuring an isolation stage (1 : 1 transformer) with very low coupling capacitance (highlighted in blue). Photos of the PSU **(a.ii)** without and **(b)** with metallic shields, plastic enclosure and overall dimensions.

which allows an operating time > 2 hours (power consumption between 1.5 W and 2 W).

4.3.3 Low Coupling Capacitance Isolated Power Supply Unit

Battery-operated measurement systems have the advantage that no additional power supply connections and/or isolation capacitances towards PE are required, which by increasing the small C_{earth} achieved with careful design, potentially degrade the CMRR. A fundamental drawback, however, is their limited operating time before manual intervention in the measurement setup is required to recharge or replace the battery. A compact overall solution (small C_{earth}) is only possible with relatively low capacity batteries, hence there is an inherent trade-off between operating time and system size. To achieve unlimited measurement time, a low coupling capacitance isolated PSU is therefore required. Power-over-Fiber (PoF) solutions with highly compact photovoltaic cells, illuminated by a laser beam, can transmit several Watts of electrical power over wide distances with virtually unlimited isolation [150, 151]. PoF is used in different applications such as commercially available isolated probes [126–128] or as isolated GD PSU [152, 153]. Such solutions are, however, relatively large, expensive and show a poor conversion efficiency (overall electrical-to-optical-to-electrical efficiency < 5 % for an electrical output power of 1.5 W [154, 155]). Due to the poor efficiency, the resulting relatively high heat generation demands for an increased cooling effort.

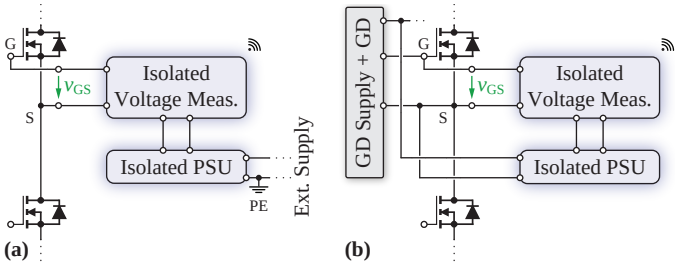


Fig. 4.8: Different options to connect the isolated auxiliary PSU to the isolated voltage measurement system. **(a)** Ground (PE) referenced auxiliary PSU input (e.g., laboratory supply). **(b)** Connection directly to a floating auxiliary power source on the DUT itself (e.g., GD supply referred to the high-side switch source potential).

An alternative solution is a custom-designed galvanically isolated PSU with magnetic isolation using a carefully constructed transformer with low coupling capacitance C_c. Thereby, a significantly higher conversion efficiency and a much more compact design is possible. **Fig. 4.7 (a.i)** and **(a.ii)** show the block diagram and the PCB of the PSU with a wide input voltage range of $V_i = 5\,\text{V}\ldots 50\,\text{V}$ to allow versatile connection to different power sources. It is designed to deliver up to 5 W output power (enough to simultaneously charge the battery and operate the measurement system plus sufficient margin). The input stage is composed of a Single-Ended Primary Inductance Converter (SEPIC) followed by a Full-Bridge (FB) transformer driver. The total coupling capacitance C_c of the isolation transformer is composed of a contribution from primary winding to core (N49 material from TDK) and from core to secondary winding (series connection of two times winding-to-core capacitance C_{w-c}, assuming an electrically conductive core at HF in the multi-MHz range [156]), and of a contribution directly from primary to secondary winding (15 turns each) over the air (winding-to-winding capacitance C_{w-w}). With the winding placement as indicated in **Fig. 4.7 (a.ii)**, i.e., a large separation between primary and secondary winding, C_c is mainly defined by the winding-to-core capacitance C_{w-c}. To minimize C_{w-c}, the primary and secondary windings are placed several mm away from the magnetic core to finally achieve a total coupling capacitance of $C_c \approx 2\,\text{pF}$. The placement is realized with a 3D printed plastic shell of several mm thickness, in which the core is placed before the windings are added. Placement of the windings as described comes at the expense of an increased leakage inductance L_σ and therefore, a reduced coupling factor, which is compensated by operating the FB transformer driver in series resonance (resonance capacitor indicated in **Fig. 4.7 (a.i)**) in order

to avoid a load dependent output voltage. The output stage is unregulated and consists of a diode rectifier and an output filter. All required supply voltages are generated directly on the measurement system with regulated point-of-load converters from the unregulated PSU output voltage ($\approx$ 14 V). **Fig. 4.7 (b)** shows the fully assembled PSU with mounted shields and a plastic enclosure that has an overall conversion efficiency above 70 %. The purpose of the metallic shields is on the one hand to prevent disturbing nearby equipment (e.g., GDs) with the emissions from the switch-mode operation of the SEPIC and transformer driver and on the other hand, conversely, to prevent distortions of the PSU in a noisy/harsh environment found, e.g., in close vicinity to fast switching power converters. The power connection between PSU output and measurement system is realized with a coaxial cable equipped with lossy ferrite cores acting as additional decoupling CM inductors. Like for the tip cable, this helps to decouple the additional C_{earth} of the PSU output stage from the fast switching transitions. In contrast to the virtually unlimited isolation of PoF solutions, the isolation capabilities of the measurement system and therefore, the maximum allowed CM input voltage range is now defined by the transformer isolation, assuming the primary side is referred to PE, e.g., connected to a non-isolated external laboratory supply as shown in **Fig. 4.8 (a)**. The isolation is verified up to 1 kV, which is sufficient for many applications. Transformers for isolated GD supplies with an isolation rating of 10 kV and at the same time extremely compact construction and very low coupling capacitance have been presented [157] and could be used in this auxiliary PSU. However, thanks to the wide input voltage range, it is possible to power the auxiliary PSU alternatively directly from a floating source, e.g., from an auxiliary GD supply in a MV power converter as shown in **Fig. 4.8 (b)**, where the additional power consumption of around $2 - 3$ W is negligible [158]. Thereby, the transformer isolation only has to withstand the voltage difference between measurement reference potential and PSU input voltage reference potential and the rating of 1 kV is sufficient. The PSU, connected to the measurement system according to **Fig. 4.8 (a)**, has no significant impact on the achievable CMRR, as experimentally verified in the next section.

4.4 Experimental Verification

This section presents measurement results in the frequency- and the time-domain to experimentally verify the performance of the designed isolated measurement system.

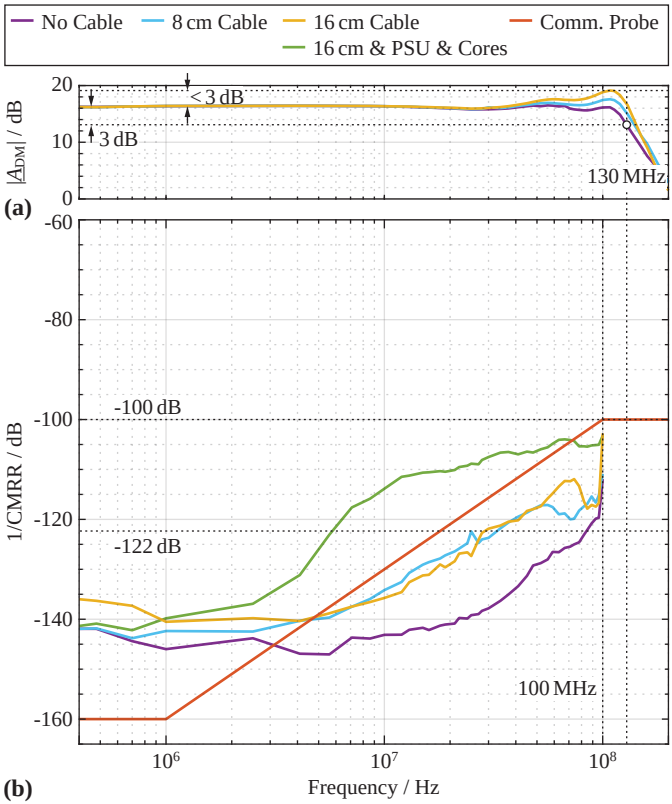


Fig. 4.9: (a) Measured DM TFs of the probe without tip cable (purple), with a 8 cm tip cable (cyan) and with a 16 cm tip cable (yellow), achieving in all cases a BW $>$ 130 MHz and $<$ 3 dB peaking. **(b)** Measured CMRR for battery operation with the same configurations as (a). For easier comparison with Fig. 4.3, 1/CMRR curves (negative dB values) are plotted. The green line shows 1/CMRR for the long tip cable with PSU operation. Further indicated is 1/CMRR of the currently best available commercial isolated voltage probe (orange).

4.4.1 Frequency-Domain Characterization

The analog BW is determined by measuring the magnitude $\left|\underline{A}_{\mathrm{DM}}\right|$ of the DM TF, depicted in **Fig. 4.9 (a)**. Thereby, the AFE is configured for maximum sensitivity, i.e., set to the highest gain of 16 dB ($\times$ 6.3) and no input voltage divider is utilized. The measurement is performed without tip cable (purple)

and with 8 cm (cyan) and 16 cm (yellow) long tip cables. As indicated, the −3 dB BW is 130 MHz in the case without tip cable. The BW is intentionally limited by the AAF in order to prevent aliasing effects in the sampling process. With the current sampling rate of 400 MSPS, the Nyquist frequency and therefore, the absolute maximum possible BW, is 200 MHz, whereas the corner frequency of 130 MHz is selected to account for finite filter steepness. To overcome the BW limitation imposed by the ADC, faster sampling devices would be required. A certain peaking in the magnitude response is visible proportional to the tip cable length. It originates from a resonance between the leakage inductance of L_{CM} (cf. **Fig. 4.6 (a)**), the additional inductance and capacitance from the tip cable and the AFE input capacitance. With the 16 cm long cable (nominal configuration offering high flexibility to connect to different DUTs), the peaking is below 3 dB. In the current realization, the tip cable is purely capacitive and inductive, i.e., does not contain any distributed damping. Peaking could be reduced by utilizing a lossy transmission line, as it is done in standard passive voltage probes [159], instead of a nearly perfect conducting copper coaxial cable. In addition, a better frequency response and in particular a lower input capacitance could then be achieved by placing R_1 and C_1 of the voltage divider directly at the measurement tip. Thereby, the cable capacitance would be in parallel to C_2 and would not add to the input capacitance seen by the DUT (less loading).

Fig. 4.9 (b) shows 1/CMRR (i.e., negative dB values to directly compare with **Fig. 4.3**) versus frequency, again for the different configurations, where in case of utilized tip cables, CM cores are distributed along the full cable length (cf. i) above). These measurements are performed in a carefully defined environment, where the measurement system is placed on an isolated distance holder inside a shielded box (referred to PE) with a distance of $\approx$ 15 cm to the walls. The input pins at the measurement tip are shorted together and excited with a 160 V peak-to-peak sinusoidal CM voltage (with respect to PE) at distinct frequencies up to 100 MHz using a Radio-Frequency (RF) Power Amplifier (PA) (AR 150A100D with maximum frequency of 100 MHz). The measured error is evaluated in the digital domain and to maximize the measurement sensitivity, the system's AFE is configured for maximum gain such that referred to the input, one Least Significant Bit (LSB) of the ADC corresponds to 0.13 mV. Therefore, the maximum directly measurable CMRR is 122 dB (one LSB toggles due to the CM excitation). CMRR values $>$ 122 dB are obtained by averaging the amplitude extracted over multiple recorded signal periods ($>$ 1000 periods per frequency). This takes into account that the LSB does not toggle every time, indicating a lower error voltage than the equivalent of one LSB. The best results (CMRR $>$ 120 dB across almost the full considered frequency range) are achieved by connecting the measurement

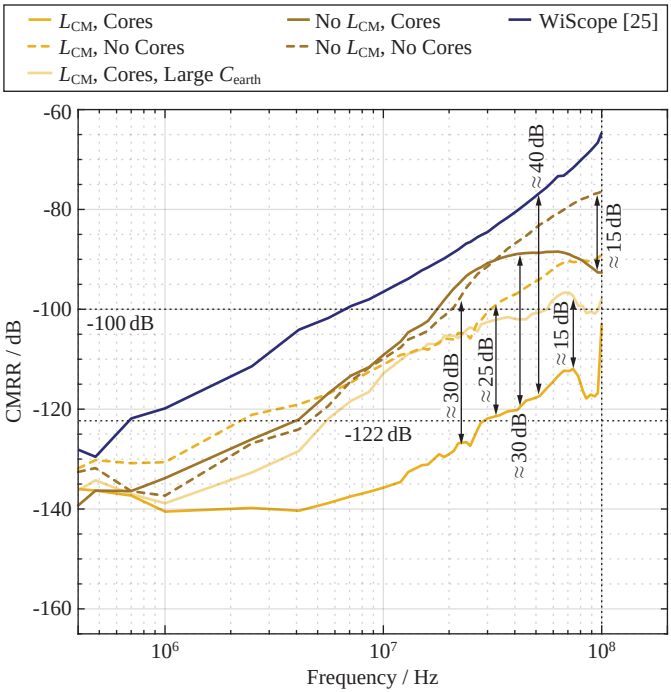


Fig. 4.10: Influence of different measures listed in Section 4.3.2 on the achievable CMRR (16 cm long tip cable attached in all cases) and comparison with the WiScope [145]. For easier comparison with Fig. 4.3, 1/CMRR is plotted.

system without tip cable (purple) because Z_{line} is accordingly minimized and the full i_{CM} flows entirely over the shielding enclosure. Adding a tip cable with CM cores (cyan for 8 cm length, yellow for 16 cm length), the CMRR decreases by around 10 dB in the frequency range between 10 MHz and 100 MHz. The cable length does not significantly influence the performance up to 70 MHz. For the nominal configuration with the 16 cm long tip cable equipped with CM cores, the green curve shows the impact of using the isolated PSU (configuration according to **Fig. 4.8 (a)**) instead of the battery. There, the CMRR decrease compared to the same configuration with battery operation is between 10 and 25 dB, starting at a few MHz. It can be seen that for all configurations of the presented measurement system, the CMRR is substantially greater than 100 dB over the full considered frequency range and

on par with the best-performing currently available isolated voltage probe (orange).

Moreover, **Fig. 4.10** demonstrates the influence of the different measures (cf. **Section 4.3.2**) on the achievable CMRR (y-axis again showing 1/CMRR, i.e., negative dB values, for easier comparison with **Fig. 4.3**), where in all cases the 16 cm long tip cable is attached to the measurement system. The yellow curves denote configurations with mounted internal CM choke L_{CM} (cf. **Fig. 4.6 (a)**), which show $\approx$ 30 dB better HF performance compared to the configurations with L_{CM} unmounted (brown curves). In case of installed L_{CM}, the tip cable equipped with CM cores (continuous yellow line) gives a benefit of $\approx$ 25 dB compared to a tip cable without CM cores (dashed yellow line). For an absent L_{CM} the benefit is smaller, and only at frequencies above 30 MHz a maximum improvement of $\approx$ 15 dB is measured. Between the best-performing configuration (yellow continuous line, all measures from **Section 4.3.2** employed) and worst-performing configuration (brown dashed line, no cable CM cores, no L_{CM}), a difference of $\approx$ 30 $-$ 35 dB is found. An important finding for practical use is that a larger C_{earth}, formed, e.g., by placing the measurement system too close to PE, only degrades the CMRR by $\approx$ 15 dB (semi-transparent yellow line). This proves the effectiveness of the provided measures to decouple i_{CM} from the sensitive measurement path. A comparison of the presented system's CMRR with the WiScope [145] reveals an improvement of $\approx$ 40 dB over a very wide frequency range. The WiScope CMRR (darkblue curve in **Fig. 4.10**) is thereby measured without any tip cable, i.e., marks the absolute best-case, whereas the presented measurement system is equipped with the 16 cm long tip cable. Based on **Fig. 4.9 (b)**, with the addition of a tip cable the WiScope's HF CMRR is expected to degrade by $>$ 10 dB, unless being equipped with CM cores as explained in **Section 4.3.2**.

4.4.2 Time-Domain Measurements

Finally, the measurement system is tested by measuring the HS GS voltage $v_{\mathrm{GS,HS}}$ in a half-bridge employing 600 V GaN power semiconductors (cf. **Fig. 4.1 (a)**), switching $V_{\mathrm{dc}} = 400\,\mathrm{V}$ at 800 kHz. **Fig. 4.11 (a)** shows the measured switch-node waveform v_{sw} for Zero-Current Switching (ZCS), i.e., without any load and/or output filter connected. A zoomed view into the rising edge indicates a very fast $\mathrm{d}v/\mathrm{d}t$ of 100 kV/µs. The measured $v_{\mathrm{GS,HS}}$ is depicted in **Fig. 4.11 (b)** where again, the results of the presented measurement system operated with the battery (yellow) and the PSU (green) are compared to the best available commercial isolated voltage probe (orange). In all cases, the 16 cm long triaxial tip cable equipped with CM cores is used. The proposed measurement system accurately captures $v_{\mathrm{GS,HS}}$, however, the BW

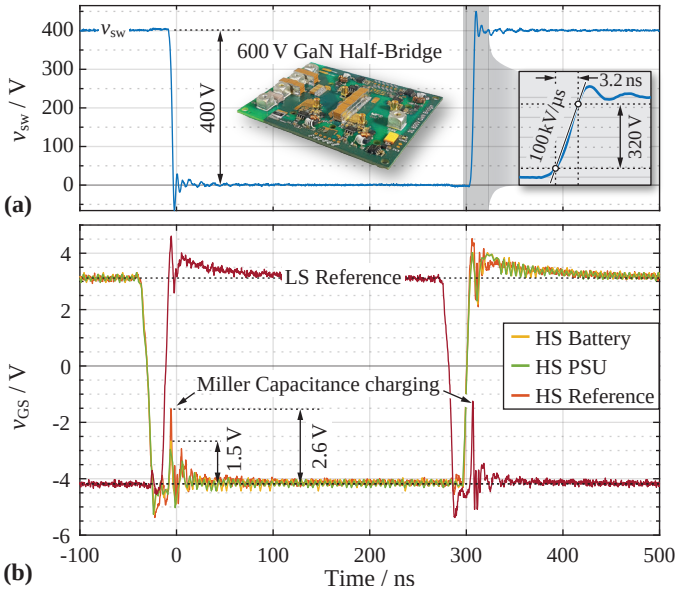


Fig. 4.11: Measurement of the HS Gate-Source voltage in a GaN half-bridge (cf. Fig. 4.1 (a)) with 400 V dc link voltage. **(a)** Measured switch-node voltage, i.e., CM disturbance voltage, with a dv/dt of 100 kV/µs. **(b)** Measured $v_{GS,HS}$ with the commercial isolated probe (orange; HS reference measurement) and the presented system with the 16 cm triaxial tip cable and CM cores on the cable with battery operation (yellow) and PSU operation (green). For further reference, the LS Gate-Source voltage is measured (red; LS reference measurement) to prove that the residual peak in v_{GS} during the fast voltage transition is due to the current that flows out of the gate and results from charging the device Miller capacitance.

of 130 MHz is just at the lower limit for measurements of signals with a rise time of only few nanoseconds. During the falling edge of v_{sw}, where $v_{GS,HS}$ is supposed to be steady at −4 V to safely keep the HS switch off, a certain voltage peak occurs. This peak is measured with all probes/system configurations, however, seems to be worse when measured with the reference probe (2.6 V compared to 1.5 V). To determine, whether the peak is an error due to the CM disturbance or indeed present, in addition, the LS GS voltage $v_{GS,LS}$ is measured with the reference probe (dark red). The peak is present in the same way as in the $v_{GS,HS}$ measurement and results from charging the device Miller capacitance C_{GD} (between gate and drain) during the rising edge of v_{sw}. This current has to flow out of the GD and causes the voltage peak. Therefore,

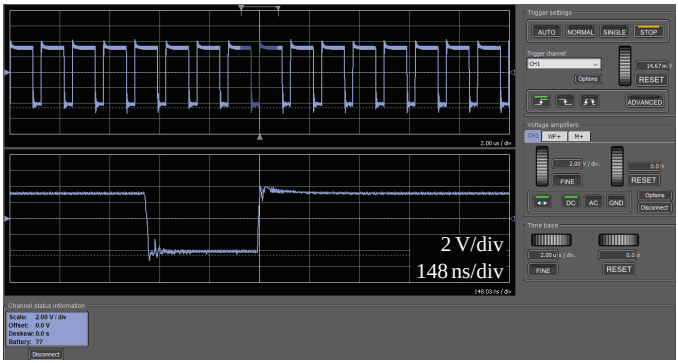


Fig. 4.12: Screenshot of the Graphical User Interface (GUI) software on the host computer displaying the $v_{GS,HS}$ measurement when the probe is battery-operated (yellow curve in Fig. 4.11 (b)).

the presented isolated measurement system as well as the reference probe are not influenced by the fast changing CM voltage. However, the supposedly smaller $v_{GS,HS}$ peak measured with the presented system during the v_{sw} transition is due to the lower BW compared to the reference probe. **Fig. 4.12** shows a screenshot of the GUI on the host computer, displaying the $v_{GS,HS}$ measurement of the battery-operated configuration (corresponding to the yellow curve in **Fig. 4.11 (b)**).

4.5 Conclusion

Very fast switching transitions (high $\mathrm{d}v/\mathrm{d}t$) achieved with today's increasingly prevalent Wide-Bandgap (WBG) semiconductors in power converters require advanced measurement technologies to accurately investigate the dynamic behavior during operation. The demands on the measurement technology are particularly high, since often measurements of small voltages referred to rapidly changing reference potentials that act as Common Mode (CM) disturbance on the measurement, must be carried out. A prominent example is the measurement of the High-Side (HS) Gate-Source (GS) voltage in a half-bridge, where the switch-node voltage acts as CM disturbance. Such situations demand equipment with superior Common Mode Rejection Ratio (CMRR) to avoid affecting the desired measurement. Switching transitions of multiple 100 V within sub 10 ns lead to significant High-Frequency (HF) disturbances, thus a high CMRR at elevated frequencies is necessary. The min-

imum required CMRR over the full frequency range of interest is determined to constrain the resulting time-domain error in the measured signal below a certain limit $\Delta v_{\varepsilon,\mathrm{pp}}$. This value is found to be constant ($\Delta v_{\varepsilon,\mathrm{pp}}/V_{\mathrm{dc}}$) up to a frequency f_{c2}, determined solely by the transition time of the CM disturbance ($f_{\mathrm{c2}} = \mathrm{d}v/\mathrm{d}t/(\pi V_{\mathrm{dc}})$) and above there, rises with +20 dB/dec. Therefore, for given V_{dc}, $\mathrm{d}v/\mathrm{d}t$ and maximum allowed measurement error, the required CMRR versus frequency is directly obtainable and is independent of the converter switching frequency f_{sw}. For $V_{\mathrm{dc}} = 800\,\mathrm{V}$ and $\mathrm{d}v/\mathrm{d}t = 100\,\mathrm{kV/\mu s}$, a CMRR of around 80 dB up to 40 MHz is required to keep the resulting error below 100 mV. There are commercially available galvanically isolated voltage measurement *probes* that achieve the demanded CMRR. However, they require a dedicated (often vendor-specific) oscilloscope to form a complete measurement system. As an alternative, this chapter presents a galvanically isolated measurement *system*, which digitizes the measured signal and transmits the data wireless to a host device (e.g., computer, laptop, tablet) with corresponding host Graphical User Interface (GUI) software, to directly and independent of other equipment perform measurements on fast changing reference potentials. Essential design aspects, in particular of the Analog Front-End (AFE) and the connection of the measurement system to a Device Under Test (DUT), imperative to achieve a HF CMRR > 100 dB at frequencies in the multi-MHz range, are highlighted and thoroughly analyzed.

Finally, the presented isolated measurement system is comprehensively tested in the frequency- and the time-domain. It achieves a measurement Bandwidth (BW) of 130 MHz and a CMRR of > 100 dB up to 100 MHz, which is on par with the best commercially available isolated voltage probes. Time-domain measurements of the HS GS voltage in a half-bridge with fast-switching Gallium-Nitride (GaN) power semiconductors verify the superior CM robustness but indicate that for capturing very fast switching transients, a higher measurement BW is required. Currently, the BW is ultimately limited by the sampling rate of the Analog-to-Digital Converter (ADC) but this could be overcome with a faster sampling device. Moreover, optical trigger synchronization with other measurement equipment is an important next implementation step to increase practical usability.

Part C

Conducted EMI Noise Assessment

5

Analysis of the Influence of Measurement Circuit Asymmetries on Three-Phase CM/DM Conducted EMI Noise Separation

This chapter summarizes the most relevant findings regarding test setup asymmetries and their impact on three-phase conducted Electromagnetic Interference (EMI) noise separation, which are also published in:

- **P. S. Niklaus**, M. M. Antivachis, D. Bortis, and J. W. Kolar, "Analysis of the Influence of Measurement Circuit Asymmetries on Three-Phase CM/DM Conducted EMI Separation," *IEEE Transactions on Power Electronics,* vol. 36, no. 4, pp. 4066-4080, April 2021.

Chapter Abstract

Electromagnetic Interference (EMI) Conducted Emissions (CEs) are of increasing concern in power electronics due to the high switching frequency and fast switching speeds (dv/dt) of the latest generation of Wide-Bandgap (WBG) power semiconductors. The decomposition of the total conducted EMI noise into its Common Mode (CM) and Differential Mode (DM) part by means of a CM/DM noise separator is a useful tool that allows for a systematic EMI filter design. Carefully designed realizations achieve a Common Mode Rejection Ratio (CMRR) and Differential Mode Rejection Ratio (DMRR) of 50 dB at 30 MHz. However, a very high-performance CM/DM noise separator is not sufficient. It is theoretically analyzed and experimentally proven that asymmetries in the EMI test setup result in an unwanted conversion between CM and DM EMI noise and therefore, significantly influence the CM/DM EMI separation. In particular, three main influences are identified: the Line Impedance Stabilization Network (LISN), the connection cables between LISN and the Equipment Under Test (EUT) and the converter EMI filter. The unwanted noise conversion is pronounced for frequencies in the MHz range, where parasitic resonances occur. Experimental results show a CM-to-DM conversion of up to −30 dB at 30 MHz (a degradation by 20 dB or a factor of 10 compared to a high-performance separator alone) considering a connection cable length mismatch of roughly 5 cm. Values as high as −21 dB result when standard commercial LISNs are used for the measurement. The impact of asymmetries in the EMI filter is most severe and clearly limits the EMI noise splitting at high frequencies. A high-performance noise separator can, however, be used to investigate such filter asymmetries (component tolerances and/or layout) and therefore, it helps to improve the filter design process and facilitates the modeling of EMI noise sources.

5.1 Introduction

Power electronic converter systems connected to the public mains must comply with international standards on Electromagnetic Compatibility (EMC) such as CISPR 11 (EN 55011) [15] for industrial, scientific and medical equipment or CISPR 14 (EN 55014) [16] for household appliances and electric tools. EMC standards mandate the maximum allowed Electromagnetic Interference (EMI) noise spectral components in a certain frequency band. The regulations distinguish between Conducted Emissions (CEs) evaluated in the frequency band between 150 kHz and 30 MHz, and Radiated Emissions (REs)

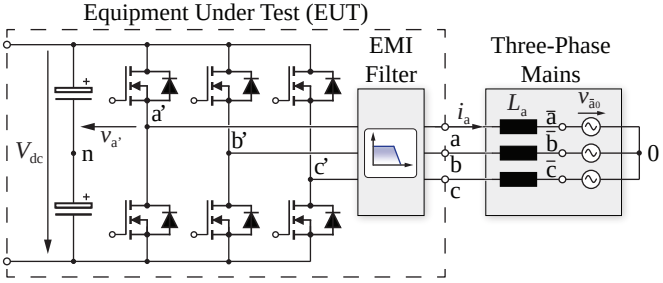


Fig. 5.1: Equipment Under Test (EUT): Photovoltaic three-phase inverter system with output EMI filter, that supplies energy to the three-phase public mains (here shown with idealized sinusoidal voltage sources $\underline{v}_{\bar{i}0}$ and corresponding inner mains inductances L_i, $i \in \{\text{a, b, c}\}$).

evaluated between 150 kHz and 1 GHz. REs can be relatively easily mitigated by placing the converter within a metallic enclosure, as it is usual practice in industrial applications. Of specific relevance for power electronic designs are typically the CEs, which are measured using a Line Impedance Stabilization Network (LISN) according to CISPR 16-1-2 (EN 55016-1-2) [160]. The LISN acts as interface between the Equipment Under Test (EUT), i.e., the converter system that has to fulfill the regulations (cf. **Fig. 5.1**), and the mains. Please note that in this chapter the term Equipment Under Test (EUT) is used instead of System Under Test (SUT), since this is in accordance to the common notation in EMC standards.

In a standard CE EMI test setup the EUT is connected to the three-phase mains and an EMI test receiver with help of a three-phase LISN (dotted line in **Fig. 5.2**). The LISN provides a standardized inner mains impedance seen by the EUT [160] and allows to measure the EUT generated conducted EMI noise appearing at the LISN High-Frequency (HF) output ports (voltages $\underline{v}_{\text{LISN},i}$). Furthermore, the LISN decouples the EUT from any HF noise present in the supplying mains and decouples the HF output port from any Low-Frequency (LF) power flow related components that would destroy the sensitive EMI measurement equipment given their large magnitude. The standard setup, however, does not distinguish between Common Mode (CM) and Differential Mode (DM) EMI noise. The LISN voltages contain both, CM and DM voltage components. Therefore, if for example, the measured EMI noise exceeds the mandated regulation limits, the designer does not know if this is caused by the CM or DM noise component. Accordingly, it is difficult to assess if the CM or DM part of the EMI filter is under-performing and/or needs to be redesigned.

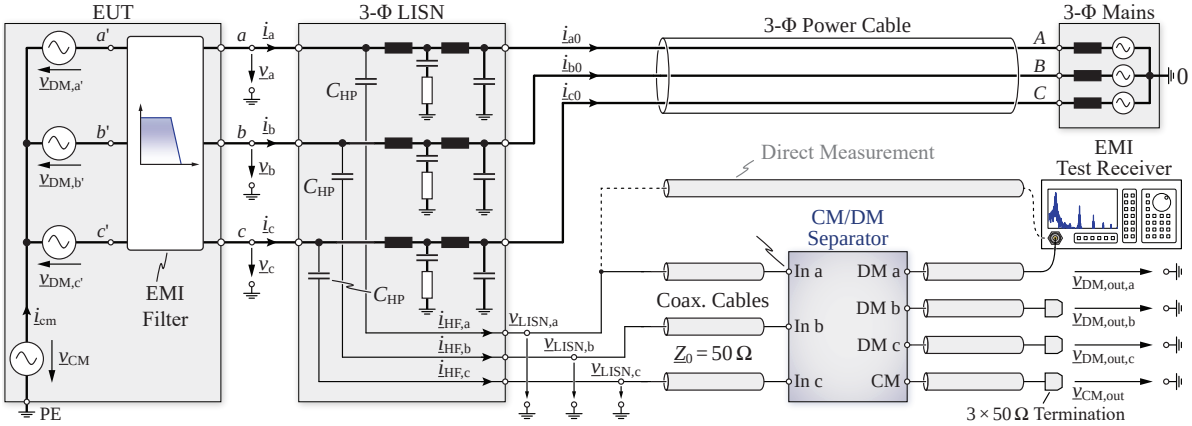


Fig. 5.2: Typical EMI pre-compliance measurement setup for a three-phase EUT. A three-phase LISN connects the EUT to the mains (bold lines indicate power transfer) and either directly (dotted line) or via a three-phase CM/DM noise separator (highlighted in blue) to an EMI test receiver. In the former case the total CE EMI noise is measured, whereas in the latter case the separated CM and DM emissions are identified. Coaxial cables with a characteristic impedance of 50 Ω are employed for the signal connections. Only one voltage at a time can be measured with typical EMI test receivers so any unused HF output terminal must be terminated with 50 Ω.

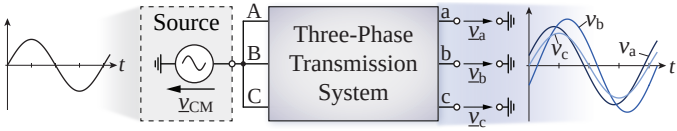


Fig. 5.3: Schematic representation of amplitude and phase mismatch in a three-phase transmission system with nominally identical transfer characteristics from each input A, B, C to the corresponding output a, b, c for a purely CM input voltage.

For this reason, a pre-compliance EMI test is often performed with the goal to also distinguish between the CM and DM EMI noise. An extension of the standard EMI test setup as shown in **Fig. 5.2** includes a CM/DM noise separator (highlighted in blue), which separates the three noise voltages $\underline{v}_{\mathrm{LISN},i}$ into one CM and three DM components ($\underline{v}_{\mathrm{CM,out}}$ and $\underline{v}_{\mathrm{DM,out},i}$). Coaxial cables with a characteristic impedance of 50 Ω are employed for the signal connections. Only one voltage at a time can be measured with typical EMI test receivers so any unused HF output terminal must be terminated with 50 Ω. The detailed insight in the noise behavior enables selective adjustments of the CM and DM filter stages of the EMI filter to ensure compliance with the respective norms. Furthermore, CM and DM EMI noise equivalent circuits can be verified when comparing simulations and measurements. In order to perform an accurate separation a noise separator with very high separation capability, i.e., without cross-conversion of CM input noise to DM output noise (CM-to-DM conversion) and vice versa is required.

It has been shown in literature [161–164] that to achieve the demanded high separation capability for three-phase noise separators a highly symmetric layout and close matching between the three phases is of paramount importance. Asymmetries and insufficient matching manifest themselves in a deviation of the amplitude and/or phase from the desired nominal values. **Fig. 5.3** shows a three-phase transmission system (highlighted in blue) with nominally identical transfer functions from each input A, B, C to the corresponding outputs a, b, c. A pure CM input voltage is assumed and the amplitude and phase mismatch resulting from the imperfectly matched transfer functions in the three-phase transmission system are highlighted. The three output voltages v_{a}, v_{b} and v_{c} are not entirely CM anymore but also contain a certain DM component. Therefore, a CM-to-DM conversion has taken place.

In noise separators the parasitic CM-to-DM conversion (and vice versa) is characterized with the Common Mode Rejection Ratio (CMRR) and Differential Mode Rejection Ratio (DMRR). It is clear, however, that not only the noise separator but all parts of the extended CE EMI test setup according

to **Fig. 5.2** are potential sources of mismatch that could lead to parasitic CM-to-DM conversion (and vice versa). Only with a very high-performance CM/DM noise separator, however, there is the confidence that any measured CM-to-DM conversion (and vice versa) is not caused by the noise separator itself but can be reliably attributed to the previously listed causes.

5.1.1 Overview of this Chapter

In this chapter, various sources of mismatch in the CE EMI test setup that impair the overall noise separation performance are identified and analyzed. Quantitative results that indicate the maximum achievable separation capability for a given mismatch are provided. Firstly, in **Section 5.2** the EMI noise equivalent circuit of a standard Voltage Source Inverter (VSI) is presented, followed by a short review of existing three-phase noise separators with the achieved separation performance. **Section 5.3** then theoretically discusses the CM-to-DM conversion resulting from certain amplitude and/or phase mismatches in a three-phase transmission system. The experimentally determined CM-to-DM conversion caused by asymmetries in the connecting cables and the LISN is quantified in **Sections 5.4** and **5.5**, respectively. Finally, **Section 5.6** analyzes a three-phase CM and DM EMI filter stage and it is shown that already small mismatches between the three phases are causing a significant conversion from CM noise into DM noise. All theoretical considerations are verified by means of experimental measurements. In summary, the sensitivity of the CE EMI test setup with respect to component and/or layout asymmetries is highlighted, while appropriate measures that reduce the CM-to-DM conversion are suggested.

5.2 Fundamentals of Three-Phase CM/DM Noise Separation in Power Converters

5.2.1 EMI Noise Equivalent Circuit of a Voltage Source Inverter

Generally, switched-mode converter systems such as a three-phase photovoltaic VSI shown in **Fig. 5.1** present substantial HF spectral components at their ac outputs originating from the Pulse Width Modulation (PWM) operation of the three half-bridges. Meeting the respective regulations therefore requires suitable EMI filtering, which typically accounts for a considerable amount of the total converter volume, contributes losses and weight and increases the overall cost. Consequently, the aim is to keep the EMI filtering

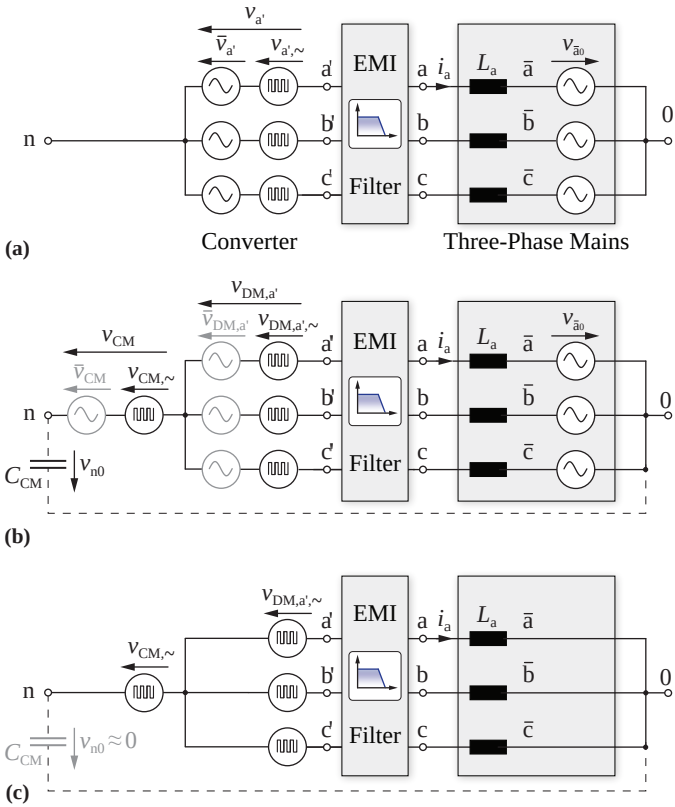


Fig. 5.4: Simplified representation of the three-phase inverter with EMI filter of Fig. 5.1 using equivalent voltage source circuits. **(a)** Three switch-node voltages $v_{a'}$, $v_{b'}$ and $v_{c'}$ with a (desired) fundamental frequency component $\bar{v}_i$ and a High-Frequency switching component $v_{i,\sim}$ and **(b)** further decomposition of both frequency components into CM and DM parts referred to the converter reference potential n. Further included is a parasitic connection of the inverter dc midpoint potential n with ground through the parasitic capacitance C_{CM}. As a worst-case condition for EMI filter design, a short circuit between n and ground can be assumed. **(c)** Only the EMI relevant HF components are considered for the worst-case with $v_{n0} = 0$.

effort as low as possible, which is achieved by a detailed analysis of the converter's EMI noise equivalent circuit. In **Fig. 5.4 (a)** each of the half-bridges from **Fig. 5.1** is replaced with two voltage sources $\bar{v}_i$ and $v_{i,\sim}$, $i = \{a', b', c'\}$,

representing the fundamental frequency component $\bar{v}_i$ (e.g. the 50/60 Hz voltage) and all switching related components $v_{i,\sim}$, respectively. It holds that $v_i = \bar{v}_i + v_{i,\sim}$. A further decomposition is possible by separately considering the CM and DM components of the corresponding phase voltages (cf. **Fig. 5.4 (b)**) according to

$$v_i = v_{\mathrm{CM}} + v_{\mathrm{DM},i}, \qquad i = \{\mathrm{a}', \mathrm{b}', \mathrm{c}'\}\,, \tag{5.1}$$

where again the fundamental and the switching frequency components can be considered separately.

By definition, the CM component is equal in all three phases and can thus be combined to a single voltage source

$$v_{\mathrm{CM}} = \frac{v_{\mathrm{a}'} + v_{\mathrm{b}'} + v_{\mathrm{c}'}}{3}, \tag{5.2}$$

with help of the identity

$$v_{\mathrm{DM,a}'} + v_{\mathrm{DM,b}'} + v_{\mathrm{DM,c}'} = 0. \tag{5.3}$$

It should be noted that this decomposition implicitly assumes equal/symmetric distribution of the phase impedances and therefore a symmetric distribution of the CM current. In practice, this is typically fulfilled with sufficient accuracy, however, not strictly required [165]. **Appendix C** explains the CM and DM decomposition in a three-phase system in more detail.

The fundamental components are usually not of importance for EMI compliance as they occur far below the relevant regulated frequency range and it is sufficient to consider only the HF switching components (**Fig. 5.4 (c)**). The inverter dc input midpoint n can be floating with respect to mains ground 0 (Protective Earth (PE)) but there will always be a certain parasitic CM capacitance C_{CM} connecting the two potentials, which in combination with $v_{\mathrm{CM},\sim}$ determines the CM noise. For EMI filter design, the worst-case condition of a short circuit between n and 0 ($v_{\mathrm{n0}} = 0$) has to be considered.

Finally, the equivalent circuit of the three half-bridges is simplified to four HF voltage sources, one CM voltage and three DM voltages. Expanding the four HF voltages as a Fourier series results in individual spectral components. For each frequency the corresponding three-phase system composed of the spectral components of the Fourier series of the CM and DM voltages can be individually described in a phasor diagram as shown in **Fig. 5.5** with help of complex phasors $\underline{v}_{\mathrm{CM}}$ and $\underline{v}_{\mathrm{DM},i}$, $i = \{\mathrm{a}', \mathrm{b}', \mathrm{c}'\}$, each representing an amplitude and phase information. It has to be noted that the 120° phase-shift between the individual phase voltages is given only for the fundamental component and is not necessarily required for the HF voltage components. For better visibility **Fig. 5.5** still shows a phase-shift of around 120°. For simplicity,

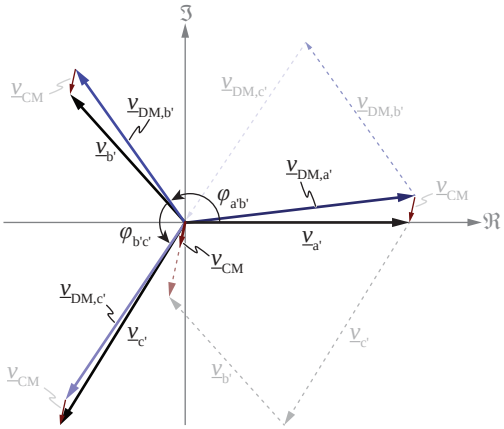


Fig. 5.5: Phasor diagram showing the decomposition of the three-phase voltage components into the respective CM and DM parts. The decomposition is performed for each HF spectral component individually.

hereinafter $\underline{v}_{CM}$ and $\underline{v}_{DM,i}$ denote complex phasors of the CM component and the three DM components of the EMI noise voltage at one specific frequency.

5.2.2 Review of Three-Phase CM/DM Noise Separators

The use of a three-phase EMI CM/DM noise separator is required to discuss the CM and DM noise components. Various implementations of three-phase noise separation circuits have been presented in the literature. Most of them are composed of magnetic components and rely on flux superposition/cancellation [161, 164, 166, 167]. Only two variants feature active operational amplifiers [162, 168] where there is no need to match magnetic components. This greatly facilitates handling, operation and the reproducibility. There are alternative implementations using current probes [163] or the separation is simply performed in post-processing [169] given the three individual noise spectra. The latter method is very sensitive to noise and/or measurement errors.

Because a very high-performance noise separator is a prerequisite for accurate CM/DM noise decomposition, the most promising approach is the three-phase active CM/DM noise separator presented in [162] by the author of this thesis (cf. **Appendix B**), which features a very high reported separation performance. Its schematic is shown in **Fig. 5.6** including a representation of the HF noise voltage sources at its input ports *a*, *b* and *c*. The input voltages

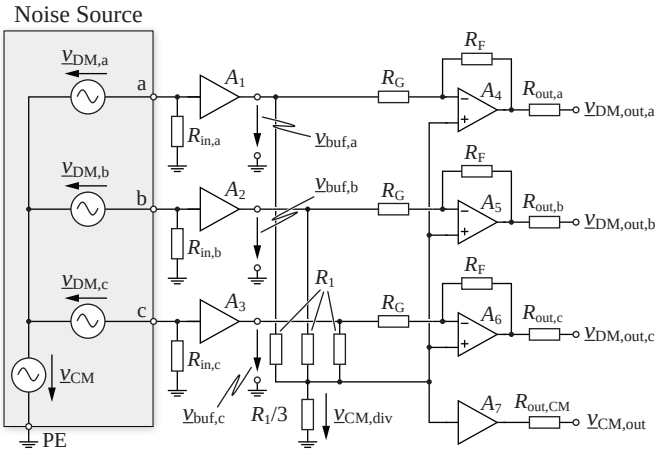


Fig. 5.6: Schematic drawing of the three-phase active CM/DM noise separator as described in **Appendix B**.

are terminated with $R_{\text{in},i} = 50\ \Omega$ as required by the standard [170] and are then buffered with amplifiers $A_1 \ldots A_3$. With the CM voltage divider composed of three resistors R_1 and resistor $R_1/3$, the CM voltage $\underline{v}_{\text{CM,div}}$ is derived according to (5.2) and is available at the CM output port after buffering with amplifier A_7. The three DM components are derived from the buffered input voltages $\underline{v}_{\text{buf},i}$ and the CM voltage based on (5.1) with three difference amplifiers $A_4 \ldots A_6$, i.e.,

$$\underline{v}_{\text{DM,out},i} = \underline{v}_{\text{CM,div}} - \underline{v}_{\text{buf},i}. \tag{5.4}$$

The inverted sign of $\underline{v}_{\text{DM,out},i}$ compared to (5.1) does not influence the measurement, since only the noise voltage magnitudes are relevant for compliance.

To assess the performance of a noise separator it is helpful to consider the Transfer Functions (TFs) and Rejection Ratios (RRs) (CMRR and DMRR), which are found by applying either a pure CM ($\underline{v}_{\text{DM,i}} = 0$) or a pure DM ($\underline{v}_{\text{CM}} = 0$) excitation. In the former case, the Common Mode Transfer Function (CMTF) is defined as the ratio between CM output voltage and CM input voltage

$$CMTF = \left| \frac{\underline{v}_{\text{CM,out}}}{\underline{v}_{\text{CM}}} \right|. \tag{5.5}$$

Similarly, the Common Mode Rejection Ratio (CMRR) describes the amount of input CM voltage converted into DM at output port i, i.e.,

$$CMRR_{\mathrm{i}} = \left| \frac{\underline{v}_{\mathrm{DM,out,i}}}{\underline{v}_{\mathrm{CM}}} \right|. \tag{5.6}$$

For an ideal noise separator the three CMRR responses of the phases are identical.

In the case of a pure DM input the Differential Mode Transfer Function (DMTF) and the Differential Mode Rejection Ratio (DMRR) are defined as

$$DMTF_i = \left| \frac{\underline{v}_{\mathrm{DM,out,i}}}{\underline{v}_{\mathrm{DM}}} \right| \tag{5.7}$$

and

$$DMRR = \left| \frac{\underline{v}_{\mathrm{CM,out}}}{\underline{v}_{\mathrm{DM}}} \right|. \tag{5.8}$$

The experimental TF and RR measurements of an active noise separator hardware demonstrator according to [162] are depicted in **Fig. 5.7** and reveal excellent separation capabilities. A CMRR and DMRR better than −50 dB is reached over almost the entire EMI relevant frequency range, while the CMTF and the DMTF both remain very flat. Particularly the performance at elevated frequencies above 1 MHz is significantly better compared to a passive separator (dashed lines in **Fig. 5.7**, concept of [161]). The deviation of the CMRR and DMRR in **Fig. 5.7** is caused by parasitic elements such as, e.g., solder joint and Printed Circuit Board (PCB) track resistances. In addition, the measurement setup to assess the CMRR and DMRR includes a residual mismatch. The operation principle, the trimming procedure and a detailed explanation of the measurement setup as well as extensive measurement results are given in **Appendix B**.

5.3 Theoretical Analysis of the Influence of Amplitude and Phase Mismatch

The investigation of the active CM/DM noise separator revealed that the symmetry of the PCB layout as well as close matching of parasitic components is of predominant importance. Even small mismatches lead to a significant degradation in the separation capabilities. As illustrated with **Fig. 5.2**, the CE EMI test setup contains many other elements besides the noise separator that could equivalently deteriorate the overall CM/DM separation, since they

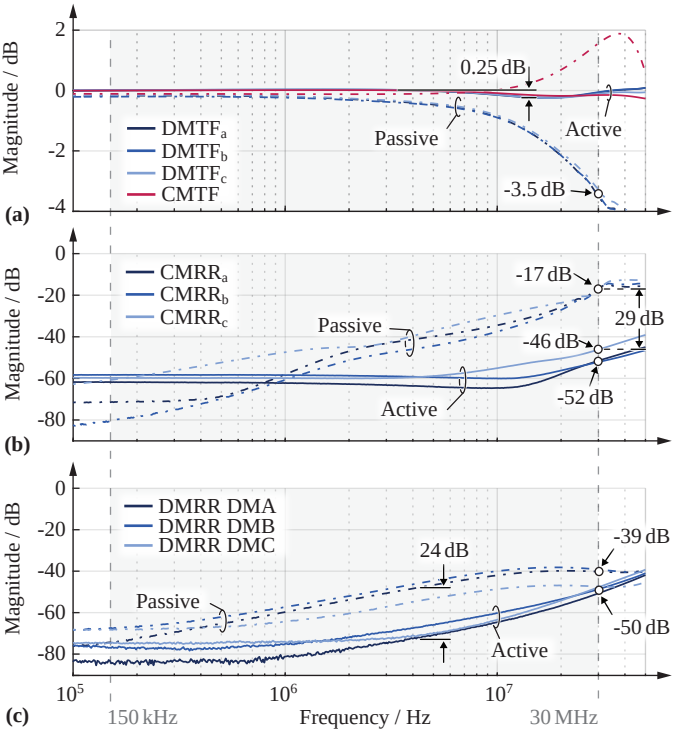


Fig. 5.7: Transfer Functions (TFs) and Rejection Ratios (RRs) for the active noise separator of [162] (continuous lines) and the passive separator described in [161] (dashed lines). **(a)** CMTF and DMTF, **(b)** CMRR for each DM output and **(c)** DMRR measured each time with one of the inputs set to zero (DM*i* means input *i* is set to zero).

are responsible for amplitude and/or phase mismatches in a three-phase transmission system (cf. **Fig. 5.3**). In this section, the CM-to-DM conversion for a certain amplitude and/or phase mismatch resulting from an asymmetric three-phase transmission system as indicated in **Fig. 5.8** is analyzed. In the course of this analysis, the separator itself is assumed ideal, i.e., with infinite CMRR and DMRR as well as perfectly flat CMTF and DMTF, such that the sole impact of external mismatches becomes evident. The amplitude and/or phase mismatches in an asymmetric three-phase transmission system lead to two conceptually identical phenomena. On the one hand a pure CM input voltage leads to a certain portion of DM components at the output (CM-

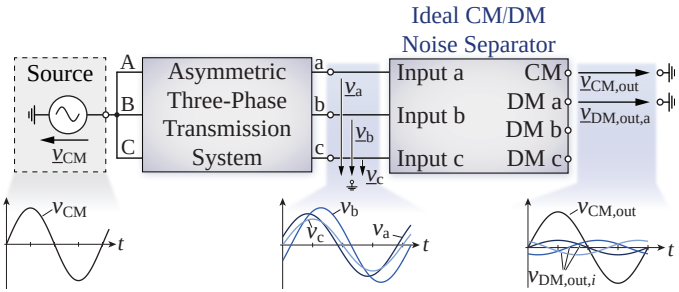


Fig. 5.8: Schematic representation of amplitude and phase mismatches in a asymmetric three-phase transmission system excited with a pure CM input voltage and the resulting CM-to-DM conversion.

to-DM conversion, indicated in **Fig. 5.8**) and on the other hand a pure DM input voltage causes a CM component at the output (DM-to-CM conversion). In **Sections 5.4** to **5.6** the influence of the elements in a practical EMI test setup according to **Fig. 5.2** will be experimentally analyzed in detail. For this, a known input signal (either CM or DM) is applied and the corresponding CM and DM voltages are measured using the active noise separator described in the previous section. The investigation is restricted to the case of a CM input and therefore the resulting CM-to-DM conversion for the following reasons:

i) To perform meaningful experiments it is crucial to apply pure CM or pure DM input signals to the system. The generation of three input voltages perfectly equal in amplitude and phase (pure CM input) is much easier to realize with high accuracy compared to a well-balanced three-phase DM voltage system. Yet, the latter would indeed be possible, e.g., with a very fast Field-Programmable Gate Array (FPGA) that generates the three 120° phase-shifted DM voltage components. In order to measure CM-to-DM conversions in the range of −60 dB, this would require a time resolution in the sub-nanosecond range as shown in [162], which is very challenging to achieve in practice.

ii) For a given amplitude or phase mismatch it was found that the worst-case CM-to-DM conversion is more pronounced compared to the reciprocal DM-to-CM conversion. Comparison plots for verification can be found in **Appendix D**.

iii) The exact CM noise source in a power converter is usually very difficult to predict in practice. Therefore, accurate measurements for this case are very valuable.

Fig. 5.9: Amplitude and phase mismatches at the output of an unsymmetric three-phase transmission system and related characterization with a CM-to-DM conversion. Input channel *a* is treated as reference and input voltages *b* and *c* show amplitude/phase mismatches with respect to voltage *a*. **(a)-(c)** Considering only an amplitude mismatch V_b/V_a and V_c/V_a and **(d)-(f)** considering only a phase mismatch φ_{ab} and φ_{ac}. The CM-to-DM output *c* conversion is identical to the CM-to-DM output *b* when the two amplitude ratio/phase-shift axes are flipped.

The remainder of this section theoretically analyzes the CM-to-DM conversion as a result of a general amplitude and/or phase mismatch.

5.3.1 Amplitude Mismatch

Given are three nominally identical sinusoidal test voltages $v_\mathrm{a}(t)$, $v_\mathrm{b}(t)$ and $v_\mathrm{c}(t)$ for channels *a*, *b* and *c* without phase-shift but different amplitudes V_a, V_b and V_c (cf. **Fig. 5.9 (a)**). With voltage *a* as reference, two relative amplitude mismatches $V_\mathrm{b}/V_\mathrm{a}$ and $V_\mathrm{c}/V_\mathrm{a}$ result, which lead to a CM-to-DM conversion. An idealized CM/DM separation according to (5.1) and (5.2) reveals the CM-to-DM component *i* conversion (CMDM_i) as

$$\mathrm{CMDM_a} = \frac{V_\mathrm{DM,a}}{V_\mathrm{CM,out}} = \frac{2 - V_\mathrm{b}/V_\mathrm{a} - V_\mathrm{c}/V_\mathrm{a}}{1 + V_\mathrm{b}/V_\mathrm{a} + V_\mathrm{c}/V_\mathrm{a}} \tag{5.9}$$

$$\mathrm{CMDM_b} = \frac{V_\mathrm{DM,b}}{V_\mathrm{CM,out}} = \frac{2 \cdot V_\mathrm{b}/V_\mathrm{a} - 1 - V_\mathrm{c}/V_\mathrm{a}}{1 + V_\mathrm{b}/V_\mathrm{a} + V_\mathrm{c}/V_\mathrm{a}} \tag{5.10}$$

$$\mathrm{CMDM_c} = \frac{V_\mathrm{DM,c}}{V_\mathrm{CM,out}} = \frac{2 \cdot V_\mathrm{c}/V_\mathrm{a} - 1 - V_\mathrm{b}/V_\mathrm{a}}{1 + V_\mathrm{b}/V_\mathrm{a} + V_\mathrm{c}/V_\mathrm{a}}. \tag{5.11}$$

The CM-to-DM conversion is normalized with respect to the CMTF (5.5), i.e., the CM-to-DM conversion is the ratio of the voltage amplitude $V_{\mathrm{DM},i}$ of CM component *i* divided by $V_\mathrm{CM,out}$. The conversion to DM components *a* and *b* ($\mathrm{CMDM_a}$ and $\mathrm{CMDM_b}$) for varying amplitude ratios $V_\mathrm{b}/V_\mathrm{a}$ and $V_\mathrm{c}/V_\mathrm{a}$ is depicted in **Fig. 5.9 (b)-(c)**, respectively. From (5.10) and (5.11) follows that the result for DM component *c* looks identical to the one for component *b* when the two amplitude ratio axes are flipped. In contrast, the result for the DM component *a* looks different, because input *a* is treated as reference channel. The $\mathrm{CMDM_a}$ is zero (minus infinity in dB) for $V_\mathrm{b}/V_\mathrm{a} + V_\mathrm{c}/V_\mathrm{a} = 2$, since the two mismatches cancel each other out perfectly. In the same way, for $2 \cdot V_\mathrm{b}/V_\mathrm{a} - V_\mathrm{c}/V_\mathrm{a} = 1$ there is no conversion from CM to DM component *b*. It is clearly visible, that an amplitude mismatch of only ±10 % can result in a CM-to-DM conversion up to −20 dB (indicated in **Fig. 5.9 (c)**).

5.3.2 Phase Mismatch

Similarly to an amplitude mismatch, the influence of a phase mismatch between three nominally identical test voltages $v_\mathrm{a}(t)$, $v_\mathrm{b}(t)$ and $v_\mathrm{c}(t)$ (cf. **Fig. 5.9 (d)**) on the CM-to-DM conversion for DM components *a* and *b* is shown in **Fig. 5.9 (e)-(f)**, again normalized with respect to the CMTF. Further, v_a is treated as reference voltage, i.e., v_b and v_c have a phase-shift of $\varphi_\mathrm{ab} = \varphi_\mathrm{b} - \varphi_\mathrm{a}$ and $\varphi_\mathrm{ac} = \varphi_\mathrm{c} - \varphi_\mathrm{a}$, respectively, with respect to v_a. When

flipping the phase mismatch axes in **Fig. 5.9 (f)**, the conversion from CM to DM component c results. It becomes clear that even small phase mismatches are related to a significant CM-to-DM conversion. Only in a very narrow range the corresponding phase mismatches cancel each other.

5.3.3 Combined Amplitude and Phase Mismatch

The analyses in the previous two subsections refer to cases where either only amplitude or only phase mismatches are present. In practice, usually both occur at the same time. For the HF EMI noise analysis the three-phase voltages are generally independent from each other meaning that the CM-to-DM conversion depends on four parameters ($V_\mathrm{b}/V_\mathrm{a}$, $V_\mathrm{c}/V_\mathrm{a}$, φ_ab and φ_ac). To reduce the complexity to two parameters, the two amplitude as well as the two phase mismatches are combined to two parameters e_V and φ, i.e., the maximum amplitude and/or phase mismatch between any two phases of the three-phase system. For each combination of phase mismatch φ and amplitude mismatch e_V **Fig. 5.10** shows the related worst-case CM-to-DM conversion for all possible combinations of phase-shifts $\{\varphi_\mathrm{ab},\, \varphi_\mathrm{ac}\} \in [-\varphi,\, \varphi]$ and amplitude mismatches $\{V_\mathrm{b}/V_\mathrm{a},\, V_\mathrm{c}/V_\mathrm{a}\} \in [1/e_\mathrm{V},\, e_\mathrm{V}]$ of test voltages v_a, v_b and v_c. A value of $e_\mathrm{V} = 1$ means that there is no amplitude mismatch. The conversion from CM to DM component a (**Fig. 5.10 (a)**) and b (**Fig. 5.10 (b)**) are depicted. The conversion to DM component c is identical to DM component b because only the worst-case of all possible mismatch combinations is considered. For the same reason the surfaces in **Fig. 5.10** are monotonically increasing with increasing φ and e_V. The slightly different appearance of the surfaces for DM output a and b is due to the choice of channel a as reference. The CM-to-DM conversion is normalized with respect to the CMTF (5.5) and the plots in **Fig. 5.10** therefore illustrate the CM-to-DM conversion relative to the actual CMTF. This will facilitate the comparison with actual measurements as will be seen later.

Based on the theoretical calculations, the CM-to-DM conversion resulting from various sources of mismatch and asymmetry can be estimated based on the expected amplitude and/or phase mismatch. In the following sections, the most prominent effects are analyzed and experimentally verified.

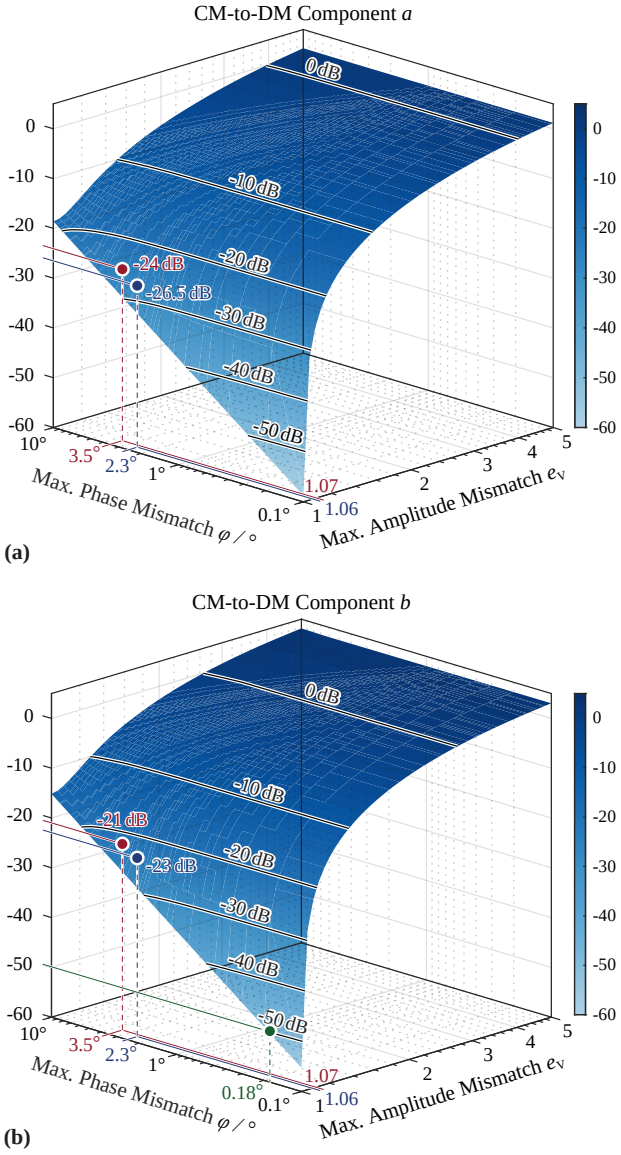


Fig. 5.10: Worst-case CM-to-DM conversions for **(a)** DM component a and **(b)** DM component b considering all possible combinations of amplitude mismatches $\{V_b/V_a,\ V_c/V_a\} \in [1/e_V,\ e_V]$ and phase mismatches $\{\varphi_{ab},\ \varphi_{ac}\} \in [-\varphi,\ \varphi]$ of inputs b and c assuming again input a as reference.

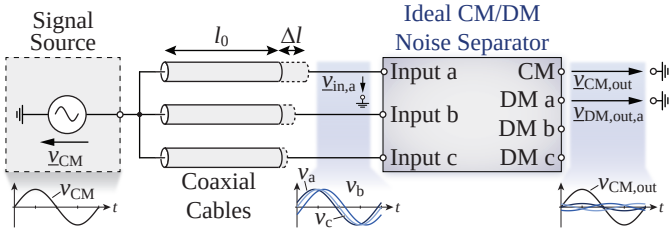


Fig. 5.11: Schematic representation of the CM-to-DM conversion introduced by connection cables with unequal length.

5.4 Mismatched Three-Phase Connections

In a first step, the impact of cables with unequal length for the connection of the EUT, LISN and noise separator is analyzed. In **Fig. 5.11** the provided measurement setup is shown, where a network analyzer [118] is used to apply a CM input voltage to the active noise separator and to measure the respective output voltages. The CM voltage $\underline{v}_{\mathrm{CM}}$ is connected to the noise separator inputs with three coaxial cables ($Z_0 = 50\,\Omega$, [171]) of nominal length l_0 and selectively added pieces with additional length Δl. Due to the three slightly phase-shifted signals at the separator inputs, a certain DM portion besides the CM component results at the separator output. **Fig. 5.12** shows the measurement results for a practically relevant case with short $l_0 = 22\,\mathrm{cm}$ cables and an additional piece with length $\Delta l = 4.8\,\mathrm{cm}$ realized with two Bayonet Neill Concelman (BNC) connection adapters (male-male and female-female connected together). All possible combinations of adding a length mismatch Δl to any of the cables are measured. For each DM output the corresponding best- and worst-case measurement result is plotted (shaded area). All other variants yield results in between the two extreme cases. It has to be noted, that the measurements in **Fig. 5.12** are obtained with the active noise separator according to **Figures 5.6** and **5.7** and therefore the separator CMRR could slightly influence the measurements. The dashed line represents the worst-case calculated CM-to-DM conversion for all considered length mismatches.

As expected, the respective best-case measurements occur when the cables of all channels have the same length l_0 or $l_0+\Delta l$. The results then closely match with the separator's inherent CMRR depicted in **Fig. 5.7**, which proofs that the absolute phase-shift has no influence on the CM-to-DM conversion but only the relative phase mismatch between the channels matters. In all channels the worst-case measurement closely matches the corresponding theoretical

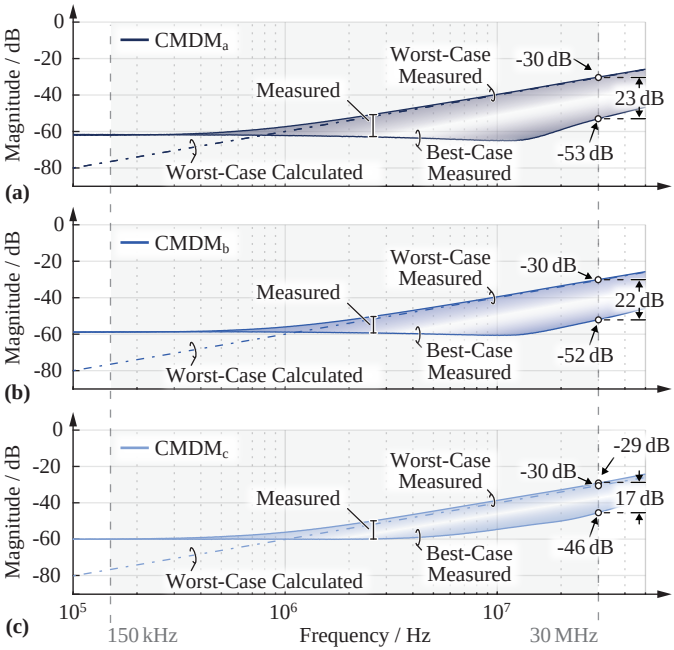


Fig. 5.12: Best- and worst-case CM-to-DM conversion measurements for all possible combinations of a cable mismatch at the noise separator inputs ($l_0 = 22\,\text{cm}$ nominal cable length, length mismatch $\Delta l = 4.8\,\text{cm}$). The calculated CM-to-DM conversion assuming an ideal noise separator is included for the worst-case length-mismatch configuration for each channel (dashed lines).

value in the frequency range above 1 MHz where the separator's inherent CMRR is much better compared to the CM-to-DM conversion resulting from the cable length mismatch.

The utilized coaxial cables show a very low insertion loss at the given frequency range ($< 0.1\,\text{dB/m}$ [171]) and therefore the amplitude is barely altered by the cable length mismatch. There is, however, a phase-shift

$$\Delta\varphi(f) = \omega \cdot \Delta t = 2\pi \cdot f \cdot \Delta t \tag{5.12}$$

linearly dependent on frequency f and time difference Δt (skew) between two signals. The latter is given by

$$\Delta t = \Delta l / v_{\text{cable}}, \tag{5.13}$$

with the cable length mismatch Δl and signal propagation speed v_{cable}. For the employed RG-58 coaxial cables [171] with $v_{\text{cable}} \approx 0.66 \cdot c = 2 \cdot 10^8$ m/s a length mismatch $\Delta l = 4.8$ cm leads to a phase-shift $\Delta\varphi \approx 2.6°$ at 30 MHz. The measurements of the worst-case in CM-to-DM conversion at 30 MHz in **Fig. 5.12** (−30 dB) coincide with the theoretical considerations visualized **Fig. 5.9 (e)-(f)** where the points corresponding to the respective worst-case ($\varphi_{\text{ab}} = \varphi_{\text{ac}} = -2.6°$ for channel *a* and $\varphi_{\text{ab}} = -2.6°$; $\varphi_{\text{ac}} = 0°$ for channel *b*) are highlighted. The results clearly show, that the connecting cables must be chosen with equal length. The separator itself achieves a CMRR of around −50 dB at 30 MHz, and in order to be not limited by the cable mismatch, the external CM-to-DM conversion must be better than −50 dB. This is achieved if it is ensured that the phase-shift is kept smaller than 0.18° (considering no amplitude mismatch, $e_{\text{V}} = 1$) according to **Fig. 5.10 (b)** (indicated with the green marker). Accordingly, using (5.12) and (5.13) the cable mismatch Δl must be lower than 3.3 mm. This clearly points out the importance of length-matched cables within the whole EMI test setup (power cables from the EUT to the LISN, coaxial cables from the LISN to the noise separator and from the noise separator to the test receiver).

Remark:
For the given case, only the length mismatch is considered as an influencing factor on the signal propagation time. However, a mismatch of the coaxial cable characteristic impedance could manifest itself in a slightly different signal propagation speed v_{cable} and thus also in a different propagation time. With the employed RG-58 coaxial cables, the measured CM-to-DM conversion matches very well with the calculated value obtained with the datasheet value of the signal propagation speed. Therefore, the assumption of a constant characteristic impedance $Z_0 = 50\,\Omega$ is sufficient in this case. Reflection coefficient measurements with the 22 cm BNC coaxial cable alone and the cable including the two BNC adapters, both terminated with the same 50 Ω load, show a change of less than 0.1 Ω in the characteristic impedance at 30 MHz between the two cases. For frequencies below some MHz hardly any effect is noticeable. With this same argumentation the realization of the length mismatch with BNC adapter pieces is justified.

5.5 Asymmetries in the LISN

5.5.1 Conventional LISN Measurement

To perform the noise separation, all three LISN output voltages must be measured at the same time. Since most three-phase LISNs do not support concurrent measurements of all three phases, in practice three single-phase

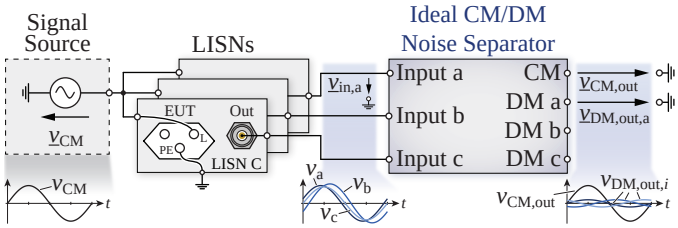


Fig. 5.13: Schematic representation of the CM-to-DM conversion introduced by asymmetries between the individual LISNs resulting in a certain DM portion besides the desired CM component at the separator outputs.

LISNs have to be used. They have to be designed according to the CISPR 16-1-2 (EN 55016-1-2) standard [160] with an EUT port input impedance $\underline{Z}_{\mathrm{EUT}}$ of nominally 50Ω||50 µH and a maximum magnitude deviation of ±20 % and phase deviation of ±11.5° (cf. **Fig. E.2** in **Appendix E.2**). A mismatch of $\underline{Z}_{\mathrm{EUT}}$ results in a mismatch of the TF from EUT input port to HF measurement output port, which means that for a pure CM input voltage at the EUT ports the measured HF output port voltages show an amplitude and phase mismatch. Fortunately, commercial LISNs show considerably tighter specifications than required by the standard. Particularly devices of the same type are very closely matched. Nevertheless, the influence of the residual asymmetry on the separation performance has to be analyzed in detail. **Fig. 5.13** shows the basic measurement setup used to evaluate the influence of LISN mismatches on the separation capability and schematically shows the aforementioned effect of CM-to-DM conversion. As mentioned in the beginning, three single-phase LISNs are utilized to allow a simultaneous measurement of all three phases. An additional advantage of using three single-phase LISNs is the superior shielding and isolation between the three measurement channels thanks to the individual enclosure of each LISN. This helps to suppress undesired cross-couplings between the three phases. In **Fig. 5.14 (a)** the TFs from EUT input to HF output for the three employed single-phase LISNs (Rohde & Schwarz ENV-216 [172]) are depicted (continuous lines: magnitude; dashed lines: phase). From the three TFs the calculated relative amplitude mismatch $e_{\mathrm{V,ab}}$ and $e_{\mathrm{V,ac}}$ and phase mismatch φ_{ab} and φ_{ac} is shown in **Fig. 5.14 (b)** and **(c)**. The measurements distinctly verify the close matching of the three LISNs but also reveal that even though the devices are the same model and type, there are still certain residual mismatches due to, e.g., internal component or assembly tolerances, in particular at high frequencies. It has to be noted that the pronounced high-pass behavior below 200 kHz results from the 50 Ω inner resistance of the network analyzer's generator port together with the

EUT port input impedance and is not inherent to the LISN itself. This effect could be calibrated out but since the amplitude and phase mismatches in this region are anyway very small, this is omitted here.

The illustrated measurements represent a practically relevant case, where two LISNs (*a* and *b*) were purchased at the same time whereas the third one (*c*) was obtained at a later date. Due to manufacturer side hardware revisions and improvements, the internal construction of the newer device may not be identical to the older ones. This becomes evident in **Fig. 5.14 (a)-(c)** where LISN *c* shows a slightly different transfer behavior, which manifests itself in a more pronounced amplitude and phase mismatch $e_{\mathrm{V,ac}} = V_{\mathrm{in,c}}/V_{\mathrm{in,a}}$ and $\varphi_{\mathrm{ac}} = \varphi_{\mathrm{c}} - \varphi_{\mathrm{a}}$ at distinct frequencies with respect to reference LISN *a*.

Based on the measured LISN transfer functions the CM-to-DM conversions to all DM output ports are calculated at each frequency individually under the assumption of an ideal separator (dashed lines in **Fig. 5.14 (d)**). Furthermore, the CM-to-DM conversions were measured using the active noise separator and are plotted in **Fig. 5.14 (d)** as well. It is seen that the measurement results are slightly worse than the calculated ones. There are multiple reasons for this such as the influence of the separator CMRR as well as possible coupling effects due to the connection of all three LISNs at the same time to the CM input. Those effects are not treated in the transfer function based calculation of the CM-to-DM conversion. It has to be noted that the plotted CM-to-DM conversions are already normalized with respect to the desired CMTF (5.5), i.e., the average of the three LISN transfer functions $\mathrm{LISN_{a,b,c}}$.

With a maximum amplitude mismatch $e_{\mathrm{V}} = 1.07$ and a maximum phase mismatch $\varphi = 3.52°$, the worst-case CM-to-DM conversion according to **Fig. 5.10** would be estimated as −24 dB for $\mathrm{CMDM_a}$ and −21 dB for $\mathrm{CMDM_b}$ and $\mathrm{CMDM_c}$ (indicated with red markers). The calculated results in **Fig. 5.14 (d)** are slightly better because the given combination of $e_{\mathrm{V,ab}}$, $e_{\mathrm{V,ac}}$, φ_{ab} and φ_{ac} does not represent the worst-case as depicted in **Fig. 5.10**, whereas the measured value becomes as low as −20.9 dB at 21.7 MHz. It has to be noted that in this particular case the estimation of the worst-case CM-to-DM conversion with help of **Fig. 5.10** using the worst-case amplitude and phase mismatches over the whole frequency range according to **Fig. 5.14** gives an over-pessimistic value because the three LISNs are closely matched over a wide frequency range and show considerable mismatches only at distinct frequencies.

In comparison with the performance of the separator itself (cf. **Fig. 5.7**), a significant degradation in the separation capabilities (around 20 dB or a factor of 10 at elevated frequencies) is observed. At some frequencies, however, the performance with the LISNs is — contrary to intuition — better than

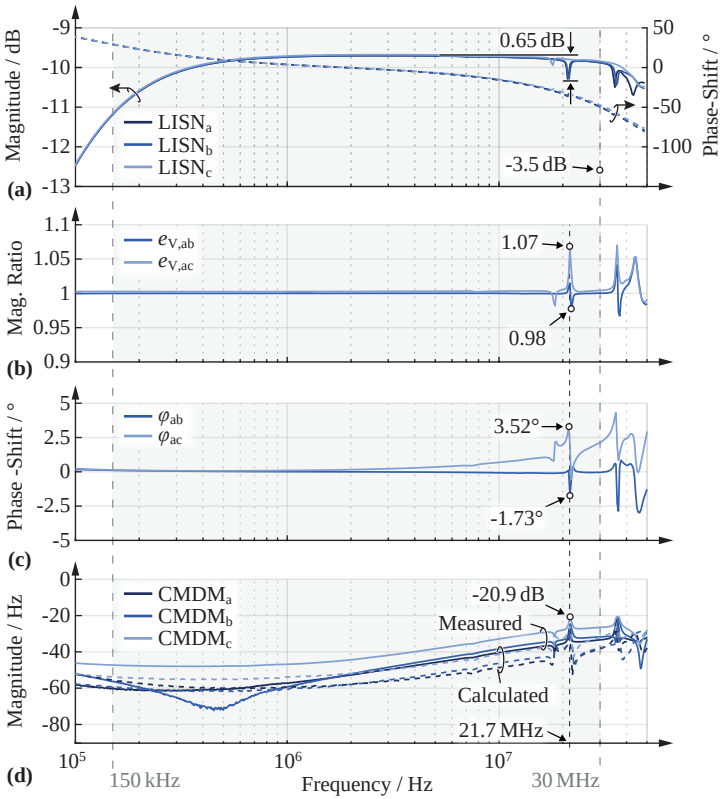


Fig. 5.14: (a) Transfer functions of the three single-phase LISNs (continuous: magnitude; dashed: phase), **(b)** the resultant calculated amplitude mismatches $e_{V,ab} = V_{in,b}/V_{in,a}$ and $e_{V,ac} = V_{in,c}/V_{in,a}$ and **(c)** the phase mismatches φ_{ab} and φ_{ac}; **(d)** shows the measured CM-to-DM conversions for each DM output channel including the finite CMRR of the noise separator (continuous lines) as well as the calculated CM-to-DM conversions assuming an ideally performing noise separator (dashed lines).

the performance of the noise separator alone. The reason is that external mismatches can counteract an internal mismatch from the separator and therefore improve the overall performance. In conclusion, it is generally inevitable to use LISNs of the exact same type and manufacturer and ideally from the same hardware revision to minimize the resulting imbalances.

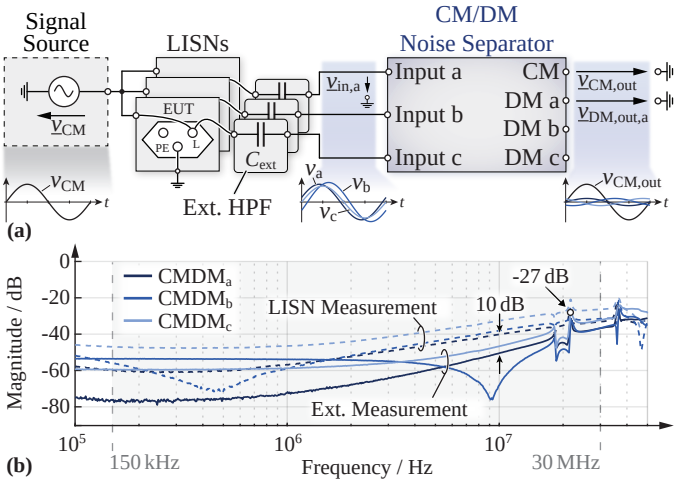


Fig. 5.15: (a) Extension of the LISN test setup with three external High-Pass Filters (HPFs) (C_{ext} together with separator input impedance) and **(b)** the resulting CM-to-DM conversion (continuous lines) in comparison with the direct LISN measurement (dashed lines) as presented before.

5.5.2 External High-Frequency Measurement

In a simplified form, the LISN HF measurement path can be described as first-order High-Pass Filter (HPF) formed by C_{HP} (cf. **Fig. 5.2**) and the 50 Ω termination. The high-pass behavior is required to attenuate any LF voltage (50/60 Hz fundamental components) that would otherwise saturate or even destroy the connected measurement equipment. With an external HPF connected at the EUT port (and with non-terminated LISN HF measurement port) to measure the EMI noise as shown in **Fig. 5.15 (a)**, potentially a closer matching can be achieved, since the LISN's internal measurement path is omitted. A certain influence of the slightly mismatched $\underline{Z}_{\text{EUT}}$ remains, since the signal source still sees a part of $\underline{Z}_{\text{EUT}}$ but the effect is less severe as verified with the CM-to-DM conversion measurements depicted in **Fig. 5.15 (b)**, again normalized with respect to the desired CMTF. The dashed lines correspond to the measurement with the LISN as seen in **Fig. 5.14 (d)**, whereas the continuous lines denote measurements with an external HPF, i.e., three matched external capacitors C_{ext} with a value of 140 nF, each in conjunction with the closely matched 50 Ω separator input impedance (cut-off frequency $f_{\text{c,HPF}} \approx 23$ kHz). Throughout almost the entire relevant frequency range a

lower CM-to-DM conversion is achieved with an improvement of at least 10 dB at 10 MHz and 6 dB (−27 dB in contrast to −21 dB, cf. **Fig. 5.14 (d)**) at the worst-case frequency of 21.7 MHz. For low frequencies the cancellation of error contributions of the separator itself and the external mismatches is very evident, particularly for channel *a*. It has to be noted that for $f > f_{c,HPF}$ the impedance seen by the EUT is primarily given by the 50 Ω input resistance of the noise separator. Therefore, in the frequency range of interest from an impedance point of view it does not matter whether the LISN's internal measurement path or the external HPF is used. This is further justified in **Appendix E.2** that shows the simulated $\underline{Z}_{EUT}$ for both cases together with the CISPR 16-1-2 limits.

Remark:
Some LISNs feature a more complex HF measurement path with higher order HPFs including capacitive and inductive filter elements [172]. This makes close matching even more difficult. Therefore, in the interest of high symmetry, a first-order HPF is clearly favorable. Additional closely matched 50 Ω attenuators can be inserted between the external HPF and the noise separator inputs to ensure sufficient attenuation of the LF voltage components, if required.

5.6 Three-Phase EMI Filter

The primary goal of precise EMI CM/DM noise separation is the identification and adjustment of insufficiently performing EMI filters in case of exceeding the limiting values. Furthermore, the measured noise voltages can be compared with expected values obtained from calculations or simulations. The corresponding models can then be adapted and improved. Provided there is a setup with very closely matched connections and highly symmetric LISNs, a very critical part for accurate splitting of CM and DM EMI noise is the EMI filter itself. Even a very simple filter structure such as the single-stage second order inverter output filter shown in **Fig. 5.16 (a)** can be responsible for the conversion of CM to DM noise and vice versa due to e.g. mismatches of the parasitic elements and the PCB layout or unwanted couplings k_{par} of magnetic and capacitive elements within a phase and also between the phases [173, 174]. The EMI filter in **Fig. 5.16 (a)** is a combined CM and DM filter with dedicated components for DM filtering (blue) and CM filtering (red and blue). Typically, the CM inductance $L_{f,CM}$ realized on a high permeability core is much larger than the DM filter inductance $L_{f,DM}$, which could be solely the stray inductance of the CM inductor. Therefore, the CM capacitance $C_{f,CM}$ is considerably smaller compared to the DM capacitance $C_{f,DM}$, assuming comparable attenuation requirements for CM and DM components (similar

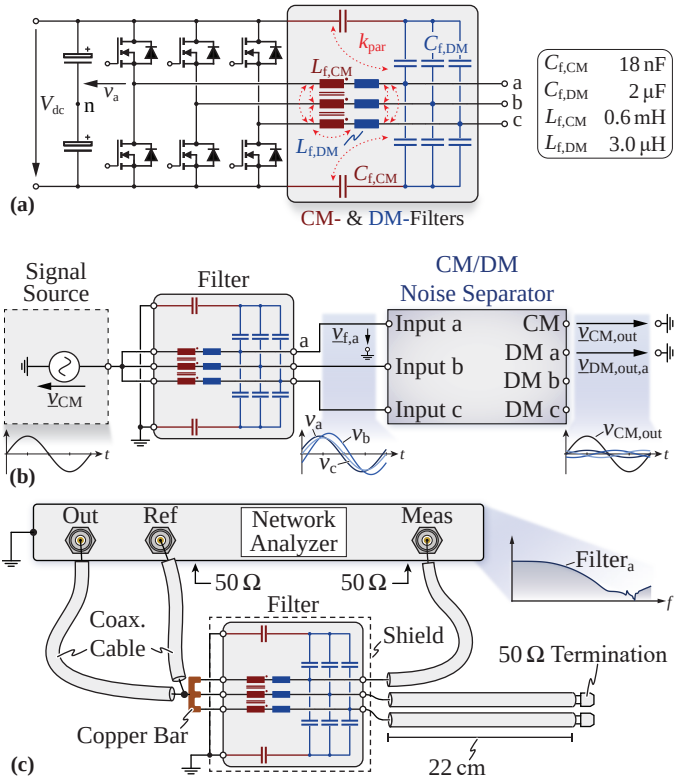


Fig. 5.16: (a) Three-phase inverter with a single-stage CM/DM output filter, where the components highlighted in red are solely responsible for CM filtering whereas the blue elements are primarily effective for DM filtering. The parasitic coupling k_{par} (magnetic or capacitive) between the individual components is highlighted. **(b)** configuration to measure the filter CM transfer function and the CM-to-DM conversion. **(c)** measurement setup to characterize the individual phase filter transfer functions with a network analyzer.

filter cut-off frequency). This particular single-stage filter is designed for a nominal CM attenuation of around −35 dB at the inverter switching frequency $f_{sw} = 350$ kHz.

In **Fig. 5.16 (b)** the filter evaluation measurement setup for a pure CM excitation is shown. The three inputs of the filter are excited simultaneously with a CM voltage source and the dc link terminals are both shorted to ground.

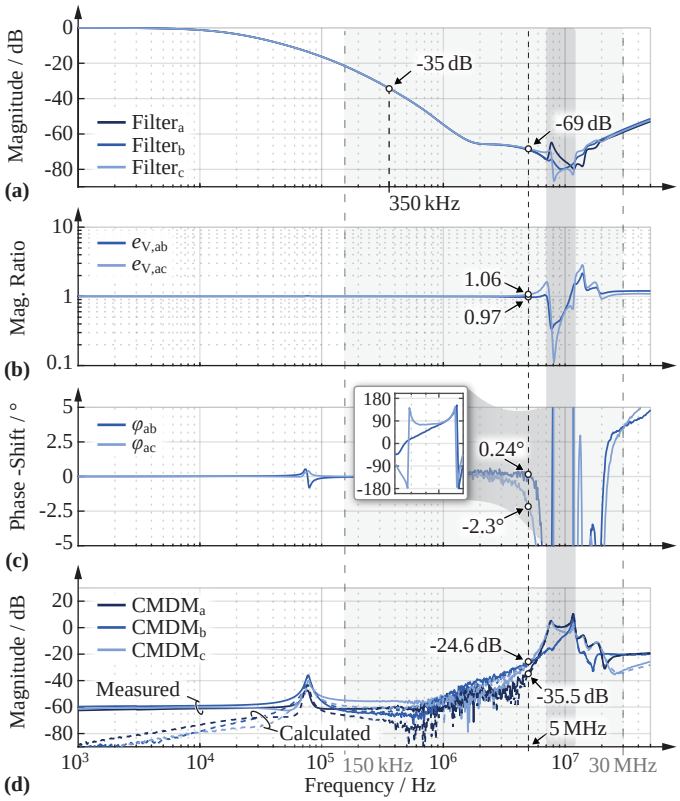


Fig. 5.17: (a) Measured filter CM transfer functions and therefrom **(b)** the calculated amplitude mismatches $e_{V,ab}$ and $e_{V,ac}$ and **(c)** the calculated phase mismatches φ_{ab} and φ_{ac}; **(d)** calculated CM-to-DM conversion based on the amplitude and phase mismatches as well as the CM-to-DM conversion measured using a three-phase active noise separator.

The filter TFs $\text{Filt}_i = \underline{v}_{f,i}/\underline{v}_{CM}$ from CM input to filter output i ($i \in \{a, b, c\}$) are measured using a network analyzer in a direct measurement configuration without the noise separator (cf. **Fig. 5.16 (c)**). They are depicted in **Fig. 5.17 (a)** together with the calculated relative amplitude and phase mismatches e_V and φ (**Fig. 5.17 (b)-(c)**). Finally, **Fig. 5.17 (d)** shows the calculated CM-to-DM conversion based on the measured filter TFs under the assumption of an ideal noise separator (dashed lines) together with the measured CM-to-DM conversion using the active noise separator (continuous lines). Both are normalized

with respect to the (desired) filter CMTF. Hence, a CM-to-DM conversion of e.g. −20 dB means, that for a pure CM input the output voltage measured at the separator's DM output port is ten times lower than the one measured at the CM output port. Because the calculated CM-to-DM conversion is obtained with phase sensitive additions and subtractions, it is very prone to measurement errors and therefore the filter TFs must be measured with the highest possible accuracy. In addition, the desired CM transfer function itself already shows significant attenuation at high frequencies and the CM-to-DM conversion is expected to be even lower (i.e., the normalized CM-to-DM conversion should be lower than 0 dB). To achieve accurate results for the case at hand, the filter is shielded with metal plates, the applied CM input voltage is measured directly at the filter input terminals (reference measurement cf. **Fig. 5.16 (c)**) and it is ensured that all outputs are connected with equally long cables and are terminated with 50 Ω. The 50 Ω terminations prevent potential reflections in the coaxial cables used to connect the network analyzer and ensures equal filter loading for all measurement scenarios. The usage of a 50 Ω termination impedance is typically found in practical applications as most measurement devices expect a 50 Ω environment. Moreover, it is a de facto standard scenario that allows to compare different measurements. Finally, the LISN EUT ports feature an impedance close to 50 Ω over the specified frequency range (cf. **Appendix E.2**), which further justifies the measurement in a 50 Ω environment. It has to be said, however, that there is a fundamental uncertainty whether the obtained performance measured with a certain test setup corresponds to the achieved performance in a practical setup.

Fig. 5.17 shows that the three channels are matched very closely up to 2 MHz resulting in a normalized CM-to-DM conversion of no more than −40 dB. At 2 MHz the desired CM attenuation of the filter is as low as −65 dB, which means the residual voltage at the DM output ports is attenuated by −105 dB (a factor of 177′000) with respect to the applied CM input voltage. This illustrates the high required measurement dynamic range. The measured CM-to-DM conversion conforms very well with the calculated one, particularly in the relevant frequency range for CEs. Only for frequencies below 50 kHz the active separator limits the performance due to its finite CMRR. As an example, the maximum magnitude mismatches $e_{\mathrm{V,ab}} = 0.24°$ and $e_{\mathrm{V,ac}} = 1.06$ and phase mismatches $\varphi_{\mathrm{ab}} = 0.97$ and $\varphi_{\mathrm{ac}} = -2.3°$ are indicated in **Fig. 5.17** at $f = 5$ MHz to allow a comparison of the measured CM-to-DM conversion with the theoretically expected worst-case values. In the diagram of **Fig. 5.10** the corresponding point with $e_{\mathrm{V}} = \max\left\{e_{\mathrm{V,ab}},\, e_{\mathrm{V,ac}}\right\} = 1.06$ and $\varphi = \max\left\{\varphi_{\mathrm{ab}},\, \varphi_{\mathrm{ac}}\right\} = -2.3°$ is indicated with blue markers. The measured CM-to-DM conversions of −35.5 dB for channel a and −24.6 dB for channels

b and c are slightly better than the predicted worst-case values of −26.5 dB and −23 dB (cf. **Fig. 5.10**), respectively. Again, this is because the relative filter amplitude and phase mismatches at $f = 5$ MHz do not correspond to the worst-case of all possible mismatch combinations $e_{V,ab}$, $e_{V,ac}$, φ_{ab} and φ_{ac} in the range of $[1/e_V, e_V]$ and $[-\varphi, \varphi]$.

The CM-to-DM conversion is attributed to filter asymmetries with very high confidence, given the very high performing noise separator together with the carefully matched measurement setup. In the frequency range between 7 and 12 MHz (highlighted in gray) the normalized CM-to-DM conversion is greater than 0 dB, meaning that even for a pure CM filter input voltage, the DM components of the output voltages have a larger magnitude compared to the CM component. At high frequencies this is of particular concern because the desired CM filter attenuation is very strong, i.e., the CM output signal is very small, but at the same time mismatches are typically more pronounced. Possible examples are the large phase mismatch (zoomed view in **Fig. 5.17 (c)**) and the impact of unwanted couplings k_{par} attributed to parasitic elements of the employed filter components (self-parasitics as well as parasitic couplings due to the component placement) and the PCB layout. A very important note is that the typically employed layout of a three-phase EMI filter consists of three identical filter cells (one for each phase) placed next to each other on a PCB. This arrangement has an inherent asymmetry, since the middle cell is surrounded by two other filter cells whereas the outer cells are on one side either close to a (shielding) enclosure or other components. This inherent asymmetry also remains if the three-phase EMI filter is shielded but is minimized if the shield is placed with a sufficient distance as it is done in this chapter. Generally, a certain mismatch can always be attributed to geometry and not only to component and layout tolerances.

The measurements manifestly show that a high-performance noise separator can not only be used to identify CM and DM components in the total EMI noise spectrum but also helps to reveal filter asymmetries. In contrast to consecutive measurements of the three filter TFs and the calculation of the CM-to-DM conversion, the direct measurement is more robust, since potential repeatability errors of the network analyzer and small changes in the setup and/or the surrounding have no influence on the measurement as all three channels are measured concurrently.

It is evident that for a normalized filter CM-to-DM conversion approaching 0 dB, no statement regarding the origin of the CEs (CM or DM) can be made by simply looking at the measured separator output voltages, even if both, the separator and the whole EMI test setup are perfectly symmetric. Therefore, from an EMI characterization point of view, a symmetric filter construction and layout is extremely important and should be taken into con-

sideration as a design criterion together with more prominent measures like overall size, losses, weight and cost. As a further benefit, careful filter design and layout allows to reduce the typically included attenuation margins, since the real filter behavior matches more closely with the simulated behavior. This in turn reduces the overall filter size.

5.7 Conclusion

The decomposition of the total Electromagnetic Interference (EMI) noise into its Common Mode (CM) and Differential Mode (DM) part is a useful tool for power electronics engineers, who want to design/commission a converter that complies with Conducted Emission (CE) regulations. A noise separator is used in order to realize the CM/DM EMI noise decomposition. Typically, a high-performance of the CM/DM noise separator, characterized by a high Common Mode Rejection Ratio (CMRR) and Differential Mode Rejection Ratio (DMRR), is required. However, this is not sufficient. It is shown in this chapter that even with an ideally performing noise separator (infinite CMRR and DMRR), the results can be ambiguous due to nonidealities in the test setup. It is deduced that the nonidealities mainly originate from asymmetries in the connection cables, the Line Impedance Stabilization Network (LISN) and the EMI filter of the converter. The nonidealities of the test setup result in an unwanted conversion of CM into DM and vice versa. For example, if the Equipment Under Test (EUT) generates purely CM noise, a CM-to-DM noise conversion occurs due to asymmetries in the test setup, before the EMI noise is processed by the separator.

This chapter quantitatively characterizes the CM-to-DM noise conversion (and not the reciprocal DM-to-CM noise conversion) because:

i) The application of a pure CM signal to all inputs for testing purposes is much more convenient compared to three perfectly 120° phase-shift DM signals.

ii) For a given mismatch the CM-to-DM conversion is typically more pronounced compared to the contrary DM-to-CM conversion.

iii) The CM noise is the main concern on converter CE compliance at high frequencies.

Three identical voltages at the separator input would be expected in case of a pure CM noise source and an ideal test setup. In reality, three marginally different voltages appear at the separator input due to the nonidealities of the setup. Namely, the three input voltages exhibit a phase mismatch φ

and/or an amplitude mismatch e_V. In a first step, a theoretical analysis is performed, where the CM-to-DM conversion (in dB) is related to the phase and/or amplitude mismatches.

The theoretical considerations are first applied on the connection cables, which cause a phase mismatch but no significant amplitude mismatch. It is calculated that for limiting the CM-to-DM conversion to −50 dB (i.e., only around 0.3 % of the generated CM noise is converted into DM noise due to the cable) a phase error of smaller than 0.18° must be achieved. At the frequency of 30 MHz (maximum frequency of the CE compliance test range) the 0.18° correspond to only 3.3 mm cable length mismatch. The very strict tolerance in the millimeter range highlights the importance of an absolutely symmetric test setup, as well as the sensitivity of the EMI measurements with respect to the connection cables.

Subsequently, the impact of imbalances in the LISN, which is placed between the EUT and the separator, is quantified. It is shown, by means of transfer function measurements, that the LISN causes both, phase and amplitude mismatch to the EMI noise. The worst-case CM-to-DM conversion for a given amplitude and phase mismatch is theoretically derived and experimentally measured and a reasonably good matching between the two values is observed. The CM-to-DM conversion of the LISN is significant with up to −21 dB (almost 10 % of the CM EMI noise is converted into DM noise). In order to address this problem, it is suggested to place an external High-Pass Filter (HPF) between the LISN and the separator to measure the EMI noise. Experimental results show that this reduces the CM-to-DM conversion by at least 10 dB over a wide frequency range.

Finally, the influence of the EMI filter is analyzed. Layout mismatches and component parasitic elements can result in inherent conversion of CM noise at the filter input into DM components at the filter output terminals. This means, that even with an ideal measurement setup and a perfect noise separator, the theoretical CM and DM noise sources cannot be identified correctly. A CM noise source for example would partially appear as DM component at the separator due to the parasitic CM-to-DM conversion in the CM filter part, and therefore could be wrongly attributed to an insufficiently performing DM filter stage. Therefore, the importance of matched components and a symmetric layout of the EMI filters becomes evident. With a high-performance noise separator such filter asymmetries and/or parasitic coupling effects that result in a CM-to-DM conversion (and vice versa) can be easily identified. For this, the filter is excited with a CM noise source and the outputs are measured with the noise separator that extracts any unwanted DM components, attributed to CM-to-DM conversion in the filter. With help of such measurements, converter simulation models can be successively improved and the predicted

results become more reliable, which greatly facilitates the EMI pre-compliance testing.

As a final remark, it should be highlighted that small mismatches already have a severe impact on the CM-to-DM conversion at the upper frequency limit of 30 MHz (according to the CISPR standards). In aerospace applications for example, different norms such as the DO-160 [175] apply, which define an upper frequency limit of 152 MHz for the CE. It is clear that at such frequencies the fulfillment of the symmetry requirements is even more important as, e.g., a cable length mismatch of 4.8 cm would already result in a CM-to-DM conversion of around −16 dB (compared to −30 dB at 30 MHz, i.e., around a factor of 4 higher).

6 Conclusion and Outlook

For the transition from fossil-based to modern renewable energy sources with the aim to reduce the worldwide carbon dioxide emissions, *Next Generation Power Electronics (NGPE)* play a pivotal role in power conversion, distribution and processing. With increasing share of modern renewable energies as well as the emergence of electrification in the transportation sector (Electric Vehicles (EVs), More Electric Aircraft (MEA)), primary energy production and consumption becomes more and more decentralized, which not only leads to a significant increase in the number of installed power electronic converter systems but also demands for ever higher efficiencies — of particular importance, e.g., for the increasingly widespread availability of ultra-fast charging stations for EVs or in applications where multiple converter stages are cascaded, e.g., in Photovoltaic (PV) power plants with intermediate energy storage systems and grid-interfacing inverters — and higher power densities, a key factor to enable, e.g., motor integrated drive systems or ultra-compact on-board chargers in EVs. Recent technological advances in the field of power electronics such as the emergence and widespread use of Wide-Bandgap (WBG) power semiconductors are key driving factors for this transition, especially because they enable approximately one order of magnitude faster switching frequencies, which results in a significant reduction of the size and mass of passive filter and storage elements (capacitors and inductors). Moreover, higher switching frequencies enable substantially faster converter dynamics, beneficial, e.g., in highly dynamic drive systems for industry automation systems or in general-purpose high-speed Power Amplifiers (PAs) for laboratory use. Nevertheless, these advantages also entail various challenges in different fields such as converter design (driving stages, Printed Circuit Board (PCB) layout, thermal limitations due to higher loss densities resulting from miniaturization), required measurement technology (monitoring and supervision circuit, current and voltage measurements for highly dynamic closed-loop operation) and Electromagnetic Interference (EMI) (considerably

faster switching transitions of WBG semiconductors generate higher frequency noise content), which potentially constrain or even inhibit the use of WBG in certain applications today.

This thesis addresses the aforementioned challenges starting with contributions on converter design, illustrated with the example of an Ultra-High Bandwidth Power Amplifier (UHBWPA) for Power-Hardware-in-the-Loop (P-HIL) test environments — an invaluable framework to characterize and verify the operation of NGPE, then continuing with considerations on advanced measurement technologies required to commission and operate such high-performance converter systems, and finally on the systematic assessment of conducted EMI noise by separation of the total noise into its Common Mode (CM) and Differential Mode (DM) parts.

In the following, the main findings and proposed concepts related to each considered aspect are briefly summarized and an outlook discussing ideas for possible future research on each topic is presented.

6.1 Converter Design

Summary

P-HIL test environments largely rely on high Bandwidth (BW) PAs to emulate fast transient phenomena and to ensure accurate tracking of the intended system behavior. That is why in **Chapter 2** a purely switch-mode UHBWPA with a large-signal (or full-power) BW of 100 kHz and an output power of 10 kVA (for a single-phase module) is presented, which compared to state-of-the-art alternatives operating in linear-mode offers substantial benefits in terms of efficiency and realization size. However, the BW of switch-mode PAs is fundamentally limited by the corner frequency of the necessary output filter and consequently by the maximum possible switching frequency. Advanced converter topologies, namely a combination of series- and parallel-interleaved Switching Cells (SCs) (one SC is composed of a half-bridge plus dc link capacitor), are analyzed and evaluated to achieve an effective switching frequency of 4.8 MHz, while keeping the efficiency under full-load operation and to a large extent also under partial-load operation above 95 %. The realized hardware demonstrator has a power-density of 25 kW/dm^3 and fulfills the efficiency target in a wide range of output frequencies and output powers (95.8 % in the nominal operating point at maximum output frequency and full output power of 10 kW (ohmic load)). Despite operation in open-loop the proposed system features excellent output voltage quality, i.e., all fundamental frequency harmonics are attenuated by more than 40 dB.

Outlook

The presented Gallium-Nitride (GaN)-based UHBWPA should serve as a demonstrator for exploring the limits in terms of maximum feasible switching frequency while meeting certain efficiency targets. It clearly demonstrates that extremely compact systems can be realized with fast switching WBG semiconductors, but also points out critical aspects that need to be addressed in the future to unlock the full potential of WBG power semiconductors. An improvement of the packaging, in particular the elimination of bonding wires to connect the die, i.e., a significant reduction of the internal lead inductances, is indispensable to benefit from even faster switching transients offered by the WBG technology and without having to accept massive overvoltages and undesired oscillations in the power path or to intentionally limit the switching transition speed penalized by higher losses. An encouraging approach now being explored by most manufacturers is to replace the bonding wires with copper clips, providing up to three times lower package inductance and significantly improved thermal performance, as shown for example in [176]. In general, the thermal performance is of major importance, especially in applications such as UHBWPAs with extremely high switching frequencies and where full ZVS cannot be guaranteed. Advanced Thermal Interface Materials (TIMs) with very low thermal impedance (high thermal conductivity) and at the same time high electrical isolation capabilities [177, 178] can in conjunction with the aforementioned optimized semiconductor packages drastically lower the overall thermal resistance from junction to a reference heatsink/coldplate temperature, which currently is the bottleneck in the presented implementation ($R_{\mathrm{th,j-c}} = 1\,\mathrm{K/W}$ from junction to package case and $R_{\mathrm{th,c-hs}} \approx 1\,\mathrm{K/W}$ from package case to the coldplate). An improvement of both contributors by a factor of two is feasible and would halve the temperature difference between heatsink/coldplate and semiconductor junction. This on the one hand lowers the conduction losses (given the pronounced temperature dependence of the on-state resistance in GaN devices) and on the other hand increases lifetime and reliability, which scales inversely with device operating temperature [179], described, e.g., with the Arrhenius equation for reliability [180].

Integration of the Gate Driver (GD) stage directly into the semiconductor package would minimize the parasitic gate commutation loop, which translates into a significant performance gain (faster switching transitions, safe turn-off state, even with lower negative gate bias voltage and thus, lower reverse conduction losses during the dead time). Furthermore, some basic monitoring and supervision functions such as temperature and overcurrent measurements could also be integrated directly into the power semiconductor package. Both are important measures that must be incorporated in future

semiconductor research and developments, again with the aim of exploiting the full potential of the WBG technology.

Apart from semiconductor-specific advances, digital control of converters with high switching frequencies demands High-Resolution PWM (HRPWM) with sub-nanosecond time steps in order to precisely apply the required voltage-time area to the output filter inductor and consequently to minimize the output voltage distortions. This in turn calls for several hundred to thousand computation cycles per switching period. There is ongoing research that analyzes the best possible implementation method for such a HRPWM directly in hardware to benefit from the extensive parallelization capabilities of Field-Programmable Gate Arrays (FPGAs) [181]. Further improvements in output voltage quality are enabled by sophisticated correction/feed-forward terms like current-dependent dead time correction, again with the aim to apply the correct voltage-time area to the output filter inductor as mandated by the subordinate current and/or voltage controller.

Finally, with the virtually limitless application scenarios of the presented UHBWPA, various control strategies can be implemented to emulate any arbitrary power source and sink behavior or even to embed complete dynamic converter and/or machine models, which thanks to the very high large-signal BW offers new possibilities, e.g., to include the capacitive properties of different machine designs with parameters extracted from Finite Element Method (FEM) simulations without cost- and time-consuming realization of multiple hardware prototypes.

6.2 Measurement Technology

Summary

Converter systems with higher switching frequencies and higher desired control dynamics have increased requirements for the measurement systems to be used, namely in terms of BW, accuracy and in case of floating measurements on fluctuating reference potentials also in terms of CM robustness (quantified with a high Common Mode Rejection Ratio (CMRR)). For closed-loop current-mode or voltage-mode control operation, converter-embedded current and voltage measurements are needed, where in particular for the former it is challenging to find compact dc-capable sensors with BWs of several tens of MHz. However, there is excellent market coverage with compact off-the-shelf dc and Low-Frequency (LF) current sensors, e.g., based on the Hall-effect, but their maximum BW is limited to below 1 MHz. Therefore, **Chapter 3** investigates approaches to combine commercially available dc/LF sensors with suitable High-Frequency (HF) sensors for a BW extension of the overall

current measurement system to several tens of MHz in order to enable the required fast current measurements for converters switching in the multi-MHz range. Based on the classical Rogowski coil, a galvanically Isolated Inductor Voltage Sensing (IVS) approach is introduced, which in case of already present output filter inductors is particularly attractive, since it only requires the addition of few turns on the magnetic core to achieve a HF measurement BW of around 10 MHz and superior CM robustness, i.e., immunity to high $\mathrm{d}v/\mathrm{d}t$ exposures. Alternatively, a small Current Transformer (CT) (volume approximately 1.2 cm^3) can be used to extend the BW to around 35 MHz. To simplify the manufacturing and to avoid manual winding of cores, in a further step, PCB integrated HF Pickup Coils (PUCs) are investigated. With a suitable coil geometry, extremely compact HF sensors (volume approximately 0.2 cm^3) with a BW of more than 50 MHz and a CMRR of almost 100 dB are possible. The required processing circuit to combine the dc/LF and the HF signal is realized as compact as possible and there is no noticeable impact of the LF/HF signal combination in the frequency response.

While non-isolated high BW voltage measurements are implemented relatively straight-forward, **Chapter 4** proposes a concept for galvanically isolated voltage measurements that are referred to rapidly changing reference potentials (several hundreds to several thousands of volts, changing with a $\mathrm{d}v/\mathrm{d}t$ of more than 100 kV/µs), such as for example, the High-Side (HS) Gate-Source (GS) voltage measurement in a half-bridge composed of WBG semiconductors. It is derived what minimum CMRR over the full considered frequency range is required to limit the measurement error in the time-domain below a certain limit. Thereby, it is found that only the switched voltage and the voltage transition rate $\mathrm{d}v/\mathrm{d}t$ have to be considered and not the actual converter switching frequency. A measurement system with a BW of 130 MHz and superior CMRR of more than 100 dB at 100 MHz is proposed and key design factors to achieve this outstanding performance are highlighted.

Outlook

While the presented high-performance measurement systems are already realized in a very compact manner that allows to embed them into current converter systems (the proposed current measurement system for example is part of the Three-Level Triple-Interleaved (3L3) converter proposed in this thesis and is also used in the system presented in [27]), continuing miniaturization necessitates even further size reduction. Eventually, complete integration of the measurement systems into the converter is inevitable because more and more, physical access with conventional measurement equipment (oscilloscope probes, external current sensors, etc.) is simply not possible anymore

or would require unnecessarily large laboratory setups with long connection leads, which are undesirable due to the above-mentioned problems arising with large parasitic inductance, especially in the power and gate commutation paths.

In the exemplary case of the presented isolated voltage measurement system, the Analog Front-End (AFE) and digitizing stage could be integrated into a single chip, which not only reduces the overall power consumption but also minimizes the connection distance between measurement point and digitizing stage, which improves the CMRR.

As a vision for future ultra-compact "smart" converter systems one could think of having all required measurements fully integrated and providing only (digital) data interfaces (electrical or preferably optical) to connect to a host unit for accessing all internal signals of interest (voltages and currents) in order to enable online (and continuous) health and condition monitoring.

6.3 Conducted EMI Noise Assessment

Summary

Along with the numerous advantages of high switching frequencies and fast switching transitions enabled by modern WBG semiconductors, one of the major challenges is to ensure compliance with regulatory EMI standards, mainly for two reasons. On the one hand, the device switching frequencies may lie within the regulated Conducted Emissions (CEs) frequency band (150 kHz to 30 MHz) and on the other hand, the faster voltage transitions (high $\mathrm{d}v/\mathrm{d}t$) lead to a significant HF noise contribution (in particular CM noise), which requires carefully designed input and output filters with sufficient attenuation also at MHz frequencies [182]. In this context, a systematic approach to assess the CEs by means of separate measurement of CM and DM noise components is of clear advantage for an optimized filter design and also to improve pre-established EMI noise models used in circuit simulation. Therefore, **Chapter 5** first introduces a three-phase active CM/DM EMI noise separator that offers superior separation capabilities, i.e., a CMRR and Differential Mode Rejection Ratio (DMRR) better than 50 dB over the full considered frequency range. This means, that a CM component at the three-phase input terminals is attenuated by more than a factor 300 at the DM output terminals (and vice versa, a DM component is attenuated by more than a factor 300 at the CM output). Afterwards, it is shown that a high-performance noise separator is not sufficient but rather the complete EMI test setup must be considered and analyzed for asymmetries that lead to unwanted cross-conversion of CM into DM and vice versa. Thereby, the connection

cables, the Line Impedance Stabilization Networks (LISNs) as well as the EMI filters themselves are identified to have a significant impact with a degradation of the separation capabilities by up to 30 dB. Practical guidelines for building an improved EMI test setup, e.g., with help of an external High-Pass Filter (HPF) as interface between Equipment Under Test (EUT) and EMI test receiver, are given.

Outlook

Raising awareness of the importance of a fully symmetric test setup in order to make a clear statement about the distribution of CM and DM noise components is a very important finding of this work. In fact, apart from a high-performance noise separator, also the utilized cables between EUT and LISN (power cables) and between LISN and EMI test receiver (coaxial cables), the utilized LISNs and the filter stages on the EUT (component values, placement and layout) must be absolutely symmetric. While a closely matched filter design and symmetric cabling is under control of the design/test engineer, the asymmetries found in commercial LISNs are more difficult to address, primarily for two reasons:

i) Three-phase noise separation requires to measure the noise of all three phases concurrently. Presently available three-phase LISNs, however, only allow to measure the noise contribution of one phase at a time. In order to measure all three phases at the same time, in the proposed EMI test setup with a three-phase noise separator, three single-phase LISNs are utilized, each connected to one phase of the EUT. Thereby, manufacturing tolerances between the individual LISNs (part-to-part tolerance) have a substantial influence on the overall matching. It is therefore suggested that future three-phase LISNs are designed to provide access to all three HF noise measurements at the same time to take advantage of (ideally) closer matching of the three channels within one three-phase LISN. For single-phase CE EMI noise measurements a LISN has recently become available, which allows both lines (phase and neutral line) to be measured simultaneously [183]. Moreover, there is an extension that directly includes a single-phase CM/DM noise separation circuit [184]. For three-phase measurements there exists a four channel EMI test receiver that supports the modal splitting into CM and DM components (calculated in the digital domain, i.e., after the concurrent measurement of all four channels) [185], but still requires an external three-phase LISN with concurrent measurement capabilities. Moreover, compared to the here presented analog CM/DM noise separator, any

phase difference and/or delay between the four receiver channels causes additional errors in the calculation of the CM and DM components.

ii) The internal HPFs to attenuate the LF signal components (50/60 Hz components of the power flow) and to pass the HF noise signals (150 kHz to 30 MHz) are typically realized as multi-order filters [172] and hence are difficult to match from device to device, particularly due to the utilized inductive elements. Therefore, it is suggested to use precisely matched external first-order RC HPFs connected in parallel to the LISN EUT port in order to maximize the symmetry between the three phases (improvement of 10 dB in the unwanted CM-to-DM conversion compared to using the LISN's internal measurement path). The external HPFs are shown to still fulfill the input impedance criterion imposed by the regulatory standards [160].

The role of symmetric placement of the filter elements, matched layout, and minimization of parasitic coupling effects between the three phases and between the filter stages (e.g., by adequate shielding and by systematic component placement to cancel out stray fields) must be given considerably more weight in future EMI filter design processes (optimization objective). Moreover, the HF behavior of the filters, which is mainly determined by parasitic elements and the aforementioned coupling effects, is of paramount importance, especially because of higher and higher frequency components in the noise spectrum.

Furthermore, using a high-performance noise separator with a symmetric test setup allows to determine the CM and DM EMI noise sources of an EUT (with EMI filter removed). Thus, the development of more accurate simulation models for predicting and estimating EMI noise is possible, which very much simplifies the dimensioning of optimized filter stages by reducing the need to consider large margins for the filter attenuation. Such simplified design processes represent a major advantage in practice, since the development effort can be significantly minimized if, for example, several iterations of the filter design and their respective verifications can be omitted.

As a final remark, it should be mentioned that an extension of current EMI regulations to cover frequencies down to 2 kHz is under discussion for quite some time [186], e.g., due to possible interference with smart metering and smart grid communication signals (Power Line Communication (PLC) [187]) that operate between 3 kHz and 95 kHz [188]. Possible limiting values down to 9 kHz are shown in the technical specification IEC-62578 [189] with three classes (C_1, C_2 and C_3) and permissible noise levels of up to 150 dBµV ($\approx$ 31 V) for class C_1 at 9 kHz are specified. In this context, the realization of the three-phase active noise separator presented in this work is particularly suitable

for use also with a possible extension of the valid standards, since thanks to the omission of any magnetic components no saturation phenomena and thus degradation/loss of separation performance occur, even at low frequencies (down to dc). With simple frequency-compensated voltage dividers (RC dividers), the input voltage range can be extended as required without introducing a mismatch in the magnitude and/or phase response.

Appendices

A

Theoretical Performance Limitation of the Three-Level Triple-Interleaved (3L3) Converter

In the following, the theoretical performance limitations, i.e., maximum output power for different load phase angles φ, imposed by two conditions, namely the maximum possible converter voltage (modulation limit) and the maximum semiconductor Root Mean Square (RMS) current (thermal/efficiency limitation), are derived.

Given the sinusoidal nature of the output voltage and current, theoretical output power limitations for the proposed converter can directly be derived using the phasor representation of output voltage and current (cf. phasor diagram in **Fig. 2.3 (a.ii)**). For the nominal operating point at $f_{\mathrm{out}} = 100\,\mathrm{kHz}$ and $V_{\mathrm{out}} = 230\,\mathrm{V}$ rms, the theoretical possible apparent output power S_{Lim} for each load phase angle φ (phase-shift between output voltage and current waveforms) is depicted in **Fig. A.1** in green. It is limited by two constraints:

i) The maximum possible voltage amplitude that can be generated at the switch node, given by $V_{\mathrm{dc}}/2$, here set to $0.95 \cdot V_{\mathrm{dc}}/2$ to have a certain margin (corresponds to a modulation depth $m_{\mathrm{M}} = 0.95$), i.e., $|\underline{v}_{\mathrm{sw,eff}}| \leq m_{\mathrm{M}} \cdot V_{\mathrm{dc}}/2$ according to the phasor diagram in **Fig. 2.3 (a.ii)**.

ii) The maximum possible switch RMS current, which is limited by the semiconductor losses and thus highly depends on the thermal design.

The RMS current derived from the conduction losses occurring for $M = 3$ and $N = 3$ and ohmic load in the nominal operating point is taken as a reference (cf. **Fig. 2.4 (a)**), i.e., $I_{\mathrm{sw,rms}} \approx 11.6\,\mathrm{A}$. The inductor current relates the switch current to the output current and its RMS value is calculated under the assumption of a triangular peak-to-peak current ripple of 100 %

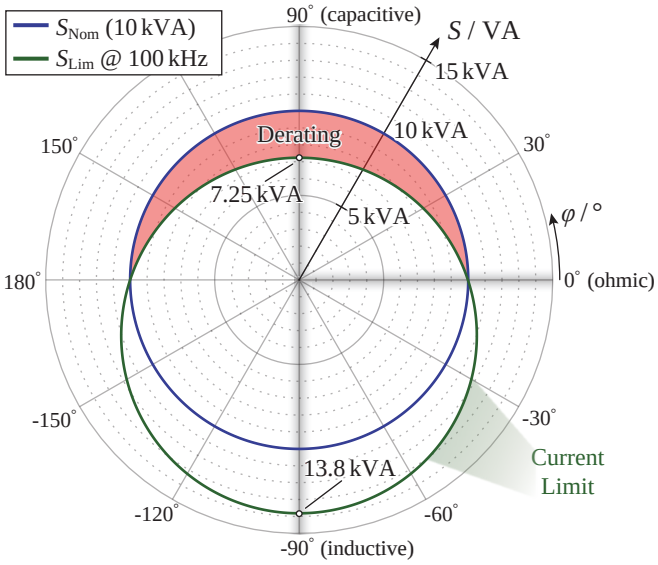


Fig. A.1: Theoretical limitation S_{Lim} (green) of the apparent output power versus the load phase angle φ (phase-shift between the output voltage and current) for the given selection of the filter elements (L_{filt} = 1.26 µH, C_{filt} = 99 nF) for a 100 kHz sinusoidal output voltage with 230 V rms relative to a nominal output power of 10 kVA (blue) and ohmic load ($\varphi = 0\,°$). The limitation is derived from the switch RMS current for $M = 3$ and $N = 3$ under the assumption of a worst-case peak-to-peak current ripple of 100 % (with respect to the fundamental component). The required derating of 27.5 % of the output power for capacitive loads is highlighted in red; Figure based on [46].

(with respect to the amplitude of the fundamental component) as worst-case approximation, i.e., in reality the current ripple is lower and not the same during the entire fundamental frequency period. Since the current limit is derived from the ohmic load case, the S_{Lim} circle intersects with the blue circle representing the nominal power S_{Nom} = 10 kVA at $\varphi = 0\,°$ and $\varphi = 180\,°$. It is shown that for capacitive-resistive loads ($0\,° < \varphi < 180\,°$) the current limitation (constraint ii) in above list) leads to an output power derating of maximum 27.5 %, which is much lower compared to state-of-the-art linear PAs (derating by a factor of three) [29]. For all other load cases, there is a sufficient margin, especially for inductive loads (> 30 % margin) because they partially compensate the reactive power of the output filter. If higher currents would be allowed, the maximum possible converter voltage (constraint i) in above list) would limit the maximum output power for inductive loads

($\varphi = -90\,^\circ$), since in this case $\underline{v}_{\mathrm{out}}$ and $\underline{v}_{\mathrm{L}}$ are in phase (cf. **Fig. 2.3 (a.ii)**) and arithmetically add up to $\underline{v}_{\mathrm{sw,eff}}$. This cannot be seen in **Fig. A.1** due to the dominating current limit (condition ii)) and because the inductance is chosen based on limiting the maximum inductor voltage to $k_{\mathrm{v}} = 15\,\%$ of the nominal peak output voltage for an ohmic load scenario, which even in case of a purely inductive load would yield

$$|\underline{v}_{\mathrm{sw}}| = 1.15 \cdot |\underline{v}_{\mathrm{out}}| = 374\,\mathrm{V} < 0.95 \cdot V_{\mathrm{dc}}/2 = 380\,\mathrm{V}. \tag{A.1}$$

B

Three-Phase Active CM/DM Noise Separator

This Appendix is meant to be read as an extension of **Chapter 5** and summarizes the most relevant findings regarding the design and commissioning of a three-phase active conducted Electromagnetic Interference (EMI) CM/DM noise separator, which are also published in:

- **P. S. Niklaus**, D. Bortis, and J. W. Kolar, "Design and Experimental Analysis of a Three-Phase Active CM/DM Conducted EMI Noise Separator," *CPSS Transactions on Power Electronics and Applications,* vol. 5, no. 3, pp. 273-288, September 2020.

Chapter Abstract

This Appendix investigates the design, realization and verification of a three-phase active Electromagnetic Interference (EMI) Conducted Emission (CE) CM/DM noise separator used to distinguish between the Common Mode (CM) and Differential Mode (DM) components in the overall measured CE noise voltage spectrum. By doing so, the converter input and/or output filter stages can be individually optimized to improve the CM or DM attenuation depending on the origin of the CE disturbances. The main advantage of the presented active solution is the absence of magnetic components in the signal path, which drastically facilitates the matching at high frequencies. The influence of asymmetries and mismatches of the component parasitics as well as in the circuit board layout are analyzed. To assess the performance of the proposed system according to widely known metrics such as CM and DM Transfer Functions (TFs) and Rejection Ratios (RRs), different test methods are established and the implied limitations regarding maximum measurable performance are considered. Finally, experimental results verifying the calculated separation capabilities are provided.

B.1 Introduction

Pre-compliance measurements with a standard Electromagnetic Interference (EMI) test setup as shown in **Fig. B.1** with a three-phase converter that has to comply to EMI standards as Equipment Under Test (EUT), a three-phase Line Impedance Stabilization Network (LISN) and a corresponding EMI test receiver allow the quantification of the total Conducted Emissions (CEs). The LISN acts as a bridge between the three-phase mains and the converter and serves three purposes:

1. It provides a fixed mains impedance of 50 Ω||50 µH to the EUT for the relevant frequency range between 150 kHz and 30 MHz [160], which is crucial for meaningful measurements, since CE noise voltage arises from impressed currents flowing through the inner mains impedance (cf. **Appendix C**).

2. It enables Low-Frequency (LF) power flow (50/60 Hz) from the mains to the EUT (and vice versa).

3. It redirects any High-Frequency (HF) content emitted from the EUT to the connected EMI test receiver where the measurements are taken and therefore prevents the HF noise from flowing into the mains. At

the same time, any LF component is attenuated at the HF output port to prevent saturation of the EMI test receiver input. Even though **Fig. B.1** shows the measurement path only as first-order High-Pass Filter (HPF) (C_{HP} together with the 50 Ω input impedance of the EMI test receiver or noise separator), in reality the filtering network attenuates LF components much stronger. **Appendix E.1** describes the equivalent circuit of a commercially available LISN and the resulting attenuation.

In order to be compliant with the standards, the spectral envelope of the total conducted noise over the specified frequency range must be below the defined limits. As mentioned above, in modern power converters, compliance is usually only achieved by employing dedicated filter stages. Obviously, overdimensioned filters must be avoided for cost, volume and weight reasons. For an optimal filter design, apart from profound knowledge of the amount of noise generated by the employed converter topology and modulation scheme, it is important to know the share of Common Mode (CM) and Differential Mode (DM) emissions, since the total noise can be composed of only one of the two components or the combination thereof. Since the LISN only measures the total CE noise, it is very convenient to have a so-called CM/DM noise separator that allows to separately quantify the CM and DM components of the total measured CEs and thereby allows to improve only the insufficiently performing filter part to reduce the CEs. Furthermore, the designer can also determine potential cross-coupling between the filter stages due to component placement and parasitic elements [173].

The CM/DM noise separator can be integrated into the standard EMI test setup, as depicted in **Fig. B.1** (highlighted in blue). Please note that **Fig. B.1** is identical to **Fig. 5.2** and is placed here again for better readability. In the standard setup (cf. dashed line labeled 'Direct Measurement' in **Fig. B.1**), the HF outputs of the LISNs are connected to the test receiver using coaxial cables with a characteristic impedance of $\underline{Z}_0 = 50\,\Omega$ and are terminated with the 50 Ω input resistance of the receiver, at which the HF noise voltages $\underline{v}_{\mathrm{LISN,a}}$, $\underline{v}_{\mathrm{LISN,b}}$, and $\underline{v}_{\mathrm{LISN,c}}$ are measured. Note that $\underline{x}$ represents a complex quantity, containing an amplitude and a phase information. When adding a three-phase noise separator between LISN and test receiver (cf. continuous lines with the highlighted noise separator in **Fig. B.1**), it must be ensured that the input impedances $\underline{Z}_{\mathrm{in,a}}$, $\underline{Z}_{\mathrm{in,b}}$ and $\underline{Z}_{\mathrm{in,c}}$ of the three separator input ports equal 50 Ω, as otherwise measurement errors due to an impedance mismatch between separator and LISN occur [190].

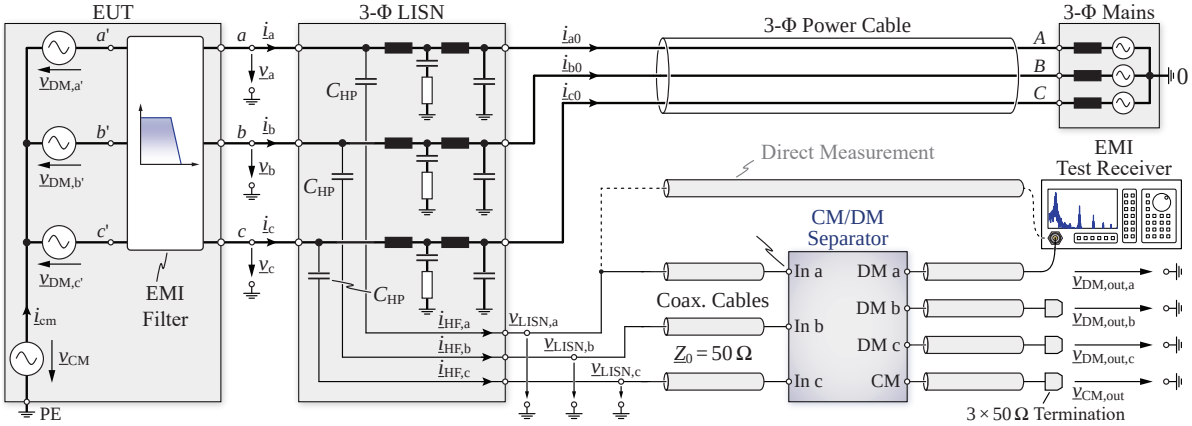


Fig. B.1: Typical EMI pre-compliance measurement setup for a three-phase EUT. A three-phase LISN connects the EUT to the mains (bold lines indicate power transfer) and either directly (dotted line) or via a three-phase CM/DM noise separator (highlighted in blue) to an EMI test receiver. In the former case the total CE EMI noise is measured, whereas in the latter case the separated CM and DM emissions are identified. Coaxial cables with a characteristic impedance of 50 Ω are employed for the signal connections. Only one voltage at a time can be measured with typical EMI test receivers so any unused HF output terminal must be terminated with 50 Ω. This figure is identical to Fig. 5.2 and is shown here again for better readability.

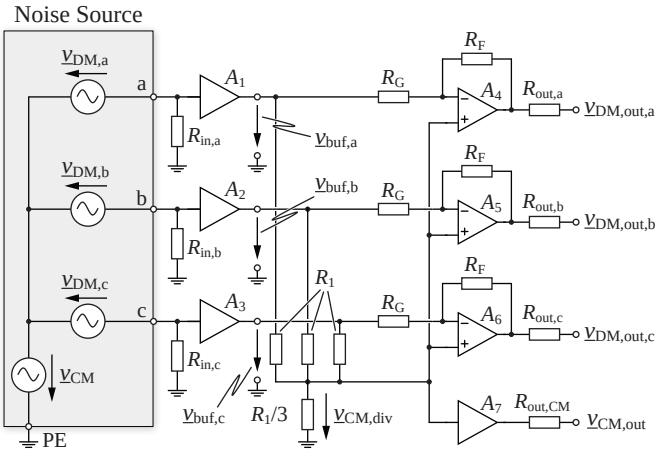


Fig. B.2: Schematic drawing of the proposed three-phase active CM/DM noise separator that uses no magnetic components. This figure is identical to Fig. 5.6 and is shown here again for better readability.

B.1.1 Target Performance

The goal of the presented active separator is to trace down any exceeding of the EMI limits to either the CM or DM filter, such that the one with insufficient attenuation can be improved. Hence, mainly qualitative measurements are of interest and to avoid misinterpretation of the obtained results, the selectivities of the separator, i.e., the ratios of the Common Mode Rejection Ratio (CMRR) to the Differential Mode Transfer Function (DMTF) and of the Differential Mode Rejection Ratio (DMRR) to the Common Mode Transfer Function (CMTF) (as defined in **Section 5.2.2**), should be at least −40 dB up to 30 MHz. This means that the error due to cross-coupling of a CM signal to the DM outputs or vice versa is less than 1 %. At the same time the DMTF and CMTF must be as flat as possible. The standard defines a deviation of no more than ±2 dB for EMI test receivers measuring sinusoidal signals [170], however, much lower values are desired. At the measurement ports an input impedance of 50 Ω in the whole considered frequency range (150 kHz to 30 MHz) is required.

B.2 Design and Implementation

The circuit of the implemented three-phase active noise separator is given in **Fig. B.2** and is composed of three identical channels, each comprising an input buffer ($A_1 - A_3$, Analog Devices AD8000 [191]) and a difference amplifier ($A_4 - A_6$, Analog Devices AD8099 [192]). Again, the input coming from a three-phase LISN is modeled with a CM and three DM noise voltage sources. The required 50 Ω input impedance is solely defined with the three resistors $R_{\text{in,a}'} \dots R_{\text{in,c}'} = 50\ \Omega$, since the input impedance $\underline{Z}_{\text{in,buf}} = 2\,\text{M}\Omega||3.6\,\text{pF}$ of the buffer amplifiers can be neglected in the given frequency range ($Z_{\text{in,buf}}\big|_{f=30\,\text{MHz}} = 1.47\,\text{k}\Omega \gg 50\ \Omega$).

According to (5.2), at the output of the buffer amplifiers, the CM voltage is obtained with the voltage divider composed of R_1 and $R_1/3$. From this voltage the buffered LISN output voltage $\underline{v}_{\text{buf,i}}$ is subtracted, such that at the DM output ports the negative DM voltage components $\underline{v}_{\text{DM,out,i}} = -\underline{v}_{\text{DM,LISN,i}}$ remain (cf. (5.4)). Finally, the amplifier A_7 (Analog Devices ADA4817 [193]) buffers the voltage $\underline{v}_{\text{CM,div}}$ at the CM node and at its output port the pure CM voltage component $\underline{v}_{\text{CM,out}}$ remains. Despite the negative sign of the DM output voltage the separation is still valid, since the CE standard only considers the magnitude but not the phase of the emitted noise. Alternatively, a further inverting stage could be added to the circuit.

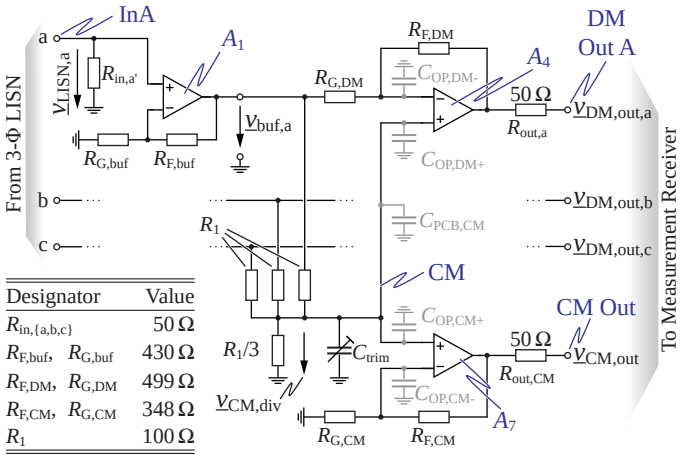
Fig. B.3 shows a more detailed schematic for one of the three channels (channel A), lists the corresponding resistor values and includes the most relevant parasitic capacitances, drawn in light gray. All the observations hold in the same way for the other two channels. The input buffer A_1 is realized as a non-inverting amplifier with a gain of +2, i.e., $R_{\text{F,buf}} = R_{\text{G,buf}}$, such that

$$\underline{v}_{\text{buf,a}} = 2 \cdot \underline{v}_{\text{LISN,a}'} = 2 \cdot \left(\underline{v}_{\text{CM,LISN}} + \underline{v}_{\text{DM,LISN,a}'}\right). \tag{B.1}$$

This additional gain compensates the division of the DM output voltage by a factor of two, due to the 50 Ω output resistors $R_{\text{out,a}} \dots R_{\text{out,c}}$ in conjunction with the 50 Ω input termination of the test receiver.

The CM voltage $\underline{v}_{\text{CM,div}}$ across the resistor $R_1/3$ in the bottom leg of the CM voltage divider is found based on

$$\underline{v}_{\text{CM,div}} = \left(\sum_{i=\{a,b,c\}} \underline{v}_{\text{buf,i}}\right) \cdot \underbrace{\frac{\left(\frac{R_1}{3}||R_1||R_1\right)}{\left(\frac{R_1}{3}||R_1||R_1\right) + R_1}}_{1/6}. \tag{B.2}$$



Designator	Value
$R_{in,\{a,b,c\}}$	50 Ω
$R_{F,buf}$, $R_{G,buf}$	430 Ω
$R_{F,DM}$, $R_{G,DM}$	499 Ω
$R_{F,CM}$, $R_{G,CM}$	348 Ω
R_1	100 Ω

Fig. B.3: Detailed view of one DM channel (channel A) and the CM channel. Indicated are the relevant parasitic capacitances that mainly determine the HF behavior. In addition, the table shows the resistor values used in the current implementation that are chosen based on the considerations listed below.

Using (5.2) and (B.1) the above expression can be evaluated as

$$\underline{v}_{CM,div} = \underline{v}_{CM,LISN}. \tag{B.3}$$

To prevent loading of the CM circuit node *CM* and to compensate for the −6 dB loss at the CM output port due to the output resistor $R_{out,CM}$ and the test receiver input resistance, amplifier A_7 with a gain of +2 ($R_{G,CM} = R_{F,CM}$) is inserted.

In the DM path, the amplifier A_4 is configured as difference amplifier, which subtracts the buffered input voltage $\underline{v}_{buf,a}$ from the CM voltage $\underline{v}_{CM,div}$ according to

$$\underline{v}_{out,A4} = \left(1 + \frac{R_{F,DM}}{R_{G,DM}}\right) \cdot \underline{v}_{CM,div} - \frac{R_{F,DM}}{R_{G,DM}} \cdot \underline{v}_{buf,a}. \tag{B.4}$$

Setting $R_{F,DM} = R_{G,DM}$ and inserting (B.1) and (B.3), the difference amplifier output voltage is directly given by

$$\underline{v}_{out,A4} = -2 \cdot \underline{v}_{DM,LISN,a'} \tag{B.5}$$

and reduces to

$$\underline{v}_{\mathrm{DM,out,a}} = \underline{v}_{\mathrm{out,A4}} \cdot \frac{50\,\Omega}{50\,\Omega + R_{\mathrm{out,a}}} = -\underline{v}_{\mathrm{DM,LISN,a'}} \tag{B.6}$$

when considering again the voltage divider formed by the 50 Ω input resistance of the EMI test receiver together with the 50 Ω output resistor $R_{\mathrm{out,a}}$ of the separator. As already mentioned, the signal inversion from input to DM output is not problematic, since the targeted application is the characterization of the dominant noise contributor (CM or DM), hence only the magnitude of the respective voltages are of interest. However, connecting the CM signal at the non-inverting input terminals of the difference amplifiers makes the matching easier, as further explained in the next section. With this configuration, the maximum allowed voltage of ±1.75 V (124 dBµV) at the separator input is determined by the output voltage range of the operational amplifiers. The reason is the required gain of +2, to drive the double terminated 50 Ω line. Therefore, to get ±1.75 V at the EMI test receiver input, the operational amplifiers must have an output voltage swing of ±3.5 V. It has to be noted, that 124 dBµV is orders of magnitude higher than the EMI limiting values and therefore, sufficient margin is provided.

B.3 Critical Design Aspects

As already mentioned in [163] and [194], symmetry of the overall structure is very crucial to achieve sufficient performance, especially good Rejection Ratios (RRs) at high frequencies and therefore high selectivities. The symmetry requirement can be split into several parts, each treated individually. The critical aspects regarding component selection and Printed Circuit Board (PCB) layout are investigated in this section.

B.3.1 Matching and PCB Layout

From all metrics, the CMRR is most severely affected by any asymmetries, since for a pure CM excitation, the DM output measured with the difference operation according to (B.4) must stay at zero, which means that both inputs of amplifiers $A_4 \ldots A_6$ must be perfectly equal in magnitude and phase. In [136], it was shown that especially the phase matching of the amplifier input signals has a big influence on the maximum achievable CMRR of a difference amplifier, even if the amplifier itself is assumed ideal. A relative phase error of less than 0.035 % with respect to 180° (absolute phase mismatch of 0.06° or a skew of less than 6 ps at 30 MHz) is required to achieve a CMRR of −60 dB. Apart

from reactive elements, a phase-shift between two nominally identical signals is also introduced by unequal signal path lengths (PCB tracks), leading to different signal propagation delays t_{pd}. Mathematically, the phase-shift $\Delta\phi$ in radians can be calculated as

$$\Delta\phi(f) = \omega \cdot \Delta t_{\mathrm{pd}} = 2\pi \cdot f \cdot \frac{\Delta l}{c} \tag{B.7}$$

where Δl denotes the length difference between the two tracks and c the wave propagation speed, which for a 50 Ω microstrip on the utilized layer stack-up is calculated as approximately $1.68 \cdot 10^8 \, \frac{\mathrm{m}}{\mathrm{s}}$ using a standard PCB calculator [195]. It becomes clear, that for a given length mismatch the phase error is proportional to the signal frequency. To keep the absolute phase error below 0.06° over the whole frequency range, i.e., to achieve a CMRR better than −60 dB, the overall length mismatch has to be lower than 0.9 mm, resulting from solving (B.7) for Δl at the maximum frequency $f = 30\,\mathrm{MHz}$.

Length matching needs to be fulfilled at several stages in the circuit layout. First and foremost, the tracks from each input port *InA, InB,* and *InC* to the respective buffer amplifiers *BufA* (A_1)*, BufB* (A_2)*,* and *BufC* (A_3) must have equal length. The buffer outputs are connected to the inverting inputs of the difference amplifiers *DiffA* (A_4)*, DiffB* (A_5) and *DiffC* (A_6) with tracks of length $l_{\mathrm{Buf}i,\mathrm{Diff}i}$, $i = \{A, B, C\}$ respectively and to the respective non-inverting inputs via the CM divider network. Hence, for each channel the sum of the lengths $l_{\mathrm{Buf}i,\mathrm{CM}}$ (track length from the buffer output to the CM node) and $l_{\mathrm{CM,Diff}i}$ (track length from the CM node to the non-inverting input of the difference amplifier) needs to be equal to the length $l_{\mathrm{Buf}i,\mathrm{Diff}i}$ (track length from the buffer output to the inverting input of the difference amplifier), such that for a pure CM input signal the voltages at the inverting and non-inverting input terminals of the difference amplifier have no phase-shift. The connections between difference amplifier output and separator output ports ($l_{\mathrm{Diff}i,\mathrm{DM}i}$) only need to be length-matched if the three DM outputs are monitored simultaneously in time-domain. The above requirements can be summarized mathematically with three conditions

$$l_{\mathrm{InA,BufA}} = l_{\mathrm{InB,BufB}} = l_{\mathrm{InC,BufC}} \tag{B.8}$$

$$l_{\mathrm{BufA,DiffA}} = l_{\mathrm{BufB,DiffB}} = l_{\mathrm{BufC,DiffC}} \tag{B.9}$$

$$l_{\mathrm{Buf}i,\mathrm{Diff}i} = l_{\mathrm{Buf}i,\mathrm{CM}} + l_{\mathrm{CM,Diff}i}, \quad i = \{A, B, C\}. \tag{B.10}$$

The last condition is graphically represented with three triangles and therefore, a semicircular arrangement of the channels with interleaved input and output ports and the CM port located in the center as will be shown in **Fig. B.5** allows for a very convenient implementation. **Table B.1** lists the PCB track

Tab. B.1: PCB track lengths and length mismatch of the critical signal paths. All numbers are given in mm.

Ch.	$l_{\mathrm{In,Buf}}$	$l_{\mathrm{Buf,CM}}$	$l_{\mathrm{CM,Diff}}$	$l_{\mathrm{Buf,Diff}}$	Δl_{Diff}
A	14.163	12.144	14.199	26.341	-0.002
B	14.169	12.157	14.201	26.354	-0.004
C	14.173	12.148	14.202	26.350	0

lengths of the critical signal paths including the mismatch $\Delta l_{\mathrm{Diff}} = l_{\mathrm{Buf,Diff}} - (l_{\mathrm{Buf,CM}} + l_{\mathrm{CM,Diff}})$ at the difference amplifier input for each channel. All tracks are realized as 50 Ω microstrips with a track width of 0.2 mm on a standard FR-4 PCB. Possible tolerances during the PCB manufacturing are very likely to exceed the calculated length mismatch of 4 µm between the critical signal paths to the difference amplifier inputs.

B.3.2 Matching and Selection of Passive Components

Apart from the layout, the selection of the passive components also has a substantial influence on the symmetry and therefore the CMRR and DMRR. The general idea is that all resistive dividers of one channel are matched to the respective dividers of the other channels and that there is no phase mismatch between the two inputs of the three difference amplifiers. For the lower frequency range this is accomplished by choosing resistors with the lowest available tolerance of $\varepsilon_{\mathrm{R}} = \pm 0.01\,\%$, which for an ideal difference amplifier gives a worst-case CMRR of −74 dB [123]. While the network of **Fig. B.2** features only resistors and amplifiers, parasitic capacitances, as for example the amplifier input capacitance denoted in **Fig. B.3**, introduce a phase-shift at frequencies above several MHz, which unfortunately still lay in the considered frequency range. The HF CMRR is trimmed to diminish the phase mismatch of the difference amplifier input signals due to e.g. loosely matched parasitic capacitances. The time constant of the effective node impedances, assumed as first-order *RC* circuits, must be equal for both inverting and non-inverting input. To achieve this, trimming capacitors need to be placed on the CM voltage divider, whereby three possibilities exist: i) placement of a capacitor in parallel to R_1 in each channel or ii) placement of one single capacitor in parallel to $R_1/3$, which then acts on all three channels together or iii) a combination of both variants. The first variant allows individual channel matching to precisely account for the specific parasitic elements in each channel. Albeit this trimming method promises the highest possible CMRR for all three DM outputs, it unfortunately influences the DMRR as well. To

keep the DMRR at an acceptable level, accurate trimming of all three channels against each other is required. This is because the CM divider only performs the voltage addition according to (5.2) if all three resistors R_1 have equivalent parallel capacitance (equal impedance over the whole frequency range). When trimming each channel for maximum CMRR, this is not necessarily given. The second variant, however, omits any external capacitance in parallel to R_1 thereby providing the best possible accuracy in the determination of the CM voltage component. It is found that the residual parasitic capacitance of the three resistors is very well controlled with a symmetric PCB layout. This results in a very good DMRR. On the contrary, the CMRR can not be trimmed for each channel separately but thanks to the very symmetric layout the performance of all three channels is improved by matching the nominal time constant using one single trimming capacitor. In practical applications the calibration/compensation effort must be kept to a minimum. Therefore, despite not yielding the absolute highest possible CMRR in all three channels, variant ii) is a very good compromise between usability and performance and is preferred.

In **Fig. B.3** the dominant parasitic elements for one channel are highlighted, namely the difference amplifier input capacitances $C_{\mathrm{OP,DM+}}$ and $C_{\mathrm{OP,DM-}}$ (2 pF each), the CM amplifier input capacitances $C_{\mathrm{OP,CM+}}$ and $C_{\mathrm{OP,CM-}}$ (1.3 pF each) and the capacitance $C_{\mathrm{PCB,CM}}$ of the PCB track connecting the obtained CM voltage $\underline{v}_{\mathrm{CM,div}}$ to all three difference amplifiers (measured as roughly 8.5 pF). The resulting node impedances at the inputs of the difference amplifiers are given as

$$\begin{aligned}\underline{Z}_{\mathrm{DM,-}} &= \left(R_{\mathrm{F,DM}} \middle\| R_{\mathrm{G,DM}} \middle\| \frac{1}{j\omega \cdot C_{\mathrm{OP,DM-}}}\right) \\ &= \frac{\left(R_{\mathrm{F,DM}} || R_{\mathrm{G,DM}}\right)}{1 + j\omega \cdot C_{\mathrm{OP,DM-}} \cdot \left(R_{\mathrm{F,DM}} || R_{\mathrm{G,DM}}\right)}\end{aligned} \tag{B.11}$$

at the inverting input terminal and

$$\underline{Z}_{\mathrm{DM,+}} = \frac{(R_1/3||R_1||R_1||R_1)}{1 + j\omega \cdot C_{\mathrm{eq}} \cdot (R_1/3||R_1||R_1||R_1)} \tag{B.12}$$

at the non-inverting input terminal where

$$C_{\mathrm{eq}} = 3 \cdot C_{\mathrm{OP,DM+}} + C_{\mathrm{OP,CM+}} + C_{\mathrm{CM,PCB}} + C_{\mathrm{trim}}. \tag{B.13}$$

Therefore, the two cut-off frequencies

$$f_{\mathrm{c,DM-}} = \frac{1}{2\pi \cdot C_{\mathrm{OP,DM-}} \cdot R_{\mathrm{F,DM}}/2} \tag{B.14}$$

$$f_{\mathrm{c,DM+}} = \frac{1}{2\pi \cdot C_{\mathrm{eq}} \cdot R_1/6}, \tag{B.15}$$

are obtained, where also the condition $R_{\mathrm{F,DM}} = R_{\mathrm{G,DM}}$ is used to simplify the expressions. It should be noted that the parasitic shunt capacitance of the resistors is neglected in this step, since for a 0603 surface mount 1 MΩ resistor a maximum value of 100 fF was measured with a precision impedance analyzer (Agilent 4294A [80]). This is considerably lower than all the other parasitic capacitances. The frequency $f_{\mathrm{c,DM+}}$ is likely to be lower than $f_{\mathrm{c,DM-}}$, since $C_{\mathrm{eq}} = 15.8\,\mathrm{pF}$ (without considering C_{trim}) is much larger than $C_{\mathrm{OP,DM-}}$. Adding the trim capacitor in parallel to $R_1/3$ according to **Fig. B.3** adds more capacitance to the CM node and therefore decreases $f_{\mathrm{c,DM,+}}$ even more. To end up with $f_{\mathrm{c,DM-}}$ being smaller than $f_{\mathrm{c,DM+}}$, such that adding more capacitance (C_{trim}) to the CM node makes the two frequencies equal, either a large $R_{\mathrm{F,DM}}$ and/or a small R_1 must be chosen. According to [192], the value of $R_{\mathrm{F,DM}}$ should be chosen in the range of 250 Ω to 499 Ω where the maximum value is selected here. This directly defines the upper bound $R_{1,\mathrm{max}}$ for the CM divider resistance R_1 as

$$R_{1,\mathrm{max}} = \frac{3 \cdot R_{\mathrm{F,DM}} \cdot C_{\mathrm{OP,DM-}}}{C_{\mathrm{eq}}} = 189.5\,\Omega \geq R_1. \tag{B.16}$$

For the presented implementation, a lower value of $R_1 = 100\,\Omega$ is chosen such that matching is still possible even when $C_{\mathrm{OP,DM-}}$ is significantly lower and/or C_{eq} substantially higher than the respective nominal values. Assuming the parasitic capacitances according to the nominal values and given the above specified resistances, C_{trim} must be set to 14.2 pF to equalize the two cut-off frequencies.

At this point, again the question could arise why to add even more capacitance to the CM node, instead of adding capacitors parallel to the resistor R_1 in each CM divider. This would indeed facilitate the selection of R_1, $R_{\mathrm{F,DM}}$ and $R_{\mathrm{G,DM}}$ but as mentioned would also lead to the necessity of trimming all three channels against each other, in order to get a sufficient DMRR and a flat CMTF apart from the good CMRR. Another option would be to reduce $f_{\mathrm{c,DM-}}$ according to (B.14) by increasing the capacitance $C_{\mathrm{OP,DM-}}$. This is, however, undesired because the operational amplifier phase margin is reduced by the placement of any capacitance at the inverting input terminal.

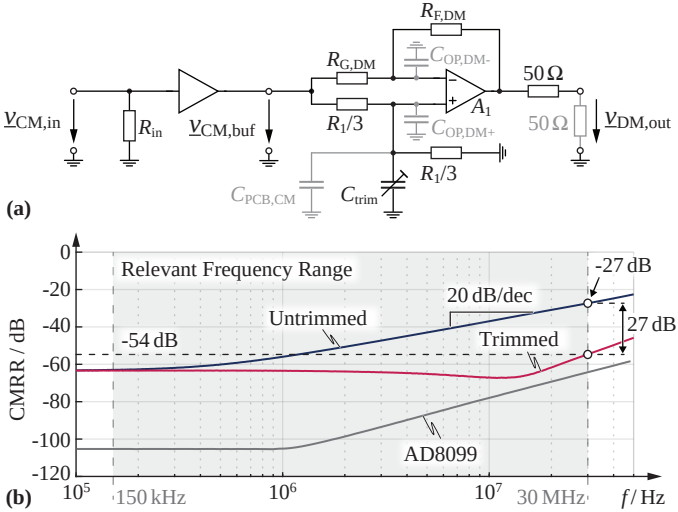


Fig. B.4: (a) Schematic of the configuration used for testing the difference amplifier alone and **(b)** the resulting CMRR responses for the case where $C_{trim} = 0$ pF (dark blue) and for the case of an optimally trimmed response (red). In addition, the measured CMRRs are compared to the CMRR of the AD8099 obtained from the datasheet (gray), which equals to the maximum achievable CMRR when all resistors would be perfectly matched and no parasitic components would exist.

While channel to channel trimming is not needed with the selected trimming method, the CMRR of only one channel can be optimized due to the slightly different $f_{c,DM-}$ in each channel coming from variations in $R_{F,DM}$, $R_{G,DM}$ and component parasitics. Therefore, slight deviation in the CMRR responses of the three channels are to be expected but can be minimized by careful PCB layout and by using components from the same batch to decrease deviations due to manufacturing process variations.

The DMRR is mainly dependent on the matching of the resistors R_1 in each channel because only if the three upper resistors R_1 are exactly identical, the sum of the three resistor currents is zero for a pure DM excitation, resulting in no output signal at the CM output port.

To test the effectiveness of the employed matching method on the CMRR, a reduced version of the circuit from **Fig. B.2** was built on a PCB with the exact same layout and parasitic elements as the PCB of the three-phase separator will have. The schematic is shown in **Fig. B.4 (a)** and features only one channel with input buffer and difference amplifier. To get the same node impedance

at the non-inverting input of the difference amplifier A_1, the upper resistor is changed from R_1 to $R_1/3$, resulting in the same effective resistance as on the three-phase separator for CM excitation. The only difference between the final separator and the given test circuit is the absence of the two other channels as well as the CM buffer amplifier. The transfer characteristic was measured using a network analyzer (Omicron Lab Bode 100 [118]) and the result is shown in **Fig. B.4 (b)** where the relevant EMI frequency range between 150 kHz and 30 MHz is highlighted. The LF CMRR is around −63 dB, hence 11 dB worse than the expected value of −74 dB resulting from the resistor tolerances. This can be explained by the fact that the absolute deviation of $R_1 = 100\,\Omega \pm 0.01\,\%$ is only ±10 mΩ. Therefore, the total error is also strongly influenced by factors such as the solder joint and PCB track resistances. A PCB track with a width of 0.2 mm and a length of 5 mm already has a dc resistance of 12 mΩ and predominates the error. The LF CMRR could be improved by employing a resistive trimmer (or higher values of the resistors, yet below the limit of (B.16)), however, the value of −60 dB is sufficient for the targeted application and hence further LF trimming is omitted. At elevated frequencies the untrimmed circuit shows insufficient performance as the CMRR already starts to increase with +20 dB/dec at around 300 kHz, reaching a value of only −27 dB at 30 MHz. After trimming with the aforementioned method, a significant performance improvement is observed and the CMRR of −63 dB is maintained up to around 20 MHz before it increases, reaching a value of −54 dB at 30 MHz. The improvement of 27 dB (factor of 22) compared to the untrimmed circuit proves that the applied trimming method works as intended.

B.3.3 Difference Amplifier

Up to now, an ideal difference amplifier was assumed and the only degradation in the separator performance was addressed to an asymmetry in the layout and/or component mismatch. In reality, a difference amplifier has only a limited CMRR, typically getting worse towards higher frequencies due to internal mismatches. This results in a limited maximum possible CMRR even for perfect matching of the amplitude and phase at the amplifier input ports. The selected difference amplifier (AD8099) features a very good HF CMRR which is also indicated in **Fig. B.4 (b)** (gray curve) and it is observed that at low frequencies, the resulting overall performance is limited by a resistive mismatch, while at frequencies above 10 MHz it is very close to the performance of the amplifier itself and therefore is mainly limited by the internal CMRR and not by the parasitics or capacitor trimming [196].

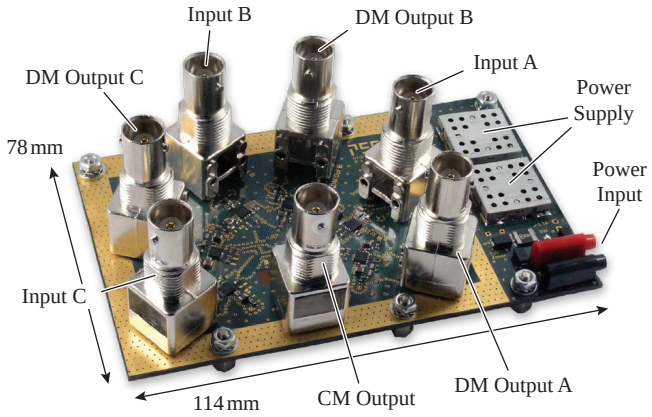


Fig. B.5: Picture of the proposed three-phase active CM/DM noise separator showing all input and output connections as well as the auxiliary power supply.

B.3.4 Distortion and Noise Considerations

Another important aspect is to have low noise and distortion at the output ports. Otherwise, significant spurs in the measured spectrum could occur even without a EUT connected, leading to misinterpretation of the obtained measurements. Noise concerns are less critical due to the fact that the EMI test receiver has a measurement Bandwidth (BW) of only 9 kHz. Therefore, broadband noise has minor influence on the total displayed noise floor. Other distortions, however, can occur for various reasons, such as switching spurs on the supply rails or harmonic distortion in the amplifiers. To mitigate the former, a two-stage power supply with switch-mode and linear regulators is employed. The switch-mode supplies regulate the input voltage to a value that is just above the minimum required linear regulator input considering the dropout. The linear regulators are selected for a high Power Supply Rejection Ratio (PSRR) at the given switching frequencies. Very little distortion on the analog supply rails is therefore expected. The remaining distortions are reduced by the good harmonic distortion performance of the employed operational amplifiers.

B.3.5 Realized Hardware Prototype

A picture of the realized hardware prototype considering all the above mentioned effects is shown in **Fig. B.5** with labeled input and output ports as well as auxiliary power supply. The overall dimensions of 114 mm × 78 mm

result mainly from the employed Bayonet Neill Concelman (BNC) connectors and also partially from restrictions of the component placement due to the symmetry requirements. Further miniaturization could be achieved by using smaller coaxial connectors (e.g. SMA or SMC).

A prominent difference compared to a passive noise separator is the requirement for an external power supply. However, the power consumption of measurement equipment is usually not of great importance, since there is not a continuous operation. Therefore, the total power consumption of 1.5 W, which is mainly composed of the quiescent power of the operational amplifiers, is acceptable, in particular in comparison with the several tens of watts that are consumed by the EMI test receiver. The measurement signal is loaded with an entirely resistive 50 Ω impedance, hence it does not significantly contribute to the losses.

B.4 Measurement Procedure and Results

B.4.1 Signal Injection Adapters

To characterize the overall performance of the three-phase active noise separator, a test setup that allows to apply pure CM or DM input signals to the separator and measure the corresponding outputs is used. The input signal is applied through matched adapter PCBs, one for CM and three for DM, which can be directly plugged on top of the separator. The stringent symmetry and matching requirements from the separator PCB layout equally apply to those adapters.

Providing a CM input is straight forward and in **Fig. B.6 (a)** the schematic of the utilized CM signal adapter is shown. It is implemented as purely resistive power splitter with one input port, to which a signal generator is connected, and three output ports which are connected to the separator. The CM adapter shows a nominal impedance of 50 Ω when looking into the input port, provided the three output ports are terminated with 50 Ω, which is inherently given when the CM adapter is connected to the separator. Such an implementation guarantees that the signal source connected to the input is properly terminated and no reflections occur. At the same time it can be realized with only one resistor R_t and without the need of having an additional series resistor between the star-point S (cf. **Fig. B.6**) and each output port. The resistor R_t in **Fig. B.6** is chosen such that in series with the parallel combination of the three 50 Ω terminations at the output ports an input impedance $\underline{Z}_\mathrm{in}$ equal to the nominal coaxial cable impedance of

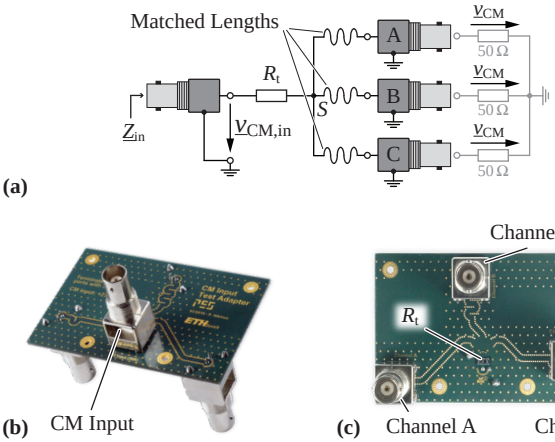


Fig. B.6: (a) Schematic of the CM adapter which is basically a very well matched power splitter with $\underline{Z}_{in} = 50\Omega$, providing the input signal $\underline{v}_{CM,in}$ on each of its output ports A, B and C with equal magnitude and phase. Picture of **(b)** the top side and **(c)** the bottom side of the assembled adapter showing the matched traces from the input to each output port.

$\underline{Z}_0 = 50\ \Omega$ results, i.e,

$$R_t = R_{out} - \frac{R_{out}}{3} = \frac{2}{3} R_{out} \overset{R_{out}=50\Omega}{=} 33.\overline{3}\ \Omega. \tag{B.17}$$

Given the value R_t, the theoretical insertion loss, i.e., the attenuation $G_{CM,i,theo}$ of the CM input signal in the CM adapter, is derived as

$$G_{CM,i,theo} = \frac{(R_{out}||R_{out}||R_{out})}{R_t + (R_{out}||R_{out}||R_{out})} = \frac{1}{3} = -9.54\ \text{dB}. \tag{B.18}$$

The implementation with a single resistor is favorable, since the focus of the CM adapter is to guarantee minimum channel-to-channel imbalance between A, B, and C and therefore, any component between the star-point S and the output ports with its inevitable tolerances would change the transfer behavior, especially the phase response as explained above. The three tracks from the star-point towards each of the output ports are length-matched and impedance-matched, resulting in an overall channel-to-channel skew of less than 2 ps, corresponding to a phase-shift of around $0.02°$ at 30 MHz.

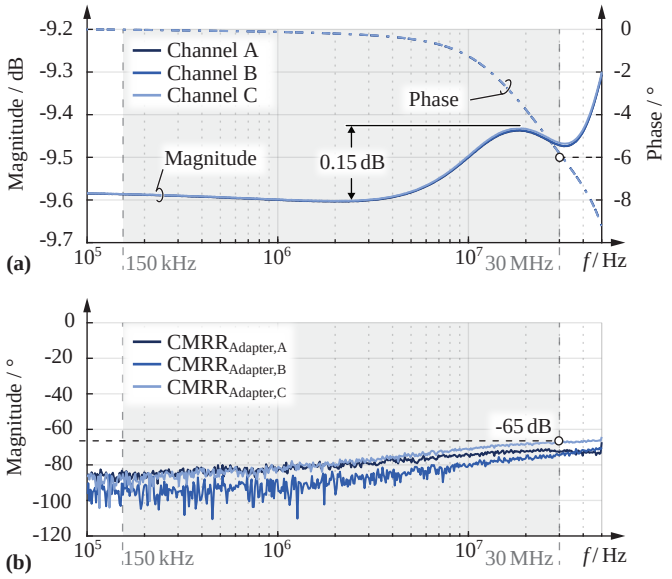


Fig. B.7: (a) Magnitude and phase response of the three channels on the CM adapter and **(b)** the calculated maximum measurable CMRR ($CMRR_{\text{Adapter}}$) for channels A, B and C, assuming an ideal separator with the only asymmetry arising from the CM adapter.

Fig. B.6 (b) and **(c)** show pictures of the realized CM adapter while **Fig. B.7 (a)** shows the measured amplitude and phase responses of the transfer functions of all three channels of only the CM adapter. Note, that each channel is measured separately with the network analyzer while the other two are terminated with 50 Ω. The measured insertion loss closely matches the nominal value of −9.54 dB calculated in (B.18) and the magnitude deviation is maximum 0.15 dB within the considered frequency range while the phase turns by −6°. Between the three channels, however, no significant magnitude and phase imbalance is visible. From these measured transfer functions $\underline{G}_{\text{CM,A}}, \ldots, \underline{G}_{\text{CM,C}}$, the theoretically maximum measurable CMRR

$$CMRR_{\text{Adapter},i} = \frac{\underline{G}_{\text{CM},i} - (\underline{G}_{\text{CM,A}} + \underline{G}_{\text{CM,B}} + \underline{G}_{\text{CM,C}})/3}{(\underline{G}_{\text{CM,A}} + \underline{G}_{\text{CM,B}} + \underline{G}_{\text{CM,C}})/3} \tag{B.19}$$

for $i = \{A, B, C\}$ is calculated under the assumption of an ideal separator based on (5.2) and (5.4). This means that the only error contribution to the

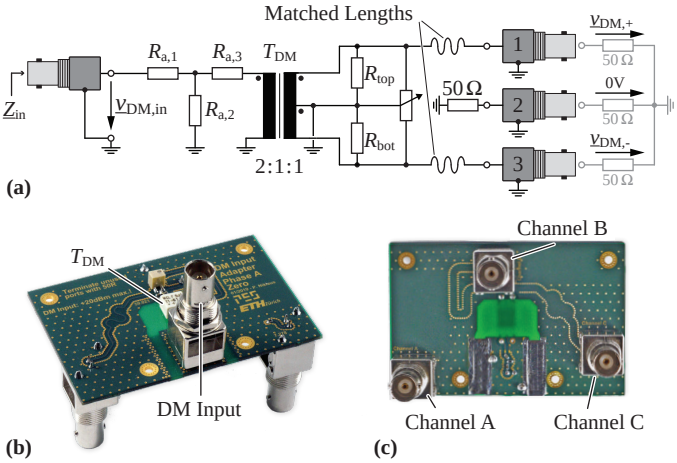


Fig. B.8: (a) Schematic drawing of the DM adapter which by means of a wideband transformer with secondary center-tap configuration converts a single-ended input signal $\underline{v}_{DM,in}$ to differential output voltages $\underline{v}_{DM,+}$ and $\underline{v}_{DM,-}$ being connected to two of the output ports, while the third is connected to ground via a termination resistor. There exist three variants of the DM adapter with either phase A, B or C connected to ground respectively (*DMA*, *DMB*, *DMC*). In **(b)** and **(c)** pictures of the top and bottom side of the variant *DMA* are shown, again indicating the matched traces on the board to equalize the propagation delay to ensure maximum symmetry.

CMRR is the imbalance of the three CM adapter channels, which must be much lower than the CMRR error contribution of the separator in order to properly quantify the CMRR performance of the separator. The maximum measurable CMRR according to (B.19) is corrected for the adapter insertion loss.

The results are shown in **Fig. B.7 (b)** and at 30 MHz a CMRR of at least −65 dB is achieved for all channels. Considering the results from the previous measurements with the difference amplifier (cf. **Fig. B.4**), this is sufficient to characterize the separator. It has to be emphasized, that the CMRR responses in **Fig. B.7 (b)** are created by post-processing based on measurements taken consecutively. Hence, a potential repeatability error of the network analyzer is included in these calculations.

Besides a CM adapter for the DMRR performance evaluation of the separator also a DM adapter is needed, since it is very difficult to generate a perfectly symmetric three-phase CM-free DM system. Thus, the DM characteristics were tested using a DM signal adapter that excites only two phases with two

signals 180° out of phase and leaves the third phase connected to ground, as shown in **Fig. B.8 (a)**. The input signal is fed to a wideband signal transformer (Mini-Circuits T1-6T-KK81+ [197]) whose center-tap configured secondary side is connected to two of the separator's input channels, providing two signals with half the magnitude and a phase-shift of 180°, denoted as $\underline{v}_{\mathrm{DM+}}$ and $\underline{v}_{\mathrm{DM-}}$. Imbalances in the transfer ratio from primary side to the two secondary sides can be adjusted with the two resistors R_{top} and R_{bot}, both set to 50 Ω nominally. Although the circuit would also work with no connection of the center-tap, measurements showed better performance when it is connected to the ground potential. The third separator input is terminated with 50 Ω to ground and therefore three variants of the DM adapter exist, hereinafter denoted with *DMA, DMB* and *DMC*, where the last letter denotes the phase that is connected to ground. All three adapters fulfill (5.2) when setting $\underline{v}_{\mathrm{CM}}$ to zero, i.e., $\underline{v}_{\mathrm{DM+}} + \underline{v}_{\mathrm{DM-}} = 0$. The resistive −6 dB attenuator composed of $R_{\mathrm{a},1\ldots3}$ at the input ensures an input impedance $\underline{Z}_{\mathrm{in}}$ sufficiently close to 50 Ω despite the frequency dependent transformer impedance transfer ratio.

In **Fig. B.9 (a)** the magnitude responses for both DM channels (DM+ and DM-) of all three DM adapters are shown. The insertion loss is around −12.2 dB for all three adapters and the worst-case channel imbalance occurs for *DMC* where the two responses DM+ (solid lines) and DM- (dashed lines) deviate by 0.1 dB at 30 MHz. The overall shape is very similar for all adapters and a flatness of 0.15 dB is achieved. **Fig. B.9 (b)** shows the phase error between the DM+ and DM- channels in each adapter, i.e., the deviation from the nominal 180° phase-shift. Here, it can be seen that *DMC* performs best with almost no phase error whereas *DMA* shows a deviation of 0.15° and *DMB* 0.55° respectively, both measured at 30 MHz. As a comparison, the same measurement was performed with a commercially available power splitter (Mini-Circuits ZSCJ-2-1+ [198]), which shows even more phase imbalance (around 0.7°). Based on the complex DMTFs $\underline{G}_{\mathrm{DM}i,+}$ and $\underline{G}_{\mathrm{DM}i,-}$ from the input $\underline{v}_{\mathrm{DM,in}}$ to the respective outputs $\underline{v}_{\mathrm{DM}i,+}$ and $\underline{v}_{\mathrm{DM}i,-}$ ($i = \{A, B, C\}$) the maximum measurable DMRR for each adapter

$$DMRR_{\mathrm{Adapter,DM}i} = \frac{(\underline{G}_{\mathrm{DM}i,+} + \underline{G}_{\mathrm{DM}i,-})/3}{\underline{G}_{\mathrm{DM}i,\pm}} \tag{B.20}$$

is calculated in accordance with (5.2). It corresponds to the ratio of the voltage at the CM output port of an ideal separator with respect to its DM input voltage and it is only affected by asymmetries of the DM signal adapters. The resulting responses are depicted in **Fig. B.9 (c)** and for a simpler comparison to the results of the separator (cf. **Fig. B.11**), the $DMRR_{\mathrm{Adapter,DM,i}}$ responses are corrected for the nominal insertion loss of the corresponding DM signal

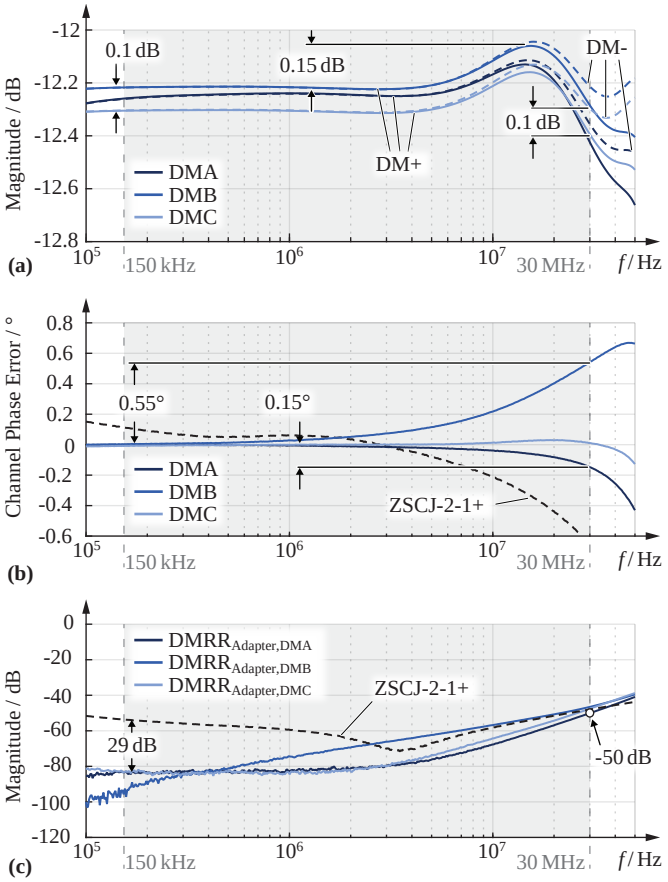


Fig. B.9: **(a)** Amplitude responses for all three DM adapter variants (*DMA*, *DMB* and *DMC*), showing the ratio $\underline{G}_{\mathrm{DM},+} = \underline{v}_{\mathrm{DM},+}/\underline{v}_{\mathrm{DM,in}}$ (solid lines) and $\underline{G}_{\mathrm{DM},-} = \underline{v}_{\mathrm{DM},-}/\underline{v}_{\mathrm{DM,in}}$ (dashed lines) respectively, **(b)** the deviation from the nominal phase difference of 180° and **(c)** the maximum measurable DMRR assuming an ideal separator (corrected for the DM adapter insertion loss). In addition, **(b)** and **(c)** show the phase error and maximum measurable DMRR when using a commercial power splitter [198] (dashed line).

adapter. Since the magnitude response of both, $\underline{G}_{\mathrm{DM}i,+}$ and $\underline{G}_{\mathrm{DM}i,-}$ is almost identical (cf. **Fig. B.9 (a)**), it does not matter which of the two is taken for the correction in (B.20). It can be seen that for frequencies below 3 MHz a DMRR

better than −80 dB can be measured. At elevated frequencies, however, the DMRR starts to rise and at 30 MHz the error contribution due to asymmetries in the DM adapters gives a DMRR of −50 dB, which means that even if the separator would achieve a DMRR *better* than −50 dB, a DMRR *worse* than −50 dB would be measured, since the adapter board is limiting the maximum measurable DMRR. All three DM adapters achieve approximately the same DMRR at 30 MHz, since e.g. *DMB* has a considerable phase deviation but a very low amplitude error whereas *DMC* has almost no phase deviation but the highest amplitude error. It is observed that *DMB* shows inferior performance compared to the other two adapters, which can be improved with better trimming of R_{top} and R_{bot} on the secondary side (cf. **Fig. B.8**). Additionally, the same curve is shown for the commercial power splitter and the achievable performance is worse particularly at low frequencies (29 dB worse), which justifies the usage of the custom-made adapters.

Remark:
Instead of two input signals with 180° phase-shift a three-phase DM system with 120° phase-shift between the individual signals could be realized with a Digital Signal Processor (DSP) or a Field-Programmable Gate Array (FPGA). However, to achieve a phase accuracy of 0.5° as it is reported for the presented DM signal adapters (cf. **Fig. B.9 (b)**), particularly at high signal frequencies, a time resolution in the sub-nanosecond range would be required. This would be very difficult to realize in practice and therefore, the purely passive DM signal adapters are a very convenient method.

B.4.2 Measurement Setup

The separator transfer and rejection characteristics are captured using the Omicron Lab Bode100 network analyzer with the corresponding test setup shown in **Fig. B.10**. The output of the network analyzer is fed to the separator via the CM or one of the DM adapters. The output port to be measured (DM output A in **Fig. B.10**) is connected to the receiver of the analyzer while all others are terminated with 50 Ω. All the transfer and rejection characteristics shown hereinafter are corrected with respect to the adapter insertion loss, such that for example a unity-gain CMTF means that there is no attenuation between a CM input signal at ports *InA, InB* and *InC* of the separator and the corresponding CM output port *CM*.

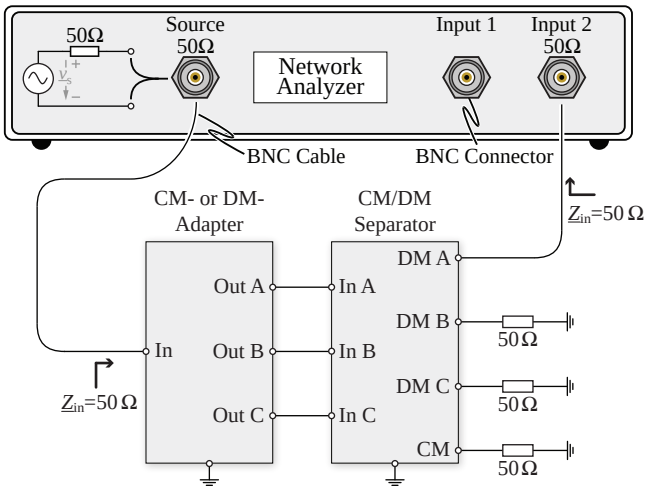


Fig. B.10: Test setup for measuring the active separator characteristics using the Omicron Lab Bode100 network analyzer. The CM or DM input from the Bode100 source is fed to the separator via the CM- or DM-adapter shown in Figs. B.6 and B.8 respectively and the corresponding output is directly connected back to the Bode100 receiver input, while all other separator outputs are terminated with 50 Ω.

B.4.3 Separator Transfer Function and Rejection Ratio Measurements

The resulting separator transfer and rejection characteristics are indicated in **Fig. B.11**. The DMTF and CMTF in **Fig. B.11 (a)** are very flat, showing an absolute deviation of less than 0.25 dB and practically no relative deviation (< 50 mdB) over the whole considered frequency range with nominal unity-gain, i.e., 0 dB. The CMRR in **Fig. B.11 (b)** is very similar to the response found for the difference amplifier (cf. **Fig. B.4**), starting at −60 dB and staying at this value until around 10 MHz, before reaching values of −52 dB (channels A and B) and −46 dB (channel C) at 30 MHz. Although there are three channels, the previously mentioned trimming method can only optimize the CMRR of one channel (here channel A, which consequently shows the best CMRR). While channels A and B show very similar behavior at high frequencies, channel C shows a slightly worse (9.5 dB worse at 10 MHz), yet still sufficiently good performance, which can be explained with different parasitics in amplifier A_6 and/or a mismatch in $R_{\mathrm{F,DM}}$ or $R_{\mathrm{G,DM}}$ compared to the other channels. The difference at lower frequencies is again explained with the influence

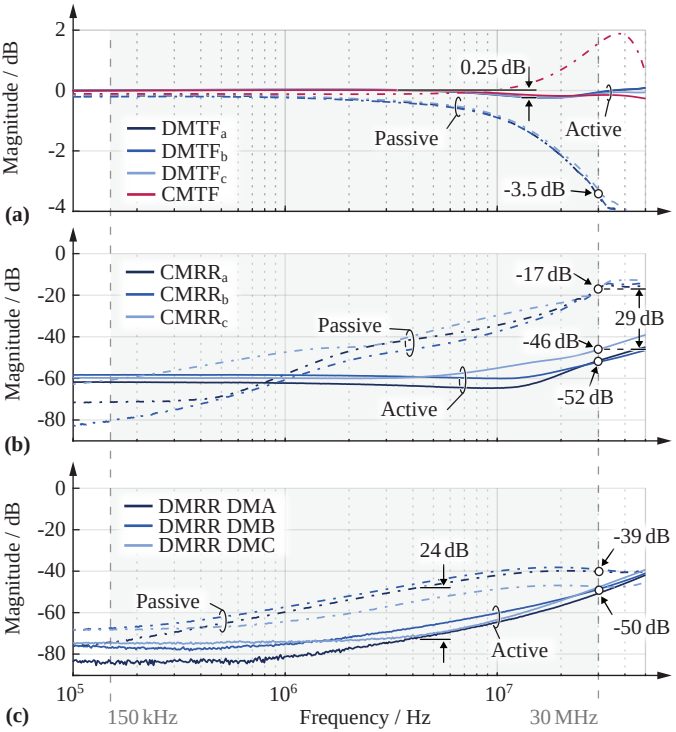


Fig. B.11: Transfer Functions (TFs) and Rejection Ratios (RRs) for the active noise separator of [162] (continuous lines) and the passive separator described in [161] (dashed lines). **(a)** CMTF and DMTF, **(b)** CMRR for each DM output and **(c)** DMRR measured each time with one of the inputs set to zero (measured with the three DM signal adapters; DM*i* means input *i* was set to zero). This figure is identical to Fig. 5.7 and is shown here again for better readability.

of parasitic resistances from the PCB tracks, solder joints etc. which are superimposed to the 0.01 % tolerance of the resistors. The DMRR depicted in **Fig. B.11 (c)** starts at around −80 dB at low frequencies and reaches −50 dB at 30 MHz. There are three responses *DMRR DMi*, $i = \{A, B, C\}$ illustrated, since the CM output port is measured for an excitation with each of the three DM adapters *DMi*. The deviation between these three curves is explained with the slightly different transfer characteristics of the DM adapter (cf. **Fig. B.9**) as well as with the selected trimming method where only one channel can be optimized. Interestingly, comparing **Fig. B.9 (c)** with **Fig. B.11 (c)**, the

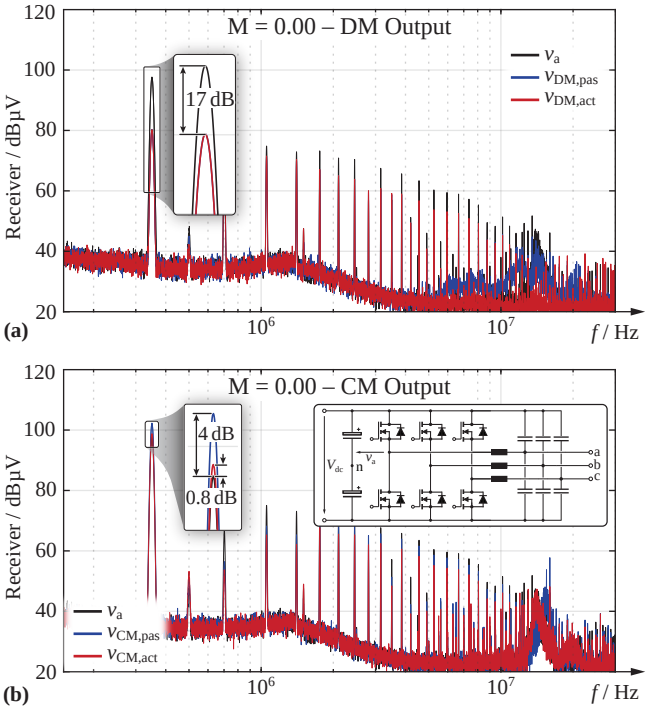


Fig. B.12: Noise spectra captured of a three-phase Voltage Source Inverter (VSI). **(a)** DM and **(b)** CM output spectrum for a converter modulation depth $M = 0$. This corresponds to pure CM switching noise. A comparison measurement using a passive noise separator is performed as well. The overall noise level is deliberately selected considerably higher than the EMI standards to highlight the separator dynamic range.

HF DMRR is mainly determined by the finite symmetry of the DM signal adapters. Therefore, it is very likely that the separator performs better than the measurements here indicate. Important to note is that due to the unity-gain CMTF and DMTFs the selectivities, i.e., $DMTF/CMRR$ and $CMTF/DMRR$ are simply the inverse of the $CMRR$ and $DMRR$ and are not explicitly shown here.

B.4.4 Separator Converter Measurements

Finally, spectral measurements with a three-phase VSI are performed using the presented active noise separator to demonstrate its practical applicability.

Comparison measurements with a pre-existing passive separator allow a performance comparison between the two variants. The test setup from **Fig. B.1** is extended by placing the noise separator between the LISN [172] and the EMI test receiver [199]. **Fig. B.12** shows measured spectra for zero modulation depth ($M = 0$). This corresponds to the case where the three bridge legs are switching ($f_{sw} = 350\,\text{kHz}$) but do not generate any output voltage, resulting in pure CM noise. Measurements are taken at **(a)** the DM output port and **(b)** the CM output port. The tested inverter is not mains-interfaced and therefore, does not need to comply with the EMI regulations. Hence, in all cases the measured values are exceeding the limiting values. This case allows to illustrate the function of the separator also with large input signals. The black curves denote the total phase voltage noise spectrum, whereas the red and blue curves are the measurement results obtained with the active and passive noise separator, respectively. In addition, **Fig. B.12 (b)** shows the utilized converter structure. Its output filter is referenced to the dc link and therefore, the filter components are effective for CM and DM noise. It is clearly visible that the separator CMRR is not the limiting factor, since the switching frequency DM component is only 17 dB below the total noise voltage component. Despite the pure CM switching operation of the VSI, there is apparently a DM noise voltage component present at the output due to non-idealities and/or asymmetries in the switching control and circuit. This demonstrates, that a reliable decomposition of EMI noise into CM and DM components does not only require a high-performance noise separator but also a very symmetric overall test setup.

Overall, the presented spectral measurements proof the practical applicability of the active noise separator even for very large noise voltages. Furthermore, the HF behavior is considerably better compared to the passive separator, which particularly suffers from an insufficient CMRR as revealed by the substantial noise components at its DM outputs (cf. **Fig. B.12 (a)**). It becomes clear that a practical measurement setup contains many asymmetries, which can only be determined and quantified when a high-performance noise separator is used (cf. **Chapter 5**).

C

Three-Phase CM/DM Decomposition

In the following, the decomposition of an arbitrary, not necessarily balanced three-phase voltage system into its respective Common Mode (CM) and Differential Mode (DM) components is derived.

Fig. C.1 (a) shows a general asymmetric three-phase arrangement ($\underline{v}_i$ indicating the High-Frequency (HF) noise source of phase i, $\underline{Z}_i$ the inner noise source impedance or filter circuit impedance and $\underline{Z}_0$ the capacitive coupling to ground) with the following properties:

$$\underline{v}_{\mathrm{LISN,a}} = \underline{i}_{\mathrm{a}} R_{\mathrm{LISN}} = \underline{v}_{\mathrm{a}} - \underline{i}_{\mathrm{a}}\underline{Z}_{\mathrm{a}} - (\underline{i}_{\mathrm{a}} + \underline{i}_{\mathrm{b}} + \underline{i}_{\mathrm{c}})\underline{Z}_0 \tag{C.1}$$

$$\underline{v}_{\mathrm{LISN,b}} = \underline{i}_{\mathrm{b}} R_{\mathrm{LISN}} = \underline{v}_{\mathrm{b}} - \underline{i}_{\mathrm{b}}\underline{Z}_{\mathrm{b}} - (\underline{i}_{\mathrm{a}} + \underline{i}_{\mathrm{b}} + \underline{i}_{\mathrm{c}})\underline{Z}_0 \tag{C.2}$$

$$\underline{v}_{\mathrm{LISN,c}} = \underline{i}_{\mathrm{c}} R_{\mathrm{LISN}} = \underline{v}_{\mathrm{c}} - \underline{i}_{\mathrm{c}}\underline{Z}_{\mathrm{c}} - (\underline{i}_{\mathrm{a}} + \underline{i}_{\mathrm{b}} + \underline{i}_{\mathrm{c}})\underline{Z}_0 \tag{C.3}$$

Three individual noise voltages $\underline{v}_{\mathrm{LISN},i}$, the effect of a filtering measure or of specific properties of the noise sources $\underline{v}_i$, cannot be translated into a CM and DM part concerning (C.1) — (C.3), especially considering the typically inductive behavior of $\underline{Z}_i$ (increasing impedance with increasing frequency) and the capacitive behavior of $\underline{Z}_0$ (decreasing impedance with increasing frequency).

Following the symmetry of the supplying three-phase mains, three-phase power electronic converter systems are built considering phase symmetry, which also ensures equal loading of the phase bridge legs. In consequence, also the filter circuits show phase symmetry (neglecting, e.g., the influence of different instantaneous phase current levels on the inductance value of the phase filter inductors) and we have

$$\underline{Z}_{\mathrm{a}} = \underline{Z}_{\mathrm{b}} = \underline{Z}_{\mathrm{c}} = \underline{Z}. \tag{C.4}$$

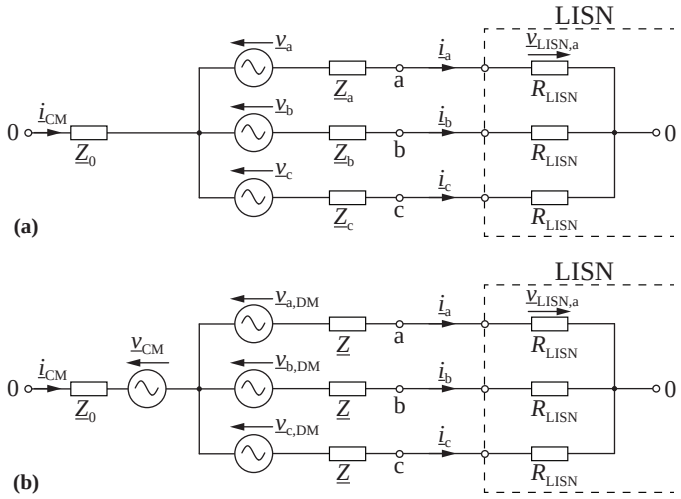


Fig. C.1: (a) High-Frequency (HF) equivalent circuit of a three-phase converter with inner noise source impedances connected to the Line Impedance Stabilization Network (LISN) and **(b)** decomposition into CM and DM components.

Based on (C.4) the leakage current to ground,

$$\underline{i}_{CM} = \underline{i}_a + \underline{i}_b + \underline{i}_c \tag{C.5}$$

is equally distributed to the phases and driven by a voltage component, which is equally contained in the phase noise voltages $\underline{v}_i$ and called CM voltage

$$\underline{v}_{CM} = \frac{1}{3}\left(\underline{v}_a + \underline{v}_b + \underline{v}_c\right). \tag{C.6}$$

Accordingly, the remaining voltages

$$\underline{v}_{DM,a} = \underline{v}_a - \underline{v}_{CM} \tag{C.7}$$
$$\underline{v}_{DM,b} = \underline{v}_b - \underline{v}_{CM} \tag{C.8}$$
$$\underline{v}_{DM,c} = \underline{v}_c - \underline{v}_{CM} \tag{C.9}$$

with

$$\underline{v}_{DM,a} + \underline{v}_{DM,b} + \underline{v}_{DM,c} = 0 \tag{C.10}$$

are driving noise currents $\underline{i}_{\mathrm{DM},i}$, which are remaining inside the three-phase circuit arrangement, called DM noise currents. Finally, this results in a splitting of the measured noise voltage

$$\underline{v}_{\mathrm{CM,LISN}} = \underline{v}_{\mathrm{cm}} - \underline{i}_{\mathrm{CM}} \left(\underline{Z}_0 + \frac{1}{3}\underline{Z} \right) \tag{C.11}$$

$$\underline{v}_{\mathrm{DM,LISN},i} = \quad \underline{v}_{\mathrm{DM},i} - \underline{i}_{\mathrm{DM},i} \cdot \underline{Z} \tag{C.12}$$

which is of clear advantage,

- as the composition of the noise source voltage can be directly influenced through the modulation of three-phase converter circuits,
- dedicated filter arrangements can be provided to combat a CM *or* DM noise problem, which is facilitated by the fact that
- the above mentioned inductive and capacitive characteristics of $\underline{Z}_i$ and $\underline{Z}_0$ are now taking mainly influence only on one of the two noise components. The CM capacitance C_{CM} has a very high impedance at low frequencies and only at elevated frequencies has a low impedance, where it effectively leads to a CM noise voltage source with low inner impedance.

D

DM-to-CM Conversion in Three-Phase EMI Noise Separation

In the following, the conversion of a Differential Mode (DM) signal at the input of a three-phase CM/DM Electromagnetic Interference (EMI) noise separator for Conducted Emissions (CEs) into a Common Mode (CM) signal at its output is briefly explained to complement the thorough analysis of the reciprocal CM-to-DM conversion from **Chapter 5**. As mentioned in **Section 5.3**, in an asymmetric three-phase transmission system besides the CM-to-DM conversion also the reciprocal DM-to-CM conversion takes place. Assuming a perfectly balanced three-phase DM voltage system at the input of the asymmetric transmission system, similarly to the case of a pure CM input voltage from **Fig. 5.8**, a certain amplitude and phase mismatch at the transmission system output results. With channel *a* as reference channel, there are amplitude ratios $V_\mathrm{b}/V_\mathrm{a}$ and $V_\mathrm{c}/V_\mathrm{a}$ as well as phase-shifts φ_ab and φ_ac. **Fig. D.1** shows the DM-to-CM conversion resulting from imperfect amplitude ratios ($V_\mathrm{b}/V_\mathrm{a} \neq 1$ and $V_\mathrm{c}/V_\mathrm{a} \neq 1$) and phase-shifts deviating from the nominal values of $\varphi_\mathrm{ab} = 120°$ and $\varphi_\mathrm{ac} = 240°$, respectively. Notable is that for the DM-to-CM conversion there exists no mutual cancellation of the amplitude and/or phase error compared to the CM-to-DM conversion (cf. **Fig. 5.9**). Therefore, for certain amplitude and/or phase error combinations, there is a more pronounced DM-to-CM conversion. However, as stated in **Section 5.3**, for a given maximum amplitude or phase error, the worst-case DM-to-CM conversion in a three-phase system is typically less pronounced compared to the CM-to-DM conversion. This is exemplary indicated in **Fig. D.1 (b)** for the point corresponding to a phase error of $-2.6°$ for both, φ_ab and φ_ac, respectively. The DM-to-CM conversion results in -36.5 dB whereas for the same phase error a CM-to-DM conversion of -30.4 dB results (cf. **Fig. 5.9 (e)-(f)**).

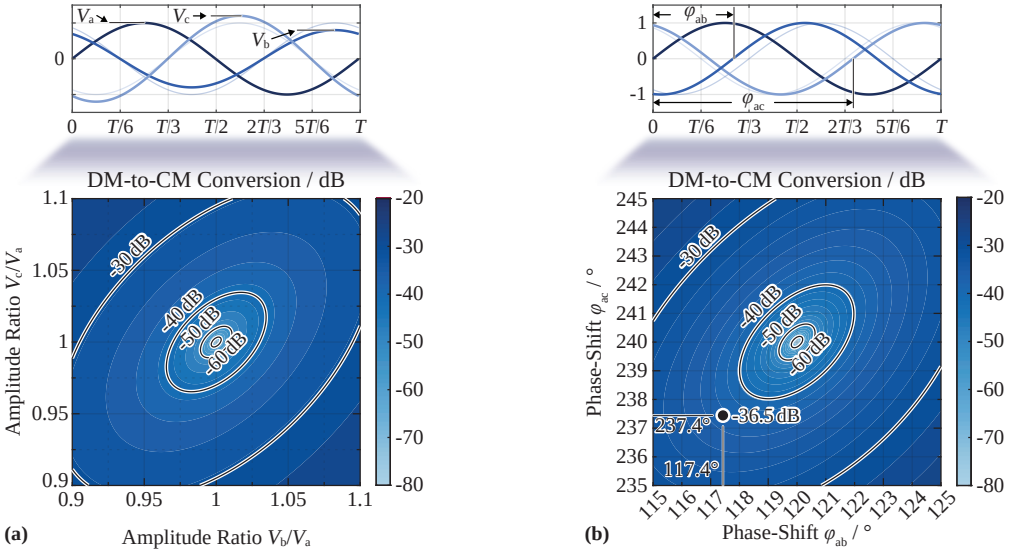


Fig. D.1: Amplitude and phase mismatches at the output of an unsymmetric three-phase transmission system and related characterization of the transmission system with a DM-to-CM conversion. A perfectly balanced three-phase DM input voltage system and an ideal separator are assumed thereby. In all cases, input channel *a* is treated as reference. Therefore, the noise separator input voltages *b* and *c* show amplitude/phase mismatches with respect to voltage *a*. **(a)** Considering only an amplitude mismatch V_b/V_a and V_c/V_a ($\varphi_{ab} = 120°$ and $\varphi_{ac} = 240°$) and **(b)** considering only a phase mismatch φ_{ab} and φ_{ac} ($V_b/V_a = 1$ and $V_c/V_a = 1$).

E

Internal LISN Structure

In the following, the internal structure of a commercially available Line Impedance Stabilization Network (LISN) [172] is investigated. Thereby, the measured and simulated Transfer Function (TF) from Equipment Under Test (EUT) port to the High-Frequency (HF) measurement output port is presented as well as the simulated input impedance seen by looking into the EUT port. The latter is compared with the requirements from the applicable Electromagnetic Compatibility (EMC) standard [160]. Moreover, the same comparison is done for the case when the LISN's internal measurement path is bypassed by means of an external High-Pass Filter (HPF) as shown in **Section 5.5.2**.

E.1 LISN High-Frequency Transfer Function

Fig. E.1 (a) shows the internal structure of a commercially available LISN [172] according to the CISPR 16-1-2 (EN 55016-1-2) standard [160]. The EUT is decoupled from the mains with large cylindrical air-core inductors (50 µH and 250 µH) and capacitors. Resonances are damped with resistors in parallel to the large inductors. The HF signal (highlighted in blue) passes through a HPF composed of two 1 µF capacitors and a 1.5 mH inductor. Low-Frequency (LF) signals such as the 50/60 Hz component related to the power flow (highlighted in red) are heavily attenuated. Below the HPF's cut-off frequency of around 6 kHz the gain drops with approximately −50 dB/dec. This is illustrated in **Fig. E.1 (b)** with the simulated and measured TF $\left|\underline{v}_{\mathrm{HF}}/\underline{v}_{\mathrm{EUT}}\right|$ from the EUT input port to the HF measurement port (blue lines). The 50/60 Hz mains voltage component with a peak value of 325 V is attenuated by almost 120 dB, hence only around 0.5 mV appear at the HF measurement port. This particular LISN model features an additional 10 dB attenuator to protect measurement equipment connected to the HF port from large voltages that can occur if

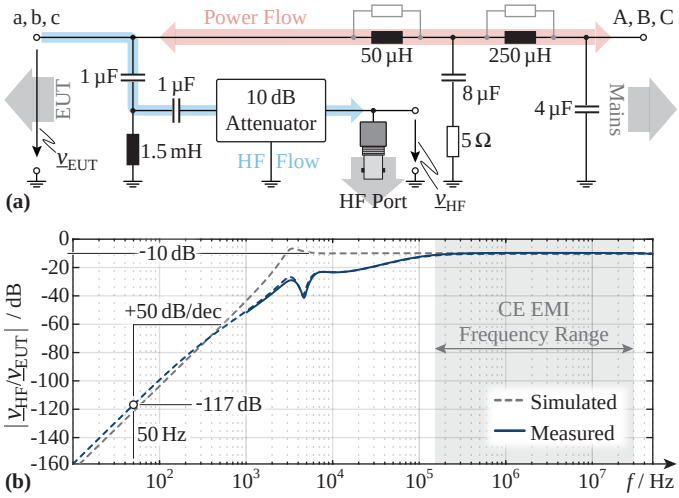


Fig. E.1: (a) Internal structure for one channel of a commercially available LISN. Indicated are the power and HF signal flow. **(b)** Measured (continuous line) and simulated (dashed line) TF from EUT port ($\underline{v}_{\mathrm{EUT}}$) to HF measurement port ($\underline{v}_{\mathrm{HF}}$).

the EMI noise is not attenuated sufficiently by the EMI filter in the EUT. In the relevant frequency range, the transfer function is flat and only the 10 dB attenuation remains.

Remark:
The roll-off with roughly −20 dB/dec starting at around 100 kHz is due to the network analyzer's internal 50 Ω resistor in series with its output port. Together with the EUT port impedance that is lower than 50 Ω at frequencies below 150 kHz, this leads to an additional apparent filtering behavior. In practice, this does not influence the fundamental frequency (50/60 Hz) component attenuation of almost 120 dB as verified with the gray dashed line that corresponds to the simulated transfer function where the effect of the network analyzer's internal 50 Ω resistor is corrected.

E.2 LISN EUT Port Input Impedance

Fig. E.2 shows the simulated LISN input impedance **(a)** magnitude and **(b)** phase angle seen at the EUT port ($\underline{Z}_{\mathrm{EUT}}$) for the internal and the external HF measurement paths (cf. **Section 5.5.1** and **Section 5.5.2**). Further depicted is the nominal value of $\underline{Z}_{\mathrm{EUT}}$ (dotted lines) and the corresponding tolerance

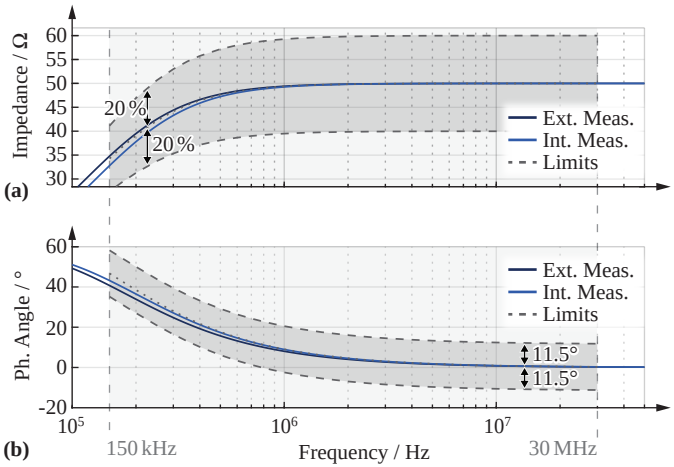


Fig. E.2: Simulated LISN input impedance at the EUT port for both, internal and external High-Frequency (HF) measurement paths. **(a)** Magnitude and **(b)** phase angle, including the tolerance band around the nominal value according to CISPR 16-1-2.

bands (dashed lines) according to the CISPR 16-1-2 regulations (±20 % for the magnitude and ±11.5° for the phase angle) [160]. This demonstrates, that even with an external HPF the setup complies with the standards.

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