25kW Three-Phase Unity Power Factor Buck Boost Rectifier with Wide Input and Output Range for Pulse Load Applications

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***Abstract*—Pulse loads, like solid state pulse modulators, generate short pulses with a high peak power that exceeds the average power by 100 to 1000 times depending on the pulse repetition rate. There, the peak power usually is drawn from an energy buffer such as a capacitor bank. The pulse discharges the energy buffer and it is fully recharged in the time between the pulses by a power supply, which is usually connected to the mains.**

Due to the world-wide variation in mains voltages and the desired ability to adapt to the capacitor voltage of the modulator, the power supply has to support a wide input and output voltage range. Additionally, the supply should draw a sinusoidal current from the mains while providing energy to the pulse modulator due to EMI regulations. Therefore, a general control concept for pulse load applications, which guarantees continuous power consumption from the mains and power factor correction (PFC), is described in this paper. Furthermore, measurements of the control principle, which is independent from the converter topology, are presented for a three-phase buck boost rectifier.

***Index Terms*—Buck Boost Rectifier, Capacitor Charging, Constant Input Power, Pulse Modulator, Power Factor Correction.**

I. Introduction

SOLID state pulsed power systems containing IGBTs are often operated with input voltages between 100V and 6.5kV due to the maximum allowable blocking voltage of the switches. Nevertheless, high output voltages of several kilovolts (e.g. ~100-200kV) can be achieved, for example, by the use of pulse transformers, adder topologies or Marx generator configurations [1],[2].

Generally, the pulse power (e.g. 20MW for the case considered in this paper) is provided from a capacitor bank, whereas the average power (20kW) is supplied by a converter [3] connected to the mains, as shown in Fig. 1. There, the three-phase line-to-line voltage can vary from 177V to 528V to enable world-wide operation.

Additionally, a variation of the capacitor voltage v_{C0} of the modulator is often desired for adapting the pulse voltage. Therefore, a wide input and output voltage range of the rectifier is needed. These requirements can be fulfilled with a three-phase buck-boost rectifier [4] (cf. Fig. 2), which operates either in the buck or the boost mode, depending on the ratio of the mains voltage to the capacitor bank voltage v_{C0}. In case of the assumed high pulse repetition rate of 500-1000Hz, the capacitor bank has to be recharged before the next pulse is generated, which would demand, especially during load changes, a high dynamic voltage control. There, the voltage should be regulated within ±1% of the reference voltage after 5 pulses for a load step from zero to full load (25kW). This, for example, corresponds to a settling time of 5ms for a pulse repetition frequency of 1000Hz.

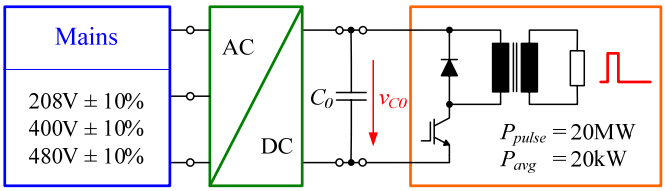

Fig. 1. Pulse modulator supplied by an AC-DC power converter for unity power factor and sinusoidal mains currents.

To enable unity power factor operation of the three-phase buck-boost rectifier, a constant inductor current i_{L0} is required [4]-[6]. The pulse load in combination with a conventional high dynamic voltage control, however, would result in periodic peak currents in the buck-boost inductor and also in the input/mains currents $i_{N,i}$. These current distortions make unity power factor operation of the converter impossible.

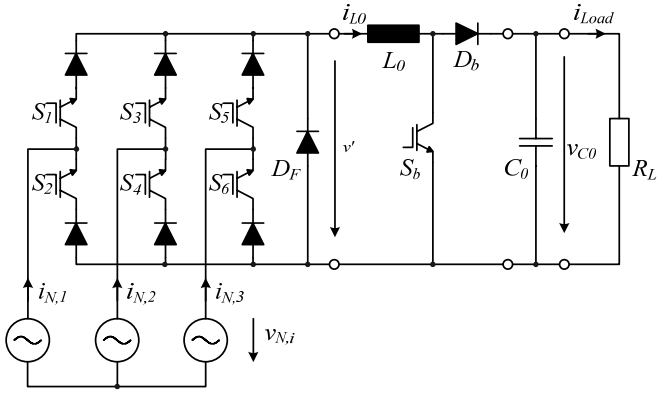

Fig. 2. Schematic of the considered buck-boost converter. There, the input filter is not shown for the reason of simplicity.

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Hence, a control strategy for pulse load applications, which achieves unity power factor as well as accurate regulation of the output voltage, must be applied.

In **Section II** the operating principle, including the basic structure of the controller [4]-[6], is described. Conventional control of the converter is then explained and its drawbacks, which result in distorted mains, are highlighted in **Section III**. Following this, the proposed control method is described, which enables approximately constant power consumption with unity power factor. Finally the control approach is validated with measurement results of the input and output current/voltage waveforms, which are presented in **Section IV**.

II. Buck Boost Rectifier

As shown in Fig. 2 the input stage of the buck-boost converter consists of six switches S_1-S_6 with series connected diodes, which are connected to either a common negative or positive voltage terminal. The following boost stage consists of switch S_b, diode D_b and the inductance L_0. The buck input stage operates as PFC input stage, which produces sinusoidal mains currents.

In case the output voltage v_{C0} is lower than the peak line-to-line mains voltage, only the input stage is used and the converter operates in the buck mode.

For higher output voltages, the boost switch S_b must be activated. The prototype, which has been used for validating the control scheme, is shown in Fig. 3 and the specifications are given in Table. 1.

In order to limit the current ripple ΔI_{L0} the converter is operated in continuous conduction mode (CCM) with an average value I_{L0} of the inductor current i_{L0}. At high switching frequencies and with a large inductance L_0, the ripple current

Fig. 3. Photograph of the three-phase buck boost rectifier with unity power factor and a wide input and output range.

TABLE I
Specifications of the Considered Buck Boost Rectifier

Input voltage v_N	*177V – 528V*
Output voltage v_{C0}	*150V – 450V*
Load current I_{Load}	*55A – 167A*
Average Power P_{avg}	*25kW*

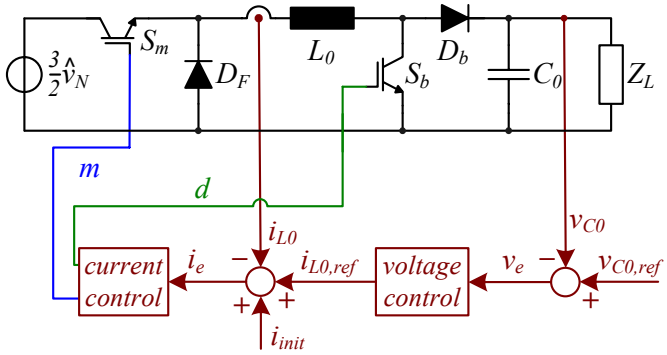

Fig. 4. Single phase DC-DC equivalent circuit of the three-phase buck boost converter with cascaded current and voltage control structure.

is neglected for simplification. Assuming a constant current $i_{L0}=I_{L0}$, the duty cycles of the buck stage switches directly can be calculated to achieve unity power factor operation, which is described in detail in [4]-[6].

In order to obtain a constant output voltage the duty cycles of the switches must be adapted to the input voltage and the load by a controller. For a symmetrical three-phase supply the control behavior of the three-phase buck boost rectifier can be modeled by a single phase DC-DC converter with constant input voltage [6], as shown in Fig. 4. There, also the proposed and implemented cascaded control structure of the converter with an outer voltage control and an inner current control loop is depicted.

For the control of the output voltage, the voltage v_{C0} is measured and compared to the reference voltage $v_{C0,ref}$. The voltage difference, which is equal to the voltage error v_e, is the input of the voltage controller. This controller is implemented as a PI-controller and its output is the reference current $i_{L0,ref}$ for the inner current control loop. The current error i_e, which is feed into the current control block, is obtained by subtracting the measured inductance current i_{L0} from the current reference $i_{L0,ref}$. With the error signal i_e the duty cycles m and d of the buck and boost stage are calculated in the current controller. In order to achieve a higher dynamic response an initial current i_{init} can be added to the reference current $i_{L0,ref}$.

III. Control Concept for Pulse Load Applications

The control structure in Fig. 4 is usually designed for continuous loads, where the output voltage is controlled to a constant value. With a constant voltage and a constant load at the output also continuous energy consumption from the mains and sinusoidal mains currents are obtained.

In case of a solid state modulator the power consumption of the load is discontinuous (only a few µs) and has a high peak value (20MW) compared to the average power (20kW). The energy for the pulses is usually provided from capacitor banks (cf. C_0 in Fig. 1) [1], [2]. Due to the large peak power the capacitor voltage v_{C0} drops (here: 1%/10V) below its reference values $v_{0,ref}$ during the pulse (cf. Fig. 5). Consequently, the voltage error v_e increases rapidly. Assuming a controller with high dynamic, the "step like"

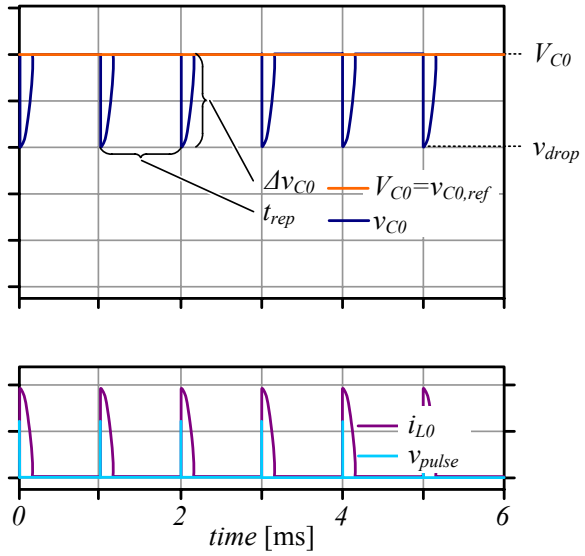

Fig. 5. Schematic waveforms of the capacitor voltage v_{C0} and the load current i_{L0} with conventional control and pulse load. For example, the pulse repetition frequency was selected to 1000Hz.

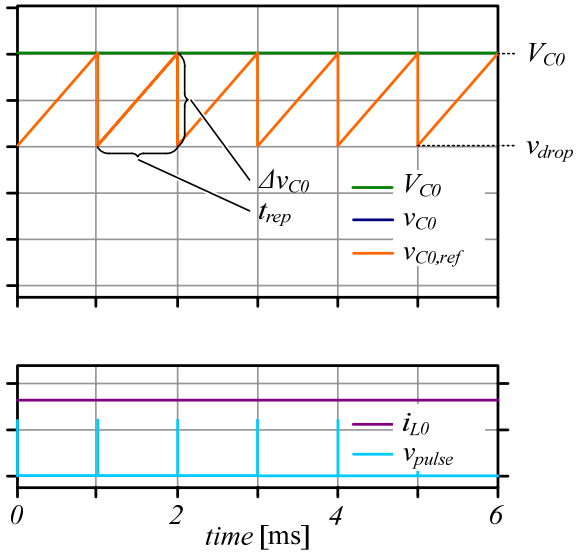

Fig. 6. Schematic waveforms of the reference voltage $v_{C0,ref}$, the pulse voltage v_{Pulse} and the inductor current i_{L0} for the proposed control method with unity power factor for *case A* (pulse repetition frequency of 1000Hz).

increase of the error signal results in a rapidly increasing inductor current i_{L0} for recharging the capacitor bank up to the reference value $v_{0,ref}$.

As soon as the reference value is reached the controller must decrease the inductor current down to zero again, since the load current is zero in between two consecutive pulses. This control behavior could be observed after every pulse, what would result in a highly distorted pulsating /discontinuous mains current with a low power factor.

A. Control based on reference signal modulation

In order to achieve sinusoidal currents with high power factor and a continuous power flow from the mains for pulse load applications a control principle with modulated reference signal is derived in the following. There, two conditions must be fulfilled for proper system operation:

1) For constant pulse amplitude a constant capacitor voltage v_{C0} at the beginning of the pulse is required.
2) To achieve a unity power factor the converter modulation described in [4]-[6] a constant input power is required. There are two cases, which can be distinguished.
   Case A: The ripple of the capacitor voltage Δv_{C0} is small and could be neglected. Consequently, constant input power demands, due to the approximately constant capacitor voltage v_{C0} and $p_{out} = v_{C0} \cdot i_{L0}$, a constant inductor current i_{L0}.
   Case B: The voltage ripple Δv_{C0} is large. Therefore, the inductor current i_{L0} is, due to $p_{out} = v_{C0} \cdot i_{L0}$, not constant any more. Consequently, the ripple current must be calculated as time function of the voltage v_{C0}.

In both cases the first condition only has to be satisfied at the time steps $n \cdot t_{rep}$ when the pulses are generated. Therefore,

$$v_0(n \cdot t_{rep}) = const. \quad (1)$$

In case A, which is considered first, the second condition must be always fulfilled, i.e.

$$i_{L0} = const. \quad (2)$$

For the pulse modulator with a capacitive storage bank C_0 the current i_{L0} respectively the capacitor voltage v_{C0} has to satisfy equation (3).

$$i_{L0}(t) = \frac{C_0}{(1-d)} \frac{dv_{C0}(t)}{dt} = I_{L0} = const. \quad (3)$$

Generally, the load current can be expressed as a function of

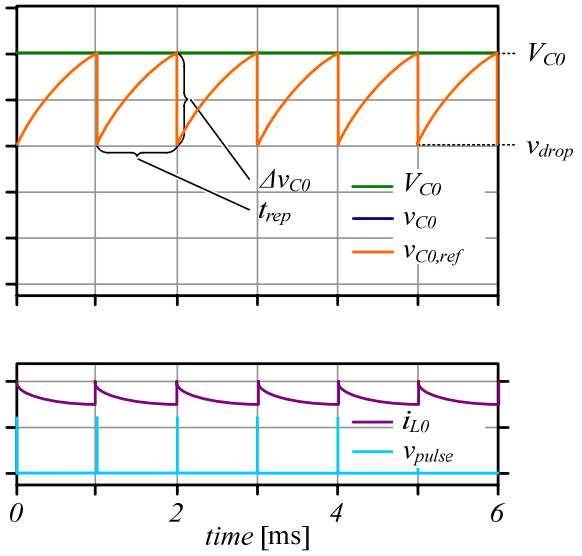

Fig. 7. Schematic waveforms of the reference voltage $v_{C0,ref}$, the pulse voltage v_{Pulse} and the inductor current i_{L0} for the proposed control method with unity power factor for *case B* (pulse repetition frequency of 1000Hz).

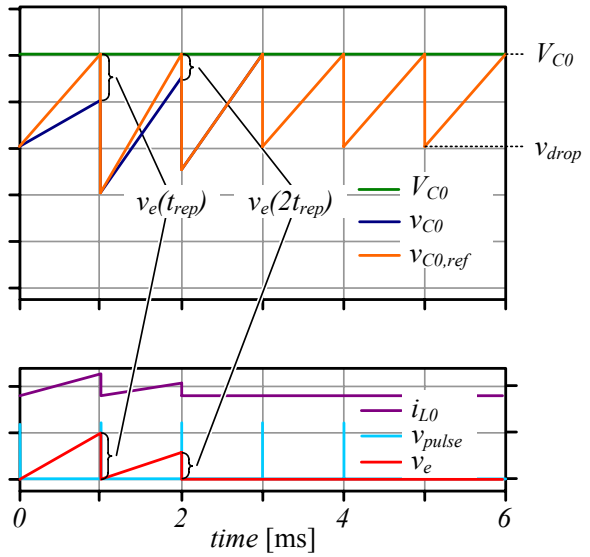

Fig. 8. Discontinuous inductance current i_{L0} at the beginning of a pulse sequence and after a load change due to the reset of the reference voltage $v_{C0,ref}$ after each pulse (pulse repetition frequency of 1000Hz).

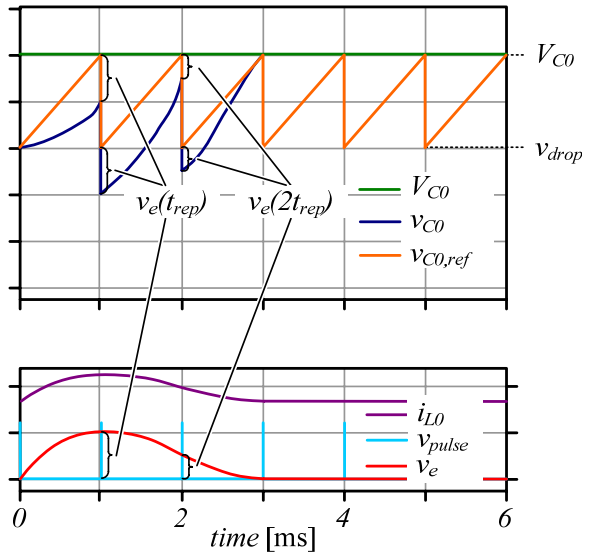

Fig. 9. Schematic waveforms of the continuous error voltage v_e and the inductance current i_{L0} at the beginning of a pulse sequence or after a load step (pulse repetition frequency of 1000Hz).

arbitrary complex load impedance Z_{Load}:

$$i_{L0} = f(Z_{Load}) \tag{4}$$

Integrating (3) for v_{C0}(t) and assuming a constant inductor current i_{L0} results in

$$v_{C0}(t) = \frac{(1-d)}{C_0}\int_0^t I_{L0}dt = v_{C0}(0) + \frac{(1-d)I_{L0}}{C_0}\cdot t \tag{5}$$

Consequently, the capacitor voltage v_{C0} must change linearly in order to achieve a constant current i_{L0} for unity power factor. There also (1) has to be fulfilled.

Thus, a linear increasing reference voltage $v_{C0,ref}$ instead of a constant reference voltage V_{C0} is used for the proposed control method. The slew rate of the reference voltage $v_{C0,ref}$ could be determined with the pulse repetition time t_{rep} and the voltage drop Δv_{C0} during the pulse since also (1) must be satisfied.

The initial reference voltage $v_{C0,ref}$ at the end of the pulse is set to the minimum actual capacitor voltage v_{drop} (= v_{C0}(0)) resulting in

$$v_{C0,ref}(t) = v_{drop} + \frac{\Delta v_{C0}}{t_{rep}}\cdot t = (V_{C0} - \Delta v_{C0}) + \frac{\Delta v_0}{t_{rep}}\cdot t \tag{6}$$
$$\text{for } t = 0...t_{rep}\,.$$

The waveform of the reference voltage $v_{C0,ref}$(t) to achieve a constant current i_{L0} and a unity power factor for pulse loads is shown in Fig. 6.

For case B, where the ripple voltage Δv_{C0} is large, the inductor current i_{L0}(t) is no longer constant. The power consumption of the converter with capacitive load can be written as

$$P(t) = v_{C0}(t)i_{L0}(t) = C_0 v_{C0}(t)\frac{dv_{C0}(t)}{dt} = const.\,, \tag{7}$$

which has to be constant.
Solving (7) leads to the capacitor voltage

$$v_{C0}(t) = \sqrt{\frac{{v_0}^2 - v_{C0}(0)^2}{t_{rep}}t + {v_0}^2} \tag{8}$$

which is the reference voltage for large voltage ripples. Based on the capacitor voltage the current in the inductor is given by

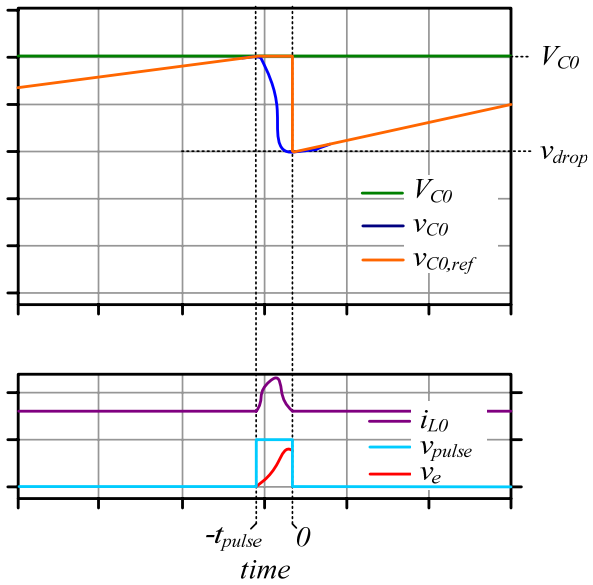

Fig. 10. Spike in the inductance current i_{L0} due to the constant reference voltage $v_{C0,ref}$ during the pulse. Disabling the control during the pulse prevents from a current spike.

$$i_{L0}(t) = P_{avg}\left(\sqrt{\frac{v_0^{\,2} - v_{C0}(0)^2}{t_{rep}}t + v_0^{\,2}}\right)^{-1}. \qquad (9)$$

B. Beginning of pulse sequence and load steps

The reference voltage in (6) is derived for steady state conditions with a constant load and pulse repetition rate. At the beginning of a pulse sequence, the storage capacitor C_0 is charged up to V_{C0} and the buck-boost converter transfers no power to the modulator. After the first pulse is detected, the controller of the buck boost converter resets the reference voltage $v_{C0,ref}$ to v_{drop} and ramps $v_{C0,ref}$ linearly up to V_{C0} to recharge the capacitor C_0 with a constant current i_{L0}. There, the pulse repetition rate t_{rep} must be given by the control of the modulator.

Since the current i_{L0} in the buck-boost inductor starts from zero and has a limited slew rate, the current i_{L0} is too small so that the capacitor voltage $v_{C0}(t)$ can not follow the reference value and it does not reach its nominal value V_{C0} until the second pulse (cf. Fig. 8). Therefore, the error voltage $v_e(t)$ is increasing over time and the capacitor voltage $v_{C0}(t)$ is below the nominal value V_{C0} at the beginning of the second pulse.

After the second pulse, the voltage reference $v_{C0,ref}$ would be reset again to the actual capacitor voltage $v_{C0}(2t_{rep})$ as described for steady state operation. This reset of $v_{C0,ref}$ also would lead to a reset of the voltage error $v_e(2t_{rep}) = 0$ and therefore to a sawtooth shaped waveform of $v_e(t)$ (cf. Fig. 8). Because of the cascaded and highly dynamic control (cf. Fig. 4) the voltage error v_e would lead to a reference current i_{ref}, which has a similar shape as the error voltage v_e. Consequently, the waveform of the current i_{L0} in the buck-boost inductor L_0 also would be sawtooth-like and the mains currents would be distorted at the beginning of a pulse sequence.

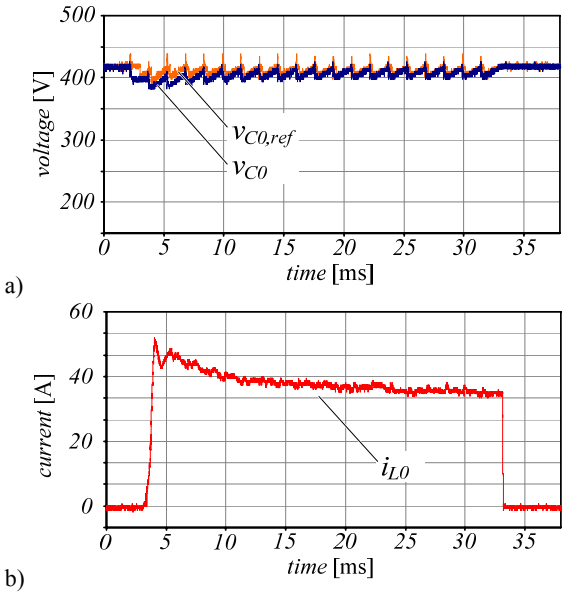

Fig. 11. (a) Reference voltage $v_{C0,ref}$ and capacitor voltage v_{C0} for a pulse sequence with 20 pulses and 10kW average power. (b) Corresponding inductance current i_{L0}.

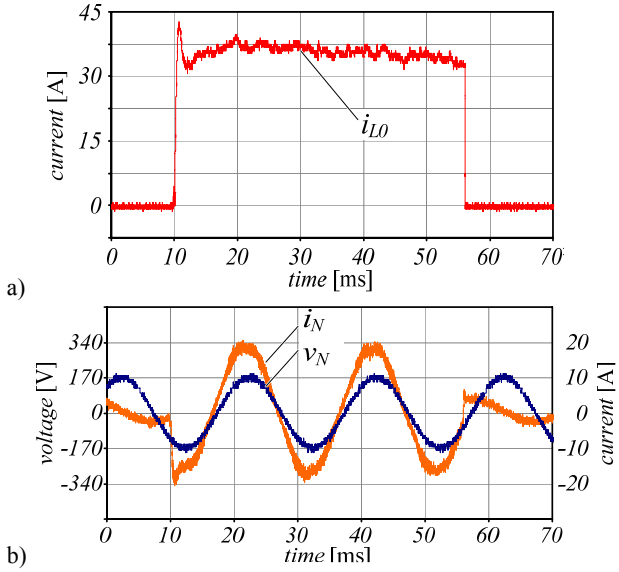

Fig. 12. (a) Measured inductance current i_{L0} and (b) corresponding mains current i_N and voltage v_N of one phase.

In order to avoid the discontinuities of the error voltage v_e and the current i_{L0}, the initial value of the reference voltage $v_{C0,ref}$ after the pulse has to be reset in such a way, that the error voltage v_e is continuous. Therefore, the error voltage v_e before and after the pulse must be equal.

$$v_e(n \cdot t_{rep}) = v_e(n \cdot t_{rep} + t_{pulse}) \qquad (7)$$

This can be achieved by adding the last error voltage v_e (cf. Fig. 10) before the pulse to the voltage v_{drop}. Therefore,

$$v_{0,ref}(n \cdot t_{rep}) = v_{drop} + v_e(n \cdot t_{rep} - t_{pulse}) \qquad (8)$$

Additionally, the slew rate of the voltage reference $v_{C0,ref}$ must be adjusted because of the shifted initial voltage $v_{C0,ref}(0)$. Therefore, (6) is modified to

$$v_{0,ref}(t) = \left(v_{drop} + v_e(nt_{rep} - t_{pulse})\right) + \frac{(\Delta v_0 - v_e(nt_{rep} - t_{pulse}))}{t_{rep}}t \qquad (9)$$

which results in a continuous waveform of v_e and i_{L0} (cf. Fig. 9). The described procedure also leads to a continuous error signal v_e and inductor current after a load step.

C. Disabling the control during the pulse

For correct calculation of the reference voltage $v_{C0,ref}$ the converter is synchronized with the trigger signal of the modulator. Additionally, the minimum capacitor voltage v_{drop} has to be detected after receiving the synchronisation signal. Consequently, the reference voltage $v_{C0,ref}$ can not be updated during the pulse until the minimum capacitor voltage v_{drop} has been detected and is therefore fixed at V_{C0} during the pulse as shown in Fig. 10.

Moreover, the voltage error v_e increases rapidly during the

pulse and the cascaded control would increase the inductor current i_{L0}. In order to prevent the controller from increasing the current i_{L0} during the pulse, the voltage controller is disabled, i. e. the current reference $i_{L0,ref}$ and therefore also the current i_{L0} is kept constant, until the voltage reference $v_{C0,ref}$ is updated again.

IV. Measurement results

In Fig. 11(a) the reference voltage $v_{C0,ref}$ and the capacitor voltage v_{C0} for a sequence of 20 pulses with a pulse repetition frequency of 720Hz and an average output power of 10kW are shown. At the beginning of the pulse sequence a voltage error, due to the start-up behavior as described before, can be noticed. The corresponding inductance current i_{L0} is depicted in Fig. 11(b). As can be recognized, the current i_{L0} converges to a constant value as soon as the voltage reaches the value V_0.

In Fig. 12(a) the inductor current i_{L0} for the same pulse sequence with a pulse repetition frequency of 440Hz and an average output power of 8kW is shown. The corresponding sinusoidal mains current i_N and voltage v_N of one phase are depicted in Fig. 12(b). The measured phase shift is caused by the input filter capacitors and is reduced when the converter operates at the nominal output power of 25kW.

V. Summary

In this paper a control scheme for AC-DC converters with pulsating loads, such as pulse modulators, is explained in detail. This method modulates the reference signal such that continuous power flows from the mains and sinusoidal mains currents are drawn even though the load power consumption is discontinuous. To validate the theoretical concepts, the control, which is basically independent of the converter topology, has been successfully implemented with a three-phase buck-boost converter and measurement results are presented in the paper.

The concept has been derived for pulse modulators with relatively small variations of the DC link voltage. In case of large variations modified reference values, as presented in the paper, for the capacitor voltage must be applied in order to obtain constant power consumption.

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Dominik Bortis (S’06) studied electrical engineering at the Swiss Federal Institute of Technology (ETH) Zurich. During his studies he majored in communication technology and automatic control engineering. After the internship at ABB, where he designed an AC/DC-Power supply for Synchronizing Systems he did his diploma thesis in cooperation with the company Levitronix, where he designed and realized a galvanic isolation system for analog signals. He received the M.Sc. degree in 2005, and he has been a Ph.D. student at the Power Electronic Systems Laboratory, ETH Zürich, since then. His research is currently focused on the design of pulsed power systems.

Stefan Waffler studied electrical engineering at the Friedrich-Alexander University in Erlangen, Germany. During his studies he dealt in particular with simulation and realization of a three-phase AC/DC converter with power factor correction. After he had received his diploma degree in December 2006 he started working as a Ph.D. student at the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich with focus on highly-compact, bi-directional multi-phase DC/DC converters.

Juergen Biela (S’04) studied electrical engineering at the FAU Erlangen, Germany. During his studies he dealt in particular with resonant DC-link inverters at the Strathclyde University, Scotland and the active control of series connected IGCTs at the Technical University Munich, Germany. After he had received his diploma degree with honours from FAU Erlangen in October 2000, he worked on inverters with very high switching frequencies, SiC components and EMC at the research department of A&D Siemens, Germany. From July 2002 he has been a Ph.D. student at the PES, ETH Zurich. After he finished his Ph.D. in December 2005 he is now working as PostDoc at the PES, ETH Zurich. His current research is focused on design, modeling and optimization on PFC/DC-DC converters with emphasis on passive components and the design of pulsed power systems.

Johann W. Kolar (M’89 SM’02) studied industrial electronics at the University of Technology Vienna, Austria, where he also received the Ph.D. degree (summa cum laude). From 1984 to 2001 he was with the University of Technology in Vienna, where he was teaching and working in research in close collaboration with industry in the fields of high performance drives, high frequency inverter systems for process technology and uninterruptible power supplies. Dr. Kolar has published over 150 scientific papers in international journals and conference proceedings and has filed more than 50 patents. He was appointed Professor and Head of the Power Electronics Systems Laboratory at the Swiss Federal Institute of Technology (ETH) Zurich in 2001.

The focus of his current research is on novel ac-ac and ac-dc converter topologies with low effects on the mains for telecommunication systems, More-Electric-Aircraft applications and distributed power systems utilizing fuel cells. A further main area of research is the realization of ultra-compact intelligent converter modules employing latest power semiconductor technology (SiC) and novel concepts for cooling and EMI filtering. Dr. Kolar is a member of the IEEJ and of Technical Program Committees of numerous international conferences (e.g. Director of the Power Quality branch of the International Conference on Power Conversion and Intelligent Motion). From 1997 through 2000 he served as an Associate Editor of the IEEE Transactions on Industrial Electronics and since 2001 as an Associate Editor of the IEEE Transactions on Power Electronics.