

# Optimization of the Current Distribution in Press-Pack High Power IGBT Modules

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**Abstract**—Today’s IGBT modules achieve high current ratings by paralleling several semiconductor switches. For high power and high voltage applications, the press-pack IGBT design is a technology of increasing importance, since it is designed for a low inductance series connection in a module stack. This work examines the module-internal current distribution in a press-pack configuration during switching transients by means of the PEEC simulation method. Parasitic effects which result in current unbalances between the paralleled switches are determined and quantified, where special emphasis is put on the power module external interconnection wiring and its influence on the current distribution and power loss in the distinct switches. A hardware test setup is discussed in detail, and a layout design optimization is which balances the loss distribution among the switches.

**Index Terms**—IGBT Press-pack IGBT current unbalance, Partial Element Equivalent Circuit (PEEC) method, loss modeling.

## I. INTRODUCTION

For high power converters, such as in industrial motor drives, traction applications or pulsed power systems, the insulated gate bipolar transistor (IGBT) has become the most attractive device due to its high current and high voltage ratings, low power control and high switching speed. In order to obtain a high current handling capability, IGBT power modules usually contain several paralleled IGBT chips in combination with anti-parallel diodes. For parallel switch arrangements, a positive temperature coefficient is necessary to prevent thermal runaway, which is typically the case for non-punch-through IGBT structures [1]. As the required converter voltages often exceed the maximum blocking voltage of a single IGBT, a series connection of several semiconductor devices is applied. Thus, the application of the press-pack IGBT module is very attractive for high voltage direct current (HVDC) [2] and multi-level inverters [3]. The press-pack IGBT module is designed for a low inductance series connection in a module stack, where additional requirements such as a uniform mechanical pressure distribution or a proper handling of fault conditions are essential [4, 5]. Additionally, the pressure contacted switches exhibit advantageous thermo-mechanical properties [6, 7], which lead to an increased module lifetime in comparison to bonded IGBT modules, where thermal load cycles are causing bond wire lift-off.

In these high voltage IGBTs, switching losses are dominant in comparison to conduction losses. This work focuses on the evaluation of the internal IGBT module current distribution during switching events. Electro-

magnetic parasitic effects can lead to non-equal current loading of paralleled switches, and such current unbalances lead to unequal thermal losses within a power module. The optimum silicon utilization can only be achieved when losses are distributed equally, otherwise hot-spots can degrade the module performance, reliability and lifetime.

Since a direct measurement of the internal module current distribution is quite cumbersome, a simulation approach is applied to gain insight into the electromagnetic effects that determine current unbalances. In this work, the software tool “GeckoEMC”, which is based on the partial element equivalent circuit (PEEC) method, is used to simulate the electromagnetic layout properties of a 4.5 kV press-pack IGBT power module together with its external interconnection wiring. As the rate of change of the current at switching events is typically in the order of 1...10 kA/μs, current displacements due to skin- and proximity effect have to be considered in a simulation. Additionally, stray inductances and couplings between power and gate circuits in the internal module interconnection paths can lead to switching delays that affect the current balancing.

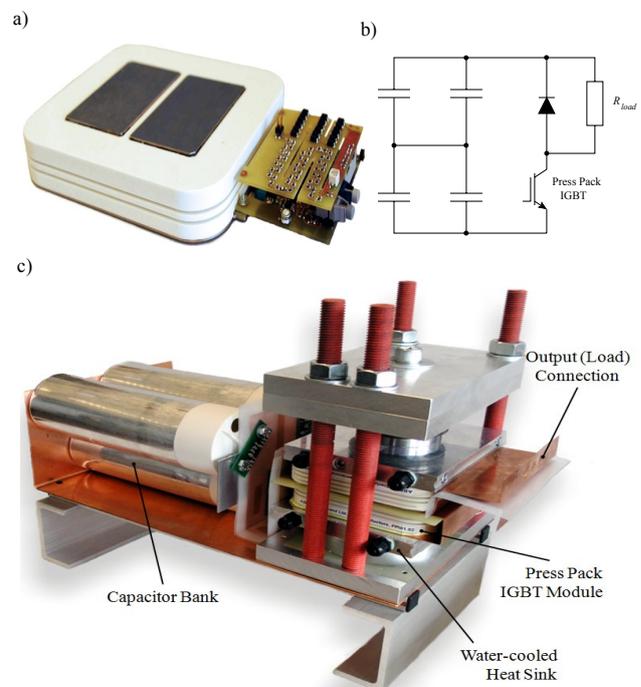


Fig. 1. Test bench configuration: a) press-pack IGBT power module with attached gate drive unit, b) circuit diagram, c) photograph of the realized press-pack IGBT test bench.

Two different parasitic layout properties will be considered in this work: Commutation path inductances in combination with mutual couplings (section III B) and induced voltages in the distinct switch gates (section III C) due to current transients in the commutation path, which lead to switching delays between the paralleled IGBTs. Using the parasitics obtained by PEEC simulations, the current and loss distributions will be determined in a SPICE-like simulation which includes a detailed switch model (section IV). Finally, a layout design improvement for the investigated test setup in Fig. 1 will be given in section V, which improves the current and loss distribution.

## II. ELECTROMAGNETIC INTERCONNECTION LAYOUT MODELING AND THE PEEC SIMULATION METHOD

For a proper selection of an electromagnetic solver that is well suited for simulating the power module layout internals as well as the external press-pack interconnection wiring, the following aspects have to be considered: The solver should be able to cover both frequency and time domain solutions, since a simulation of the switching event should be performed in time-domain, whereas the evaluation of parasitic impedances is easily obtained from a frequency-domain solution. Further, an inclusion of lumped circuit elements into the model is required, as the excitation source and the capacitors together with their series equivalent inductance have to be modeled.

It has been stated in several publications [8, 9, 10] that a finite element method (FEM) based software is not very well suited for such kind of simulation, because the large aspect ratio between width and height of flat conducting structures leads to an excessive mesh refinement in FEM solvers, and thus to long simulation times and convergence problems. Therefore, the simulation models in this work are realized with the electromagnetic solver “GeckoEMC” [11], which is based on the partial element equivalent circuit method (PEEC) [12]. The PEEC method fulfils all the previously mentioned requirements and therefore enables an easy modeling of the current distribution of the press-pack power module, together with its external interconnection structure.

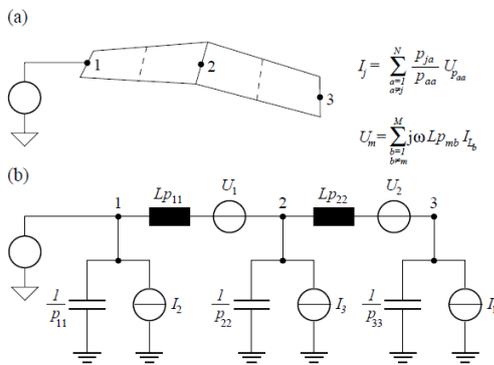


Fig. 2. PEEC simulation model: Conducting structures (a) are discretized into lumped circuit elements (b), namely resistors, (mutual) inductances and cell-to-cell capacitances. Here, the mutual couplings are represented by controlled current and voltage sources.

Furthermore, the PEEC approach itself is leading to a simplified circuit modeling approach, as detailed in section III. Figure 2 illustrates the basic PEEC modeling approach: Conducting structures are discretized into lumped circuit components, namely resistors, inductors, mutual inductances and capacitances, whose values are determined solely by material properties and geometric considerations. In fact, the whole 3D layout geometry is mapped into a large circuit, and therefore any additional circuit component like excitation sources, capacitances, etc. can be added easily to the model.

## III. EQUIVALENT CIRCUIT MODELING OF THE PRESS- PACK POWER MODULE

In the following paragraphs, the modeling of the layout parasitic inductances in the IGBT test bench configuration is detailed. First, the layout of the current paths will be characterized in the geometry description. Then, the PEEC model of the commutation path together with a simplified circuit model is given. Finally, the modeling of the gate-emitter inductance common to power and gate drive path will be discussed.

### A. Geometry Description

The press-pack IGBT module is designed with a short and hence a very low inductance collector-emitter current path. Figure 3 shows an explosion drawing of the power module internals. When the switch is in on-state, the current enters the collector plate (bottom), propagates through the semiconductors into the press-pack spring connectors and leaves the module through the emitter plate (top). Figure 4 shows the positions of the 12 individual switches inside the module, each labeled with a number; this numbering will be used consistently throughout this work. The anti-parallel freewheeling diodes will not be considered for modeling, since they are not used the test setup.

The gate connection trace consists of a PCB-like structure in close proximity to the emitter plate to keep the common emitter-gate inductance as low as possible. In the studied test setup, the gate-driver is then attached directly to the power module gate connection output and the emitter plate (cf. Fig. 1), so that the gate driver is not adding further parasitic inductances. Modeling the gate wiring will be detailed later on.

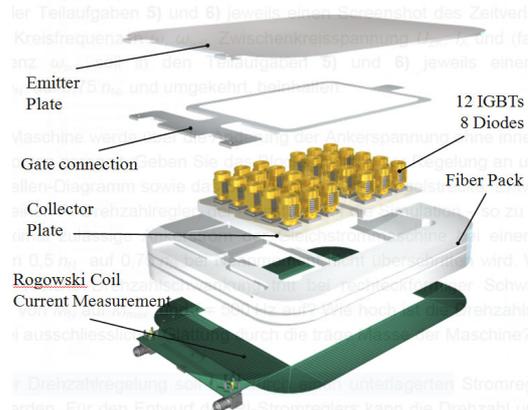


Fig. 3. CAD explosion drawing of the stack pack IGBT power module.

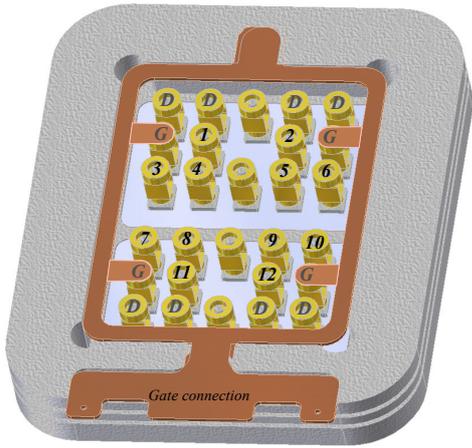


Fig. 4. Positioning of the 12 IGBTs spring connectors (named 1-12), the 6 anti-parallel free-wheeling diodes *D* and 4 gate-connectors *G*.

In HVDC applications or in multilevel converters, the high blocking voltage capability of the switching devices is achieved by a series connection of several semiconductor. The press pack IGBT was originally designed for these applications, where an easy series connection is achieved through a stacked construction [4], see Fig. 5a). However, as the studied setup is intended for a pulsed power application, fast rising edges in the current pulses applied to the load are one of the main targets. To achieve this sharp pulses, the interconnections from the capacitor banks through the switches and finally to the load must be carefully designed.

In Fig. 5a), a typical interconnection which considers a stacked construction with a water-cooled heat-sink between the modules is shown together with the current path during conduction of the IGBT. An alternative construction is presented in Fig. 5b), where the IGBT module is flipped, leaving the heat-sink on the lowest face of the stack. It should be noted that, as the silicon chips are placed on the collector plate, the heat-sink must be attached to the collector surface in order to efficiently extract the heat generated by the chips. Additionally, for safety reasons, the heat sinks in this case must be isolated from the switches.

The inductance of the commutation path is directly related the size of the dashed area  $A_c$  in Figs. 5a) and 5b). As can be seen, this area is larger in the case of the stacked setup (cf. Fig a), leading to larger inductances and consequently longer rising times in the current pulses. Moreover, the heat-sink between the modules would be subject to high magnetic fields, leading to induced eddy currents and additional losses in the system. For these reasons, a construction as displayed in Fig. 5b) was chosen for the studied setup.

*B. Commutation Path Layout Simulation*

Figure 6 shows the 3D PEEC model of the test setup within the electromagnetic solver “GeckoEMC” [11]. The interconnection copper sheets are modeled as well as the 12 IGBT spring connectors. Here, the rather complicated

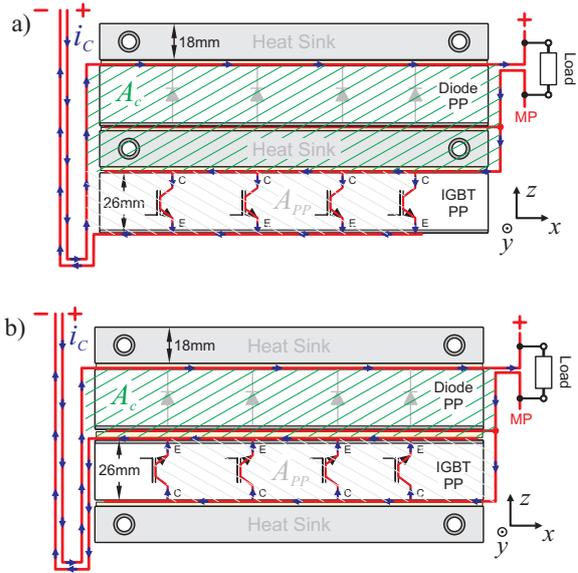


Fig. 5. Two possible configurations for the press pack IGBT test bench.

layout of the spring connectors is represented as a cylindrical PEEC cells for simplification. The shown PEEC model is considering all electromagnetic parasitic layout effects, in particular the current distribution and current sharing between the 12 IGBTs. However, the PEEC model does not contain a detailed semiconductor switch model. Hence for a first analysis, the IGBT was assumed as an ideal switch which is initially in on-state, i.e. conducting, and a total turn-on current ramp was enforced by an excitation current source having a rise-time of 100 ns and amplitude of 1000 A, cf. Fig. 7.

The simulation result shows a strong current load asymmetry: IGBTs 2, 6, 10, and 12 are carrying the main current load during turn-on, whereas the other switches draw a smaller current. Due to symmetry reasons, the results for switch turn-off would look similar. At steady state, the currents in Fig. 7 equilibrate due to the DC characteristics of the switches. Since the utilized model only takes parasitic layout properties into account, the origin of the asymmetry is the module layout itself,

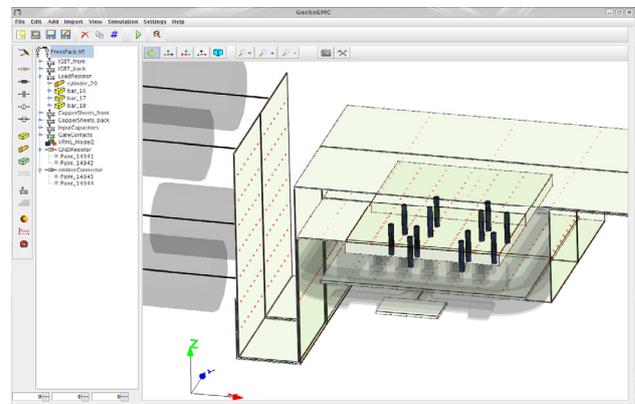


Fig. 6. Screenshot of the graphical user interface of the electromagnetic solver GeckoEMC. The shown three-dimensional test bench model contains the power module internals, the interconnection copper sheets and the input capacitors.

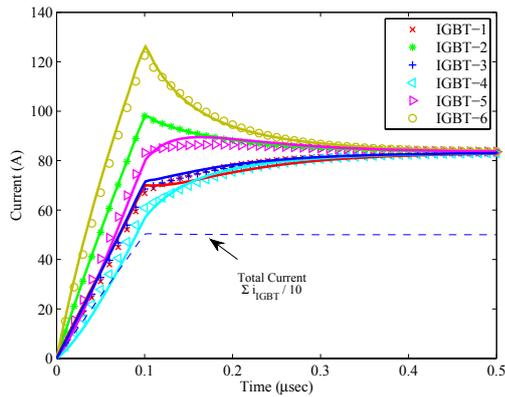


Fig. 7. Current sharing between IGBT switches arising from magnetic current displacement/attraction of the interconnection layout. The solid lines show results from a PEEC simulation, whereas the markers depict the lumped component approximation from the circuit simulation.

in combination with the external interconnection wiring. Regarding the floor plan in Fig. 8, the current sharing asymmetry can be explained by means of skin- and proximity-effect:

Considering high frequency AC currents in a conductor with a diameter larger than the skin-depth, the current has the tendency to distribute itself near the surface of the conductor, which is due to a repelling behavior of current density vectors that point into the same direction. On the other hand, currents flowing anti-parallel behave attractive to each other (proximity effect). This is exactly the same effect as observed in the simulation of the power module test setup. In Fig. 8, the dashed circle indicates two different types of IGBT positions outside and inside the circle, respectively. For a fast switching transient, currents will tend to flow through the outer IGBTs. The floor plan also shows the copper sheet interconnections outside the power module (cf. Fig. 1), which connects the module to the input capacitor bank (left sheets) and the load (right sheet). As the magnetic field of the load connector on the right-hand side is not compensated by a corresponding backward current path with opposite current direction, a further asymmetry in  $x$ -direction is introduced: Due to

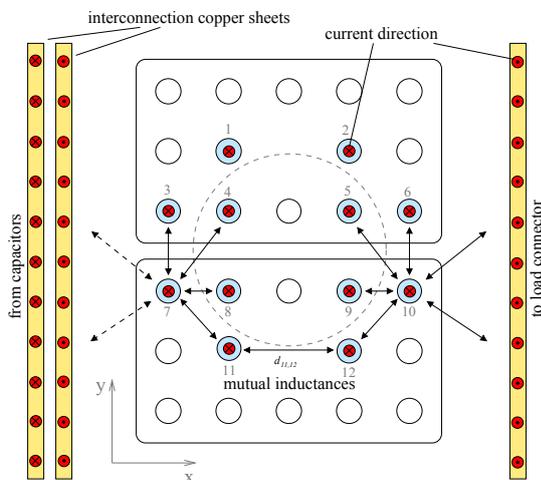


Fig. 8. Top view floor plan of the IGBT module and interconnection copper sheets. The current directions are indicated by red markers.

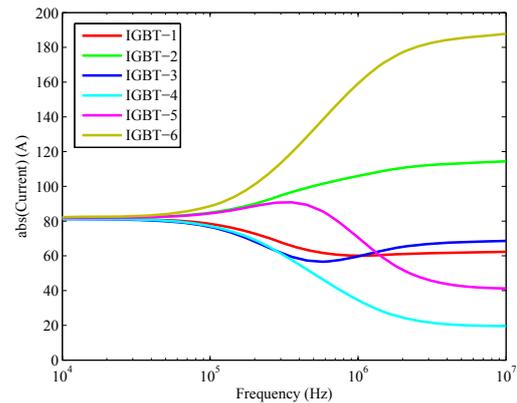


Fig. 9. Frequency-domain solution of current distribution.

proximity effect, the current paths closest to the load connector, namely through IGBTs 2, 6, 10 and 12, show the highest current density values.

For verification of this consideration and the time domain analysis, a corresponding frequency domain simulation was performed in GeckoEMC, see Fig. 9. The frequency domain solution shows similar behavior, where at higher frequencies skin- and proximity effects dominate the current distribution.

#### C. Power Path Equivalent Circuit Modeling

Since the full PEEC model contains thousands of inductances together with their mutual couplings, a simplified equivalent circuit model is required, which can then be used in a SPICE-like circuit simulator. The simplified modeling approach, shown in Fig. 10a), is based on a quasi-geometric representation of the module layout, similar to the PEEC approach itself, but with a reduced number of inductances and couplings. Here, the mutual inductances between the IGBT sprint connectors inside the module are calculated via the analytic equation [13]

$$M_{ij} = 0.2 \cdot l \left( \ln \left( \frac{l}{d_{ij}} + \sqrt{1 + \frac{l^2}{d_{ij}^2}} \right) - \sqrt{1 + \frac{d_{ij}^2}{l^2}} + \frac{d_{ij}}{l} \right), \quad (1)$$

where  $l$  is the connector length,  $r$  the connector radius and  $d_{ij}$  the distance between connector  $i$  and  $j$ . The mutual inductance between the external copper sheets and the IGBT connectors was then selected by fitting the PEEC simulation to the simplified circuit model, a comparison between both is shown in Fig. 7, where the simplified model results are indicated by markers.

#### D. Common Gate-Emitter Inductance Modeling

A common gate-emitter inductance is leading to a switching delay and a limitation of switching speed, since the commutation current  $di/dt$  reduces the applied gate-emitter voltage of every switch by  $\Delta u_g = L_e di/dt$ , see Fig. 10b). To overcome this problem, conventional IGBT packages utilize auxiliary emitter connectors, to reduce the common emitter inductance in the gate driver current path. However, the examined press-pack power module exhibits a common emitter connector. Hence, to simulate the IGBT current sharing in a correct manner, a detailed

modeling of the gate-emitter current path is required. Especially asymmetric magnetic couplings between gate connections to the power path of separate IGBTs are of interest, because those asymmetric couplings lead to different gate voltages of the paralleled IGBTs and hence to unbalanced current sharing between the distinct switches.

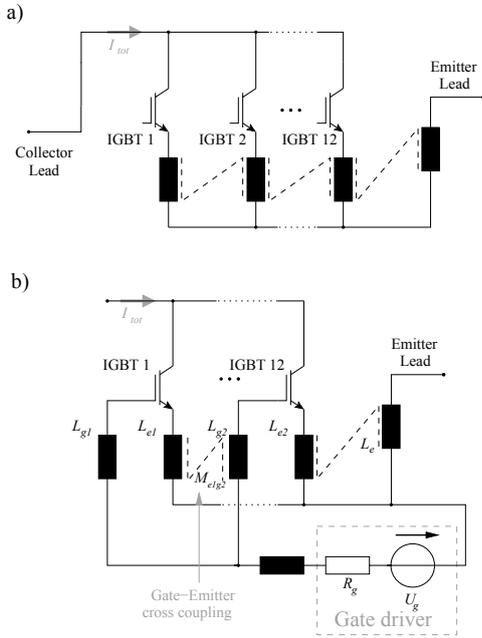


Fig. 10. a) Simplified circuit model of IGBT power current path: 3 of the 12 IGBTs are shown together with their emitter lead inductances. Due to parasitic effects, every inductor is connected via mutual couplings to all other inductors. b) The common emitter inductance is leading to a switching delay, and parasitic couplings between different switches are leading to module current unbalances. For a simplified illustration, the figure only shows magnetic couplings to direct neighbors, whereas the implemented circuit model contains a full coupling matrix.

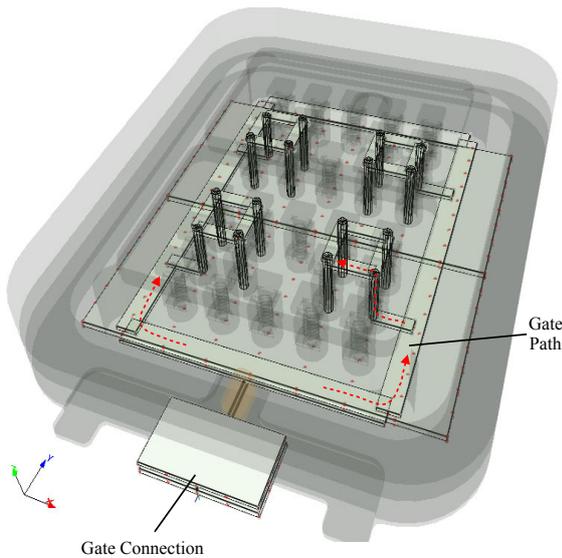


Fig. 11. PEEC model of the power module gate interconnection. The gate driver is attached at the front connectors, where the gate current path shares a common emitter inductance with the power current path, potentially leading to an asymmetric current sharing.

Figure 11 shows the gate interconnections of the press-pack IGBT module in a screenshot from the PEEC solver graphical user interface. For a first analysis, an ideal current sharing between the switches is assumed, which means that all switches carry the same current load over time. The induced gate voltage at each IGBT during the switching event was simulated with the simulation tool GeckoEMC [11]. The time domain simulation results are given in Fig. 12. There, the induced gate voltages at each of the 12 IGBTs is shown during the application of a total current pulse with a rise-time of 0.5  $\mu$ sec and 1000 A. The actual gate voltage at the single switches calculates then as the sum of gate driver input voltage and the shown induced gate voltage. Please note that the result in Fig. 10 was obtained by enforcing the same current in all IGBTs by means of a current source at each switch position. Later on in a circuit simulation, an impedance matrix that is extracted from the PEEC model will take into account the non-equal current distributions in a correct way.

The simulation of the turn-on behavior reveals that the voltage at the gates of IGBTs 6 and 10 will be highest, followed by the gate voltages of IGBTs 2 and 12. Hence, the mentioned IGBTs will also exhibit the most turn-on power, as detailed later in the SPICE-like circuit simulation in section IV. The results in Fig. 12 can be regarded as characteristic of the power module gate interconnection layout. It is noteworthy that not the gate voltage drop itself results in an asymmetric current distribution, but the difference between the voltage drops among the paralleled switches. Therefore, an ideal optimized layout should result in a figure that shows the same induced gate voltage for all 12 IGBTs.

In order to include the PEEC simulation results in a circuit simulation, the gate connector inductances have to be extracted together with common gate-emitter parasitic inductances from the 3D layout simulation, which results in an inductance coupling matrix, as denoted in Fig. 10b). Finally, in the circuit simulation in the following section, the total current will not be equally distributed among the switches, the extracted impedance matrix will take into account the unbalance of the distinct switch currents.

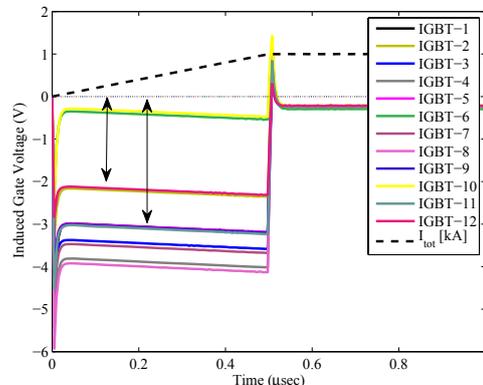


Fig. 12. Induced gate voltages during switch turn-on. The gate voltage offset (indicated by arrows) is leading to a slower switching behavior and hence to an unbalanced current during the switching transients. The dashed curve shows the applied current pulse of 1000 A amplitude.

#### IV. CIRCUIT SIMULATION RESULTS

##### A. Circuit Simulation with Detailed IGBT Switch Model and Parasitic Inductances

The parasitic magnetic effects, as discussed above, are now included in a SPICE-like circuit model by means of an impedance matrix. Additionally, a detailed IGBT model is included in the circuit model that takes into account the switch characteristics, semiconductor capacitances and the tail current. Figure 13 shows the total switching behavior of the IGBT module. The circuit parameters of 3000 A total current and the switching voltage of 3000 V will be retained for the subsequent analysis. Please note that the simulation results are obtained by 12 paralleled IGBT models, including simplified magnetic couplings from the PEEC simulation.

In the following, the current- and power distribution among the single IGBT switches will be evaluated in detail. Figure 14 shows the simulated current sharing within the single IGBTs. The steady-state current is balanced, since the switch model is identical for all 12 IGBTs in the circuit simulation. Possible deviations from a balanced steady state current could be caused by device variations within the power module, which is not in the scope of this work, since switching losses dominate the conduction losses of high power IGBTs.

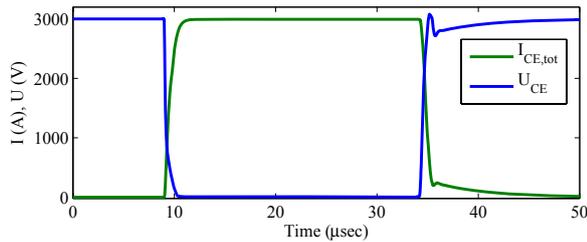


Fig. 13. Simulated switching voltage and total switching current (resistive load), i.e. the sum of the 12 IGBT currents in the power module.

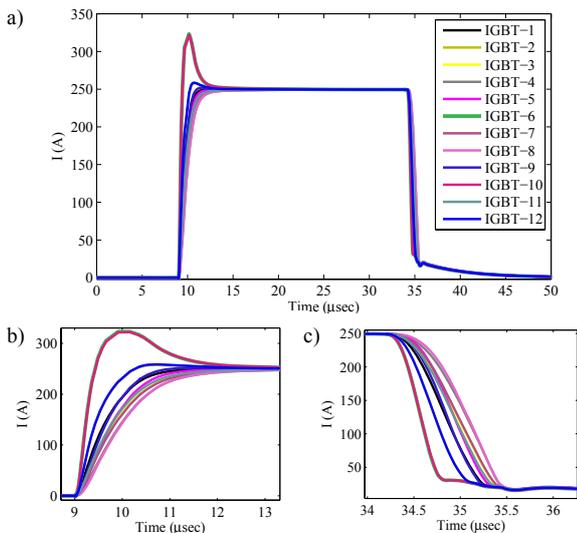


Fig. 14. a) Simulated current distribution in the press-pack power module for an ohmic load. A magnified view of turn-on and turn-off current distribution is shown in b) and c), respectively.

Figure 14 shows that the turn-on currents are strongly unbalanced, where IGBTs 6 and 10 carry the main current load with an overshoot. As a result, those IGBTs suffer from increased thermal losses during turn-on. Likewise, the turn-off behavior shows a delay in the current distribution, whereas the current load in IGBTs 6 and 10 are turning off first.

##### B. Loss Energy Analysis

It is apparent that the simulated current unbalance has its origin in the parasitic couplings as detailed in section III, as these couplings are the only source of asymmetric parameters among the 12 IGBT current paths in the circuit simulation. Both parasitic effects as described earlier, namely the commutation path inductances and couplings from the emitter path to the IGBT gate wiring, contribute to the unequal power distribution. The calculated turn-on and turn-off power of the current distribution from Fig. 14 is shown in Fig. 15, and Fig. 16 illustrates the corresponding energy distribution for a single switch event.

The turn-off energy loss distribution in Fig. 15 seems to be more balanced than the turn-on energy. This is due to the IGBT current tail during turn-off. As the current tail exhibits a time constant in the range of 5 µs, it contributes with a nearly constant loss energy of about 0.3 J per switching event at every IGBT. However, the turn-off power distribution in Fig. 15 shows strongly unbalanced maximum values during the switching transient.

Please note that the turn-off power distribution is inverted in comparison to the turn-on distribution, i.e. the switches having highest turn-on energy dissipate the lowest turn-off energy. This inversion is caused by the respective current delays as depicted in Figs. 14 b) and c). For instance, IGBTs 6 and 10 exhibit the least switching delay within the power module for turn-on as well as turn-off. Thus, taking into account the falling and rising collector-emitter voltage transients, respectively, to calculate the power loss, the mentioned inversion is justified.

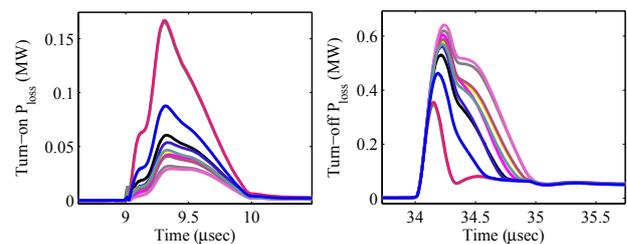


Fig. 15. Simulated turn-on and turn-off power dissipation of the IGBT switches in the press-pack module.

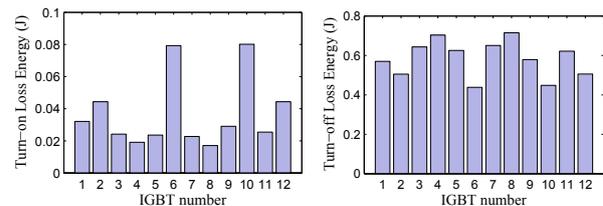


Fig. 16. Turn-on and turn-off loss energy per switching event. The values are calculated from the power dissipation as shown in Fig. 15.

V. TEST BENCH LAYOUT OPTIMIZATION

In the preceding analysis, the origin of unequal current sharing between the IGBTs of the test bench was determined as the interconnection layout and its parasitic couplings to the power module. Therefore, a redesign of the external press-pack interconnection wiring could lead to an improved switching current symmetry. Two different approaches for a change in the connection layout change were investigated by means of simulation within this work:

In the first approach, the copper sheet contact at the collector plate was modified with the intention to enforce a different current distribution in the collector plate (cf. Fig. 3), e.g. by introducing specially shaped gaps in the copper sheet connector. Hence, the induced gate voltages during switching transients will change due to the modified current path. Indeed, the corresponding PEEC simulation showed deviating results in comparison to the induced voltages of the conventional layout in Fig. 12. However, a significant improvement in the transient switch current sharing could not be found by this layout variation.

As second approach, an additional copper sheet connector was introduced in the test bench simulation, hence an alternative current path from the collector plate is able to balance the base plate current distribution, cf. Figs. 17 and 18. This approach is advantageous for the following reasons: First, the layout asymmetry and the subsequent proximity effect are reduced by this alternative configuration. Second, the distribution of the induced gate voltages as detailed in section III C is more compact and thus leading to less switching delay between the distinct IGBTs.

Taking into account the modified geometric configuration, the same methodology as described in the previous section was applied to obtain a circuit simulation model including the electromagnetic layout effects. Figure 19 shows a PEEC simulation of the induced gate voltages for the modified interconnection layout similar

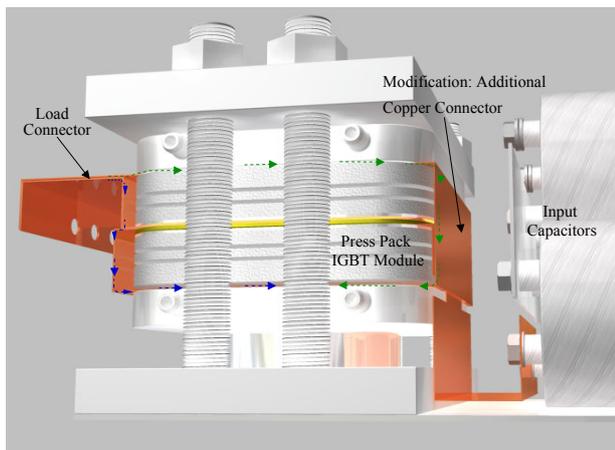


Fig. 17. CAD drawing of the test bench setup. An additional copper connector improves the IGBT current balance during switching. The green arrows indicate the newly introduced alternative current path to the load connector. For a better overview, the positive voltage connector is not depicted in the figure.

to Fig. 12. It is apparent that the induced gate voltages of most IGBTs are clustered around -2 V, and only few switches have larger deviations in their gate voltage. Finally, the simulation results in Figs. 20 and 21 show the improved distribution of switching power and energy loss for the modified interconnection layout.

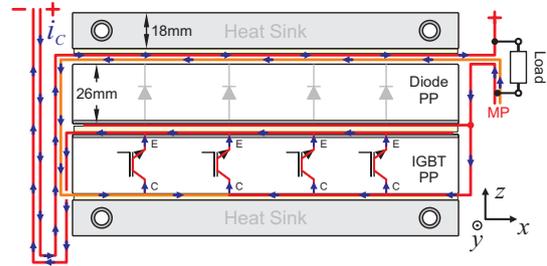


Fig. 19. Sheer plan of the modified test bench layout. In comparison to the original layout in Fig. 5, the modified layout improves the current unbalance during switching.

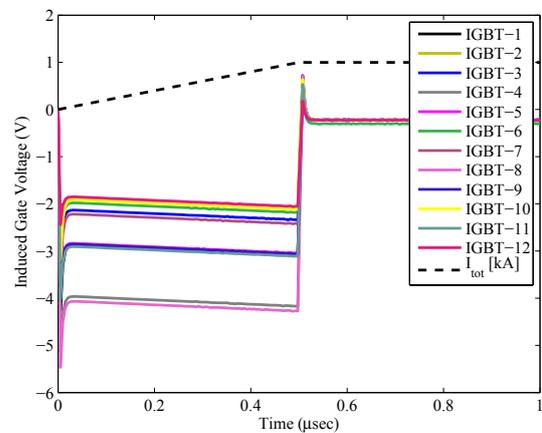


Fig. 19. Induced gate voltages for the modified interconnection layout as given in Fig. 16. In comparison to the results from Fig. 10, the induced gate voltages of most IGBTs are clustered around -2 V.

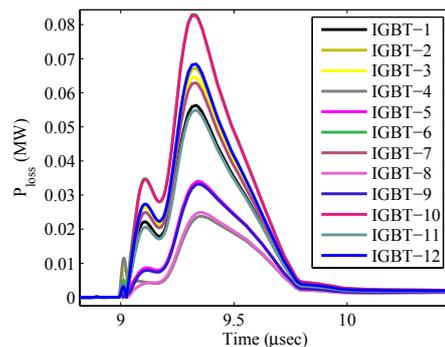


Fig. 20. Turn-on loss power distribution for the modified interconnection layout as given in Fig. 17.

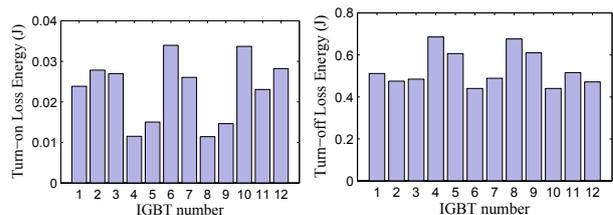


Fig. 21. Turn-on and turn-off loss energy per switching event for the modified interconnection layout as given in Fig. 17.

## VI. CONCLUSIONS

This work detailed parasitic layout effects that have influence on the current distribution between paralleled IGBTs within a high power press-pack module. The application of the PEEC simulation method allowed an easy extraction of parasitic inductances, which represent the magnetic coupling effects of the power module layout and its external interconnection wiring. In a subsequent circuit simulation including a detailed switch model and parasitic inductances, the current sharing between the module switches was calculated. The simulation results show a current load asymmetry during the switching event. Hence, the losses are distributed unequally in the power module, which could lead to thermal hot spots and a reduced power module lifetime.

Subsequently, a modification to the external interconnection wiring of the studied press-pack test bench was proposed, which improved the current sharing simulation results. Besides the internal skin effect as discussed in section III B, the press-pack module itself would nearly have inherent current load symmetry, though the external interconnection layout is leading to further current unbalances.

Since a direct measurement of the internal module current distribution is a time-consuming effort, this work was based on computer simulation results, to obtain a first insight into the dominating electromagnetic effects. As a significant influence of the interconnection wiring on the module current distribution was predicted, future work will focus on an experimental validation of the presented simulation results. This could be performed by measuring the different switch currents in the pressure-contact IGBTs by means of Rogowski coils [14]. In comparison to wire bonded modules, the press-pack module design is advantageous for this kind of measurement, because the currents in the pressure contacts are more easily accessible than currents in wire bonds.

In the future, increasing switching speeds as achieved by new switch technologies, e.g. applying silicon carbide semiconductors, will further worsen the problem of unequal power loss within paralleled switches due to parasitic electromagnetic effects. As concluded in this work, the IGBT module current sharing depends also on the external interconnection layout. Therefore, it may be useful for power module manufacturers not only to consider the module as an enclosed device, but additionally take into account the external interconnection wiring. This could ideally be performed in giving more detailed design guidelines in the datasheets on how to attach the device to its environment for achieving the optimal current sharing and switching performance.

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