

EMI Noise Prediction for Electronic Ballasts

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Abstract—The design of electromagnetic (EM) interference filters for converter systems is usually based on measurements with a prototype during the final stages of the design process. Predicting the conducted EM noise spectrum of a converter by simulation in an early stage has the potential to save time/cost and to investigate different noise reduction methods, which could, for example, influence the layout or the design of the control integrated circuit. Therefore, the main sources of conducted differential-mode (DM) and common-mode (CM) noise of electronic ballasts for fluorescent lamps are identified in this paper. For each source, the noise spectrum is calculated and a noise propagation model is presented. The influence of the line impedance stabilizing network (LISN) and the test receiver is also included. Based on the presented models, noise spectrums are calculated and validated by measurements.

Index Terms—Electromagnetic interference (EMI), electronic ballast, EMI prediction, EMI simulation, fluorescent lamp.

I. INTRODUCTION

ELECTRONIC ballasts for the fluorescent lamp have replaced electromagnetic ballasts in a large number of applications due to their numerous advantages such as an improved efficiency or flicker-free operation of the lamp. A typical circuit of a two-stage electronic ballast is shown in Fig. 1. The basic functions of the inverter stage are: 1) generation of the filament current and lamp voltage to ensure the ignition of the lamp and 2) operation of the lamp with a sinusoidal current typically at a frequency of 40–50 kHz because of electromagnetic interference (EMI) reasons. The inverter stage is often realized using a load-resonant half-bridge topology [1]. An active power factor correction (PFC) stage is required in order to meet the regulations for the input current harmonics and to realize a near-unity power factor. The PFC stage is realized with a boost converter operating at the border between discontinuous and continuous current conduction (so-called boundary conduction mode or critical conduction mode), which is the most popular control scheme for power levels required by the ballasts for the fluorescent lamps.

The high-frequency operation of the PFC stage and the inverter causes conducted noise on the input line and radiated electromagnetic noise in the environment of the ballast. In order to prevent interference with other systems, the custom-designed

EMI filters are required to meet the limits for conducted and radiated EM noise, which are regulated to international standards. In the European Union, the relevant standards for lighting systems are EN55015 for conducted and radiated EMI in the range 9 kHz to 30 MHz and EN55015 or EN55022 for radiated noise in the range 30 MHz to 1 GHz.

The conventional way to design an EMC input filter is to build a prototype of the system with an initial filter derived by approximate calculations or experience. The final filter design is found by the iterative EMC measurements and modification of the filter until the standards are met with minimal cost of the filter components. An alternative approach for designing an input filter is to simulate the conducted EM noise of the converter [2]–[10]. A simulation has the potential to avoid expensive and time-consuming redesigns of the hardware prototypes. Furthermore, the influence of the modulation, topological modifications, layout, dv/dt , etc., can be investigated before building hardware. Therefore, a simulation model for predicting the conducted EM noise spectrum of electronic ballasts for the fluorescent lamps is presented and validated in this paper. The model includes the PFC and inverter stages and is based on simple models of the waveforms in the ballast so that no additional circuit simulation software is required for the calculation of the spectrum.

The main challenge for EMI simulations is that the EM noise generation in a converter system is highly dependent on the circuit and semiconductor parasitics, which are difficult to model and which lead to complex simulations. Therefore, the most important part of this paper is to identify the main sources of differential-mode (DM) and common-mode (CM) noise and the corresponding propagation paths in electrical ballasts and to derive robust and computationally efficient models for the EMI behavior of the ballast.

The simulation approach presented in this paper is based on the calculation of the waveforms of each noise source in the time domain followed by a fast Fourier transform (FFT) to calculate the spectrum of the noise source. Then, a noise propagation transfer function is identified for each source in order to calculate the spectrum at the input of the EMC test receiver from the noise source spectrum. Therefore, in Section II, the modeling of the test receiver including the line impedance stabilizing network (LISN), the input cable, and the EMC test receiver is described. In Section III, the main noise sources for DM and CM noise in the PFC stage are identified and the noise propagation models are presented. The noise sources for the inverter stage are analyzed in Section IV. Section V describes the simulations and measurements done for the extraction of the parasitic capacitances. Finally, the implementation of the model and the comparison of the simulation results with measurements are presented in Section VI.

Manuscript received September 21, 2009; revised January 26, 2010. Date of current version July 16, 2010. Recommended for publication by Associate Editor M. Ponce-Silva.

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Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TPEL.2010.2046424

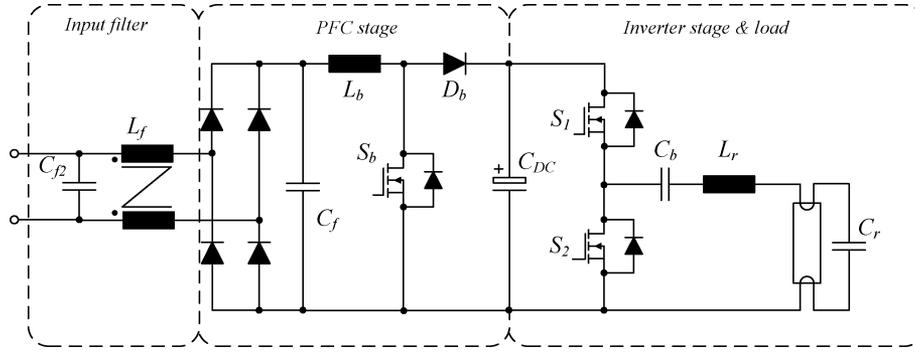


Fig. 1. Typical circuit of a two-stage electronic ballast.

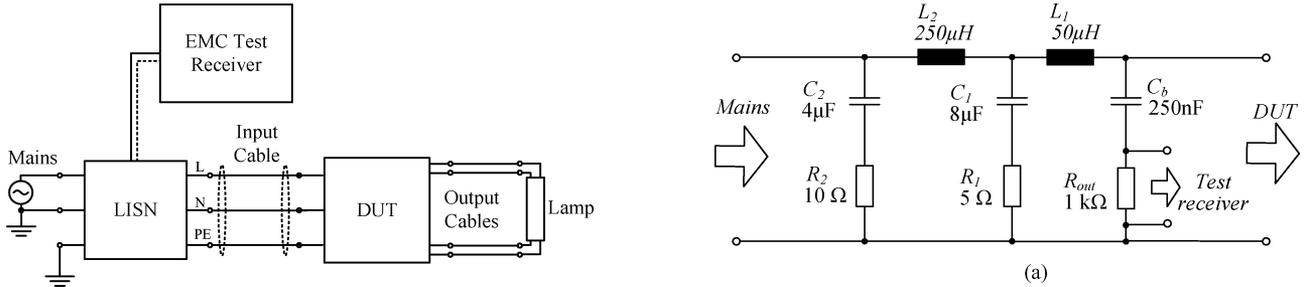


Fig. 2. Conducted noise emission measurement setup.

II. TEST SETUP MODELING

The setup for conducted EMI measurements consists of an LISN, the input cable, and an EMC test receiver (see Fig. 2). The LISN presents a defined impedance between the mains and the device under test (DUT) in order to guarantee the reproducibility of the measurements. Additionally, it provides an interface between the DUT and the test receiver. The EMC test receiver is a specialized spectrum analyzer implementing the measurement procedures specified in the EMC standards (e.g., CISPR-16).

A. Model of the LISN

The circuit diagram of a single-phase LISN according to CISPR-16 is shown in Fig. 3(a). For frequencies above 9 kHz, the influence of the filter stage comprising L_2 , C_2 , and R_2 on the impedance of the LISN can be neglected. Therefore, the simplified model shown in Fig. 3(b) is used for the presented simulations. The voltage V_{rec} is the noise voltage at the input of the test receiver, which has an input resistance R_{in} of 50 Ω .

B. Model of the Test Receiver

Fig. 4 shows a simplified block diagram of a test receiver based on the superheterodyne principle. The input voltage is buffered and attenuated in the first stage and applied to a mixer, which multiplies the attenuated signal with the output of a tunable local oscillator. The output of the mixer is the input signal shifted by the output frequency of the local oscillator, allowing to select the part of the input spectrum, which is mapped to the center frequency of the intermediate frequency (IF) filter by tuning the frequency of the oscillator.

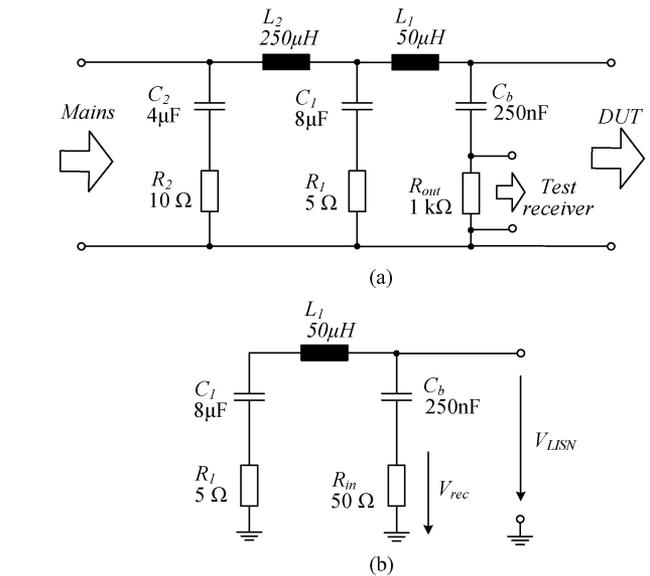


Fig. 3. (a) Schematic of an LISN according to CISPR-16. (b) Simplified model applied in the simulation.

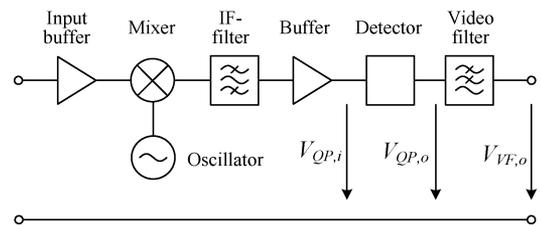


Fig. 4. Simplified block diagram of an EMC test receiver.

In CISPR-16, different IF filters are defined depending on the frequency range of interest. In Band A (9–150 kHz), the 6 dB bandwidth is 200 Hz, and in Band B (150 kHz–30 MHz), it is 9 kHz (see Table I).

Several detector types are used for EMC measurements: quasi-peak (QP), peak, average, and rms. The final stage of the test receiver is a mechanical time constant defined in the standard for moving coil meters, which is equivalent to a critically damped second-order low-pass filter.

In the simulation model, the bandpass filtering is done in the frequency domain, where the operation of the mixer and IF filter

TABLE I
FILTER BANDWIDTH AND TIME CONSTANTS ACCORDING TO CISPR-16

	Band A	Band B
IF-filter bandwidth	200 Hz	9 kHz
QP charging time constant	45 ms	1 ms
QP discharging time constant	500 ms	160 ms
Mechanical time constant	160 ms	160 ms

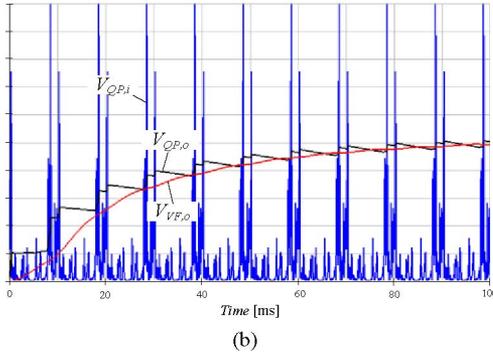
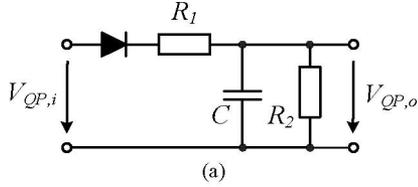


Fig. 5. (a) Quasi-peak detector circuit. (b) Simulation of the voltages at the input of the detector $V_{QP,i}$, at the output $V_{QP,o}$, and after the video filter $V_{VF,o}$.

is equivalent to the multiplication of the input spectrum with the earlier calculated frequency response of the filter shifted to the frequency under consideration.

For an accurate simulation of the detectors, the time-domain voltage waveform at the input of the detector has to be calculated for one mains half-period. For a certain frequency f under consideration, this is done by multiplication of the input spectrum with the response of the IF filter shifted to f and a subsequent inverse FFT. The output of the peak detector is the maximum of the resulting voltage waveform.

Fig. 5(a) shows the circuit of a quasi-peak detector. The resistors R_1 and R_2 set the time constants for charging and discharging the capacitor C as defined in CISPR-16 (see Table I). Due to the discharge, the output of the quasi-peak detector depends not only on the amplitude envelope of the incoming signal, but also on the pulse repetition rate.

The simulation model of the quasi-peak detector is implemented in the time domain. The input voltage waveform is the same as the one for the peak detector model, but due to the long time constants involved, this signal has to be repeated until the output of the detector reaches the steady state. Finally, the output signal of the QP detector is applied to the video filter, resulting in an averaging of the signal. Fig. 5(b) shows an example of the

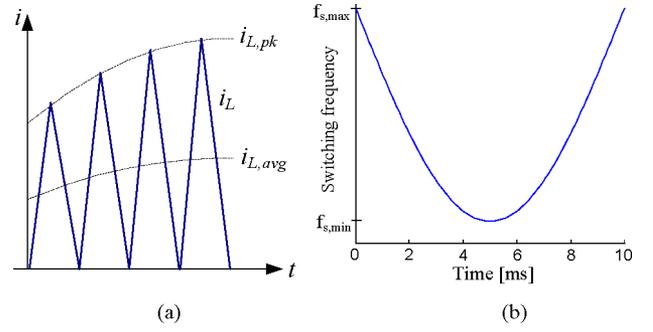


Fig. 6. (a) Inductor current waveform. (b) Variation of the switching frequency over a mains half cycle.

signals at the input of the detector $V_{QP,i}$, the output $V_{QP,o}$, and the final signal after the video filter $V_{VF,o}$.

III. PFC STAGE MODELING

The main source of DM noise is the input current of the PFC stage. In the boundary conduction mode, the switch is turned on for a constant time t_{ON} , resulting in a peak inductor current proportional to the instantaneous rectified line voltage. During the OFF-time of the switch, the inductor current decreases, and as soon as it reaches zero, the next switching cycle begins. The result is a triangular current waveform with a sinusoidal envelope [see Fig. 6(a)]. Due to the varying turn-off time, the switching frequency is not constant and has a minimum at the peak of the line voltage [see Fig. 6(b)]. The peak current is two times the average current; therefore, the input current spectrum shows high harmonic content in the range of the switching frequency.

The CM noise is caused by the parasitic capacitances from switching nodes to the metal case/ground, which is connected to the protective earth (PE). It is assumed in the following that surface-mounted device components are used for the power semiconductors. Consequently, the parasitic capacitances are low compared to the transistors mounted on an earthed heat sink. Nevertheless, the CM noise levels exceed the limits and need to be considered in the filter design. Furthermore, the lamp is typically mounted in an earthed luminaire; therefore, additional capacitances exist between the lamp and the luminaire.

A. Calculation of the PFC Waveforms

Due to the variation of the inductor current amplitude and of the switching frequency, a cycle-by-cycle approach is used to calculate the PFC waveforms for one mains half-period [11]. Assuming a constant ON-time t_{ON} and dc-bus voltage V_{dc} , the ON-time is given by

$$t_{ON} = \frac{4P_{out}L_b}{\hat{v}_{ac}^2\eta} \quad (1)$$

where P_{out} is the output power of the PFC stage, η is the efficiency of the lamp ballast, L_b is the boost inductance, and \hat{v}_{ac} is the peak amplitude of the mains voltage.

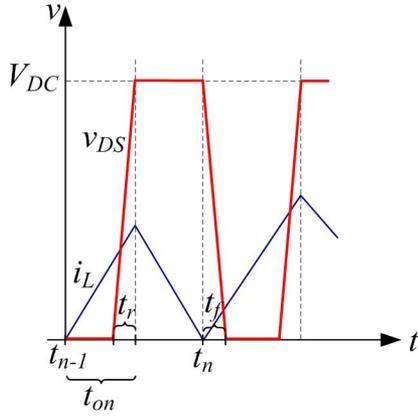


Fig. 7. Drain-source voltage of the PFC switch (t_r and t_f enlarged to improve visibility).

The mains voltage v_{ac} is given by

$$v_{ac}(t) = \hat{v}_{ac} \cos(2\pi f_{ac} t) \quad (2)$$

where f_{ac} is the mains frequency. Assuming a constant line voltage v_{ac} during a switching cycle, the current is increasing linearly and the peak current at the end of the ON-time is

$$\hat{i}_{L,n} = \frac{t_{ON} v_{ac} (t_{n-1} + 0.5 t_{ON})}{L_b} \quad (3)$$

where t_{n-1} is the start of the last switching cycle. During the OFF-time of the switch, the current decreases linearly and the time when i_L reaches zero is

$$t_{OFF,n} = \frac{\hat{i}_{L,n} L_b}{V_{dc} - v_{ac} (t_{n-1} + 0.5 t_{ON})}. \quad (4)$$

Equations (3) and (4) are calculated repeatedly for half a mains period.

The waveform required for the calculation of the CM spectrum is the drain-source voltage v_{DS} of the PFC MOSFET (see Fig. 7). For the calculation of v_{DS} , a constant dc-link voltage V_{dc} is assumed and the ON-state voltage is neglected. In order to simplify the simulation, constant voltage rise and fall times (t_r and t_f) are used, which is not the case in reality due to the varying mains voltage.

In case a modulation function is used for noise shaping [12], [13] or improvement of the input current total harmonic distortion [14], the output of the controller depends on the modulation function. Therefore, (1) cannot be applied and a simulation including the controller is required. Fig. 8 shows the model used for the simulation applied in this paper. The energy storages are modeled with different equations and a simple constant time-step simulation is used to calculate multiple mains cycles until the dc-bus voltage is stable.

B. Differential-Mode Model

Fig. 9 shows the model used for the calculation of the DM noise spectrum. The LISN is modeled as described in the earlier section and the input capacitor of the PFC is modeled with its first-order parasitics.

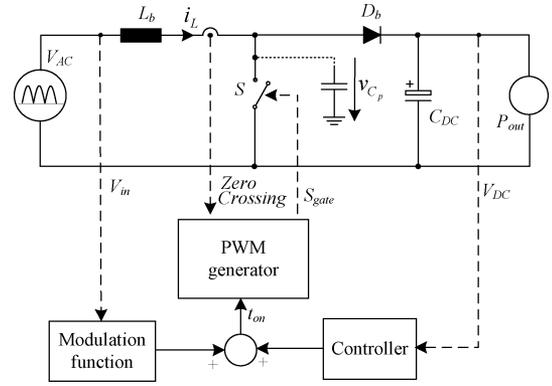


Fig. 8. Model used for the calculation of the current and voltage waveforms of the PFC.

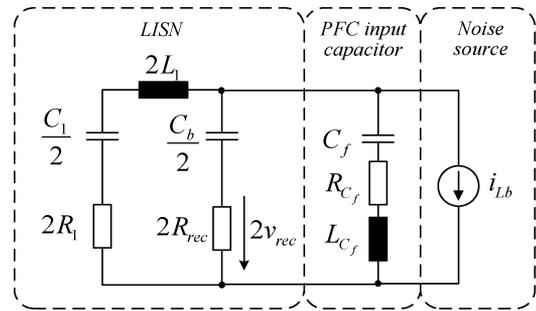


Fig. 9. DM noise propagation model.

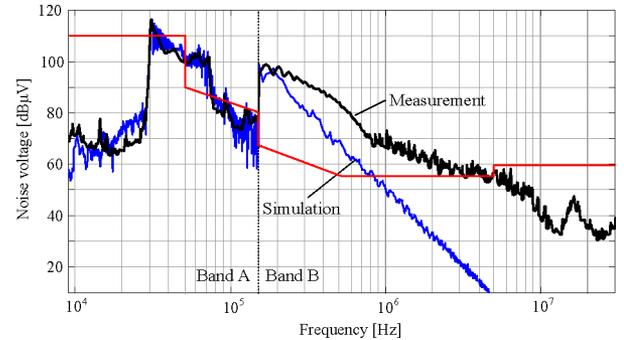


Fig. 10. Measurement and simulation of the DM peak spectrum.

The model is used for deriving the transfer function $G_{DM}(s) = v_{rec}(s)/i_{DM}(s)$ which is required for calculating the voltage spectrum at the input of the test receiver resulting from the inductor current spectrum.

Fig. 10 shows the comparison of the DM measurement and the simulation result using the propagation model from Fig. 9. In band A (9–150 kHz), the simulation shows good agreement with the measurement. In band B (150 kHz to 30 MHz), the simulated noise level drops too fast compared to the measurement.

The comparisons of the simulated results with a circuit simulation using Simplerer show that the bridge rectifier, which is neglected in the noise propagation model, causes significant deviations and must be included in the calculations of the spectrum as explained in the following section.

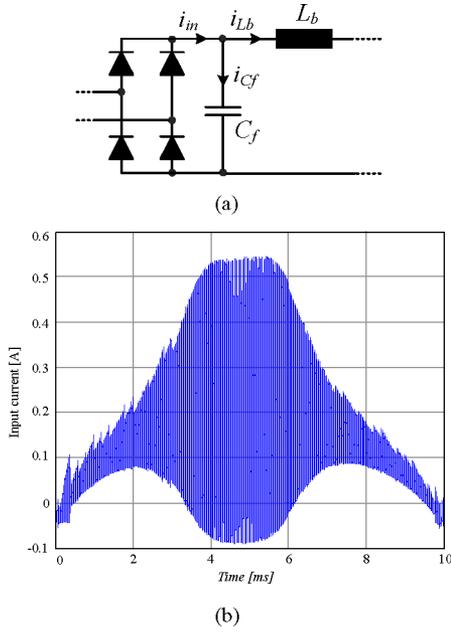


Fig. 11. (a) Input current without rectifier. (b) Simulation of the input current i_{in} resulting from the model without rectifier (Fig. 9).

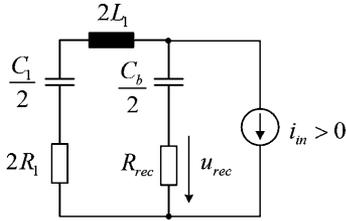


Fig. 12. Modified noise propagation model.

C. Improved Model Including Rectifier

The input current passing through the bridge rectifier i_{in} is the sum of the inductor current i_{Lb} and the filter capacitor current i_{Cf} [see Fig. 11(a)]. In Fig. 11(b), the simulated current i_{in} using the noise propagation model without rectifier (see Fig. 9) is shown. The resulting current waveform has also negative values, which would be blocked by the rectifier in the real circuit.

This effect of the rectifier is approximated by the following modified simulation procedure: First, the input current i_{in} is calculated in the frequency domain using the noise propagation model without rectifier and then an inverse FFT is used to find the time-domain current waveform [see Fig. 11(b)]. The rectifier is then approximated by setting all negative parts of the current to zero. Finally, the noise voltage at the input of the test receiver is calculated using the noise propagation mode shown in Fig. 12. The inclusion of the rectifier in the simulation results in a good agreement of the simulated DM spectrum with the measurements [see Section VI, Fig. 21(a)].

D. Common-Mode Model

The main source of CM noise in the PFC is the parasitic capacitance C_p from the drain node of the PFC switch to the

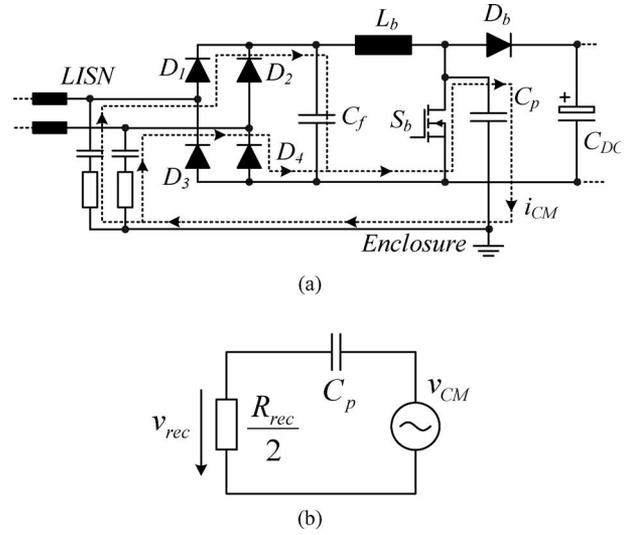


Fig. 13. (a) CM noise current when D_1 and D_4 conduct. (b) Simplified CM noise propagation model.

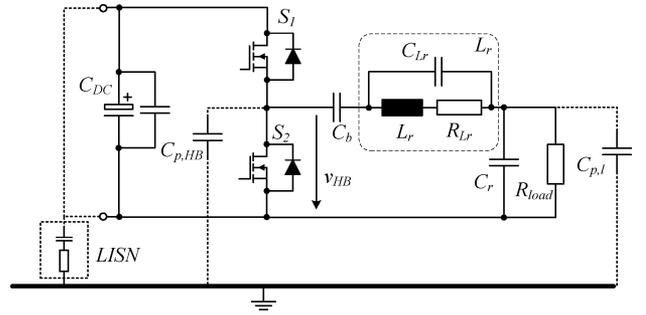


Fig. 14. Schematic of the inverter stage with parasitic capacitances.

case of the ballast. Fig. 13(a) shows the path of the CM noise current i_{CM} for the case diodes D_1 and D_4 are conducting.

The simplified noise propagation model for the calculation of the CM noise spectrum is shown in Fig. 13(b). Due to the very small parasitic capacitance of 2 pF (see Section V) for the considered setup, the dc-blocking capacitors of the LISN and the PFC filter capacitor C_f can be modeled as short circuits at the frequencies of interest. For the same reason, the inductor L_1 of the LISN and the boost inductor L_b are assumed to be open.

This model is only valid for the case in which a filter capacitor is used across the input or output terminals of the rectifier. If no capacitor is present, the CM current flows only through the diode D_4 or D_3 because of the high impedance of the boost inductance L_b [4]. The result is a noise voltage across only one of the LISN impedances, contributing to DM as well as CM noise.

IV. INVERTER STAGE MODELING

Fig. 14 shows the schematic of the resonant half-bridge inverter stage. The inverter consists of the MOSFETs S_1 and S_2 , the resonant tank L_r and C_r , and a dc-blocking capacitor C_b . The main source of differential-mode noise is the switching

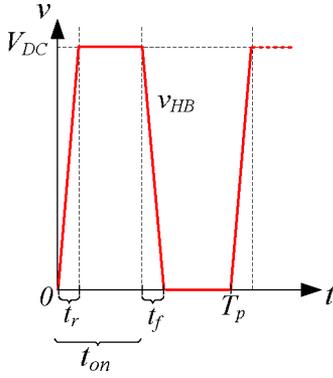


Fig. 15. Voltage at the midpoint of the half-bridge v_{HB} (t_r and t_f shown exaggerated).

action of the half-bridge, but due to the filtering effect of the dc-bus capacitor C_{dc} , the DM noise of the inverter stage is small compared to the PFC stage and does not show in noise measurements. Therefore, DM noise of the inverter is not included in the model.

The CM noise emission of the inverter stage is caused by the high-frequency voltage changes at the switching nodes and the parasitic capacitances to PE. In the model, two parasitic capacitances are included: $C_{p,HB}$ from the midpoint of the half-bridge to the enclosure of the ballast and $C_{p,l}$ which models the capacitance from the lamp and the cable to the earthed luminaire. The simulations and measurements used to get the values of the parasitic capacitances are described in Section V.

A. Inverter Waveforms

The noise source for the CM noise in the inverter is the voltage at the midpoint of the half-bridge. For the simulation, a trapezoidal voltage waveform with constant rise and fall times (t_r and t_f) is assumed (see Fig. 15). Two simulation modes are implemented: In the first mode, the switching frequency of the inverter is constant, corresponding to a ballast without active control of the lamp current. In the second mode, an active control of the lamp current is assumed. This results in a 100-Hz modulation of the switching frequency because the control loop compensates the voltage ripple on the dc link. In this case, a cycle-by-cycle approach is used to calculate the voltage v_{HB} . The amplitude of the lamp voltage is assumed to be constant, corresponding to a perfect compensation of the dc-link ripple by the controller. For every switching cycle, the instantaneous switching frequency is calculated from the instantaneous dc-link voltage v_{DC} and the lamp voltage and the period T_p of this switching cycle is adjusted accordingly.

B. Common-Mode Model

For parasitic capacitance $C_{p,HB}$, the same noise propagation model [see Fig. 16(a)] is used as for the PFC section and the same reasons apply for neglecting most impedances in the propagation path (see Section III-D). The propagation model for capacitor $C_{p,l}$ is shown in Fig. 16(b). In addition to capacitance $C_{p,l}$ and input impedance of the test receiver R_{rec} , the resonant tank is

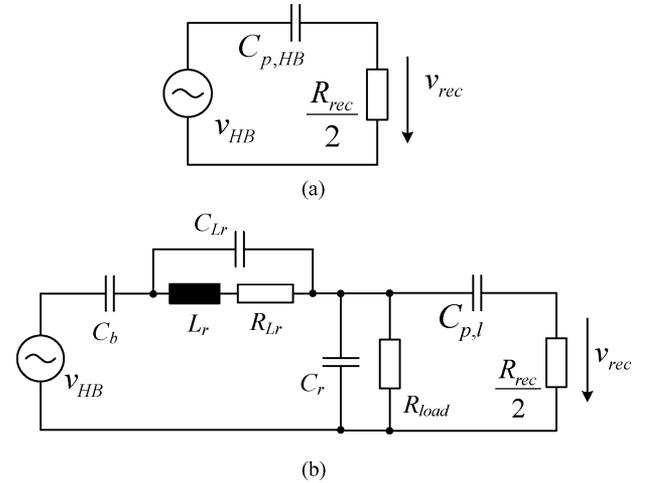


Fig. 16. Noise propagation models for the parasitic capacitances from (a) half-bridge midpoint to the case and (b) lamp and cables to the luminaire.

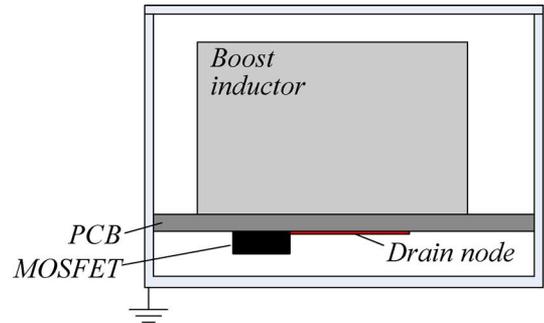


Fig. 17. Cross-sectional view of the ballast in the PFC section.

modeled with first-order parasitic for the resonant inductor L_r . The lamp impedance R_{load} is assumed to be purely resistive.

Both CM propagation models for the inverter are used to calculate the voltage spectrum at the input of the test receiver from the spectrum of the noise source v_{HB} . Finally, the CM noise spectrums of the two inverter sources and the PFC source are added in order to find the total CM noise spectrum.

V. PARASITIC CAPACITANCES

There are two different types of parasitic capacitances in the model. Here, C_p and $C_{p,HB}$ are capacitances from PCB tracks to the earthed enclosure and depend on the specific ballast. Also, $C_{p,l}$ is the capacitance from the wires connecting ballast and lamp to the earthed luminaire. As a result, $C_{p,l}$ depends only on the luminaire but not on the ballast.

Fig. 17 shows a cross-sectional view of a typical ballast for T5 lamps. The power semiconductors are mounted on the bottom of a single-layer PCB while the larger passive components are mounted on top. The main factors for the parasitic capacitances are the PCB layout of the nodes with switched potential and the distance between PCB and enclosure. For this reason, a model of the enclosure and the PCB with the copper area of the nodes was built in the finite-element method (FEM) simulation software Maxwell (see Fig. 18). With this model, an

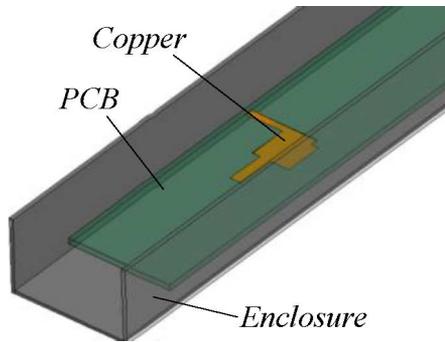


Fig. 18. Electrostatic FEM simulation of the drain node on the bottom of the PCB.

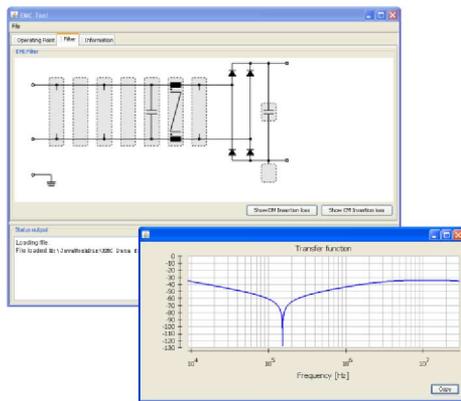


Fig. 19. Screenshot of the *Java* program showing the filter editor and a calculated filter transfer function including parasitics.

electrostatic simulation was applied to determine the parasitic capacitances.

Capacitor $C_{p,l}$ depends on the geometry of the luminaire; the most important factors are the length of the wires from ballast to lamp and how the wires are arranged in the luminaire. For the measurements in this paper, a reference luminaire according to CISPR 30 has been used. The parasitic capacitance was determined by measurement using an Agilent 4285 A precision LCR meter.

Finding the parasitic capacitances C_p and $C_{p,HB}$ is the most time-consuming part of the CM spectrum calculation as it involves using an external program and building the model for the simulation. However, for largely standardized products like electronic ballasts, these capacitances will not vary too much between similar products (e.g., ballasts for different wattages) and the values can be adjusted from experience. For this reason, an exact calculation of the parasitic capacitances is not always required to get a first prediction of the EMI spectrum for the design of the filter.

VI. IMPLEMENTATION AND COMPARISON WITH MEASUREMENTS

The simulation method described in the earlier sections was implemented in a stand-alone *Java* program (see Fig. 19). The input parameters for the simulation of the circuit waveforms are

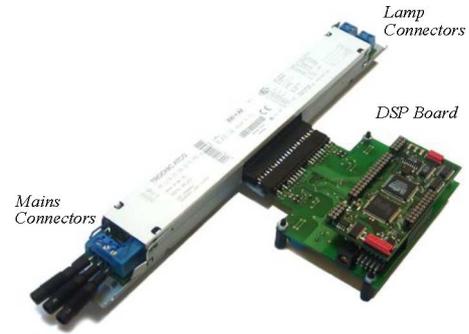


Fig. 20. Photograph of the 35 W ballast and the external DSP control board.

TABLE II
VALUES OF THE MOST IMPORTANT COMPONENTS

PFC	Value	Inverter	Value	Parasitic cap.	Value
L_b	4.2 mH	C_b	68 nF	C_p	2 pF
C_{DC}	10 μ F	L_r	1 mH	$C_{p,HB}$	5 pF
C_f	220 nF	C_r	3.9 nF	$C_{p,l}$	30 pF

the component values and the operating point of the ballast. Additionally, an EMI filter editor allows selecting the type and the values of the filter components, which are simulated including first-order parasitics.

In order to verify the models used for the EMI simulation, EMI measurements have been performed with a 35 W T5 ballast (see Fig. 20) using a lamp as load. The values of the most important components and the parasitic capacitances for the simulation are shown in Table II.

For the EMC measurements, the input filter of the ballast was removed, with the exception of the PFC input capacitor (C_f in Fig. 1). A single-phase version of a CM–DM noise separator described in [15] was used to measure the emission modes independently [16].

A comparison of the simulated DM spectrum with a DM noise measurement can be seen in Fig. 21(a). The simulation shows good correlation of the simulated results with the measurement over the whole range of the spectrum.

The comparison of the CM simulation with the measurements [see Fig. 21(b)] shows good agreement up to a frequency of about 7 MHz. Fig. 21(c) shows the contributions of the PFC and the inverter stage to the CM spectrum. The varying switching frequency of the PFC stage results in a flat spectrum from 150 kHz to 7 MHz. The differences between the measurement and the simulation above this frequency range are likely caused by the variation of the dv/dt at turn-on/turn-off of the PFC switch over a mains half-period, which is not modeled in the simulation. The CM noise of the inverter stage is visible as peaks around multiples of the switching frequency (50 kHz). The double peaks are caused by the lamp current control, which results in a 100-Hz modulation of the switching frequency. Fig. 21(d) shows the results of a simulation including the filter components L_f and C_{f2} (see Fig. 1), which are modeled in the DM and CM noise propagation models [see Figs. 9 and 13(b)] with their first-order parasitics.

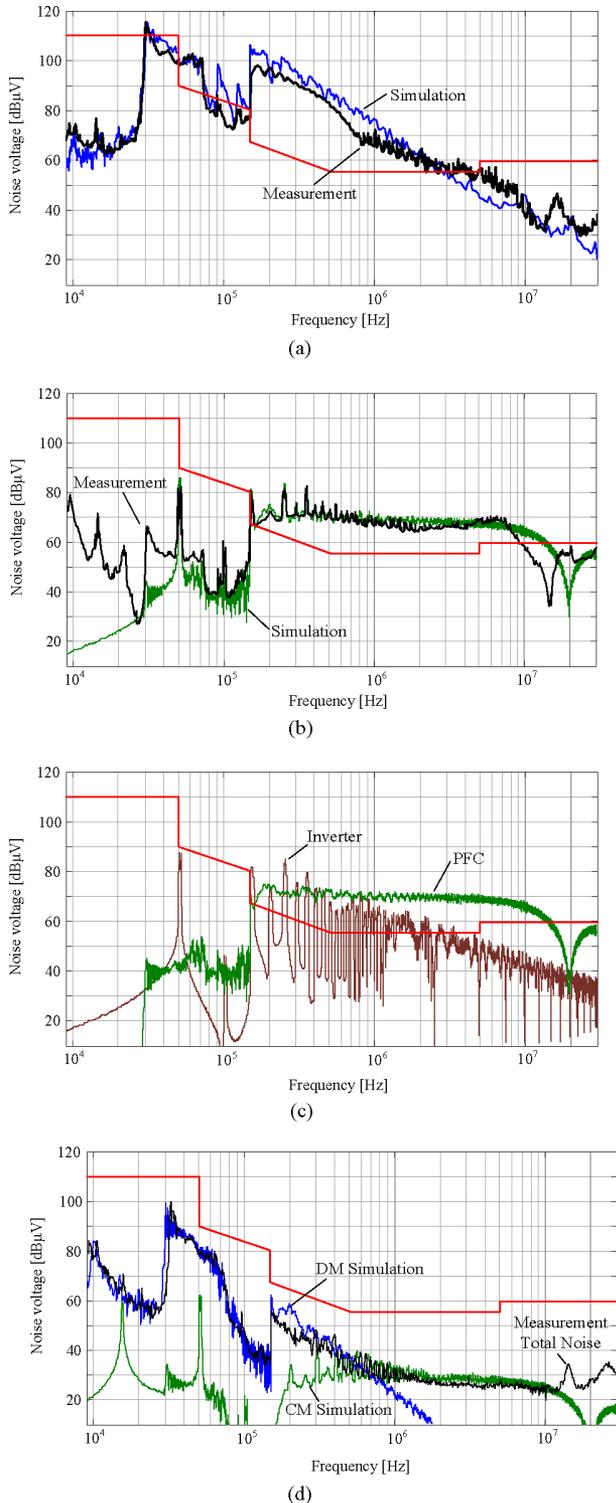


Fig. 21. Measurement and simulation of (a) DM peak spectrum and (b) CM peak spectrum. (c) CM noise contributions of the PFC and the inverter stage. (d) Total noise measurement and DM and CM simulations including all EMC filter components.

As a further verification, a commercially available ballast for two 54 W T5 fluorescent lamps was simulated. Fig. 22 shows the simulation results in comparison with an EMC measurement of the ballast.

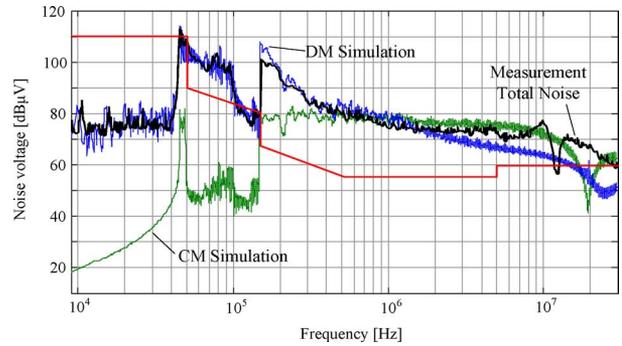


Fig. 22. Total noise measurement and DM and CM simulations without EMC filter for a commercial 2×54 W T5 ballast.

VII. CONCLUSION

In this paper, a model for the conducted noise emission of electronic ballasts is derived. There, the significant CM and DM noise sources and paths of the PFC and the inverter stage have been identified and the influence of the measurement setup has been considered. The model is based on the analytical calculations and on the simulations, which are all implemented in a stand-alone *Java* program. For validating the model, measurement results are presented, which show a very good correspondence between the calculated and the measured spectrum.

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