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New Series-Resonant Solid-State DC Transformer Providing Three Self-Stabilized Isolated Medium-Voltage Input Ports

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New Series-Resonant Solid-State DC Transformer Providing Three Self-Stabilized Isolated Medium-Voltage Input Ports

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Abstract—This work analyzes the properties of a new four-port, series-resonant, and bidirectional DC transformer topology in steady-state and transient conditions. The investigated topology evolves from the Integration of Three (3) Series-Resonant Converters (I3SRC), enables the realization of a converter with high efficiency (99.0%) and high power density (7.1 kW/dm^3), due to the utilization of a three-phase High Frequency (HF) transformer and reduced capacitor currents in the secondary-side DC link, and features the use of a six-pack power module on the secondary side. The analysis is based on the results of detailed circuit simulations of an I3SRC, which takes the couplings between the phases, introduced by the three-phase transformer, into account and considers a DC transformer, i.e., DC–DC converter, with a total rated power of 15 kW, three primary-side DC voltages of 1.1 kV, and a secondary-side DC voltage of 700 V, which is a core part of a scaled demonstrator of a Solid-State Transformer (SST). The obtained findings clarify the self-stabilizing capabilities of the I3SRC for operation with Half-Cycle Discontinuous Conduction Mode (HC-DCM), even if the three isolated DC ports are subject to time-varying and substantially different power levels and different directions of energy transfer.

I. INTRODUCTION

AC–DC Solid-State Transformers (SSTs), which are becoming increasingly popular for fast EV battery chargers [1]–[3], are classically realized based on multi-cell structures where each cell implements an isolated DC–DC converter, to achieve galvanic isolation, and a H-bridge circuit on the AC side, which enables the series-connection of multiple cells. Advantages of the multi-cell concept are modularity and high AC voltage capability of the SST.

From numerous conceivable arrangements of converter cells, a grouping according to **Fig. 1(a)** allows the use of a four-port DC–DC converter, obtained by integration of three AC–DC converters into a single three-phase AC–DC converter, low output-side DC link capacitance requirements due to the absence of a Low Frequency (LF) power pulsation at the output side, and does not restrict the possible number of converter cells (e.g., to multiples of three); the red frame in Fig. 1(a) indicates the parts of the corresponding four-port DC–DC converter. Initial investigations of this converter topology are related to a non-resonant realization, which is based on the concept of the Dual Active Bridge converter, and confined to a series-connection of the three primary-side DC ports and symmetric operating conditions with same currents and voltages at the DC ports, $i_1(t) = i_2(t) = i_3(t)$ and $V_1 = V_2 = V_3$ [4]. Further investigations reveal that the non-resonant

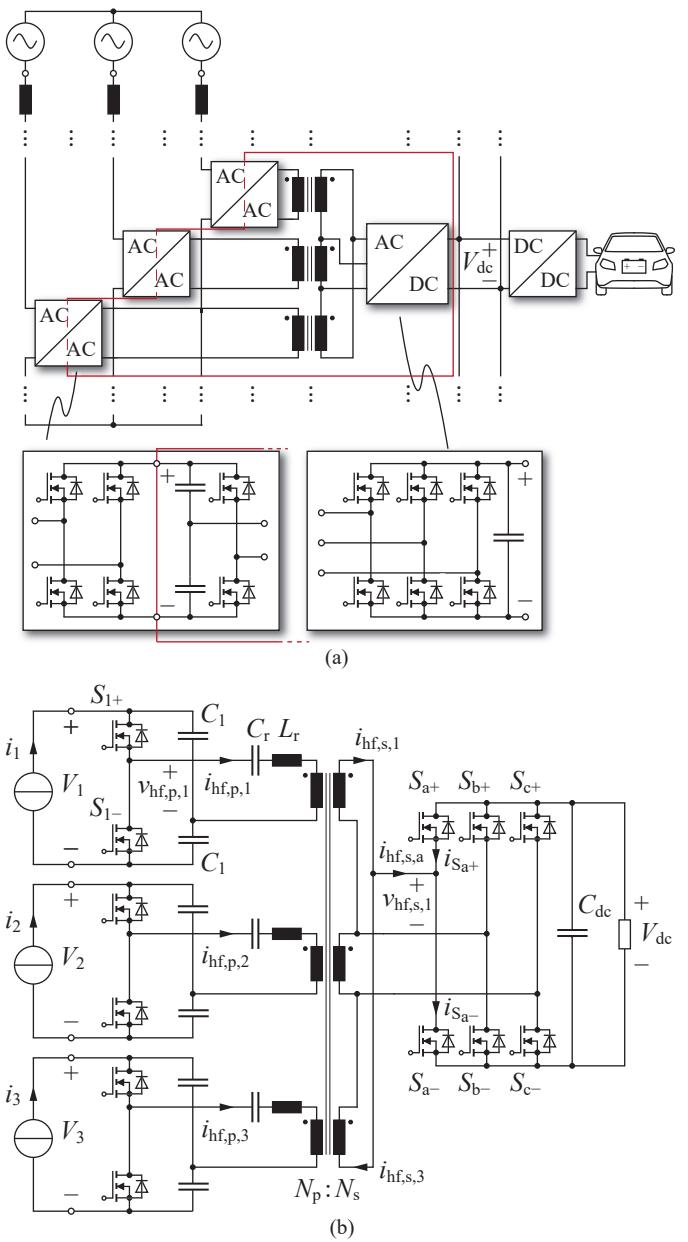


Fig. 1: (a) Block diagram of a Medium-Voltage (MV) AC grid connected, fast battery charging system for electric vehicles. (b) Circuit of the investigated I3SRC with three half-bridge inverter circuits on the primary sides, a three-phase HF transformer, and a two-level three-phase rectifier on the secondary side. The inductors L_r and the capacitors C_r form three series-resonant circuits.

TABLE I: Specifications and component values of the I3SRC.

Nominal primary-side DC voltages	$V_1 \approx V_2 \approx V_3 \approx 1.1 \text{ kV}$
Nominal secondary-side DC voltages	$V_{dc} = 700 \text{ V}$
Nominal power at the secondary side	$P_{out,nom} = 15 \text{ kW}$
Mains frequency	$f_m = 50 \text{ Hz}$
Switching frequency	$f_s = 50 \text{ kHz}$
Transformers' turns ratio	$n = 22/28$
Resonance frequency of L_r and C_r	$f_r = 75 \text{ kHz}$
Transformer's stray inductance	$L_r = 11.2 \mu\text{H}$

four-port DC–DC converter also allows for operation under asymmetric operating conditions with $i_1(t) \neq i_2(t) \neq i_3(t)$ and $V_1 \neq V_2 \neq V_3$ [5]. However, current and/or voltage control loops are required for both, symmetric and asymmetric operating conditions, to stabilize the voltages of the isolated DC links, which leads to increased system complexity, due to the additionally needed measurement and control circuits. Since the MV-side H-bridge circuits depicted in Fig. 1(a) readily implement input current control, in order to achieve Power Factor Correction (PFC) capability, minor changes of the DC port voltages, $V_{1,2,3}$, are acceptable, since the input current controllers will adapt the duty cycles for the H-bridges accordingly. In this context, a resonant DC–DC converter, which is operated with Half-Cycle Discontinuous Current Mode (HC-DCM), would allow for a substantial reduction of system complexity since it gains self-stabilizing capability [6]. In addition, low switching losses (ZVS) can be achieved with HC-DCM.

From numerous publications on related resonant converters, most investigations focus on multi-phase systems that employ parallel [7]–[10] or series [11] connections of the different half- or full-bridges and, due to this reason, distribute the total power uniformly to the different HF links. The principal feasibility of operating the HF links at different power levels is described in [12] for a generalized unidirectional resonant converter, however, no specific details with regard to converter topology, operation, and design are presented, and for multi-port LLC converters [13], [14], which are based on a different converter topology.

This paper analyzes a new resonant, bidirectional four-port isolated DC–DC converter topology, depicted in Fig. 1(b), that is based on the Integration of Three (3) Series Resonant Converters (I3SRC) and employs HC-DCM. The nominal voltages are 1.1 kV and 700 V on the primary-side and secondary-side DC ports, respectively; the total rated power is 15 kW. Besides the inherent property of the HC-DCM I3SRC of stabilizing the DC link voltages $V_{\{1,2,3\}}$, the considered converter features a low number of power semiconductors, low switching losses, and the possibility to operate with a single three-phase HF transformer. Due to these properties, a high power density of 7.1 kW/dm³ and a high efficiency of 99.0% are calculated. **Section II** discusses the steady-state operation of this system, how to achieve ZVS, and a converter design utilizing a three-phase transformer and **Section III-A** presents the small-signal converter model. The derived analytical results are verified by means of detailed circuit simulations, which clarify that HC-DCM operation of the I3DAB is feasible for bidirectional operation with the different phases being operated at different

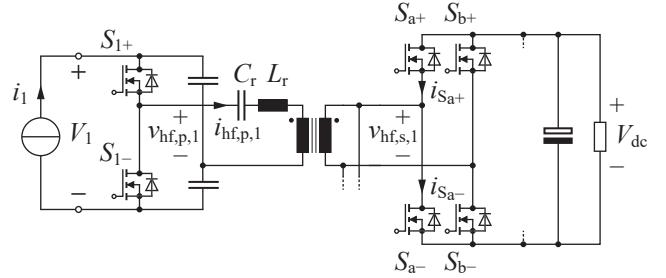


Fig. 2: Circuit diagram of solely the first converter phase of the proposed topology, cf. Fig. 1(b).

power levels. With this, operation with 120° phase shifted power levels pulsating at 100 Hz is successfully demonstrated in **Section III-B**. **Section IV** summarizes the main findings of the paper.

II. STEADY-STATE OPERATION OF THE I3SRC WITH HC-DCM

A. Operating principle

Tab. I lists the main specifications and component values of the HC-DCM I3SRC, which serves for an integrated solution replacing three single-phase DC–DC converters of a scaled SST demonstrator with a rated total power of 90 kW and a line-to-line voltage of 6.6 kV [15]. The listed specifications are used for all simulations conducted in the scope of this paper and the power levels for steady-state DC–DC operation are

$$P_1 = 9 \text{ kW}, \quad P_2 = 500 \text{ W}, \quad P_3 = 5.5 \text{ kW} \quad (1)$$

at the respective MV ports in order to explain the converter operation for the more general case of substantially different port power levels. Furthermore, (1) is of practical relevance, since these power levels e.g. occur 2 ms after the peak of the phase current $i_1(t)$ (in case of a mains frequency of 50 Hz).

Initially, each converter phase is considered separately, according to Fig. 2, to facilitate a more comprehensible explanation of the operating principle. However, this simplification neglects the implications of the couplings between different phases, e.g. introduced by the three-phase transformer, on the converter operation; therefore, the obtained findings need to be verified with the full system. Different to a two-port HC-DCM SRC, the secondary-side three-phase rectifier can only provide duty ratios of 2/3 to the secondary-side transformer windings [4], [5]. For this reason, HC-DCM operation is achieved if the duration of the resonant half-cycle complies with the condition

$$\frac{T_r}{2} = \frac{1}{2f_r} < \frac{2}{3} \frac{1}{2f_s}. \quad (2)$$

With this, the resonance frequency given in Tab. I results.

Fig. 3 depicts simulated gate signals, currents, and voltages in the system specified in **Tab. I**, with emphasis on the first phase of the HC-DCM I3SRC, for MV-side power levels according to (1) and a constant output-port voltage of $V_{dc} = 700 \text{ V}$. Fig. 3(a) shows the gate signals used for the switches of the first MV-side half-bridge. Both switches, S_1 and S_2 , are deactivated during one third of each half-bridge to

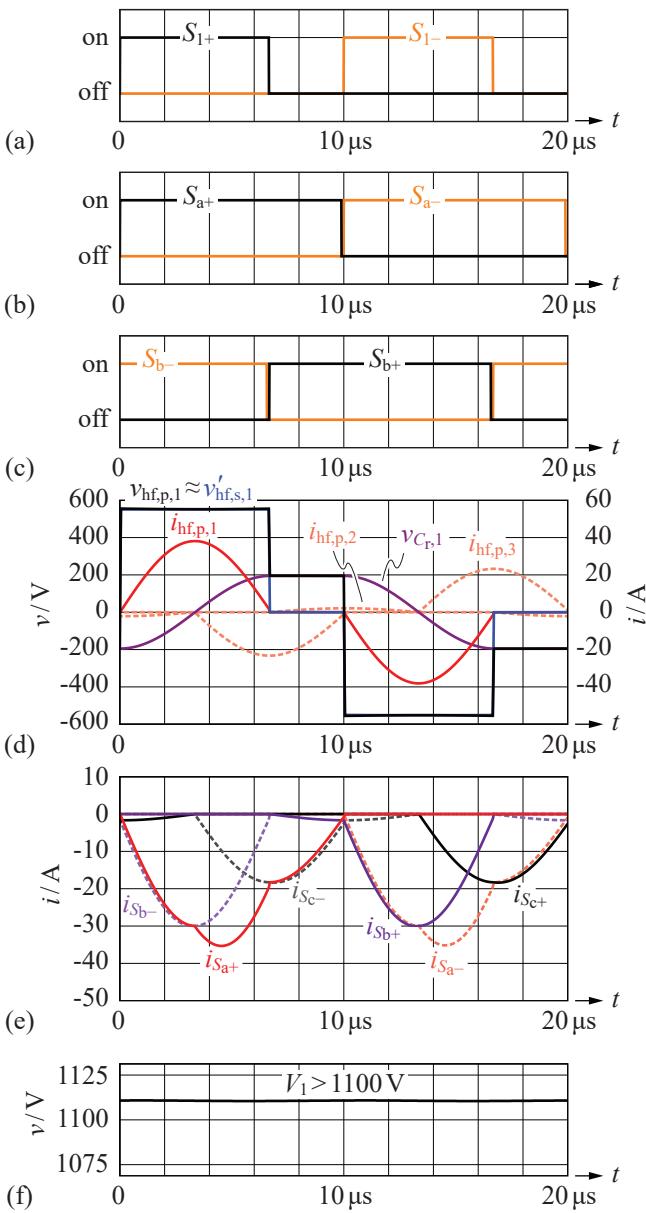


Fig. 3: Simulated current and voltage waveforms for a simplified converter system using three dedicated transformers (instead of a three-phase transformer) and without parasitic components, for operation with the power levels defined in (1): (a) gate signals, MV side, phase 1; (b) and (c) gate signals, LV side, phases a and b; (d) HF voltages applied to the resonant tank of phase 1 and resonant tank currents; (e) currents in the switches of the LV-side three-phase rectifier; (f) MV-side port voltage V_1 for $V_{dc} = 700$ V.

enable zero current in the resonant tank during the respective time interval. Figs. 3 (b) and (c) present the gate signals of phases a and b of the three-phase rectifier, which are phase shifted by 120°. Gate signals are simultaneously provided to the primary-side and secondary-side power converters in order to enable bidirectional operation. Fig. 3(d) depicts the voltages $v_{hf,p,1}$ and $v'_{hf,s,1} \approx v_{hf,s,1}$ applied to the resonant tank of phase 1 and the resonant tank currents in the series resonant circuit and reveals HC-DCM operation with a reduced duty cycle of 2/3. Furthermore, during time intervals with zero resonant current, the output voltage of the MV-side half-

bridge is equal to the voltage across the resonant capacitor, $v_{hf,p,\{1,2,3\}} = v_{C_r,\{1,2,3\}}$ $\forall i_{hf,p,\{1,2,3\}} = 0$, which leads to the condition

$$\max |v_{C_r,\{1,2,3\}}| < V_{\{1,2,3\}}/2. \quad (3)$$

Since the peak values of the resonant currents are directly related to the port power levels,

$$I_{r,pk,\{1,2,3\}} = \frac{\pi}{2} \frac{3}{2} \frac{P_{\{1,2,3\}}}{V_{\{1,2,3\}}/2}, \quad (4)$$

condition (3) implies a limitation of the output power according to

$$P_{\{1,2,3\}} < \frac{2}{\pi} \frac{2}{3} \sqrt{\frac{C_r}{L_r}} \left(\frac{V_{\{1,2,3\}}}{2} \right)^2. \quad (5)$$

Fig. 3(e) presents the currents in the switches of the three-phase rectifier, which, in each case, are differences of two secondary-side transformer currents. For this reason, the rectifier's switches are subject to currents for the durations of their on-states, which enables effective utilization. Fig. 3(f) reveals that the MV-side port voltage, V_1 is 1109 V and, with this, very close to the primary-side referred value of the LV-side port voltage, $2nV_{dc} = 1100$ V. The difference between the two voltages is needed to cover losses and is often derived based on a fundamental frequency approach. However, due to the long relative duration of the current gap, a time-domain approach is preferred for the I3SRC. The expressions for the inductor current and the capacitor voltage in a series resonant tank with series resistor R_s , zero initial inductor current, and initial capacitor voltage, $v_{C_r,0}$ [$= v_{C_r}(t = 0)$ in Fig. 3(d)], are

$$i_{L_r}(t) = \frac{\Delta V - v_{C_r,0}}{Z_0} \frac{\omega_0}{\omega_r} \sin(\omega_r t) e^{-\frac{\omega_0 t}{2Q}}, \quad (6)$$

$$v_{C_r}(t) = \Delta V + (v_{C_r,0} - \Delta V) \times \left[\cos(\omega_r t) + \frac{1}{2Q} \frac{\omega_0}{\omega_r} \sin(\omega_r t) \right] e^{-\frac{\omega_0 t}{2Q}}, \quad (7)$$

$$\omega_0 = \frac{1}{\sqrt{L_r C_r}}, \quad Z_0 = \sqrt{\frac{L_r}{C_r}}, \quad Q = \frac{Z_0}{R_s}, \quad \omega_r = \omega_0 \sqrt{1 - \left(\frac{1}{2Q} \right)^2}, \quad (8)$$

where ΔV denotes the difference between input and output voltages applied to the resonant tank, e.g., in case of the first phase, $\Delta V = V_1/2 - nV_{dc}$ applies. Steady-state operation is attained for $v_{C_r,0} = -v_{C_r}(T_s/2)$ and the analysis returns

$$v_{C_r,0} = -\Delta V \coth \left(\frac{\pi}{4Q} \frac{\omega_0}{\omega_r} \right). \quad (9)$$

For the assumption of low damping, the peak inductor current occurs at $t \approx \pi/(2\omega_r)$ and the input power at each MV port can be determined with (4), (6), and (9),

$$P_{\{1,2,3\}} = \frac{2}{\pi} \frac{2}{3} \frac{\omega_0}{\omega_r} \frac{1}{\sinh \left(\frac{\pi}{4Q} \frac{\omega_0}{\omega_r} \right)} \frac{\Delta V_{\{1,2,3\}}}{Z_0} \frac{V_{\{1,2,3\}}}{2}. \quad (10)$$

For $\omega_r \approx \omega_0$ and $Q \gg 1$, the above expression reduces to

$$\Delta V_{\{1,2,3\}} \approx \frac{3\pi^2}{8Q} \frac{P_{\{1,2,3\}}}{V_{\{1,2,3\}}/Z_0} = \frac{3\pi^2 R_s}{8} \frac{P_{\{1,2,3\}}}{V_{\{1,2,3\}}}. \quad (11)$$

TABLE II: Comparison of simulated and calculated results for the voltage differences applied to the three resonant tanks.

$P_{\{1,2,3\}}$	$V_{\{1,2,3\}}$ (sim.)	$\Delta V_{\{1,2,3\}}$ (sim.)	$\Delta V_{\{1,2,3\}}$ [calc. with (11)]
Three separate transformers			
1 kW	1101.1 V	0.6 V	0.5 V
-1 kW	1098.8 V	-0.6 V	-0.5 V
5 kW	1105.3 V	2.7 V	2.4 V
-5 kW	1094.4 V	-2.8 V	-2.4 V
10 kW	1109.8 V	4.9 V	4.8 V
-10 kW	1089.7 V	-5.2 V	-4.8 V
{9, 0.5, 5.5} kW	{1108.5, 1101.2, 1105.7} V	{4.3, 0.6, 2.9} V	{4.4, 0.2, 2.7} V
{-9, -0.5, -5.5} kW	{1091.2, 1098.7, 1094.0} V	{-4.4, -0.7, -3.0} V	{-4.4, -0.2, -2.7} V
Three-phase transformer; no-load volt.: {1088.5 V, 1088.6 V, 1088.4 V}			
1 kW	{1089.6, 1089.8, 1089.4} V	{0.6, 0.6, 0.5} V	0.5 V
-1 kW	{1087.4, 1087.5, 1087.3} V	{-0.6, -0.6, -0.6} V	-0.5 V
5 kW	{1094.0, 1094.1, 1093.3} V	{2.8, 2.8, 2.5} V	2.4 V
-5 kW	{1083.1, 1083.4, 1083.4} V	{-2.7, -2.6, -2.5} V	-2.4 V
10 kW	{1098.8, 1098.7, 1097.5} V	{5.2, 5.1, 4.6} V	4.8 V
-10 kW	{1078.4, 1079.0, 1079.4} V	{-5.1, -4.8, -4.5} V	-4.8 V
{9, 0.5, 5.5} kW	{1099.5, 1091.1, 1090.0} V	{5.5, 1.3, 0.8} V	{4.4, 0.2, 2.7} V
{-9, -0.5, -5.5} kW	{1078.1, 1085.9, 1086.8} V	{-5.2, -1.4, -0.8} V	{-4.4, -0.2, -2.7} V

Tab. II presents a comparative evaluation of (11), using simulated results for ΔV of the considered system, two different transformer configurations, i.e., three separate transformers and the three-phase transformer discussed in Section II-C, and eight different operating points. Furthermore,

$$R_s = \underbrace{\frac{80 \text{ m}\Omega}{2}}_{\text{C2M0045170P, two in parallel}} + \underbrace{21 \text{ m}\Omega}_{\text{ESRs of capacitors, transformer coils}} + \underbrace{n^2(20 \text{ m}\Omega + 3 \times 38 \text{ m}\Omega)}_{\text{C2M0025120D}} = 144 \text{ m}\Omega \quad (12)$$

applies, cf. Section II-C, where the on-state resistance of the switches of the three-phase rectifier is multiplied by 3, by reason of a wye-delta conversion [5]. Calculated and simulated results match closely in all operating points except for very low power of 0.5 kW, by reason of disregarded factors (e.g. conducting anti-parallel diodes during dead-times), and the last two points. There, the couplings between the phases, introduced by the three-phase transformer, cause minor deviations of the port voltages. Furthermore, a slightly deviating no-load voltage of 1088.5 V is obtained for the three-phase transformer (instead of 1100 V). Besides these aspects, no further implications of the couplings, e.g., on rms or peak values of resonant transformer currents, have been observed.

B. Switching Operation, ZVS

The magnetizing currents that are present in each phase of the three-phase transformer can be utilized to achieve low

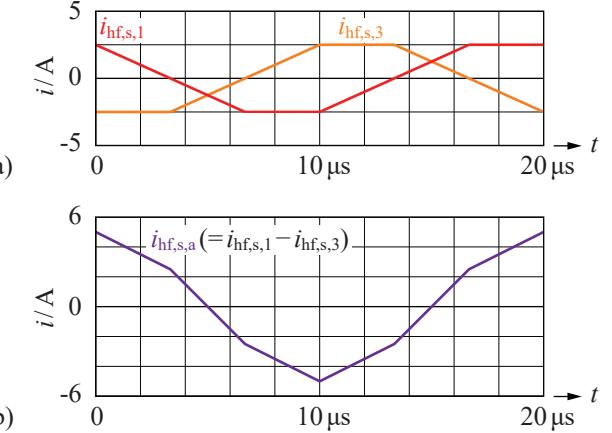


Fig. 4: (a) Waveforms of the secondary-side transformer currents in phases 1 and 3 if only magnetizing currents are considered ($L_m = 933 \mu\text{H}$, $V_{dc} = 700 \text{ V}$, $f_s = 50 \text{ kHz}$); (b) corresponding current in phase a of the three-phase rectifier.

switching losses in the I3SRC [8]. However, the MV-side half-bridges enforce zero currents in the connected primary-side transformer windings during the time intervals when both switches of the corresponding half-bridge are turned off, and any remaining (magnetizing) transformer current appears on the secondary side, where the switches of the three-phase rectifier provide a current path for it.

Since the HC-DCM I3SRC applies rectangular voltages with duty cycles of 2/3 to the three-phase transformer, the magnetizing currents in the transformer phases are trapezoidal, remain constant during 1/3 of each half switching period, and feature same amplitudes of $V_{dc}/(6f_s L_m)$. **Fig. 4(a)** depicts example waveforms for magnetizing currents in phases 1 and 3 for magnetizing inductances of $L_m = L_{m,1} = L_{m,3} = 933 \mu\text{H}$. The phase currents of the three-phase rectifier are the differences of the currents of the connected secondary-side transformer phases, cf. **Fig. 4(b)** for phase a, which leads to an instantaneous magnetizing current for ZVS of

$$I_{ZVS} = \frac{V_{dc}}{3f_s L_m}. \quad (13)$$

For the selected SiC MOSFETs, a useful selection is $I_{ZVS} = 5 \text{ A}$, i.e., $L_m = 933 \mu\text{H}$ (referred to the secondary side) applies.

Fig. 5 depicts simulated waveforms of voltages across the switches during switching operations for a voltage change in phase a (same findings apply to phases b and c), for a dead-time of 300 ns between turn-off and turn-on of the switches of the three-phase rectifier, and for different operating points, i.e., for different directions of energy transfer and different power levels. In particular, in Fig. 5(d) and (f), a low power level of 500 W is considered in order to investigate whether ZVS is maintained, there. The results of Fig. 5 enable two major observations:

- Turn-on of all switches occurs at zero voltage across them;
- ZVS is also achieved on the MV side, since the LV-side current, $i_{hf,s,a}$, first enforces a change of $v_{S_{at}}$, i.e., on the LV side, which leads to a large voltage across the resonant tank and a respective fast change of the current

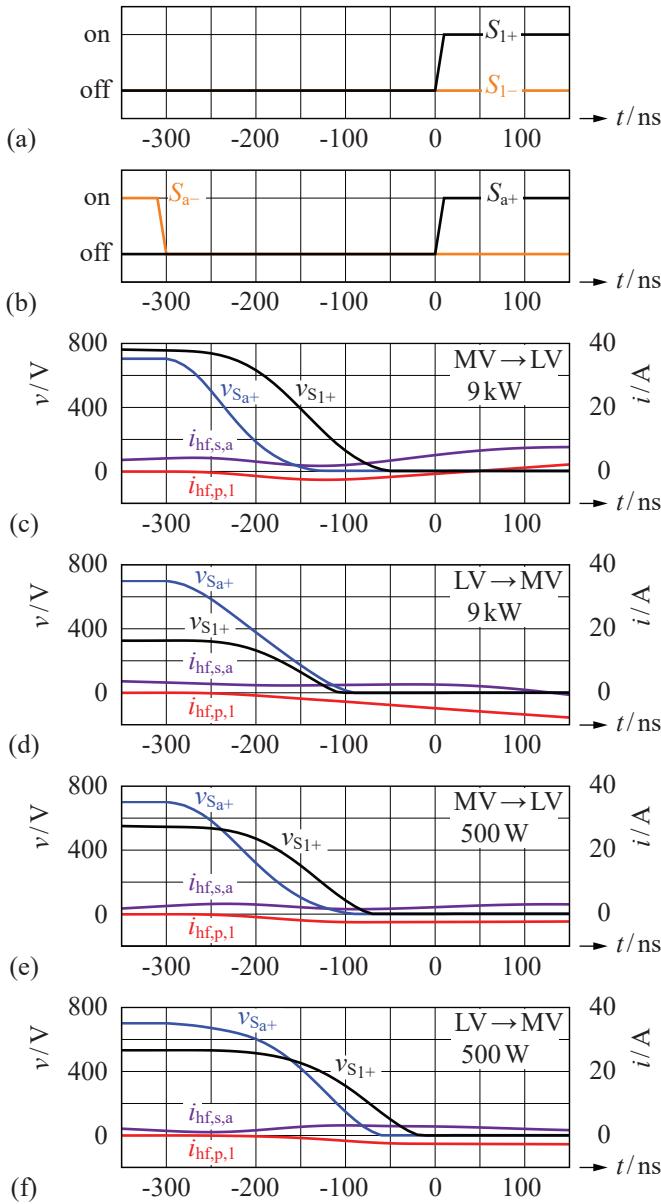


Fig. 5: Simulation results for transient voltage changes in phase a by reason of a turn-off of S_{a-} and a subsequent turn-on of S_{a+} with a dead-time of 300 ns, for different operating points (similar waveforms result for phases b and c): (a) and (b) MV-side and LV-side gate signals, respectively; (c) energy transfer from the MV side to the LV side, 9 kW; (d) MV to LV side, 500 W; (e) LV to MV side, 9 kW; (f) LV to MV side, 500 W.

in the resonant tank, $i_{hf,p,1}$, that enforces a change of v_{S1+} , i.e., on the MV side. Depending on the direction of energy transfer, the sign of $i_{hf,s,a}$ or $i_{hf,p,1}$ changes after this process, which can be observed in Fig. 5(c), at $t = 50$ ns and in Fig. 5(d), at $t = 130$ ns.

Thus, with correct settings of dead-time and magnetizing inductance, the HC-DCM I3SRC is capable of full-range ZVS.

C. Converter Design

In order to achieve both, high efficiency and high power density, SiC MOSFETs are used. The MV side operates two 45 mΩ/1700 V-devices (C2M0045170P by Cree) in parallel per switch and, at an assumed junction temperature of $T_j = 125^\circ\text{C}$,

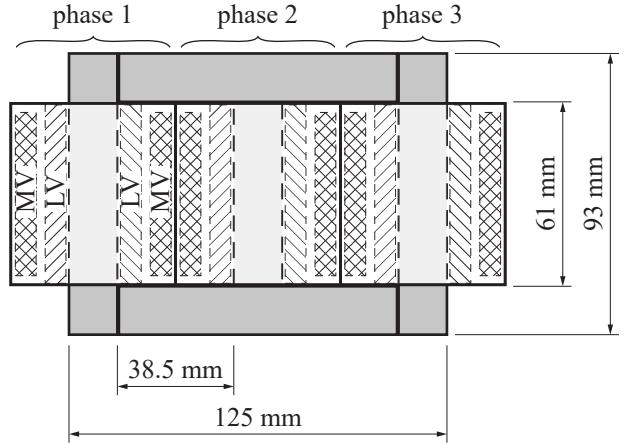


Fig. 6: Proposed construction of the three-phase transformer from five I 93/28/16 cores (the inner core-leg is shortened to 61 mm) featuring a total power of 15 kW, an efficiency of 99.7%, and a boxed volume of 1.04 dm³.

125°C, achieves an effective total on-state resistance of 40 mΩ per switch. The LV side employs a single 25 mΩ/1200 V-device (C2M0025120D by Cree) for each switch, with an on-state resistance of 38 mΩ at $T_j = 125^\circ\text{C}$. Due to the presence of ZVS, very low switching losses occur. The C2M0025120D device generates losses of 11 µJ during each switching operation (from Fig. 8(a) in [16]), which is only 16 % of the energy stored in the effective output capacitance. Based on this result, an energy loss of 30 µJ per switching operation is assumed for the C2M0045170P device (25 % of the stored energy to avoid underestimation of switching losses).

Fig. 6 depicts a schematic drawing of the three-phase transformer, which evolved from the single-phase transformer of [15] and features isolation distances of 3 mm between the primary-(MV)-side and secondary-side coils, between adjacent primary-side coils, and between the primary-side coils and the core.¹ It is based on a ferrite core that is made of five I 93/28/16 cores, where the inner core-leg is shortened from 93 mm to 61 mm. The air gaps at the junctions between adjacent limbs and yokes of the core are utilized to realize the magnetizing inductances needed for ZVS, cf. Section II-B. The total air gap lengths have been identified based on FEM simulations and are 0.5 mm between outer limbs and yokes and 0.3 mm between center limb and yokes. The self inductances of the six coils (primary and secondary sides, 3 phases) and the couplings between the coils, determined with FEM simulations,

$$(L_{p1}, L_{s1}, L_{p2}, L_{s2}, L_{p3}, L_{s3})^T = (391 \mu\text{H}, 633 \mu\text{H}, 485 \mu\text{H}, 786 \mu\text{H}, 391 \mu\text{H}, 633 \mu\text{H})^T, \quad (14)$$

$$k_{tr} = \begin{pmatrix} 1 & 0.986 & -0.541 & -0.543 & -0.348 & -0.350 \\ 0.986 & 1 & -0.543 & -0.546 & -0.350 & -0.352 \\ -0.541 & -0.543 & 1 & 0.988 & -0.541 & -0.543 \\ -0.543 & -0.546 & 0.988 & 1 & -0.543 & -0.546 \\ -0.348 & -0.350 & -0.541 & -0.543 & 1 & 0.986 \\ -0.350 & -0.352 & -0.543 & -0.546 & 0.986 & 1 \end{pmatrix}, \quad (15)$$

¹These isolation distances are first assumptions and are finally adapted to the insulation strength of the chosen insulation material such that the transformer can be used at any position within the phase stack, cf. Fig. 1(a).

are used in a circuit simulator to verify proper converter operation in presence of realistic couplings between the phases. The calculation of the core losses uses the Steinmetz equation and Steinmetz parameters from a software tool provided by TDK/EPCOS [17], which, for the considered N95 core material, 50 kHz, 200 mT, and an assumed core temperature of 80°C returns

$$k = 0.374, \quad \alpha = 1.576, \quad \beta = 2.73. \quad (16)$$

The transformer coils employ HF litz wires with single strand diameters of $d_s = 0.1$ mm:

- Primary side: two wires with 420 single strands in parallel,
- Secondary side: single wire with 735 strands.

The AC resistances are calculated based on the approach presented in [18] and the approximations given in [19], with

$$c_{\text{HF,litz}} = \frac{R_{\text{ac}}}{R_{\text{dc}}} = 1 + \zeta d_s^{6-4\beta_{\text{litz}}} \left(\frac{I'_{\text{rms}}}{I_{\text{rms}}} \right)^2, \quad (17)$$

$$\zeta = \left(\frac{\sqrt{3}\mu_0 b_w h_w k_{\text{fill}} k_{\text{ref}} d_{\text{ref}}^{2\beta_{\text{litz}}-2}}{12\rho b_c \alpha_{\text{litz}}^2} \right)^2, \quad (18)$$

$$I'_{\text{rms}} = \sqrt{f_s \int_0^{1/f_s} \left(\frac{di}{dt} \right)^2 dt} = \omega_0 I_{\text{rms}}, \quad (19)$$

where b_c is the breadth of the core window, b_w the breadth of the coil, h_w the height of the coil, k_{fill} the fill factor (if solid round wire with the same outer diameter as the HF litz wire would be considered), and ρ denotes the resistivity of the conductor. The remaining parameters,

$$\alpha_{\text{litz}} = 1.16, \quad \beta_{\text{litz}} = 0.915, \quad k_{\text{ref}} = 0.6, \quad d_{\text{ref}} = 0.079 \text{ mm}, \quad (20)$$

are related to the HF litz wire and obtained from a least means square calculation that is applied to manufacturer's data. The calculated AC resistances of the coils at the MV and LV sides are $R_{\text{tr,MV}} = 13 \text{ m}\Omega$ and $R_{\text{tr,LV}} = 20 \text{ m}\Omega$, respectively, assuming a copper temperature of 100°C.

Due to low energy storage requirements, all capacitors are polypropylene film capacitors in order to achieve low losses. The half-bridges on the MV side employ 4.7 μF capacitors (B32774H9475 by TDK/EPCOS, $R_{\text{esr}} = 6.4 \text{ m}\Omega$), a single 22 μF capacitor is used in the LV-side DC link (B32776H9226, $R_{\text{esr}} = 4.9 \text{ m}\Omega$), and the parallel connection of four 100 nF and a single 22 nF capacitor (B32684A7104, B32683A7223) realizes the capacitor of each resonant tank with an approximated equivalent series resistance of $R_{\text{esr}} = 5 \text{ m}\Omega$.

Fig. 7 and **Fig. 8** present simulation results for the final system with the three-phase transformer described in this Section, bidirectional operation, and port power levels according to (1). The three primary-side transformer currents, depicted in Fig. 7(a) and Fig. 8(a), reveal different amplitudes, by reason of different power levels, and zero average value with superimposed ringing during the time intervals where the MV-side half-bridge is turned off, which originates from the transformer's leakage inductances and the parasitic output capacitances of the MV-side MOSFETs. Fig. 7(b) and Fig. 8(b) show the currents in the switches of the three-phase rectifier, which are mainly negative in case of energy being transferred

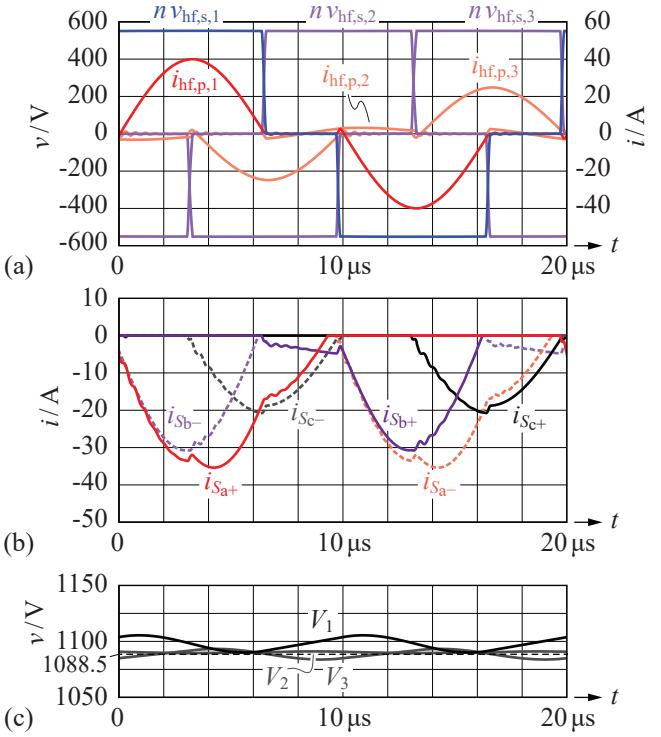


Fig. 7: Voltage and current waveforms in the final HC-DCM I3SRC, with three-phase transformer, energy transfer from the MV to the LV side, operation with different power levels of the three phases according to (1), and active operation of all MV- and LV-side switches using gate signals according to Figs. 3(a)-(c): (a) HF transformer voltages and currents; (b) currents in the switches of the LV-side three-phase rectifier; (c) voltages resulting at the MV-side DC ports.

to the LV side and positive for the reverse direction of energy transfer. The superimposed magnetizing current, observed in Fig. 7(b) and Fig. 8(b), features full-range ZVS. Fig. 7(c) and Fig. 8(c), finally, present the voltages at the MV-side DC ports, which, besides small deviations of their average values from the no-load voltage of 1088.5 V, cf. Tab. II, are also subject to HF voltage ripples.

III. TRANSIENT OPERATION

A. Small-signal converter model

According to [20], [21], the dynamic small-signal model of the HF-part, i.e., inverter, resonant tank, and rectifier, of a HC-DCM SRC can be represented by an equivalent inductor and a resistor. **Fig. 9** depicts the proposed model for the HC-DCM I3SRC, which neglects couplings between the phases except for the common coupling point at the LV-side DC link. The values of the equivalent inductor and resistor are determined according to [21] and the values of DC link capacitances and load resistance need to be referred to the voltage levels of the primary-side resonant tank, i.e.,

$$L_{\text{r,eq}} = \alpha^2 L_{\text{r}} = 5.55 \times 11.2 \mu\text{H} = 62 \mu\text{H}, \quad (21)$$

$$R_{\text{r,eq}} = \beta^2 R_{\text{s}} = 1.85 \times 144 \text{ m}\Omega = 266 \text{ m}\Omega, \quad (22)$$

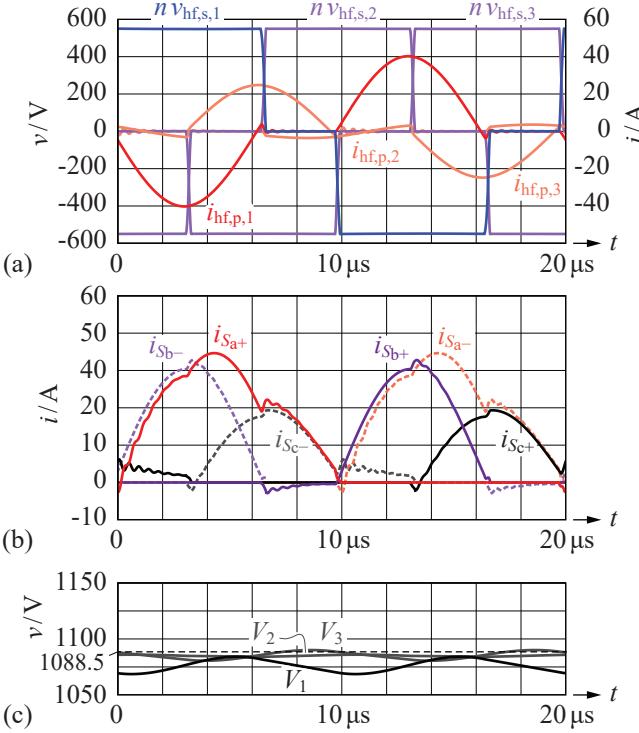


Fig. 8: Voltage and current waveforms in the final HC-DCM I3SRC, with three-phase transformer, reverse energy transfer from the LV to the MV side, operation with different power levels, cf. (1), and active operation of all MV- and LV-side switches using gate signals according to Figs. 3(a)-(c): (a) HF transformer voltages and currents; (b) currents in the switches of the LV-side three-phase rectifier (operating as inverter in the considered case); (c) voltages resulting at the MV-side DC ports.

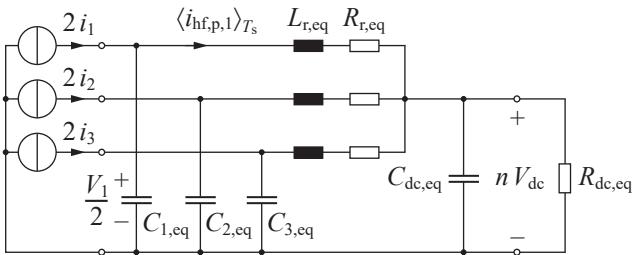


Fig. 9: Small-signal equivalent circuit of the HC-DCM I3SRC. Each single phase of this model originates from [20], [21] and the MV-side DC link is assumed to be the common coupling point of the three phases.

apply, with

$$\alpha = \frac{\pi f_r}{2 f_s} = 2.356, \quad \beta = \frac{\pi}{2\sqrt{2}} \sqrt{\frac{f_r}{f_s}} = 1.36, \quad (23)$$

$$C_{\{1,2,3\},eq} = 2C_{\{1,2,3\}}, \quad C_{dc,eq} = \frac{C_{dc}}{n^2}, \quad R_{dc,eq} = n^2 R_{dc}. \quad (24)$$

Fig. 10 depicts simulated and calculated results for an input current step in phase 1 from 6.4 A to 8.2 A, constant currents of 0.45 A and 5 A in phases 2 and 3, respectively, and is conducted for \$R_{dc,eq} = 19.7 \Omega\$, which represents nominal load of 15 kW at \$V_{dc} = 700\$ V [using the slightly different transfer ratio of the three-phase transformer, which is 5.44/7 rather than 5.5/7, to evaluate (24)]. Furthermore, the simulation considers the couplings between the phases introduced by the three-

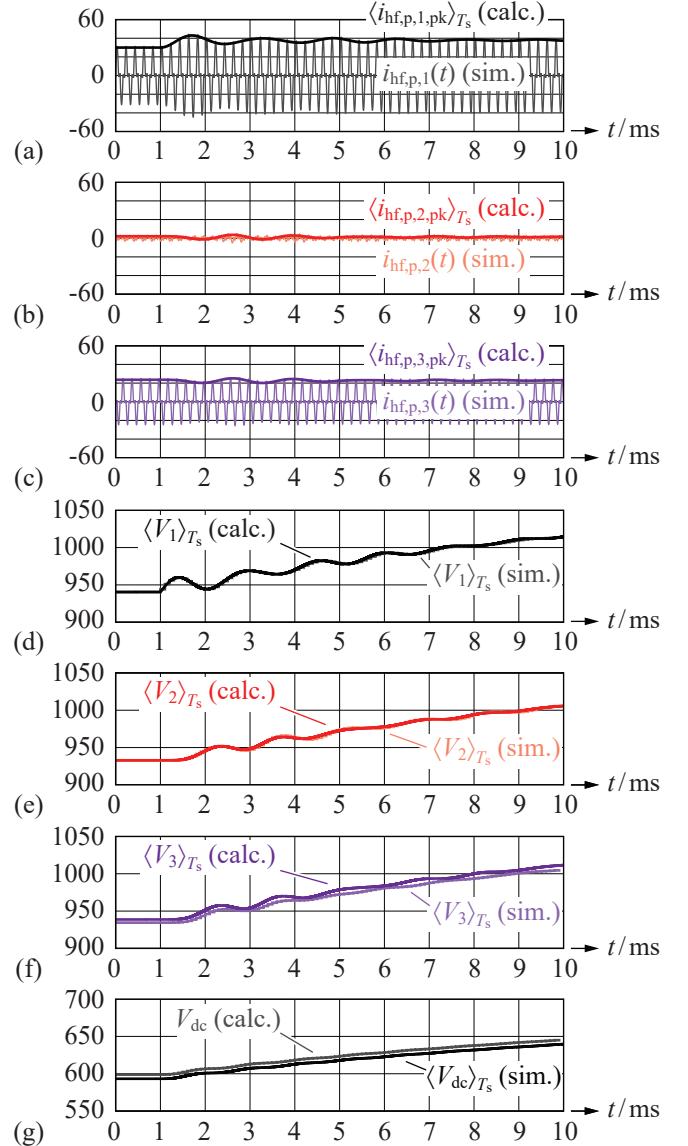


Fig. 10: Simulated and calculated step responses for an input current step in phase 1 from 6.4 A to 8.2 A and nominal load resistance of \$R_{dc,eq} = 19.7 \Omega\$ (the input currents of phase 2 remains at 0.45 A and of phase 3 at 5 A): (a)-(c) calculated envelopes \$\langle i_{hf,p,\{1,2,3\},pk} \rangle_{T_s}\$ and simulated currents in the resonant tanks; (d)-(g) simulated and calculated step responses of the local average values of the DC port voltages. The step responses are similar to that of a 2nd-order low-pass filter with a cutoff frequency of 645 Hz.

phase transformer. Figs. 10(a) to (c) show a comparison of the calculated envelopes of the currents in the resonant tanks, \$\langle i_{hf,p,\{1,2,3\},pk} \rangle_{T_s}\$, to the simulated currents and Figs. 10(d) to (g) illustrate simulated and calculated step responses of the voltages at the DC ports. The results reveal good matching except for Fig. 10(b), where the power is low and the magnetizing current, which is not considered in the model, dominates, cf. [21]. According to this result, transient voltage changes at the common LV-side DC link are the main source of interactions between the phases and the effects of couplings of nearby phases of the employed three-phase transformer can be neglected. The step responses of the system are similar to that of a 2nd-order low-pass filter with a bandwidth of 645 Hz,

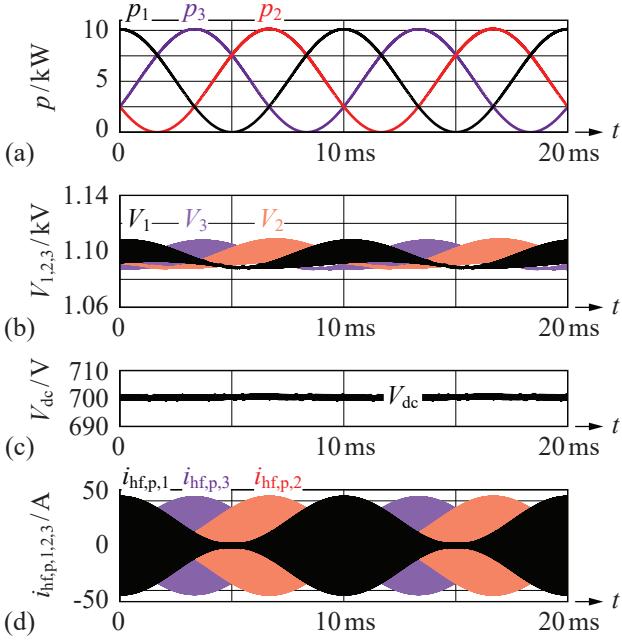


Fig. 11: Three-phase operation of the HC-DCM I3SRC according to Fig. 1(a) with total active power of 15 kW: (a) instantaneous power levels at the three MV-side DC ports; (b) MV-side DC link voltages; (c) LV-side DC link voltage; (d) currents in the resonant tanks. In accordance to the results obtained in Section III-A, the dynamic properties of the HC-DCM I3SRC are sufficient to accomplish the 100 Hz power pulsation without the need for a controller. Furthermore, very low ripple of the LV-side DC link voltage is observed, even though, only a small DC link capacitance of 22 μF is used, since the LF power pulsation of phases 1–3 cancels, there.

thus, the system is expected to adapt well to changes at mains frequency, which is investigated in the next Section III-B.

B. Operation in low-frequency AC mains

The MV-side half-bridges of the HC-DCM I3SRC can be located in the different phases of a three-phase mains, according to Fig. 1(a), in order to achieve a cancellation of the LF power pulsation at the LV side and avoid large DC link capacitances. Provided that the MV-side H-bridges of the complete system shown in Fig. 1(a) realize PFC functionality, approximately sinusoidal input currents with twice the mains frequency results for $i_{\{1,2,3\}}$, due to nearly constant DC link voltages. **Fig. 11** depicts the waveforms of DC link voltages and resonant tank currents over a full mains period for operation with a total active power of 15 kW. Each MV-side DC port is subject to time-varying power, according to Fig. 11(a), which leads to time-varying voltages in the MV-side DC links [Fig. 11(b)] and time-varying current amplitudes in the resonant tanks [Fig. 11(d)]. However, no LF component appears in V_{dc} , cf. Fig. 11(c), due to the cancellation of LF power pulsations at the LV side.

Due to the bidirectional capability of the HC-DCM I3SRC, also the generation of purely reactive input power is achievable, which, for 15 kVA (inductive), leads to the results presented in **Fig. 12** (this simulation uses a voltage source at the LV-side DC link to cover the losses). In this mode of operation, each module reverses its direction of energy transfer every 5 ms. This property is reflected by the MV-side DC link voltages

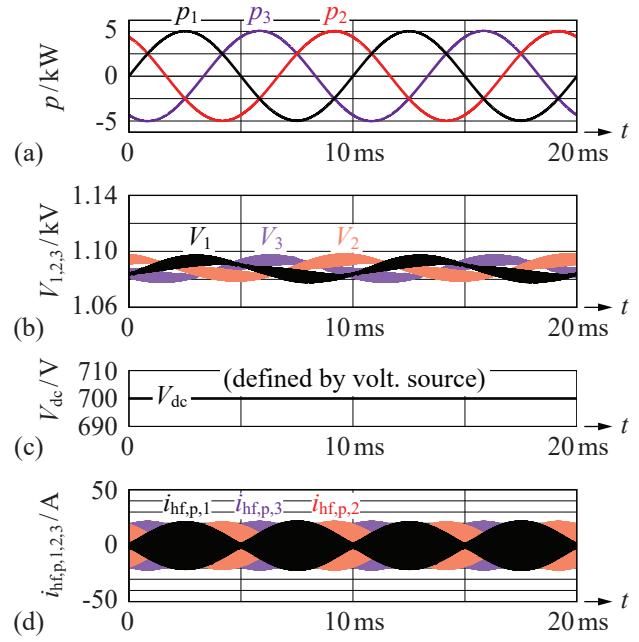


Fig. 12: Three-phase operation of the HC-DCM I3SRC according to Fig. 1(a) with total reactive power of 15 kVA (inductive): (a) instantaneous power levels at the three MV-side DC ports; (b) MV-side DC link voltages; (c) LV-side DC link voltage; (d) currents in the resonant tanks. According to this result, the HC-DCM I3SRC is fully capable of repetitive and phase-independent changes of the directions of energy transfer (a voltage source keeps the LV-side DC link voltage constant, to cover the losses in the HC-DCM I3SRC).

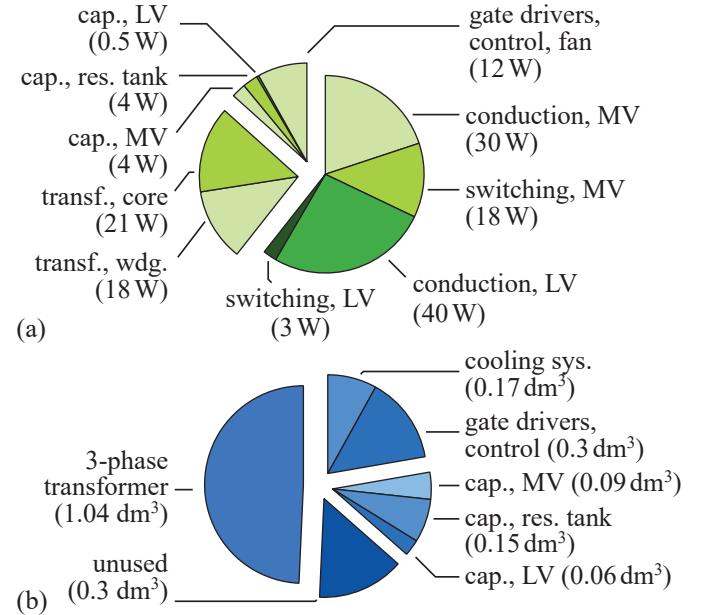


Fig. 13: (a) Breakdown of the losses in the HC-DCM I3SRC for three-phase operation with 15 kW according to Fig. 11. (b) Breakdown of the volume of the presented HC-DCM I3SRC taking into account that 15% of the total volume remain unused (air).

shown in Fig. 12(b), which show a LF oscillation around the no-load voltage of the simulated three-phase transformer, cf. Section II-A.

Fig. 13(a) depicts the calculated breakdown of the losses that are determined for converter operation with a total power

of 15 kW according to Fig. 11. The semiconductor losses dominate with a share of 61% in the total losses and the transformer's core and copper losses have a share of 26%. The remaining losses are capacitor losses and estimated power requirements for control, gate drivers, and fan. With total losses of 148 W, the converter achieves an efficiency of 99.0%.

With regard to converter volume, a total boxed volume of 2.1 dm³ and a corresponding power density of 7.1 kW/dm³ are estimated. According to **Fig. 13(b)**, half of the total converter volume is needed for the transformer, 15% for the capacitors, 15% for gate drivers and control, and 15% is considered to be unused (air). Based on the assumption of a Cooling System Performance Index (CSPI) of 13 $\frac{\text{W}}{\text{dm}^3 \text{K}}$ [16], the volume of the cooling system is 8% of the total volume.

Remark: it is noted that the operation with pulsating power leads to increased rms currents and losses in the converter, which can be mitigated by installing additional capacitors in all MV-side DC links. However, a related analysis reveals that large additional capacitors are required to achieve minor loss reductions (e.g., 1000 μF per DC link for a total loss reduction of 12 W), since a minor change of the DC voltage at a MV-side port causes a substantial change of the power level of the corresponding phase.

IV. CONCLUSION

According to the presented results, the HC-DCM I3SRC is found to enable a low-complexity solution for the isolating DC–DC converter stages of a SST and due to its inherent properties of low switching losses and zero instantaneous residual flux in the core of a three-phase transformer, it achieves a high power density of 7.1 kW/dm³ and a high efficiency of 99.0%. The conducted simulations demonstrate proper operation of the considered four-port power converter even for bidirectional operation and for the three phases being operated at substantially different power levels. Furthermore, the average voltages at the MV-side DC links, i.e., without considering the HF voltage ripple, are found to deviate by less than $\pm 1\%$ for operation within the specified power range. The considered HC-DCM, thus, achieves very stable DC link voltages without the need of controllers.

A close inspection of the losses in the three-phase transformer further reveals that its operation with a reduced duty cycle of 2/3 leads to a decrease of the core losses, which predominates the increase of the winding losses by reason of an increased rms values of the transformer currents and leads to a more efficient utilization of the transformer. However, this comes at the cost of increased losses in the switches of the MV-side half-bridges. Furthermore, ringing is observed during the time intervals with zero primary-(MV)-side transformer current in the voltages at the switching nodes of the MV-side half-bridges. Thus, in a next step, a comprehensive comparative evaluation of competitive converter topologies will be conducted, to obtain a more complete picture concerning the performance of the proposed concept.

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