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Analysis of Double-Bridge Inverters for Drive Systems with Open-End Winding Motors

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***Abstract*—The double-bridge voltage source inverter (DB-VSI) is a promising inverter topology for high performing motor drives. A DB-VSI comprises two VSIs, connected to the opposite sides of an open-end winding motor (no floating neutral point). Thanks to its inherent properties, a DB-VSI requires only half DC supply voltage, compared to a simple VSI, in order to generate the same motor voltage. Thereafter, by processing/switching only half of the DC supply voltage, the DB-VSI benefits from significantly lower semiconductor devices' switching losses. The DB-VSI technology is the main focus of this paper. Namely, two different DB-VSI variants and/or modulation strategies are comparatively evaluated. After detailing the operating principle of each modulation strategy, the stresses on the inverter components are analytically derived. It is shown that the selection of the DB-VSI modulation strategy impacts the efficiency/power density of the inverter and the voltage quality of the motor. The theoretical considerations are subsequently verified within the context of a high-speed motor drive. In the investigated drive system, a fuel-cell supplies the inverter, which in return controls a 280 krpm 1 kW electric compressor. Two DB-VSI hardware prototypes are purposely assembled and compared against a third state-of-the-art hardware prototype of the same specifications. It is shown that, thanks to the DB-VSI technology it is possible to reduce simultaneously the volume and the losses by up to 50% compared to the state-of-the-art solution. The low DB-VSI volume enables a seamless integration of the inverter in the motor housing. Accordingly, the open-end winding motor is directly attached to the inverter, eliminating the need for cumbersome and costly interconnecting cables. A final, integrated (inverter/motor) hardware prototype is presented, that further highlights the advantages of the DB-VSI technology.**

***Index Terms*—Variable-speed drives, Inverter, Fuel-cell, Battery, Wide voltage range, Modulation strategy, Integration**

I. Introduction

Motor drives, supplied by a fuel-cell (or a battery) must cope with a wide input voltage range [1], [2]. The supply voltage U_i can significantly fluctuate, depending on the power loading of the employed fuel-cell (or depending on the charging status/temperature of the employed battery). In this paper, the fuel-cell application depicted in **Fig. 1**, with the specifications of **Tab. I**, is examined. A 10 kW fuel-cell unit requires a continuous supply of oxygen, which is provided by the high-speed electric compressor. A motor drive system, directly supplied by the fuel-cell controls the electric compressor [3]. The employed high-speed 280 krpm compressor/motor is shown in **Fig. 2**. The compressor uses 10% of the fuel-cell power, i.e. 1 kW, and has a nominal phase voltage amplitude of $\hat{U}_\mathrm{o}$=40 V [4]. The fuel-cell features a nominal voltage of $U_\mathrm{i} = 40\,\mathrm{V}$ at full-load condition and a maximum voltage of $U_\mathrm{i} = 120\,\mathrm{V}$ at no-load condition.

TABLE I: Variable-speed motor drive specifications. The nominal operating condition, where the highest component stresses appear, is highlighted in bold.

Fuel-Cell Voltage	U_i	**40V**...120V
Fuel-Cell Current	I_i	0A...**25A**
Motor Voltage Amplitude	$\hat{U}_\mathrm{o}$	0V...**40V** (phase)
Motor Current Amplitude	$\hat{I}_\mathrm{o}$	0A...**16.6A**
Motor Speed	n	0rpm...**280krpm**
Motor Frequency	f_o	0Hz...**5kHz**
Power	P	0...**1kW**
Maximum Power	P_max	1.1kW

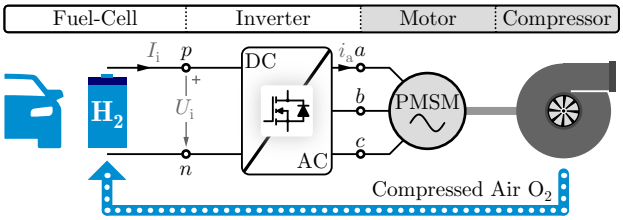

Fig. 1: Motor drive application for fuel-cells. An electric compressor provides oxygen to the fuel-cell, while a motor drive, directly supplied by the same fuel-cell, controls the electric compressor.

Fig. 2: High-speed 280 krpm electric compressor designed by Celeroton AG. [4].

Typically in such drive applications, a single-bridge voltage source inverter (SB-VSI) drives a motor with a floating neutral point, as depicted in **Fig. 3(a)**. A dedicated boost-type DC/DC stage must precede the inverter DC/AC stage in order to adapt the insufficient fuel-cell voltage U_i to a higher DC link voltage U_DC. The DC/DC stage guarantees that the nominal motor voltage can be generated, even if the input voltage U_i is inadequate. Thereby, the two-stage inverter solution of **Fig. 5** results. The SB-VSI solution exhibits low efficiency/power density due the two-stage energy conversion and the additional losses/volume originating from the DC/DC stage. In order to

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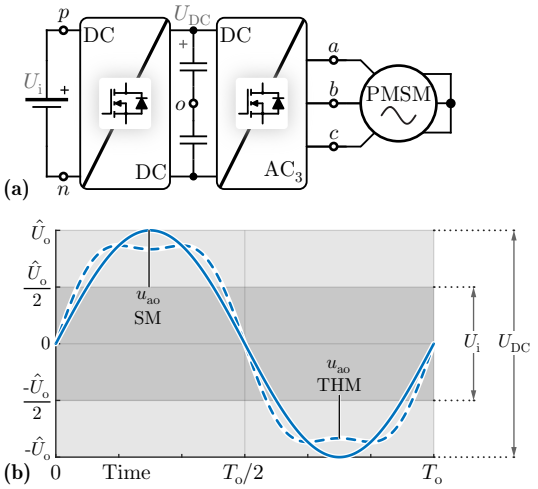

Fig. 3: **(a)** Single-bridge voltage source inverter (SB-VSI) driving a conventional motor with a floating neutral point and **(b)** output voltage waveforms. A DC link voltage of $U_{DC} = 2\hat{U}_o$ is required in the case of simple sinusoidal modulation (SM) or $U_{DC} = \sqrt{3}\hat{U}_o$ in the case of third harmonic injection modulation (THM).

generate the nominal motor voltage amplitude of $\hat{U}_o = \hat{U}_{o,max}$, a high DC link voltage of $U_{DC} = 2\hat{U}_o = 80\,V$ is required in the case of sinusoidal pulse width modulation (or a DC link voltage of $U_{DC} = \sqrt{3}\hat{U}_o = 69.3\,V$ in the case of third harmonic injection modulation) [5] as is illustrated in **Fig. 3(b)**. This high DC link voltage, is possessed/switched by all the semiconductor devices (DC/DC stage and DC/AC stage) resulting in high switching losses.

In order to address the shortcomings of the SB-VSI the promising double-bridge voltage source inverter (DB-VSI) technology [6]–[9] is investigated in this paper. The DB-VSI features two VSIs which are connected to the opposite sides of an open end winding motor as is visualised in **Fig. 4(a)**. An open-end winding motor allows access to both terminals of each phase winding (i.e. terminals a_1 and a_2 for the phase a), in contrast to a conventional motor with a floating neutral point which provides access to only one terminal per phase (cf. **Fig. 3(a)**). Historically, DB-VSI inverter technology originates from high voltage/power motor drives [10]–[14] and has been proposed as an alternative to multi-level inverters [15]. A DB-VSI controls the voltage on both sides of the open-end motor winding (in contrast to SB-VSI). Accordingly, the nominal motor phase voltage amplitude of $\hat{U}_o = \hat{U}_{o,max}$ can be generated by means of a DC supply voltage of only $U_i = \hat{U}_o$. The advantageous features of a DB-VSI are utilized in the investigated fuel-cell application [16]. Thanks to the excellent utilization of the DC supply voltage, it is possible to directly connect the DB-VSI inverter to the fuel-cell, without using a dedicated boost-type DC/DC stage. Opposite to the SB-VSI, the DB-VSI is a single-stage converter, thus the power P is processed only once and is delivered more efficiently to the motor. Furthermore, the semiconductor devices of the DB-VSI, process/switch the low fuel-cell nominal voltage of $U_i = 40\,V$. In contrast, the semiconductor devices of the SB-VSI must switch the high DC link voltage $U_{DC} = 2\hat{U}_o = 80\,V$, in order

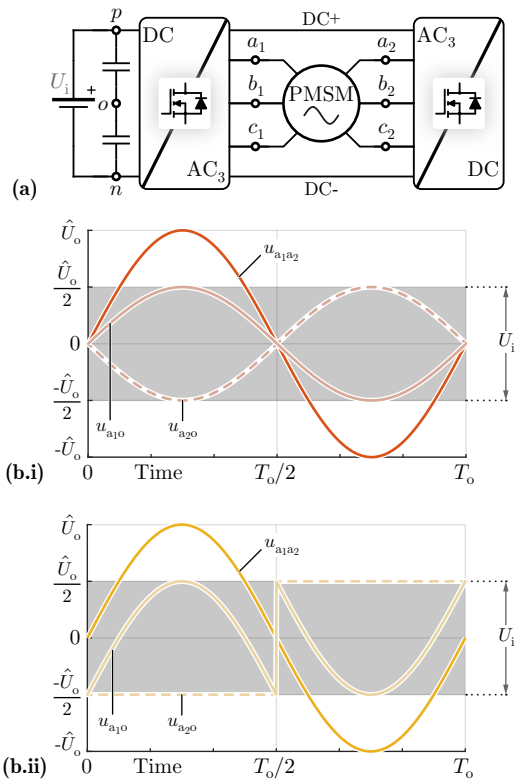

Fig. 4: **(a)** Double-bridge voltage source inverter (DB-VSI) driving an open-end winding motor. Output voltage waveforms for **(b.i)** unipolar modulation and **(b.ii)** unfolder modulation.

to generate the same motor phase voltage amplitude $\hat{U}_o$. Since the switching losses of a unipolar semiconductor device scale with the square U_{sw}^2 of the commutation voltage U_{sw}, the DB-VSI can achieve lower overall switching losses than a SB-VSI. By utilizing the superior performance of the DB-VSI solution, this paper aims for an integration of the inverter in the motor housing [17]–[19]. Accordingly, the open-end winding motor is directly attached to the inverter, eliminating the need for cumbersome and costly interconnecting cables.

The exact shape of the motor terminal voltages u_{a_1o} and u_{a_2o} depends on the employed DB-VSI modulation strategy, however the resulting motor phase voltage $u_{a_1a_2} = u_{a_1o} - u_{a_2o}$ must be sinusoidal. Two DB-VSI modulation strategies are comparatively evaluated in this paper. First the unipolar modulation [20]–[22] is investigated, where both motor terminal voltages u_{a_1o} and u_{a_2o} (of phase a) are actively controlled and have a complementary sinusoidal shape ranging within $-U_i/2... + U_i/2$, as illustrated in **Fig. 4(b.i)**. The unipolar modulation requires continuous operation of both VSIs with a high switching frequency f_s. In order to generate continuous/sinusoidal voltages for the motor, two output filters ($L_o - C_o$) are employed and placed between the two switched VSIs and the motor. As a result, the DB_{II}-VSI inverter variant of **Fig. 6** is derived, where the subscript "II" denotes that both VSIs are switched. Sinusoidal motor voltages are necessary in the case of high-speed motors, in order to limit the generated rotor losses [23]–[25]. The thermal management of the rotor is a main concern in high-speed motors, since the high

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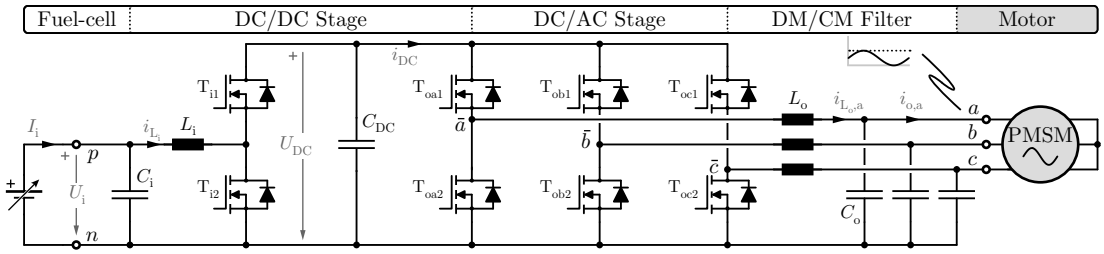

Fig. 5: State-of-the-art single-bridge voltage source inverter (SB-VSI) solution for motor drives with a wide input-output voltage range. The SB-VSI is a two-stage converter, i.e. a dedicated DC/DC stage steps up the battery voltage U_i to a higher DC link voltage U_DC, while a DC/AC stage generates the three-phase motor voltage system. A differential-mode/common-mode (DM/CM) filter is placed before the motor in order to protect the latter from high $\mathrm{d}u/\mathrm{d}t$.

rotational speed and the small rotor volume impede the rotor cooling. As a further advantage, the output filters mitigate the high $\mathrm{d}u/\mathrm{d}t > 30\,\mathrm{kV/\mu s}$, caused by the latest generation of GaN semiconductor devices [26], [27]. If not mitigated, high common-mode (CM) $\mathrm{d}u/\mathrm{d}t$ would lead to premature bearing failure due to parasitic CM currents [28]–[30], while differential-mode (DM) $\mathrm{d}u/\mathrm{d}t$ would stress the insulation of the motor windings [31].

In an effort to extract more performance from a DB-VSI, the unfolder modulation [32], [33] is investigated. There, only one out of the two VSIs is continuously operated with the switching frequency f_s, while the second VSI is operated with the fundamental motor frequency f_o. It is thereby possible to generate a three-phase voltage system for the motor, with the discontinuous, non-sinusoidal terminal voltages $u_{\mathrm{a_1o}}$ and $u_{\mathrm{a_2o}}$ of **Fig. 4(b.ii)**. Thanks to the unfolder modulation, the switching losses are reduced in half compared to the respective losses of the unipolar modulation, since the VSI which is operated with the low fundamental motor frequency f_o exhibits negligible switching losses. Furthermore, the fundamental frequency f_o operated VSI can be directly connected to the respective motor terminals. It is hence possible to dispense with half the filter passive components of the $\mathrm{DB_{II}}$-VSI inverter (unipolar modulation). As a result, the simplified and more compact $\mathrm{DB_I}$-VSI inverter variant of **Fig. 10** is derived, where the subscript "I" denotes that only one VSI is switched.

In **Sec. II**, the operating principle of the unipolar modulation and the unfolder modulation is explained. Subsequently, the stresses on the different inverter components are analytically derived in **Sec. III**. Three hardware prototypes are purposely designed and assembled in **Sec. IV**, corresponding to the $\mathrm{DB_{II}}$-VSI (unipolar modulation), the $\mathrm{DB_I}$-VSI (unfolder modulation) and the conventional SB-VSI. An experimental comparison of the efficiency η and power density ρ of the three hardware prototypes validates the superior performance of the DB-VSI inverter technology compared to a conventional SB-VSI and highlights the trade-offs between the two DB-VSI modulation strategies. The experimental verification is completed by integrating a DB-VSI inverter and a high-speed compressor in the same housing. The conclusions are drawn in **Sec. V**.

II. Operation Principle

A DB-VSI inverter comprises two VSIs connected to the opposite sides of an open-end winding motor. Each VSI controls the voltage on one side of the open-end winding motor e.g. voltages $u_{\mathrm{a_1o}}$ and $u_{\mathrm{a_2o}}$ for phase a, and thus a three-phase motor voltage system is indirectly generated. The exact waveforms of the motor terminal voltage $u_{\mathrm{a_1o}}$ and $u_{\mathrm{a_2o}}$ depend on the employed modulation strategy. However, the motor phase voltages, which are equal to the difference of the motor terminal voltages, e.g. $u_{\mathrm{a_1a_2}} = u_{\mathrm{a_1o}} - u_{\mathrm{a_2o}}$, must be sinusoidal regardless of the employed modulation strategy

$$\begin{aligned} u_{\mathrm{a_1a_2}}(t) &= \hat{U}_\mathrm{o}\sin(\omega_\mathrm{o}t) \\ u_{\mathrm{b_1b_2}}(t) &= \hat{U}_\mathrm{o}\sin(\omega_\mathrm{o}t - \frac{2\pi}{3}) \\ u_{\mathrm{c_1c_2}}(t) &= \hat{U}_\mathrm{o}\sin(\omega_\mathrm{o}t + \frac{2\pi}{3}), \end{aligned} \tag{1}$$

where $\omega_\mathrm{o} = 2\pi f_\mathrm{o}$ is the fundamental motor angular frequency. The modulation index M is defined as the ratio of the motor voltage amplitude with respect to the half of the fuel-cell voltage

$$M = \frac{\hat{U}_\mathrm{o}}{\frac{1}{2}U_\mathrm{i}} = 0...2. \tag{2}$$

Each phase-leg is operated independently of the other two phases. Therefore, the analysis of the DB-VSI focuses only on phase-leg a, when possible. The derived results can be easily extended to the other two phases b and c.

A. $\mathrm{DB_{II}}$-VSI Inverter - Unipolar Modulation

The $\mathrm{DB_{II}}$-VSI of **Fig. 6** employs a unipolar modulation: Two complementary sinusoidally shaped duty cycles $d_{\mathrm{a_1}}$ and $d_{\mathrm{a_2}}$, ranging within $0...1$, control the two half-bridges of phase a as shown in **Fig. 8**. Subsequently, the duty cycles $d_{\mathrm{a_1}}$ and $d_{\mathrm{a_2}}$ are compared to the respective carriers, in order to derive the gating signals of the semiconductor devices. In the case of unipolar modulation, the same carrier is used for the two half-bridges $\bar{a}_1$ and $\bar{a}_2$ of phase a [20]. Furthermore, an identical carrier is also used for phases b and c.

The duty cycles $d_{\mathrm{a_1}}$ and $d_{\mathrm{a_2}}$ are derived

$$d_{\mathrm{a_1}} = \frac{1+d_\mathrm{a}}{2}, \quad d_{\mathrm{a_2}} = \frac{1-d_\mathrm{a}}{2}, \tag{3}$$

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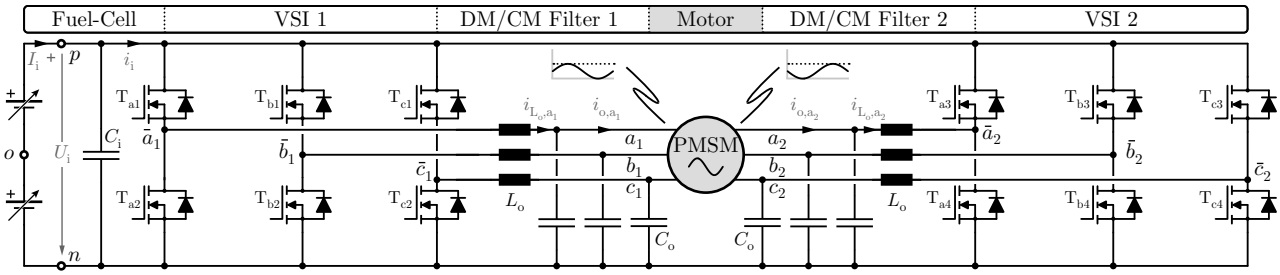

Fig. 6: DB$_{\text{II}}$-VSI inverter solution driving an open-end winding motor. A unipolar modulation is employed i.e. both VSIs are continuously operated with the switching frequency f_s. A DM/CM output filter is placed at each side of the open-end winding motor in order to protect the latter from high du/dt.

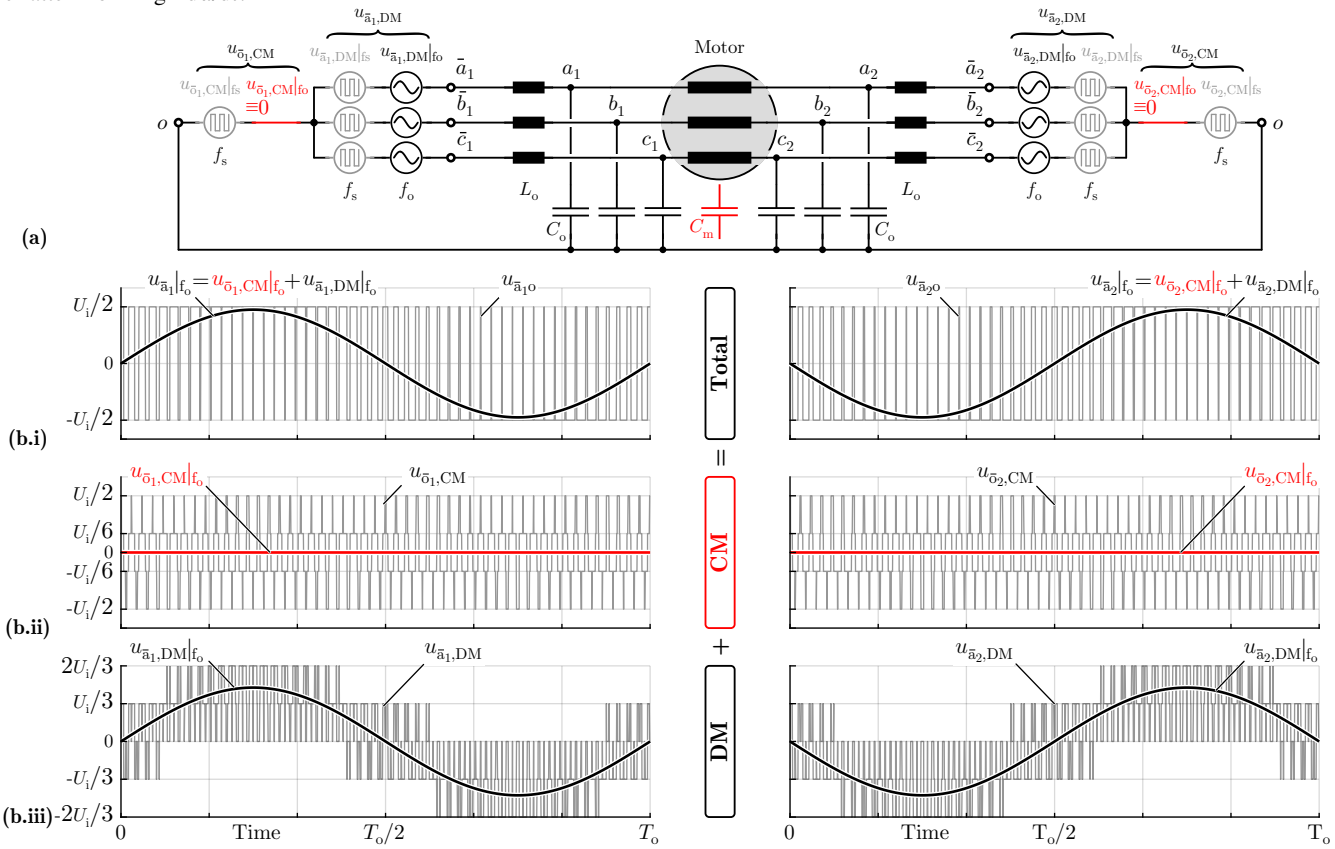

Fig. 7: Voltage equivalent circuit of the DB$_{\text{II}}$-VSI inverter, which allows to assess voltage quality of the motor. Each switch-node voltage is broken down into four components: low-frequency (LF) common-mode (CM) voltage ($u_{\bar{o}_1,\text{CM}}|_{f_o}$), LF differential-mode (DM) voltage ($u_{\bar{a}_1,\text{DM}}|_{f_o}$), high-frequency (HF) CM voltage ($u_{\bar{o}_1,\text{CM}}|_{f_s}$) and HF DM voltage ($u_{\bar{a}_1,\text{DM}}|_{f_s}$).

where d_a is

$$d_{\text{a}}(t) = \frac{u_{\text{a}_1\text{a}_2}}{U_{\text{i}}} = \frac{\hat{U}_{\text{o}}}{U_{\text{i}}}\sin(\omega_{\text{o}}t) \overset{(2)}{=} \frac{M}{2}\sin(\omega_o t). \tag{4}$$

The terminal motor voltages $u_{\text{a}_1\text{o}}$ and $u_{\text{a}_2\text{o}}$, which are proportional to the control duty cycles d_{a_1} and d_{a_2}, have a complementary sinusoidal shape as shown in **Fig. 4(b.i)** and are equal to

$$\begin{aligned} u_{\text{a}_1\text{o}} &= \left[d_{\text{a}_1}(t) - \frac{1}{2}\right] U_{\text{i}} = +\frac{\hat{U}_{\text{o}}}{2}\sin(\omega_o t) \\ u_{\text{a}_2\text{o}} &= \left[d_{\text{a}_2}(t) - \frac{1}{2}\right] U_{\text{i}} = -\frac{\hat{U}_{\text{o}}}{2}\sin(\omega_o t). \end{aligned} \tag{5}$$

The motor phase voltage is also sinusoidal $u_{\text{a}_1\text{a}_2} = u_{\text{a}_1\text{o}} - u_{\text{a}_2\text{o}} = \hat{U}_{\text{o}}\sin(\omega_o t)$.

As a result of the unipolar modulation, both VSIs are continuously operated over time with the switching frequency f_s as is illustrated in **Fig. 8**. Accordingly, both switch-node voltages $u_{\bar{a}_1\text{o}}$ and $u_{\bar{a}_2\text{o}}$ feature a two-level PWM voltage profile, as shown in **Fig. 7(b.i)**. In order to protect the motor from the switch-node PWM voltages (du/dt), two DM/CM output filters ($L_{\text{o}} - C_{\text{o}}$) are used (one for each VSI), as visualized in **Fig. 6**. Those DM/CM output filters are based on passive components and belong to the filter family of DC link referenced filters [34], [35], i.e. the filter capacitors C_{o} are connected/referenced to the negative DC rail n. This feedback connection of the capacitors C_{o} to the DC link allows to

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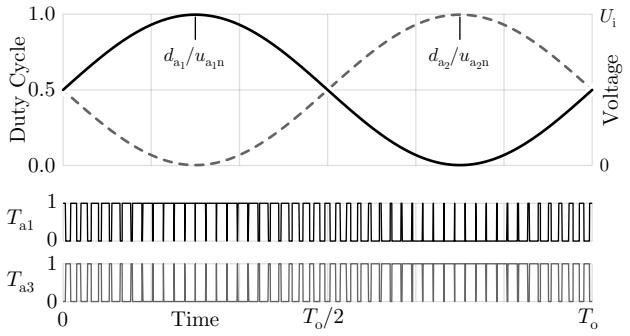

Fig. 8: Unipolar modulation: Two complementary sinusoidal duty cycles control the two half-bridges $\bar{a}_1$ and $\bar{a}_2$ of phase a, resulting in continuous switching over time.

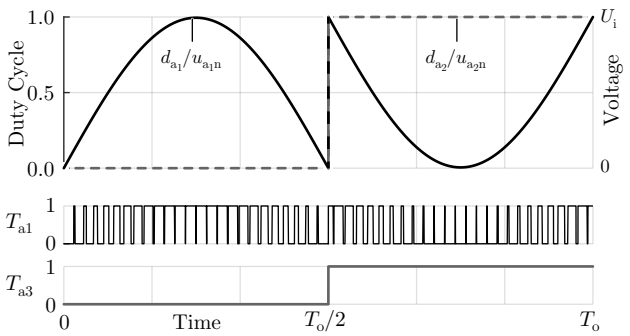

Fig. 9: Unfolder modulation: Only half-bridge $\bar{a}_1$ is continuously operated with the switching frequency f_s, while the second half-bridge $\bar{a}_2$ of phase a is operated with the fundamental motor frequency f_o.

suppress both the DM and the CM $\mathrm{d}u/\mathrm{d}t$ of the semiconductor devices, resulting in a continuous/smooth motor phase voltage.

The motor voltage quality, is now analysed in detail. To this end, each thee-phase switch-node voltage system, e.g. $[\bar{a}_1, \bar{b}_1, \bar{c}_1]$, is substituted by a voltage equivalent circuit [30], [36]. Accordingly, the $\mathrm{DB_{II}}$-VSI of **Fig. 6** can be represented by the equivalent circuit of **Fig. 7(a)**. For example, the two-level PWM voltage of the switch-node $\bar{a}_1$, illustrated in **Fig. 7(b.i)**, is broken down into

$$u_{\bar{a}_1 o} = u_{\bar{o}_1,\mathrm{CM}} + u_{\bar{a}_1,\mathrm{DM}}. \tag{6}$$

The quantity $u_{\bar{o}_1,\mathrm{CM}}$ is the switch-node CM voltage. As shown in **Fig. 7(b.ii)**, $u_{\bar{o}_1,\mathrm{CM}}$ is a four-level PWM voltage and can be further broken down into

$$u_{\bar{o}_1,\mathrm{CM}} = u_{\bar{o}_1,\mathrm{CM}}|_{f_o} + u_{\bar{o}_1,\mathrm{CM}}|_{f_s}, \tag{7}$$

where $u_{\bar{o}_1,\mathrm{CM}}|_{f_o}$ is the low-frequency (LF) CM voltage component and $u_{\bar{o}_1,\mathrm{CM}}|_{f_s}$ is the high-frequency (HF) CM voltage component. The quantity $u_{\bar{a}_1,\mathrm{DM}}$ of **(6)** is the DM switch-node voltage. As depicted in **Fig. 7(b.iii)**, $u_{\bar{a}_1,\mathrm{DM}}$ is a five-level PWM voltage and can be further broken down into

$$u_{\bar{a}_1,\mathrm{DM}} = u_{\bar{a}_1,\mathrm{DM}}|_{f_o} + u_{\bar{a}_1,\mathrm{DM}}|_{f_s}, \tag{8}$$

where $u_{\bar{a}_1,\mathrm{DM}}|_{f_o}$ is the LF DM voltage component and $u_{\bar{a}_1,\mathrm{DM}}|_{f_s}$ is the HF DM voltage component. The LF voltage terms $u_{\bar{o}_1,\mathrm{CM}}|_{f_o}$ and $u_{\bar{a}_1,\mathrm{DM}}|_{f_o}$ are directly related to the employed modulation strategy and the corresponding duty cycles d_{a_1} and d_{a_2}. The HF terms $u_{\bar{a},\mathrm{DM}}|_{f_s}$ and $u_{\bar{o},\mathrm{CM}}|_{f_s}$ are related to the PWM switching frequency f_s. The different switch-node voltage components of **(7)**-**(8)** are illustrated in **Fig. 7(b)**. Note that, the breakdown of a switch-node voltage into HF/LF and DM/CM voltage components **(6)**-**(8)** can be extended to the second VSI switch-node voltage system $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$.

The two-level PWM switch-node voltages $u_{\bar{a}_1 o}$ and $u_{\bar{a}_2 o}$ of phase a are processed by the two DM/CM filters. As a result, the motor terminal voltages $u_{a_1 o}$ and $u_{a_2 o}$ are smooth and continuous. The DM/CM output filters allow the LF switch-node voltage components to pass through intact, resulting in the motor terminal voltages of **(5)**. In contrast, the DM/CM output filters attenuate the HF switch-node voltage components resulting into a voltage ripple Δu_{a_1} and Δu_{a_2} at the motor terminals, as is derived in the following. For a filter inductor L_o The maximum inductor current ripple amplitude (single-side) ΔI_{L_o} can be calculated as

$$\Delta I_{L_o} = \frac{U_i}{8 L_o f_s}. \tag{9}$$

Accordingly, the maximum occurring voltage ripple amplitude (single-side) ΔU_{C_o} at the output filter capacitor C_o is

$$\Delta U_{C_o} = \frac{\Delta I_{L_o}}{8 C_o f_s} \overset{(9)}{=} \frac{U_i}{64 f_s^2 L_o C_o}. \tag{10}$$

The voltage ripple Δu_{C_o} (with a repetition frequency equal to the switching frequency f_s) appears across the capacitors of the two used output filters, since both VSIs are continuously operated with the switching frequency f_s. In other words, a voltage ripple appears on either side of the open-end winding motor i.e. at the motor terminals $[a_1, b_1, c_1]$ and $[a_2, b_2, c_2]$ when unipolar modulation is employed with a maximum value of

$$\Delta U_{a_1 o} = \Delta U_{a_2 o} = \Delta U_{C_o} = \frac{U_i}{64 f_s^2 L_o C_o}. \tag{11}$$

After quantifying the voltage of the open-end winding motor terminals individually, the motor CM voltage is now analysed. The CM voltage at each side of the open-end winding motor is

$$\begin{aligned} u_{o_1,\mathrm{CM}}(t) &= \frac{u_{a_1 o} + u_{b_1 o} + u_{c_1 o}}{3} \\ u_{o_2,\mathrm{CM}}(t) &= \frac{u_{a_2 o} + u_{b_2 o} + u_{c_2 o}}{3}. \end{aligned} \tag{12}$$

The motor CM voltage is defined at the middle of the motor winding as

$$u_{o,\mathrm{CM}}(t) = \frac{u_{o_1,\mathrm{CM}} + u_{o_2,\mathrm{CM}}}{2}. \tag{13}$$

Accordingly, a zero CM voltage is calculated in the case of unipolar modulation, based on **(5)**,**(12)** and **(13)**

$$u_{o_1,\mathrm{CM}} = u_{o_2,\mathrm{CM}} = u_{o,\mathrm{CM}} = 0, \tag{14}$$

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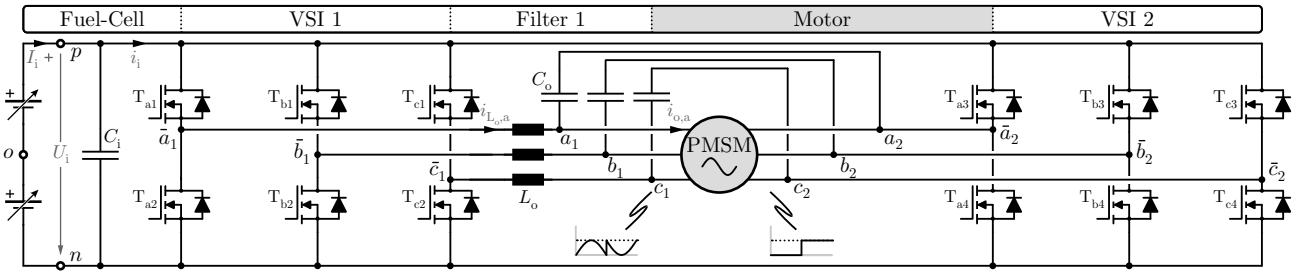

Fig. 10: DB_I-VSI inverter solution driving an open-end winding motor. An unfolder modulation is employed, i.e. only one VSI is operated with the switching frequency f_s, while the second VSI is operated with the fundamental motor frequency f_o. Only one output filter is placed between the high-frequency operated VSI and the motor, in order to protect the latter against high du/dt.

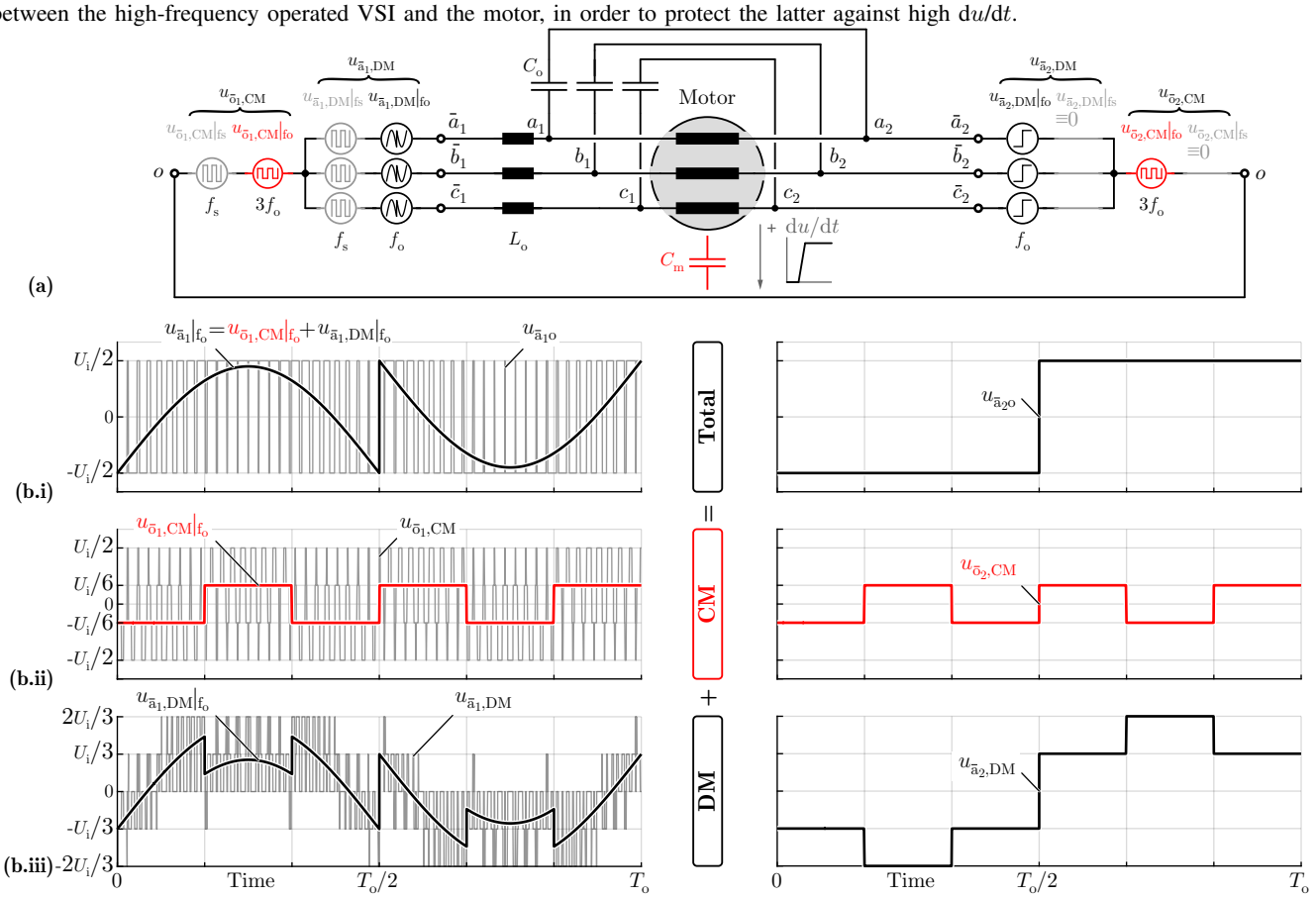

Fig. 11: Voltage equivalent circuit of the DB_I-VSI inverter, which allows to assess voltage quality of the motor. Each switch-node voltage is broken down into four components: low-frequency (LF) common-mode (CM) voltage ($u_{\bar{o}_1,CM}|_{f_o}$), LF differential-mode (DM) voltage ($u_{\bar{a}_1,DM}|_{f_o}$), high-frequency (HF) CM voltage ($u_{\bar{o}_1,CM}|_{f_s}$) and HF DM voltage ($u_{\bar{a}_1,DM}|_{f_s}$). The unfolder modulation causes a CM voltage on the motor, with a rectangular shape and a repetition frequency equal to three times the fundamental motor frequency $3f_o$.

which guarantees low electric stress on the motor. The unipolar modulation is summarized in **Tab. II**.

B. DB_I-VSI Inverter - Unfolder Modulation

The DB_I-VSI of **Fig. 10** employs an unfolder modulation. That is, only one out of the two VSIs is continuously operated with the switching frequency f_s, while the second VSI is operated with the fundamental motor frequency f_o. The resulting discontinuous duty cycles d_{a_1} and d_{a_2} for phase a are shown in **Fig. 9** and are calculated

$$d_{a1} = \begin{cases} d_a, & d_a \geq 0 \\ 1+d_a, & d_a < 0 \end{cases}, \quad d_{a2} = \begin{cases} 0, & d_a \geq 0 \\ 1, & d_a < 0 \end{cases}, \tag{15}$$

where d_a is given in **(4)**. The terminal motor voltages u_{a_1o} and u_{a_2o} are proportional to the control duty cycles d_{a_1} and d_{a_2}, respectively and are

$$\begin{aligned} u_{a_1o} &= \left[d_{a_1}(t) - \frac{1}{2}\right] U_i = \hat{U}_o \sin(\omega_o t) - \frac{U_i}{2}\mathrm{rec}(\omega_o t) \\ u_{a_2o} &= \left[d_{a_2}(t) - \frac{1}{2}\right] U_i = -\frac{U_i}{2}\mathrm{rec}(\omega_o t), \end{aligned} \tag{16}$$

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where rec(x) is a rectangular function

$$\mathrm{rec}(x) = \begin{cases} 1, & 0 < x \leq \pi \\ -1, & \pi < x \leq 2\pi \end{cases}. \tag{17}$$

The two motor terminal voltages are non-sinusoidal and discontinuous as shown in **Fig. 4(b.ii)**, but result in a sinusoidal motor phase voltage $u_{\mathrm{a_1a_2}} = u_{\mathrm{a_1o}} - u_{\mathrm{a_2o}} = \hat{U}_{\mathrm{o}} \sin(\omega_o t)$. Only the VSI $[\bar{a}_1, \bar{b}_1, \bar{c}_1]$ which is operated with the switching frequency f_{s} requires a dedicated output filter. In contrast, the VSI $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$ which is operated with the fundamental motor frequency f_{o} does not require a dedicated output filter and hence can be directly connected to the respective motor terminals $[a_2, b_2, c_2]$. Therefore, the simplified filter configuration of the DB$_{\mathrm{I}}$-VSI shown in **Fig. 10** is derived.

The motor voltage quality is now analysed in detail. To this end, the DB$_{\mathrm{I}}$-VSI of **Fig. 10** can be represented by the equivalent circuit of **Fig. 11(a)**. Similar to the DB$_{\mathrm{II}}$-VSI analysis, each switch-node voltage is broken down into HF/LF and DM/CM voltage components as described by **(6)**-**(8)**. In particular, the switch-node voltage $u_{\bar{\mathrm{a}}_1\mathrm{o}}$ of the half-bridge $\bar{a}_1$, which is operated with the switching frequency f_{s}, features a two-level PWM voltage profile as illustrated in **Fig. 11(b.i)**. Accordingly, this switch-node voltage can be broken down into a four-level PWM CM voltage component $u_{\bar{\mathrm{o}}_1,\mathrm{CM}}$ of **Fig. 11(b.ii)** and a five-level PWM DM voltage component $u_{\bar{\mathrm{a}}_1,\mathrm{DM}}$ of **Fig. 11(b.iii)**. In contrast, the switch-node voltage $u_{\bar{\mathrm{a}}_2\mathrm{o}}$ of the half-bridge $\bar{a}_2$, which is operated with the motor fundamental frequency f_{o}, features a two-level rectangular (not PWM) voltage profile with a repetition frequency equal to the fundamental frequency f_{o} (cf. **Fig. 11(b.i)**). This switch-node voltage can be broken down according to **(6)** into a two-level rectangular CM voltage component $u_{\bar{\mathrm{o}}_2,\mathrm{CM}}$ with repetition frequency equal to three times the fundamental frequency $3f_{\mathrm{o}}$ (cf. **Fig. 11(b.ii)**) and a five-level rectangular DM voltage component $u_{\bar{\mathrm{a}}_2,\mathrm{DM}}$ with a repetition frequency equal to the fundamental frequency f_{o} (cf. **Fig. 11(b.iii)**).

The switch-node $[\bar{a}_1, \bar{b}_1, \bar{c}_1]$ voltages of the switching frequency operated VSI are processed by the output filter: The output filter allows the LF switch-node voltage components to pass through intact, resulting in the LF motor terminal voltage $u_{\mathrm{a_1o}}$ of **(16)**. In contrast, the output filter attenuates the HF switch-node $\bar{a}_1$ voltage components, resulting into a small motor terminal voltage ripple $\Delta u_{\mathrm{a_1o}}$. The voltage ripple $\Delta u_{\mathrm{a_1o}}$ at the motor terminal a_1 is equal to the voltage ripple $\Delta U_{\mathrm{C_o}}$ across the output filter capacitor C_{o} which is given in **(10)**. The switch-node $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$ voltages of the fundamental frequency operated VSI are directly applied to the respective motor terminals $[a_2, b_2, c_2]$. Therefore, the motor terminal voltage $u_{\mathrm{a_2o}}$ of **(16)** results, while no voltage ripple appears at the motor terminals $[a_2, b_2, c_2]$. Accordingly, the worst case voltage ripple amplitude (single-side) at the motor terminals a_1 and a_2 is

$$\Delta U_{\mathrm{a_1o}} = \frac{U_{\mathrm{i}}}{64 f_{\mathrm{s}}^2 L_{\mathrm{o}} C_{\mathrm{o}}}, \quad \Delta U_{\mathrm{a_2o}} = 0. \tag{18}$$

TABLE II: Unipolar modulation (DB$_{\mathrm{II}}$-VSI) and unfolder modulation (DB$_{\mathrm{I}}$-VSI) summary.

	DB$_{\mathrm{II}}$-VSI	**DB$_{\mathrm{I}}$-VSI**
$d_{\mathrm{a_1}}$	$\frac{1}{2}(1 + d_{\mathrm{a}})$	$\begin{cases} d_{\mathrm{a}}, & d_{\mathrm{a}} \geq 0 \\ 1 + d_{\mathrm{a}}, & d_{\mathrm{a}} < 0 \end{cases}$
$d_{\mathrm{a_2}}$	$\frac{1}{2}(1 - d_{\mathrm{a}})$	$\begin{cases} 0, & d_{\mathrm{a}} \geq 0 \\ 1, & d_{\mathrm{a}} < 0 \end{cases}$
$u_{\mathrm{a_1o}}$	$+\frac{1}{2}\hat{U}_{\mathrm{o}} \sin(\omega_o t)$	$\hat{U}_{\mathrm{o}} \sin(\omega_o t) - \frac{1}{2} U_{\mathrm{i}} \mathrm{rec}(\omega_o t)$
$u_{\mathrm{a_2o}}$	$-\frac{1}{2}\hat{U}_{\mathrm{o}} \sin(\omega_o t)$	$-\frac{1}{2} U_{\mathrm{i}} \mathrm{rec}(\omega_o t)$
$\Delta U_{\mathrm{a_1o}}$	$\frac{U_{\mathrm{i}}}{64 f_{\mathrm{s}}^2 L_{\mathrm{o}} C_{\mathrm{o}}}$	$\frac{U_{\mathrm{i}}}{64 f_{\mathrm{s}}^2 L_{\mathrm{o}} C_{\mathrm{o}}}$
$\Delta U_{\mathrm{a_2o}}$	$\frac{U_{\mathrm{i}}}{64 f_{\mathrm{s}}^2 L_{\mathrm{o}} C_{\mathrm{o}}}$	0
$u_{\mathrm{o,CM}}$	0	$-\frac{1}{6} U_{\mathrm{i}} \mathrm{rec}(3\omega_{\mathrm{o}} t)$

A sinusoidal motor voltage $u_{\mathrm{a_1a_2}} = \hat{U}_{\mathrm{o}} \sin(\omega_o t)$ and the variable $d_{\mathrm{a}} = \frac{1}{2} M \sin(\omega_{\mathrm{o}} t)$ are assumed.

The overall motor CM voltage is now analysed. The CM voltage at each side of the open-end winding motor is calculated based on **(12)** and **(16)**

$$u_{\mathrm{o_1,CM}}(t) = u_{\mathrm{o_2,CM}}(t) = -\frac{U_{\mathrm{i}}}{6} \mathrm{rec}(3\omega_{\mathrm{o}} t). \tag{19}$$

In the case of unfolder modulation, a residual LF CM voltage appears at the motor terminals which is highlighted with red in **Fig. 11(b.ii)**. This CM voltage has a rectangular shape, a repetition frequency equal to three times the fundamental motor frequency $3f_{\mathrm{o}}$ and an amplitude of $\frac{U_{\mathrm{i}}}{6}$. The CM voltages on the two sides of the open-end winding motor are equal. If the CM voltages $u_{\mathrm{o_1,CM}}$ and $u_{\mathrm{o_2,CM}}$ would not be equal, then substantial circulating CM currents would appear in the DB$_{\mathrm{I}}$-VSI inverter. The motor CM voltage, is calculated on the middle of the motor winding based on **(13)** as

$$u_{\mathrm{o,CM}}(t) = -\frac{U_{\mathrm{i}}}{6} \mathrm{rec}(3\omega_{\mathrm{o}} t). \tag{20}$$

At the edges of the rectangular motor CM voltage, du/dt appears on the motor bearing. Then, CM current can flow through the motor bearing, which is represented by the parasitic capacitor C_{m} in **Fig. 11(a)**. It is sown in [37], that the expected lifetime of the motor bearing decreases as higher CM RMS current flows through the bearing. For the case of the DB$_{\mathrm{II}}$-VSI, du/dt appears only six times during a fundamental period T_{o} (cf. **Fig. 11(b.ii)**). Therefore, the bearing CM RMS current is low and hence non-critical for the motor reliability. The unfolder modulation is summarized in **Tab. II**.

III. Component Stresses

In this section, the voltage/current stresses on the different DB-VSI components and the switching/conductions losses are analytically derived. The results are calculated for a drive system with the specifications of **Tab. I**, however, the presented concepts are general and can be accordingly applied to drive systems with different specifications. For the considered application example, the nominal fuel-cell

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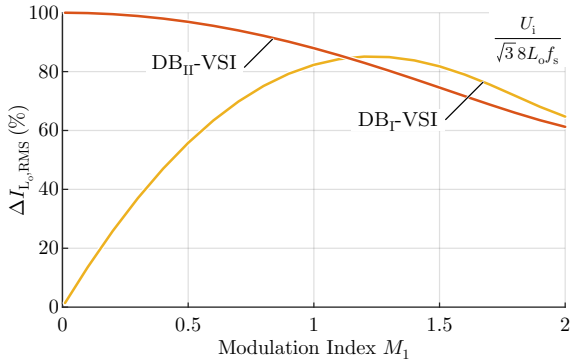

Fig. 12: Inductor RMS current ripple for (orange) DB_{II}-VSI employing unipolar modulation and (yellow) DB_I-VSI employing unfolder modulation. The RMS current ripple is normalized with respect to the maximum occurring local RMS current ripple $\Delta I_{L_o,RMS,max}$ **(34)**.

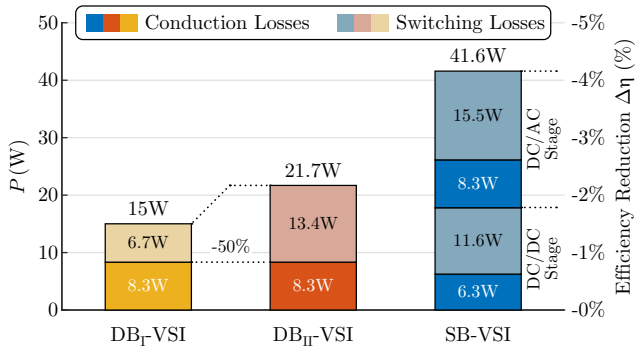

Fig. 13: Semiconductor losses breakdown into switching and conduction losses for (yellow) DB_I-VSI employing unfolder modulation, (orange) DB_{II}-VSI employing unipolar modulation and (blue) conventional SB-VSI. The numeric values are calculated for nominal motor power/voltage (i.e. modulation index $M = 2$), using the parameters of **Tab. III**.

voltage is $U_i = 40\,V$, while motor voltage ranges within $\hat{U}_o = 0\,V...40\,V$ (phase amplitude). An inverter system that can operate under any load power factor (PF) $\cos(\phi) < 1$ is desirable in this case study. Hence, the output voltage-current phase shift is $\phi = -90^o...90^o$ (i.e. capacitive or inductive load behaviour). Accordingly, the transferred apparent power $S = 0\,W...1000\,W$, active power P, fuel-cell current I_i and motor fundamental motor current amplitude $\hat{I}_o$ can be expressed as a function of the modulation index M **(2)** and the PF $\cos(\phi)$ as

$$\begin{aligned} S &= M^2\frac{3U_i^2}{8R}, \quad P = M^2\frac{3U_i^2}{8R}\cos(\phi), \\ I_i &= M^2\frac{3U_i}{8R}\cos(\phi), \quad \hat{I}_o = M\frac{U_i}{2R}, \end{aligned} \tag{21}$$

where $R = 3\hat{U}_{o,max}^2/2P_{max} = 2.4\,\Omega$. The highest component stresses and semiconductor losses appear at nominal power $P = 1000\,W$, nominal motor voltage $\hat{U}_o = 40\,V$ and unity power factor $\cos(\phi) = 1$. In order to simplify the analysis, the current ripple of the filter inductors L_o is neglected, unless stated otherwise.

First, the component stresses which are independent of the employed modulation strategy (unipolar or unfolder modulation) are derived. The voltage stress on the power semiconductor devices is analysed. All the semiconductor devices of a DB-VSI are blocking and/or switching the fuel-cell voltage U_i. Hence, the maximum fuel-cell voltage $U_{i,max} = 120\,V$ (at no load operating condition), with some additional safety margin dictates the voltage rating of the employed semiconductor devices. For this reason, $200\,V$ rated GaN semiconductor devices are selected.

In a second step, the RMS current stress on the semiconductor devices is calculated

$$\begin{aligned} I_{Ta_1,RMS} &= I_{Ta_2,RMS} = \frac{\hat{I}_o}{\sqrt{2}}\frac{1}{\sqrt{2}} \\ I_{Ta_3,RMS} &= I_{Ta_4,RMS} = \frac{\hat{I}_o}{\sqrt{2}}\frac{1}{\sqrt{2}}. \end{aligned} \tag{22}$$

The above current stress expressions do not depend neither on the modulation strategy, nor on the power factor $\cos(\phi)$. The current stresses are symmetric, i.e. the high-side and the low-side semiconductor devices of each of the employed half-bridges conduct the same RMS current. Hence, the DB-VSI inverter can conduct the nominal motor current $\hat{I}_o$ and torque under any operating condition of the motor, e.g. during motor acceleration, starting from standstill. Assuming that the two VSIs comprising the DB-VSI are identical and based on the RMS current stresses of **(22)**, the resulting total semiconductor devices' conduction losses are

$$P_{cd} = 6\frac{\hat{I}_o^2}{2}R_{T,on}, \tag{23}$$

where $R_{T,on}$ is the on-state resistance of each (unipolar) power semiconductor device. It is reminded, that for the above calculation of the conduction losses, the current ripple of the filter inductors L_o is neglected.

The input capacitance value C_i is now selected. The capacitor C_i conducts the switched input current $i_i(t)$ of the DB-VSI. The worst case current, flowing through the input capacitor over a switching period T_s is $i_i(t) = \frac{1}{2}\hat{I}_o\text{rec}(2\pi f_s t)$ The input capacitor current is in this case rectangular, with 50% duty cycle and has an amplitude of $\hat{I}_o/2$. Accordingly, a high (local) RMS current stress on the input capacitor $I_{C_i,RMS} = \hat{I}_o/2$ results. Based on the rectangular current waveform $i_i(t) = \frac{1}{2}\hat{I}_o\text{rec}(2\pi f_s t)$, the worst case voltage ripple across the input capacitor C_i and/or the fuel-cell is

$$\Delta U_i = \frac{\hat{I}_o}{8 f_s C_i}. \tag{24}$$

Therefore, in order to limit the input voltage ripple to a sufficiently low value ΔU_i the input capacitance must be

$$C_i \geq \frac{\hat{I}_o}{8 f_s \Delta U_i}. \tag{25}$$

The resulting input capacitance value C_i is inversely proportional to the switching frequency f_s and is typically small. It is noted here, that there is no need for low-frequency

energy storage in a balanced three-phase system. In summary, the input capacitor must conduct a high-frequency switched current with a high RMS value $I_{C_\mathrm{i},\mathrm{RMS}}$, while a low capacitance C_i is typically required. Ceramic and film capacitors feature a low series resistance, thus can conduct the high RMS current $I_{C_\mathrm{i},\mathrm{RMS}}$ without generating excessive losses. Therefore, ceramic or film capacitors are suggested for the C_i realization. Ceramic capacitors are in general more compact but more expensive than film capacitors. Therefore, the choice between the two capacitor types depends on the design priority, i.e. low volume or low cost.

A. DB_{II}-VSI Inverter - Unipolar Modulation

The switching losses for the unipolar modulation ($\mathrm{DB_{II}}$-VSI) are now analytically calculated. To this end, the switching energy dissipation E_sw for each hard switching transition of a half-bridge is approximated as a linear function of the commutation current I_sw as

$$E_\mathrm{sw}(I_\mathrm{sw}) = k_0 + k_1 I_\mathrm{sw}. \tag{26}$$

Accordingly, the switching power dissipation for a switching frequency f_s is

$$P_\mathrm{sw}(I_\mathrm{sw}) = f_\mathrm{s} E_\mathrm{sw} = f_\mathrm{s}(k_0 + k_1 I_\mathrm{sw}). \tag{27}$$

The parameters k_0 and k_1 depend on the switched voltage U_sw. Namely the parameter k_0 represents the constant part of the switching losses and is calculated in literature [38] (assuming unipolar power semiconductors) as

$$k_0(U_\mathrm{sw}) = Q_\mathrm{oss}(U_\mathrm{sw}) \cdot U_\mathrm{sw}, \tag{28}$$

where Q_oss is the electric charge stored in the non-linear output parasitic capacitance C_oss of the MOSFET

$$Q_\mathrm{oss}(U_\mathrm{sw}) = \int_0^{U_\mathrm{sw}} C_\mathrm{oss}(u)\mathrm{d}u. \tag{29}$$

The parameter $k_1(U_\mathrm{sw})$ represents the linear, current dependent part of the switching losses, and is specific to the semiconductor technology and the gate driver circuit [39], [40].

Subsequently, the expression **(27)** for the switching losses is applied to the two switched VSIs of the $\mathrm{DB_{II}}$-VSI inverter, where the commutation current varies over time in a sinusoidal fashion. In order to account for the sinusoidal current waveform, an integration of **(27)** over the fundamental period T_o is performed. The resulting sum of the switching losses for all three phases of the $\mathrm{DB_{II}}$-VSI are

$$P_\mathrm{sw}\left(\hat{I}_\mathrm{o}\right) = 6 f_\mathrm{s}\left[k_0 + k_1 \frac{2}{\pi}\hat{I}_\mathrm{o}\right]. \tag{30}$$

The switching losses comprise two components, a constant part $6 f_\mathrm{s} k_0$ which is independent of the converter load and a linear part $6 f_\mathrm{s} k_1 2\hat{I}_\mathrm{o}/\pi$ (proportional to the average value of a sinusoidal current half cycle) which increases linearly with the output current $\hat{I}_\mathrm{o}$ and is used to characterise the load state. The maximum switching losses occur for maximum motor voltage/power. Based on the above calculations, the switching losses are unaffected by the load power factor $\cos(\phi)$. Two alternative modulation strategies, which reduce the overall switching losses of the $\mathrm{DB_{II}}$-VSI are detailed in **Appx. A**.

The passive components of the two DM/CM output filters are now selected. In particular, six inductors L_o and six capacitors C_o are employed in total. For a filter inductor L_o The maximum inductor current ripple amplitude (single-side) $\Delta I_{\mathrm{L_o}}$ is given by **(9)**. Accordingly, in order to limit the current ripple to a maximum value $\Delta I_{\mathrm{L_o}}$ the inductor L_o value should be

$$L_\mathrm{o} \geq \frac{U_\mathrm{i}}{8\Delta I_{\mathrm{L_o}} f_\mathrm{s}}. \tag{31}$$

The maximum occurring voltage ripple amplitude (single-side) $\Delta U_{\mathrm{C_o}}$ at the output filter capacitor C_o is given by **(10)**. Therefore, in order to limit the voltage ripple to a maximum value $\Delta U_{\mathrm{C_o}} \simeq 1\,\mathrm{V}$, which is safe for the motor operation, the capacitance C_o values should be

$$C_\mathrm{o} \geq \frac{U_\mathrm{i}}{64 f_\mathrm{s}^2 L_\mathrm{o} \Delta U_{\mathrm{C_o}}}. \tag{32}$$

The inductor L_o losses are now investigated. In general, there is a direct relation between the inductor losses and the RMS inductor current ripple $\Delta I_{\mathrm{L_o},\mathrm{RMS}}$, as a high RMS current ripple results in a high frequency RMS flux density and hence substantial core losses [41]. In addition, a high RMS current ripple causes high-frequency winding losses due to skin and proximity effect. Therefore, the RMS inductor current ripple $\Delta I_{\mathrm{L_o},\mathrm{RMS}}$ is a reasonable performance indicator for the design of the inductive components and is calculated in the following. The local (instantaneous) RMS current ripple of the half-bridge $\bar{a}_1$ (or $\bar{a}_2$) inductor is

$$\Delta i_{\mathrm{L_o},\mathrm{RMS}}(t) = 4 d_{\mathrm{a_1}}(1 - d_{\mathrm{a_1}}) \frac{U_\mathrm{i}}{8\sqrt{3} L_\mathrm{o} f_\mathrm{s}}. \tag{33}$$

The worst case local RMS current ripple occurs for $d_{\mathrm{a_1}} = 0.5$ and is equal to

$$\Delta I_{\mathrm{L_o},\mathrm{RMS},\mathrm{max}} = \frac{U_\mathrm{i}}{8\sqrt{3} L_\mathrm{o} f_\mathrm{s}}. \tag{34}$$

In order to calculate the global (total) RMS current ripple, an integration of **(33)** over the fundamental period T_o is performed, resulting in a global RMS current ripple of

$$\Delta I_{\mathrm{L_o},\mathrm{RMS}}(M) = \sqrt{\frac{3}{128}M^4 - \frac{1}{4}M^2 + 1} \cdot \frac{U_\mathrm{i}}{8\sqrt{3} L_\mathrm{o} f_\mathrm{s}}. \tag{35}$$

The global RMS current ripple of the inductor is illustrated in **Fig. 12**, while the maximum value occurs for modulation index $M = 0$.

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TABLE III: DB-VSI component stresses, calculated for unipolar and unfolder modulation, at the full-load operating condition of **Tab. I**. Numerical values are derived for the hardware prototype parameters of **Tab. IV** and **V**.

		DB_{II}-VSI		**DB_{I}-VSI**
T_1, T_2, T_3, T_4 Voltage PK		$U_{\mathrm{T}} = 40\,\mathrm{V}$		$U_{\mathrm{T}} = 40\,\mathrm{V}$
T_1, T_2, T_3, T_4 Current RMS	**(22)**	$I_{\mathrm{T,RMS}} = 8.3\,\mathrm{A}$	**(22)**	$I_{\mathrm{T,RMS}} = 8.3\,\mathrm{A}$
Conduction Losses	**(23)**	$P_{\mathrm{cd}} = 8.3\,\mathrm{W}$	**(23)**	$P_{\mathrm{cd}} = 8.3\,\mathrm{W}$
Switching Losses	**(30)**	$P_{\mathrm{sw}} = 13.4\,\mathrm{W}$	**(36)**	$P_{\mathrm{sw}} = 6.7\,\mathrm{W}$
Total Semiconductor Losses		$P_{\mathrm{cd}} + P_{\mathrm{sw}} = 21.7\,\mathrm{W}$		$P_{\mathrm{cd}} + P_{\mathrm{sw}} = 15\,\mathrm{W}$
Efficiency Reduction		$\Delta\eta = -2.2\%$		$\Delta\eta = -1.5\%$
Output Inductor	**(31)**	$L_{\mathrm{o}} = 2.5\,\mu\mathrm{H}$	**(31)**	$L_{\mathrm{o}} = 5\,\mu\mathrm{H}$
PK Current Ripple	**(9)**	$\Delta I_{\mathrm{L_o}} = 6.6\,\mathrm{A}$ (40%)	**(9)**	$\Delta I_{\mathrm{L_o}} = 3.3\,\mathrm{A}$ (20%)
RMS Current Ripple	**(35)**	$\Delta I_{\mathrm{L_o,RMS}} = 2.4\,\mathrm{A}$	**(37)**	$\Delta I_{\mathrm{L_o,RMS}} = 1.2\,\mathrm{A}$
Output Capacitor	**(32)**	$C_{\mathrm{o}} = 4\,\mu\mathrm{F}$	**(32)**	$C_{\mathrm{o}} = 2\,\mu\mathrm{F}$
PK Voltage Ripple	**(10)**	$\Delta U_{\mathrm{C_o}} = 0.7\,\mathrm{V}$ (1.7%)	**(10)**	$\Delta U_{\mathrm{C_o}} = 0.7\,\mathrm{V}$ (1.7%)
Input Capacitor	**(25)**	$C_{\mathrm{i}} = 10\,\mu\mathrm{F}$	**(25)**	$C_{\mathrm{i}} = 10\,\mu\mathrm{F}$
PK Voltage Ripple	**(24)**	$\Delta U_{\mathrm{C_i}} = 0.7\,\mathrm{V}$ (1.7%)	**(24)**	$\Delta U_{\mathrm{C_i}} = 0.7\,\mathrm{V}$ (1.7%)

B. DB_I-VSI Inverter - Unfolder Modulation

In the case of unfolder modulation (DB_I-VSI) only the VSI $[\bar{a}_1, \bar{b}_1, \bar{c}_1]$ is operated with the switching frequency f_{s}. The expression **(27)** for the switching losses is applied to the switching frequency operated VSI $[\bar{a}_1, \bar{b}_1, \bar{c}_1]$. The resulting sum of the switching losses over a fundamental period T_{o} is

$$P_{\mathrm{sw}}\left(\hat{I}_{\mathrm{o}}\right) = 3 f_{\mathrm{s}} \left[k_0 + k_1 \frac{2}{\pi} \hat{I}_{\mathrm{o}}\right]. \tag{36}$$

The second VSI $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$ is operated with the fundamental motor frequency f_{o} and hence exhibits negligible switching losses. Therefore, there is a loss imbalance between the first VSI $[\bar{a}_1, \bar{b}_1, \bar{c}_1]$, which generates both switching and conduction losses, and the second VSI $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$, which generates only conduction losses. The lower overall losses of the second VSI $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$ allow for a smaller heatsink or even no heatsink at all for this VSI [42]. Thanks to the unfolder modulation, the overall switching losses are reduced by 50% compared to the unipolar modulation (DB_{II}-VSI) **(30)**.

Besides the lower switching losses, the unfolder modulation benefits from a simpler filter structure (cf. DB_I-VSI **Fig. 10**) compared to the unipolar modulation (cf. DB_{II}-VSI **Fig. 6**). The VSI $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$ which is operated with the fundamental motor frequency f_{o} can be directly connected to the respective motor terminals $[a_2, b_2, c_2]$. Therefore, only three inductive components L_{o} in total are required, opposed to six inductive components in the case of the DB_{II}-VSI inverter. The two separate inductors per phase of the DB_{II}-VSI **(31)** are combined into a single inductor in the case of the DB_I-VSI. Hence each out of the three DB_I-VSI inductor features double the inductance value compared to each one out of the six DB_{II}-VSI inductors. The DB_I-VSI capacitance C_{o} value is selected to be half compared to the respective value of the DB_{II}-VSI capacitance **(32)**. Thereby, an output filter design with double the inductance but half the capacitance is selected for the case of the DB_I-VSI, which achieves the same overall attenuation as the respective DB_{II}-VSI output filter. Accordingly, the same maximum voltage ripple of $\Delta U_{\mathrm{C_o}} \simeq 1\,\mathrm{V}$ appears across the filter capacitors.

The RMS current ripple stress of the inductor is finally calculated. In order to calculate the global (total) RMS current ripple, an integration of **(33)** over the fundamental period T_{o} is performed. The resulting global RMS current ripple of the DB_I-VSI is

$$\Delta I_{\mathrm{L_o,RMS}}(M) = \sqrt{\frac{3}{8}M^4 - \frac{16}{3\pi}M^3 + 2M^2} \cdot \frac{U_{\mathrm{i}}}{8\sqrt{3} L_{\mathrm{o}} f_{\mathrm{s}}}, \tag{37}$$

and is illustrated in **Fig. 12**.

IV. Experimental Validation

The proposed DB-VSI inverter concept is tested within the fuel-cell application of **Fig. 1** and **Tab. I**. A $10\,\mathrm{kW}$ fuel-cell unit requires a continuous supply of oxygen, which is provided by the $280\,\mathrm{krpm}$ high-speed electric compressor of **Fig. 2**. A motor drive system, directly supplied by the fuel-cell controls the electric compressor. The compressor drive system uses 10% of the fuel-cell power, i.e. $1\,\mathrm{kW}$.

A. Design Procedure

In order to design a DB-VSI inverter, the switching frequency f_{s} must be selected. The previously derived in **Sec. III** component stresses depend on the switching frequency f_{s}, however the switching frequency is till now not explicitly defined. The switching frequency represents a crucial design trade-off. A high switching frequency allows to reduce the volume of the passive components, but at the same time increases the semiconductor switching losses and accordingly requires a larger semiconductor heatsink volume. In order to select an appropriate switching frequency, a multi-objective optimization routine, with respect to inverter efficiency η and power density ρ, is emplyed [44], [45], which assesses the performance of several DB-VSI inverter designs. The optimization routine includes the $200\,\mathrm{V}$ rated EPC2034 GaN semiconductor devices [43], the heatsinks of the semiconductor devices [42], the inductive components L_{o} [41], [46], [47],

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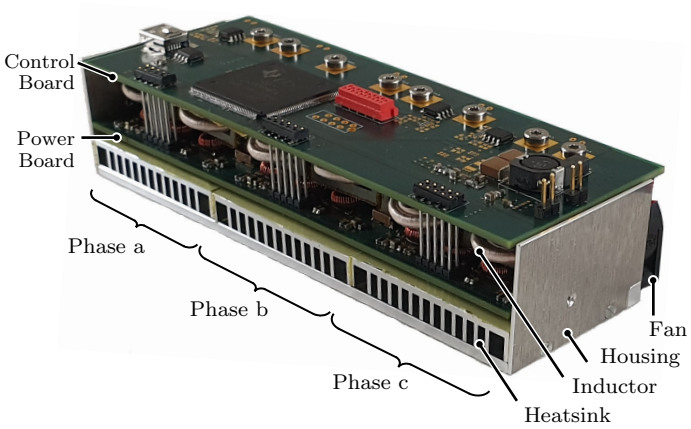

Fig. 14: DB_{II}-VSI inverter (cf. **Fig.6**) hardware prototype employing unipolar modulation. Dimensions $132\,\text{mm} \times 49\,\text{mm} \times 29\,\text{mm}$, power density 5.8 kW/dm^3 (95 W/in^3).

TABLE IV: DB_{II}-VSI hardware prototype parameter values, corresponding to the schematic diagram notation of **Fig. 6**.

DB_{II}-VSI - Unipolar Modulation	
Switching frequency f_s	300 kHz
Switches (2 devices parallel)	200 V EPC 2034
Switching parameters (40 V)	$k_0 = 3.6\,\mu\text{J}$, $k_1 = 0.4\,\mu\text{J/A}$
On-state resistance (100C°)	$R_{\text{T,on}} = 10\,\text{m}\Omega$
Inductance L_o	2.5 µH
Capacitance C_o	4 µF
Capacitance C_i	10 µF

Switching parameters are calculated based on [43].

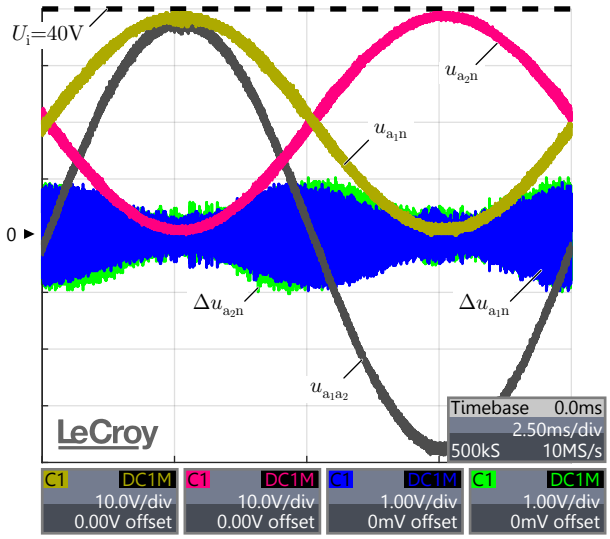

Fig. 15: DB_{II}-VSI inverter experimentally measured waveforms at nominal operating condition $M = 2, P = 1\,\text{kW}$: Motor terminal a_1 (yellow) voltage and (blue) voltage ripple, motor terminal a_2 (red) voltage and (green) voltage ripple, and (grey) phase a motor voltage.

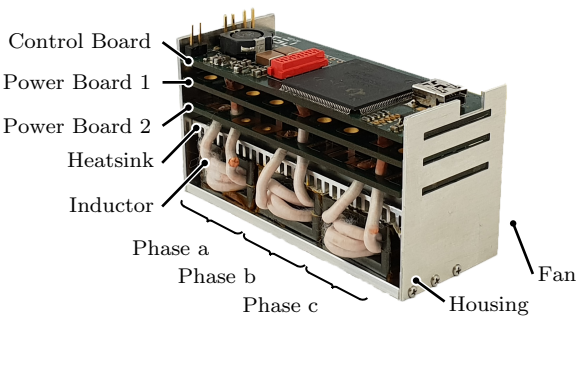

Fig. 16: DB_{I}-VSI inverter (cf. **Fig.10**) hardware prototype employing unfolder modulation. Dimensions $76\,\text{mm} \times 31\,\text{mm} \times 36\,\text{mm}$, power density 13.1 kW/dm^3 (215 W/in^3).

TABLE V: DB_{I}-VSI hardware prototype parameter values, corresponding to the schematic diagram notation of **Fig. 10**.

DB_{I}-VSI - Unfolder Modulation	
Switching frequency f_s	300 kHz
Switches (2 devices parallel)	200 V EPC 2034
Switching parameters (40 V)	$k_0 = 3.6\,\mu\text{J}$, $k_1 = 0.4\,\mu\text{J/A}$
On-state resistance (100C°)	$R_{\text{T,on}} = 10\,\text{m}\Omega$
Inductance L_o	5 µH
Capacitance C_o	2 µF
Capacitance C_i	10 µF

Switching parameters are calculated based on [43].

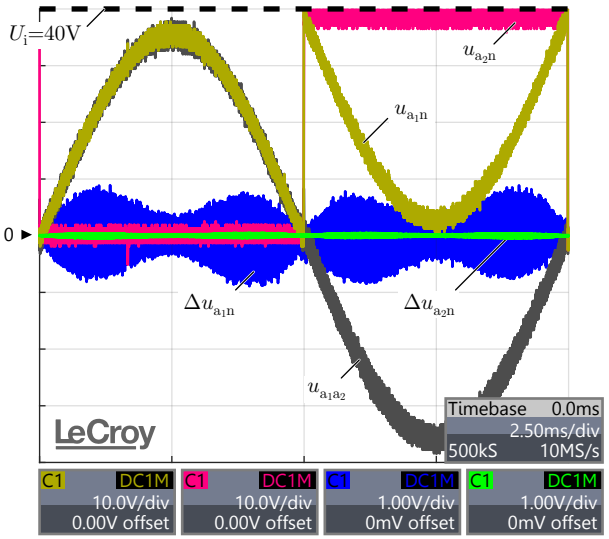

Fig. 17: DB_{I}-VSI inverter experimentally measured waveforms at nominal operating condition $M = 2, P = 1\,\text{kW}$: Motor terminal a_1 (yellow) voltage and (blue) voltage ripple, motor terminal a_2 (red) voltage and (green) voltage ripple, and (grey) phase a motor voltage.

and the ceramic capacitors C_o, C_i. Based on the optimization results, a switching frequency of $f_s = 300\,\text{kHz}$ is selected. The selected benchmark designs for the DB_{II}-VSI and DB_{I}-VSI are given in **Tab. IV** and **Tab. V**, respectively. Using the analytic formulas derived in **Sec. III**, the inverter component stresses are calculated and summarized in **Tab. III**. There, the unipolar and unfolder modulation strategies are compared. Furthermore, the semiconductor losses of the selected DB-VSI, designs, are visualized in **Fig. 13**. The unfolder modulation generates the same semiconductor conduction losses but half switching losses, compared to the unipolar modulation.

Furthermore, **Tab. III** serves as a general design guideline and can be used for motor drive systems with different specifications. After the designer selects an appropriate switching

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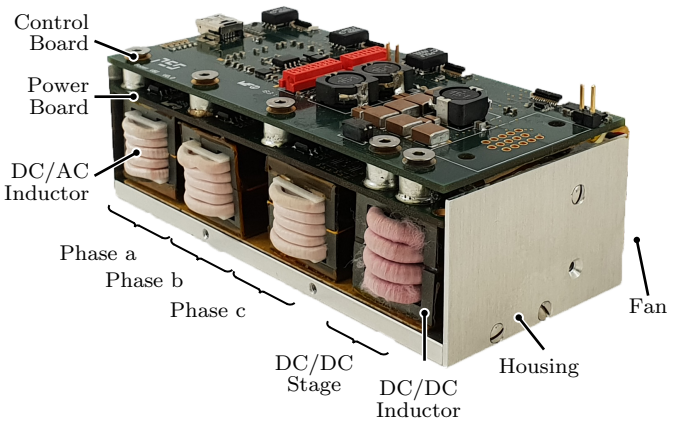

Fig. 18: SB-VSI inverter (cf. **Fig. 5**) hardware prototype. Dimensions $106\,\text{mm} \times 50\,\text{mm} \times 35\,\text{mm}$, power density 6 kW/dm^3 (98 W/in^3).

TABLE VI: SB-VSI hardware prototype parameter values, corresponding to the schematic diagram notation of **Fig. 5**.

SB-VSI - DC/DC stage	
Switching frequency $f_{\text{s,i}}$	300 kHz
Switches (2 devices parallel)	200 V EPC 2034
Switching parameters (80 V)	$k_0 = 11\,\mu\text{J}$, $k_1 = 1.1\,\mu\text{J/A}$
On-state resistance (100C°)	$R_{\text{Ti,on}} = 10\,\text{m}\Omega$
Inductance L_{i}	1.5 µH
Capacitance C_{i}	10 µF
Capacitance C_{DC}	25 µF
SB-VSI - DC/AC stage	
Switching frequency $f_{\text{s,o}}$	300 kHz
Switches (1 device)	200 V EPC 2034
Switching parameters (80 V)	$k_0 = 5.5\,\mu\text{J}$, $k_1 = 1.1\,\mu\text{J/A}$
On-state resistance (100C°)	$R_{\text{To,on}} = 20\,\text{m}\Omega$
Inductance L_{o}	5 µH
Capacitance C_{o}	2 µF

Switching parameters are calculated based on [43].

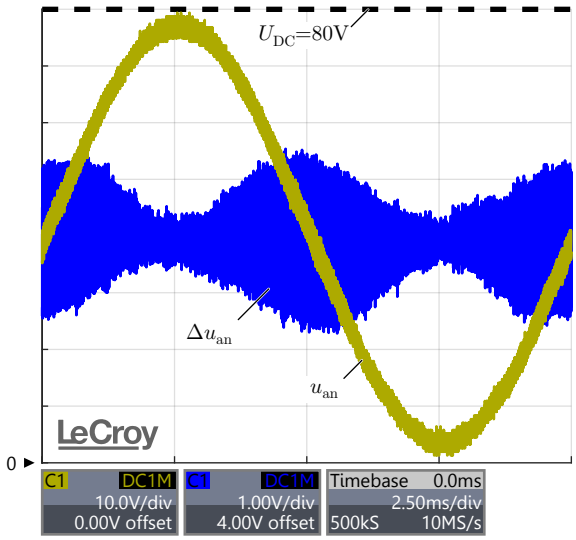

Fig. 19: SB-VSI inverter experimentally measured waveforms at nominal operating condition $M = 2, P = 1\,\text{kW}$: Phase a (yellow) output voltage and (blue) output voltage ripple.

frequency f_{s}, based on his/hers system specifications and the available semiconductor technology, **Tab. III** can be easily used in order to design a DB-VSI inverter.

For the sake of completeness, a conventional SB-VSI (cf. **Fig. 5**) is designed for the specifications of **Tab. I**. The detailed design process of a SB-VSI can be found in [48]. The selected SB-VSI benchmark design, features the same switching frequency of $f_{\text{s}} = 300\,\text{kHz}$, for both the DC/DC stage as well as the DC/AC stage. The SB-VSI component parameters are summarized in **Tab. VI**. The semiconductor losses of the selected SB-VSI design are depicted in **Fig. 13**. It is deduced, that the conventional SB-VSI inverter generates more than double semiconductor losses compared to a DB-VSI solutions, for the same switching frequency f_{s}. There are two main drivers of the high semiconductor losses in the case of the SB-VSI: **(i)** Two-stage energy conversion. The power P is processed twice, first in the DC/DC stage and subsequently in the DC/AC stage. **(ii)** High DC link voltage U_{DC}. The semiconductor devices of both the DC/DC stage and the DC/AC stage process/switch the high DC link voltage.

B. Experimental Results

Three inverter hardware prototypes are assembled:

(i) DB_{II}-VSI (unipolar modulation) of **Fig. 6**. The hardware prototype is shown in **Fig. 14** and the respective component parameters are given in **Tab. IV**.

(ii) DB_{I}-VSI (unfolder modulation) of **Fig. 10**. The hardware prototype is depicted in **Fig. 16** and the component parameters are summarized in **Tab. V**.

(iii) Conventional SB-VSI of **Fig. 5**. The hardware prototype is depicted in **Fig. 18**, while the component parameters are summarized in **Tab. VI**. This hardware serves as the state-of-the-art solution against which the following DB-VSI hardware prototypes will be compared to.

In order to enable a meaningful comparison, all the above hardware demonstrators feature the same switching frequency of $f_{\text{s}} = 300\,\text{kHz}$. In addition, the gate driver circuit of the employed MOSFETs features a dead time of $40\,\text{ns}$, a turn-on gate resistance of $5\,\Omega$ and a turn-off gate resistance of $0\,\Omega$.

First, the performance of the three hardware prototypes is experimentally compared. The conventional SB-VSI hardware prototype achieves a power density of $\rho = 6\,\text{kW/dm}^3$ (including case, cooling system and control electronics) and the lowest efficiency of $\eta = 96\%$ at $P = 1\,\text{kW}$ nominal operation. There are two main reasons behind the SB-VSI low efficiency: **(i)** The SB-VSI features two energy conversion stages (DC/DC stage and DC/AC stage), and thus suffers high losses. **(ii)** The semiconductor devices of both the DC/DC stage and the DC/AC stage have to process/switch the high DC link voltage $U_{\text{DC}} = 80\,\text{V}$, a fact that leads to high switching losses.

The DB_{II}-VSI features in contrast a single energy conversion stage. By employing a unipolar modulation, the DB_{II}-VSI achieves a power density of $\rho = 5.8\,\text{kW/dm}^3$ and a nominal efficiency of $\eta = 97.4\%$. The DB_{II}-VSI is $\Delta\eta = +1.4\%$ more efficient than the SB-VSI for a similar power

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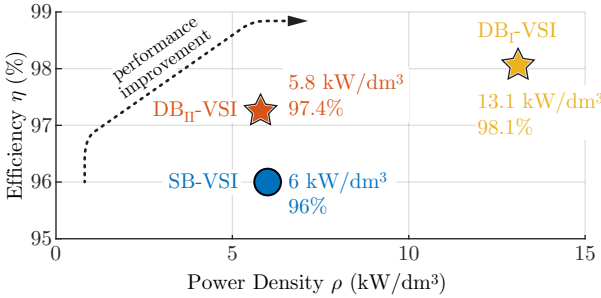

Fig. 20: Performance $[\rho, \eta]$ of (blue) conventional SB-VSI, (orange) DB$_{\text{II}}$-VSI and (yellow) DB$_{\text{I}}$-VSI hardware prototypes.

TABLE VII: Performance summary of the three inverter prototypes.

Inverter	Power Density ρ	Efficiency η
SB-VSI*	6kW/dm^3 (98W/in^3)	96%
DB$_{\text{II}}$-VSI	5.8kW/dm^3 (95W/in^3)	97.4%
DB$_{\text{I}}$-VSI	13.1kW/dm^3 (215W/in^3)	98.1%

*The efficiency is measured for an input voltage of $U_{\text{i}} = 60\,\text{V}$

density. Even though the DB$_{\text{II}}$-VSI features two VSIs (six half-bridges) continuously operated with the switching frequency f_{s} (compared to only four half-bridges for the SB-VSI), the semiconductor devices only process/switch the low nominal fuel-cell voltage of $U_{\text{i}} = 40\,\text{V}$ (compared to the high DC link voltage $U_{\text{DC}} = 80\,\text{V}$ of the SB-VSI). Since the switching losses scale with the square of the commutation voltage, the DB$_{\text{II}}$-VSI, generates lower overall switching losses than the SB-VSI.

The DB$_{\text{I}}$-VSI achieves a very high power density of $\rho = 13.1\,\text{kW/dm}^3$ and the best nominal efficiency of $\eta = 98.1\%$. Compared to the SB-VSI, the DB$_{\text{I}}$-VSI allows to more than double the power density $\Delta\rho = +118\%$, while at the same time increases the efficiency by $\Delta\eta = +2.1\%$. This remarkable performance leap is achieved thanks to the unfolder modulation: **(i)** Only one VSI is continuously operated with the switching frequency f_{s}, while the second VSI is operated with the fundamental motor frequency f_{o}. As a results, the switching losses are kept low. **(ii)** The fundamental frequency operated VSI can be directly connected to the motor, resulting in a simplified and more compact filter configuration. The comparison of the three hardware prototypes performance is summarized in **Fig. 20** and **Tab. VII**, while the whole efficiency profile of the three inverter prototypes is illustrated in **Fig. 21**.

Finally, the motor voltage quality is assessed. Experimentally measured waveforms of the conventional SB-VSI are shown in **Fig. 19**, where a sinusoidal motor phase voltage u_{an} is generated. Superimposed to the motor phase voltage u_{an}, there is a voltage ripple Δu_{an} due to the PWM operation of the half-bridge $\bar{a}$. In particular, the switch-node $\bar{a}$ two-level PWM voltage acquires two voltage values $u_{\bar{\text{a}}\text{n}} = \{0\,\text{V}, 80\,\text{V}\}$ and is processed by a DM/CM output filter ($L_{\text{o}} = 5\,\mu\text{H}, C_{\text{o}} = 2\,\mu\text{F}$). Thanks to the attenuation of the output filter (-31dB at the frequency $f_{\text{s}} = 300\,\text{kHz}$), a worst case voltage ripple value of $\Delta U_{\text{an}} = 1.4\,\text{V}$ is attained.

The DB$_{\text{II}}$-VSI employs a unipolar modulation, while experimentally measured waveforms for phase a are depicted in **Fig. 15**. The DB$_{\text{II}}$-VSI features complementary sinusoidal motor terminals voltages $u_{\text{a}_1\text{n}}$ and $u_{\text{a}_2\text{n}}$, resulting in an also sinusoidal motor phase voltage $u_{\text{a}_1\text{a}_2} = u_{\text{a}_1\text{n}} - u_{\text{a}_2\text{n}}$. In addition, each motor terminal a_1 and a_2 voltage features a voltage ripple $\Delta u_{\text{a}_1\text{n}}$ and $\Delta u_{\text{a}_2\text{n}}$ due to the PWM operation of the respective half-bridges $\bar{a}_1$ and $\bar{a}_2$. Namely, each two-level PWM switch-node $\bar{a}_1$ and $\bar{a}_2$ voltage acquires two voltage values $u_{\bar{\text{a}}_1\text{n}} \equiv u_{\bar{\text{a}}_2\text{n}} = \{0\,\text{V}, 40\,\text{V}\}$ and is possessed by a DM/CM output filter ($L_{\text{o}} = 2.5\,\mu\text{H}, C_{\text{o}} = 4\,\mu\text{F}$). Thanks to the attenuation of the filter (the same -31dB attenuation at the frequency $f_{\text{s}} = 300\,\text{kHz}$ as the SB-VSI), a worst case voltage ripple of $\Delta U_{\text{a}_1\text{n}} = \Delta U_{\text{a}_2\text{n}} = 0.7\,\text{V}$, is attained, on either side of the motor. The worst case voltage ripple stress on phase a motor winding is the sum of the voltage ripple stresses of the respective terminals a_1 and a_2. Therefore, the overall voltage ripple stress in the case of the DB$_{\text{II}}$-VSI is $\Delta U_{\text{a}_1\text{n}} + \Delta U_{\text{a}_2\text{n}} = 1.4\,\text{V}$, which the sane as in the case of the SB-VSI.

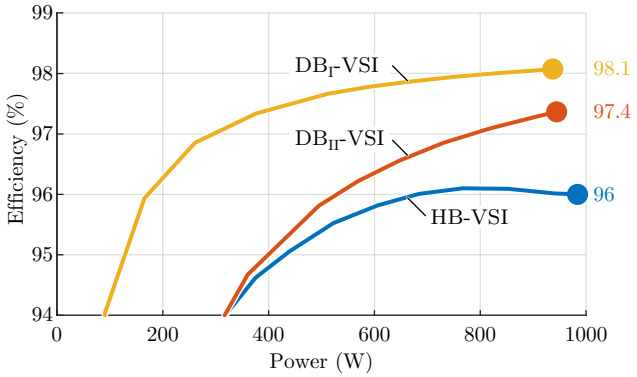

Fig. 21: Efficiency profile of (blue) conventional SB-VSI, (orange) DB$_{\text{II}}$-VSI and (yellow) DB$_{\text{I}}$-VSI. Note that, the efficiency of the SB-VSI is measured for an input voltage of $U_{\text{i}} = 60\,\text{V}$, while the efficiency of the DB-VSIs is measured for $U_{\text{i}} = 40\,\text{V}$.

The DB$_{\text{I}}$-VSI employs an unfolder modulation, while experimentally measured waveforms for phase a are illustrated in **Fig. 17**. The DB$_{\text{I}}$-VSI features discontinuous motor terminals voltages $u_{\text{a}_1\text{n}}$ and $u_{\text{a}_2\text{n}}$, however, the motor phase voltage $u_{\text{a}_1\text{a}_2} = u_{\text{a}_1\text{n}} - u_{\text{a}_2\text{n}}$ is sinusoidal. Only the motor terminal a_1 voltage features a voltage ripple $\Delta u_{\text{a}_1\text{n}}$ due to the PWM operation of the respective half-bridge $\bar{a}_1$, while the motor terminal a_2 voltage features no voltage ripple $\Delta u_{\text{a}_2\text{n}} = 0$ because the respective half-bridge $\bar{a}_2$ is operated with the motor fundamental frequency f_{o}. In particular, the two-level PWM switch-node $\bar{a}$ voltage acquires two voltage values $u_{\bar{\text{a}}_1\text{n}} = \{0\,\text{V}, 40\,\text{V}\}$ and is possessed by an output filter ($L_{\text{o}} = 5\,\mu\text{H}, C_{\text{o}} = 2\,\mu\text{F}$). Thanks to the attenuation of the filter (the same -31dB attenuation at the frequency $f_{\text{s}} = 300\,\text{kHz}$ as the SB-VSI), a worst case voltage ripple of $\Delta U_{\text{a}_1\text{n}} = 0.7\,\text{V}$ appears. The worst case voltage ripple stress on phase a motor winding is $\Delta U_{\text{a}_1\text{n}} + \Delta U_{\text{a}_2\text{n}} = 0.7\,\text{V}$, which is half compared to the respective value for the SB-VSI and/or the DB$_{\text{II}}$-VSI.

Although the DB$_{\text{I}}$-VSI benefits from a lower voltage ripple stress on the motor, it causes a residual CM voltage on the motor windings. In particular, at each discontinuity of the

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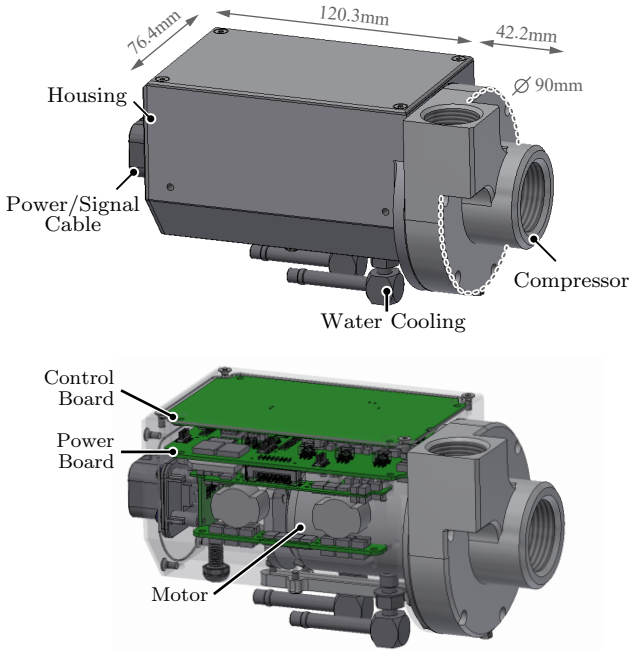

Fig. 22: Integrated high-speed $280\,\mathrm{krpm}$ compressor/inverter prototype, employing DB-VSI technology and designed by Celeroton AG.

motor terminal voltages $u_{\mathrm{a_1n}}$ and $u_{\mathrm{a_2n}}$ of **Fig. 17** a CM $\mathrm{d}u/\mathrm{d}t$ appears on the motor. As illustrated in figure **Fig. 11**, the $\mathrm{DB_I}$-VSI results in a motor CM voltage with rectangular shape and a repetition frequency equal to three time the motor fundamental frequency $3f_\mathrm{o}$. This rectangular LF CM voltage is a disadvantage of the $\mathrm{DB_I}$-VSI, but because of the low repetition frequency of $3f_\mathrm{o}$ it does not compromise the motor reliability over the drive system lifetime.

The DB-VSI technology allows for a performance improvement far beyond the SB-VSI state-of-the-art solution. The choice between the $\mathrm{DB_{II}}$-VSI (unipolar modulation) and $\mathrm{DB_I}$-VSI (unfolder modulation) inverter variants represents a crucial trade-off: The latter $\mathrm{DB_I}$-VSI offers exceptionally high performance, in terms of both efficiency and power density, but results in a residual CM voltage on the motor. In contrast, the former $\mathrm{DB_{II}}$-VSI solution sacrifices some of the performance but achieves a better motor voltage quality, with lower CM $\mathrm{d}u/\mathrm{d}t$. Besides the better performance of the DB-VSI technology compared to conventional SB-VSI solutions, the high DB-VSI power density enables a seamless integration of the inverter in the motor housing [17]–[19]. An integrated inverter-compressor example is depicted in **Fig. 22**. The integration of the inverter further adds to the DB-VSI concept advantages: The open-end winding motor is directly attached to the inverter, eliminating the need for cumbersome and costly shielded motor cables. Finally, the inverter integration adds value for the end user, since the latter receives a complete inverter-motor product and thus is not burdened with the complicated inverter-motor installation.

V. Conclusions

The double-bridge voltage source inverter (DB-VSI) technology is comprehensively analysed in this paper. A DB-VSI comprises two independent VSIs connected to the opposite sides of an open-end winding motor (without neutral point). This inverter topology is an excellent choice for variable-speed motor drive systems, supplied by a fuel-cell (or a battery). The fuel-cell exhibits a wide DC voltage variation, which must be taken into account by the inverter stage. The DB-VSI excellently utilizes its DC input voltage, hence guarantees the full speed/voltage range of the motor, independent of the DC voltage fluctuation of the fuel-cell.

Two DB-VSI inverter variants and/or modulation strategies are comparatively evaluated:
(i) Unipolar modulation strategy of **Fig. 8**. This modulation corresponds to the $\mathrm{DB_{II}}$-VSI variant of **Fig. 6** and the hardware prototype of **Fig. 14**.
(ii) Unfolder modulation strategy of **Fig. 9**. This modulation corresponds to the $\mathrm{DB_I}$-VSI variant of **Fig. 10** and the hardware prototype of **Fig. 16**.
Both DB-VSI variants incorporate an AC output filter in order to protect the motor from $\mathrm{d}u/\mathrm{d}t$ originating from the wide-bandgap semiconductor devices' fast switching transitions. A comparison between the two modulation strategies reveals that the unfolder modulation offers exceptionally high performance, in terms of both efficiency and power density, but results in a residual CM voltage on the motor. In contrast, the unipolar modulation sacrifices some of the inverter performance but completely eliminates the motor CM voltage.

Finally, the DB-VSI topology is compared to the state-of-the-art inverter solution of **Fig. 5**, which features tow energy conversion stages. Compared to the state-of-the-art hardware prototype of **Fig. 18**, the DB-VSI technology achieves a performance leap of $\Delta\eta = +2.1\%$ higher efficiency and $\Delta\rho = +118\%$ higher power density.

Appendix A
Alternative Modulation Strategies

Two alternative modulation strategies that improve the efficiency of the $\mathrm{DB_{II}}$-VSI (cf. **Fig. 6**) are now detailed. First, the hybrid modulation is analysed. This modulation strategy resembles the unfolder modulation of **Fig. 9**, but instead of an abrupt change of the duty cycles $d_{\mathrm{a_1}}$ and $d_{\mathrm{a_2}}$ at $t = T_\mathrm{o}/2$, a soft (gradual) transition takes place. The respective duty cycles of the hybrid modulation are illustrated in **Fig. 23(a)** and are analytically derived

$$d_{\mathrm{a1}} = \begin{cases} d_\mathrm{a}, & d_\mathrm{a} \geq \dfrac{d^*}{2} \\ \dfrac{1}{2} - \dfrac{d_\mathrm{a}}{d^*} + d_\mathrm{a}, & -\dfrac{d^*}{2} \leq d_\mathrm{a} < \dfrac{d^*}{2} \\ 1 + d_\mathrm{a}, & d_\mathrm{a} < -\dfrac{d^*}{2} \end{cases}, \tag{38}$$

$$d_{\mathrm{a2}} = \begin{cases} 0, & d_\mathrm{a} \geq \dfrac{d^*}{2} \\ \dfrac{1}{2} - \dfrac{d_\mathrm{a}}{d^*}, & -\dfrac{d^*}{2} \leq d_\mathrm{a} < \dfrac{d^*}{2} \\ 1, & d_\mathrm{a} < -\dfrac{d^*}{2} \end{cases}, \tag{39}$$

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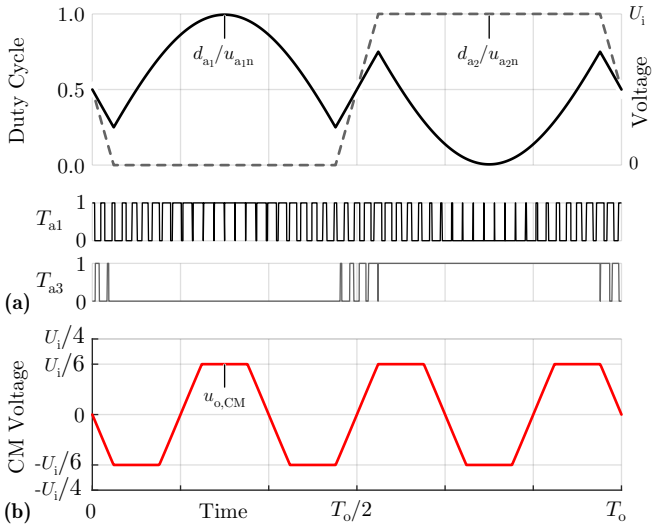

Fig. 23: **(a)** Hybrid modulation: Only half-bridge $\bar{a}_1$ is continuously operated with the switching frequency f_s, while the second half-bridge $\bar{a}_2$ of phase a is operated for a small fraction of the fundamental period with the switching frequency f_s. **(b)** CM voltage on the middle of the motor windings.

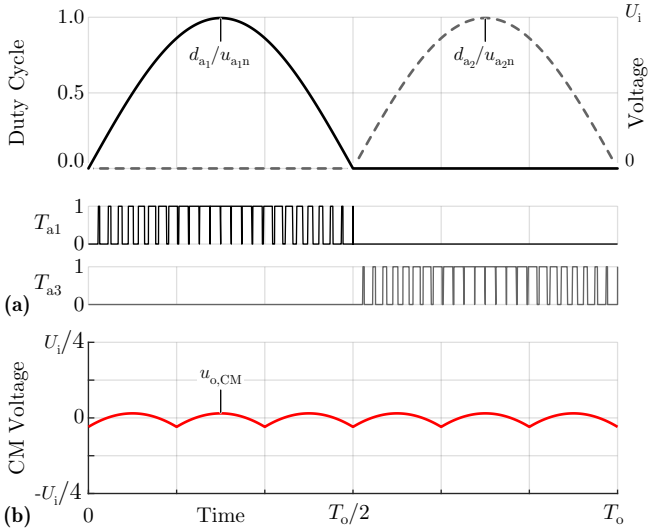

Fig. 24: **(a)** Alternative unfolder modulation: Both half-bridge $\bar{a}_1$ and $\bar{a}_2$ of phase a are partially operated, for half of the fundamental period T_o, with the switching frequency f_s. **(b)** CM voltage on the middle of the motor windings.

where d_a is given in **(4)** and d^* is a design parameter that defines the slope of the soft transition at $t = T_o/2$. According to the hybrid modulation, the VSI $[\bar{a}_1, \bar{b}_1, \bar{c}_1]$ is continuously operated with the switching frequency f_s. The second VSI $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$ is partially operated with the switching frequency f_s, for only a fraction of the fundamental period T_o (around the zero crossing of the motor phase voltage). By reducing the switching transitions of the VSI $[\bar{a}_2, \bar{b}_2, \bar{c}_2]$, the hybrid modulation is able to achieve lower switching losses compared to the unipolar modulation **(30)**. As a result of the hybrid modulation, a CM voltage appears on the motor windings which is visualized in **Fig. 23(b)**. The motor CM voltage is calculated based on the equivalent circuit of **Fig. 7**, has a trapezoidal shape and a repetition frequency equal to three times the fundamental frequency $3f_o$. In summary, the hybrid modulation allows to reduce the switching losses of the unipolar modulation at the expense of a higher CM voltage stress on the motor. It is finally noted, that for a design parameter $d^* = 2$ the hybrid modulation is equivalent to the unipolar modulation of **(3)**, while for $d^* = 0$ the hybrid modulation is equivalent to the unfolder modulation of **(15)**.

Subsequently, the alternative unfolder modulation is described, which is suitable for the DB_{II}-VSI of **Fig. 6**. The sinusoidally shaped duty cycles d_{a_1} and d_{a_2} of **Fig. 24(a)** control the two VSIs and are equal to

$$d_{a1} = \begin{cases} d_a, & d_a \geq 0 \\ 0, & d_a < 0 \end{cases}, \quad d_{a2} = \begin{cases} 0, & d_a \geq 0 \\ -d_a, & d_a < 0 \end{cases}, \tag{40}$$

where d_a is given in **(4)**. Both half-bridge $\bar{a}_1$ and $\bar{a}_2$ of phase a are partially operated with the switching frequency f_s, for half of the fundamental period T_o. The alternative unfolder moudulation resembles the unfolder modulation of **Fig. 9**, in that only three out of the six in total half-bridges are operated with the switching frequency f_s at any given moment in time. However, in contrast to the unfolder modulation, where only half-bridges belonging to the VSI $[\bar{a}_1, \bar{b}_1, \bar{c}_1]$ are continuously operated with the switching frequency f_s, in the case of alternative unfolder modulation both VSIs share an equal amount of switching transitions over the fundamental period T_o. The main disadvantage of the alternative unfolder modulation strategy is the asymmetric RMS current stress it causes on the semiconductor devices. As a result, of the alternative unfolder modulation a CM voltage appears on the motor windings which is visualized in **Fig. 24(b)**. The motor CM voltage is calculated based on the equivalent circuit of **Fig. 7**, has a sinusoidal shape and a repetition frequency equal to six times the fundamental frequency $6f_o$.

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