How to Include the Dependency of the $R_{\mathrm{DS(on)}}$ of Power MOSFET's on the Instantaneous Value of the Drain Current into the Calculation of the Conduction Losses of High-Frequency Three-Phase PWM Inverters

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***Abstract*—In this paper, the conduction losses of power MOSFET's are calculated analytically for application in three-phase voltage dc-link pulsewidth modulation (PWM) converter systems. Contrary to a conventional calculation, the dependency of the turn-on behavior on the drain current is considered in terms of a quadratic approximation. The derived relationships are represented graphically; they can be included directly into the dimensioning of the power transistors.**

***Index Terms*—Conduction losses, on-state resistance of power MOSFET's, voltage dc-link pulsewidth modulation converter.**

I. Introduction

THE on-state resistance of power MOSFET's is influenced not only by the junction temperature T_j and the gate voltage U_{GS}, but, also, by the instantaneous value of the drain current (see, e.g., [1, p. 200]). For dimensioning, this current dependency is neglected; however, in most cases, the on-state power loss is calculated for a current-independent (i.e., only a temperature-dependent) value of the on-state resistance $R_{\mathrm{DS(on)}}$. The on-state losses P_T are determined directly by the product $I_{T,\mathrm{rms}}^2 R_{\mathrm{DS(on)}}$ in this case, where $I_{T,\mathrm{rms}}$ denotes the rms value of the transistor current. In application notes, we can find formulas for the approximate calculation of $I_{T,\mathrm{rms}}$ for the application of MOSFET's in pulsewidth modulation (PWM) converters, dc/dc converters, etc. However, there can be no statement found as to which value of $R_{\mathrm{DS(on)}}$ has to be applied for obtaining the conduction losses and/or which average current could be assumed as characteristic concerning the on-resistance.

Therefore, in this paper, we shall analyze the question as to how the current dependency of the on resistance can be incorporated into the calculation of the transistor on-state losses of a three-phase voltage dc-link PWM converter system. The aim is to determine a current value $I_T = I_T'$ in dependency on the operating parameters of the system which can be applied to read an on resistance which is characteristic for the on-state losses from the characteristic $R_{\mathrm{DS(on)}} = R_{\mathrm{DS(on)}}\{I_T\}$, determined from the data sheets. In Section I, the calculation for the on-state losses for constant (not current-dependent) on-resistance is discussed briefly. This is extended in Section II to the current dependency of the on-state characteristic. Finally, in Section III, the calculated resistances are represented graphically in normalized form, and the procedure for determining the on-state power losses during the dimensioning process is discussed. The physical background for the dependency of the on-state resistance on the drain current is discussed in the Appendix based on a simple model of the power MOSFET.

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II. On-State Power Losses for Constant On Resistance

For the calculation of on-state power losses of a power transistor (power MOSFET) of a three-phase PWM converter, the voltage formation and the conduction states of a bridge leg are to be considered [see Fig. 1(a)]. For further considerations, we assume the following:

- sinusoidal modulation;
- constant pulse frequency of the system (being much higher than the fundamental output frequency);
- purely sinusoidal shape of the phase current i_N.

If, at the output of the bridge leg (on the ac side), a voltage u_U is formed based on PWM which is sinusoidal in its time average

$$u_U^* = \hat{U}_U \sin(\omega_N t + \varphi) \tag{1}$$

there follows for the relative on time α_{T_1} of the power transistor T_1 carrying the phase current

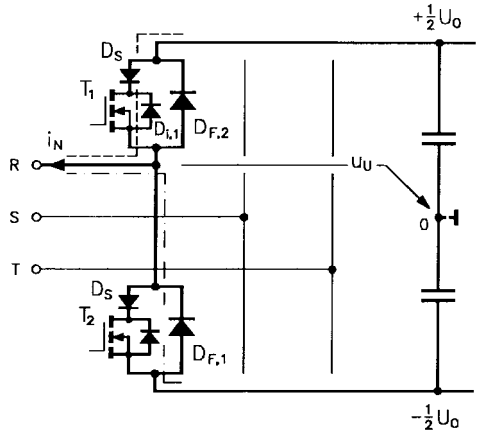
$$i_N = \hat{I}_N \sin \omega_N t \tag{2}$$

within the positive half periods $i_N > 0$

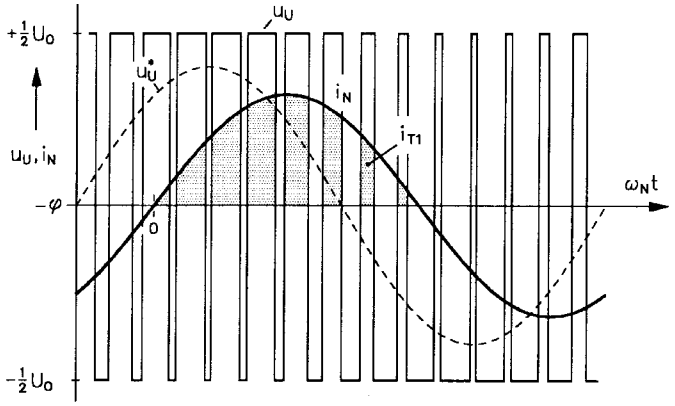
$$\alpha_{T_1} = \frac{1}{2} + \frac{M}{2} \sin(\omega_N t + \varphi) \tag{3}$$

where

$$M = \frac{\hat{U}_U}{\frac{1}{2} U_O} \tag{4}$$



(a)



(b)

Fig. 1. (a) Basic structure of a bridge leg of a three-phase dc voltage link PWM converter system. (b) Time behavior of the (ac side) output voltage u_U, of the local average u_U^* of u_U (i.e., the output voltage fundamental) and of the (idealized) output current i_N of the bridge leg. The transistor current i_{T1} is pointed out by the shaded area.

denotes the modulation depth and U_O the dc-link voltage. φ defines the phase shift between the fundamental (set value) u_U^* of the output voltage u_U (of the bridge leg considered) and of the phase current i_N [see Fig. 1(b)].

For the *local* conduction losses p_{T_1} (the average value of the on-state losses within a pulse period T_P), we have

$$p_{T_1} = \frac{1}{T_P}\int_0^{T_P} i_{T_1}^2\{t_\mu\} R_{\mathrm{DS(on)}}\, dt_\mu \tag{5}$$

where t_μ denotes a local time running within T_P. For the analytical calculation of p_{T_1}, the phase current i_N can be assumed as approximately constant according to the assumption of a pulse frequency being substantially higher than the output frequency. Then, there follows immediately

$$p_{T_1} = \alpha_{T_1} i_N^2 R_{\mathrm{DS(on)}} \tag{6}$$

(within the on time $\alpha_{T_1} T_P$ of T_1 we have $i_{T_1} = i_N$). Based on (6), the *global* conduction losses (related to a mains period T_N) are derived via averaging

$$P_{T_1} = \frac{1}{T_N}\int_0^{T_N/2} p_{T_1} dt. \tag{7}$$

If, contrary to the actual physical conditions (see the Appendix) the dependency of the on resistance $R_{\mathrm{DS(on)}}$ on the current is neglected, we obtain under consideration of (2) and (3)

$$P_{T_1} = R_{\mathrm{DS(on)}} \hat{I}_N^2 \frac{1}{T_N}\int_0^{T_N/2} \left[\frac{1}{2} + \frac{M}{2}\sin(\omega_N t + \varphi)\right] \cdot \sin^2(\omega_N t)\, dt \tag{8}$$

and

$$P_{T_1} = \hat{I}_N^2 \left(\frac{1}{8} + \frac{1}{3\pi} M\cos\varphi\right) R_{\mathrm{DS(on)}} = I_{T,\mathrm{rms}}^2 R_{\mathrm{DS(on)}} \tag{9}$$

(see [2, eq. (54)]) with

$$I_{T,\mathrm{rms}} = \sqrt{\frac{1}{8} + \frac{1}{3\pi} M\cos\varphi}\, \hat{I}_N \tag{10}$$

as the rms value of the transistor current i_{T_1}.

Now, the difficulty of calculating the on-state losses of the transistor T_1 (and/or of the transistor T_2) according to (9) results from the fact that the on-state resistance of a power MOSFET is influenced not only by the junction temperature T_j, but also by the drain current, as shown in the Appendix. Therefore, we have to set for $R_{\mathrm{DS(on)}}$ an average *effective on resistance* $R'_{\mathrm{DS(on)}}$ which considers the sinusoidal variation of i_N (the envelope of i_{T_1}). The calculation of this resistance value is the topic of the following section.

Remark: For the previous calculation, we have assumed that the power transistor T_1 conducts current only during the positive half periods of i_N and not also during the conduction intervals of the parasitic internal freewheeling (body) diode of the power MOSFET T_1 (during the negative half periods). This is justified due to the on-state resistance of a power MOSFET with high blocking voltage capability (see Section IV-A; for converter systems operated at the European low-voltage mains, one has to select a blocking voltage capability of $V_{\mathrm{DSS}} = 1000$ V in typical cases). The on-state resistance limits the current in the transistor part of the device during the conduction interval of the internal parasitic diode to small values. Also, for high pulse frequencies f_P and high dc-link voltage U_O, the body diode of the MOSFET in many cases is replaced by a discrete freewheeling diode $D_{F,2}$ (and a diode D_S connected in series to the transistor), as shown in Fig. 1(a) (see also [3, Fig. 1] or [4, Fig. 11]), completely suppressing the current flow in the MOSFET device within the freewheeling intervals. This practice eliminates the high switching losses caused by the high reverse recovery time of the MOSFET body diode. Reverse recovery time t_{rr}, reverse recovery charge Q_{RM}, and peak recovery current of the body diode lie for $V_{\mathrm{DSS}} = 1000$ V also for power MOSFET's which are optimized with respect to the dynamic properties of the internal diode (HiPerFET [6] or FREDFET [7]) higher by a factor of 3 in typical cases than for discrete fast recovery diodes (see, e.g., [6] and [8]). Therefore, the internal diode is applied in many cases only as a freewheeling diode for blocking voltages V_{DSS} less than about 200 V (see [9, p. 591]).

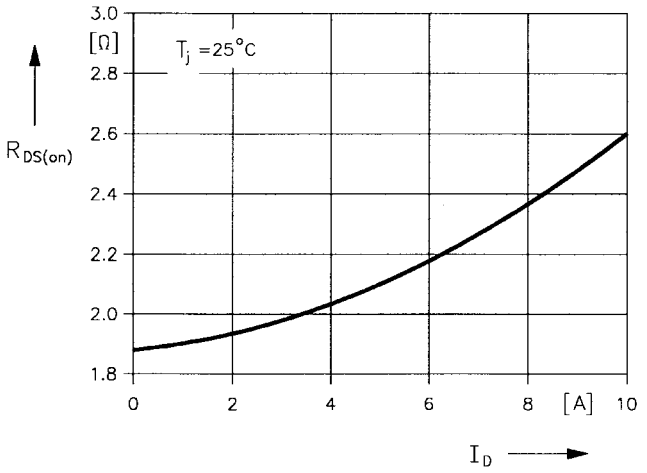


Fig. 2. Dependency of the effective on-state resistance $R'_{\mathrm{DS(on)}}$ of a power MOSFET (IXTH6N90/IXTH5N100, U_{DSS} = 900 V/1000 V, I_{D25} = 5 A/6 A, see [5, p. 39]) being typically employed in a low-power three-phase PWM converter system operated in the European low-voltage mains on the value of the drain current I_{D}. I_{D25} denotes the admissible transistor current for a case temperature of T_{C} = 25 °C; $R_{\mathrm{DS(on),0}}$ denotes the value of the on-state resistance given for $i_T \approx 0$; the dependency of the on-state resistance on the gate-source voltage U_{GS} is pronounced only to a minor extent for $U_{\mathrm{GS}} > 10$ V. Therefore, it can be neglected if one considers the turn-on voltage level being typically in the region $U_{\mathrm{GS,on}} \approx 10$ V $\cdots$ 15 V for practical applications.

III. Conduction Losses for Current-Dependent On-State Resistance

Based on the basic physical properties of a MOSFET (see the Appendix and/or Fig. 2), we use a quadratic relationship

$$R_{\mathrm{DS(on)}}\{i_T\} = (1 + a_1 i_T + a_2 i_T^2) R_{\mathrm{DS(on),0}} \tag{11}$$

as an approximation for the considerations made in the following. The values a_1 and a_2 can be determined easily from the characteristic $R_{\mathrm{DS(on)}} = R_{\mathrm{DS(on)}}\{i_T\}$ given in the data sheet of a MOSFET [see Fig. 2 and (19) and (20)]. With this, there follows for the local average of the on-state losses by extension of (5)

$$\begin{aligned} p'_{T_1} &= \alpha_{T_1} i_N^2 R_{\mathrm{DS(on)}}\{i_N\} \\ &= \alpha_{T_1} i_N^2 (1 + a_1 i_N + a_2 i_N^2) R_{\mathrm{DS(on),0}}. \end{aligned} \tag{12}$$

With (2), (3), and (7), this leads to the global on-state losses of the power transistor

$$\begin{aligned} P'_{T_1} = \hat{I}_N^2 \Bigg[&\frac{1}{8} + \frac{M}{3\pi}\cos\varphi + a_1 \left(\frac{1}{3\pi} + \frac{3M}{32}\cos\varphi \right) \hat{I}_N \\ &+ a_2 \left(\frac{3}{32} + \frac{4M}{15\pi}\cos\varphi \right) \hat{I}_N^2 \Bigg] R_{\mathrm{DS(on),0}}. \end{aligned} \tag{13}$$

Considering (10), there follows, furthermore, that

$$\begin{aligned} P'_{T_1} = I_{T,\mathrm{rms}}^2 \Bigg(1 + a_1 &\frac{\frac{1}{3\pi} + \frac{3M}{32}\cos\varphi}{\frac{1}{8} + \frac{M}{3\pi}\cos\varphi} \hat{I}_N \\ &+ a_2 \frac{\frac{3}{32} + \frac{4M}{15\pi}\cos\varphi}{\frac{1}{8} + \frac{M}{3\pi}\cos\varphi} \hat{I}_N^2 \Bigg) R_{\mathrm{DS(on),0}} \end{aligned} \tag{14}$$

and/or

$$P'_{T_1} = I_{T,\mathrm{rms}}^2 R'_{\mathrm{DS(on)}}. \tag{15}$$

Concerning the on-state losses, there is now an on-state resistance

$$R'_{\mathrm{DS(on)}} = (1 + a_1(b_1 \hat{I}_N) + a_2 (b_2 \hat{I}_N)^2) R_{\mathrm{DS(on),0}} \tag{16}$$

[see (11)] with

$$b_1 = \frac{\frac{1}{3\pi} + \frac{3M}{32}\cos\varphi}{\frac{1}{8} + \frac{M}{3\pi}\cos\varphi} \tag{17}$$

and

$$b_2^2 = \frac{\frac{3}{32} + \frac{4M}{15\pi}\cos\varphi}{\frac{1}{8} + \frac{M}{3\pi}\cos\varphi} \tag{18}$$

in effect which is dependent on modulation depth M, fundamental power factor $\cos\varphi$, and mains current amplitude $\hat{I}_N$.

IV. Dimensioning Procedure Under Consideration of the Current Dependency of the On-State Resistance

If the current dependency of the on-state resistance is described only by a linear approximation [i.e., $a_2 = 0$ in (11)], one can determine the effective on resistance $R'_{\mathrm{DS(on)}}$ (which is required for the calculation of the on-state losses) directly from the characteristic $R_{\mathrm{DS(on)}} = R_{\mathrm{DS(on)}}\{I_T\}$ given in the data sheet of a power MOSFET. There, one has to use the resistance value $R'_{\mathrm{DS(on)}}$ which is associated with the current $I'_T = b_1 \hat{I}_N$.

If a quadratic relationship is considered, we have to apply correction factors b_1 and b_2, which are associated with a given operating point M and $\cos\varphi$ from the graphical representation of (17) and (18) (see Fig. 3). Via (16), we then can calculate, in a simple way, the effective on-state value $R'_{\mathrm{DS(on)}}$, which is related to a defined mains current amplitude $\hat{I}_N$.

As Fig. 3 shows, b_1 and b_2 show an approximately constant value $b_1 \approx b_2 \approx 0.87$ for wide regions. Only for high modulation depth and energy supplied to the dc link (PWM *rectifier* operation), a lower stress on the transistors by conduction losses results, because then the current flow takes place mainly in the freewheeling diodes (see [2, Fig. 8]). With this, a simplification of the calculation can be made for *inverter* operation by application of an effective on-state resistance which is related to the current value $I'_T \approx 0.87 \hat{I}_N$, giving an upper limit for the determination of the transistor conduction losses.

A. Dimensioning Example

The application of the relations derived in Section III shall be shown, in the following, for a practical dimensioning example.

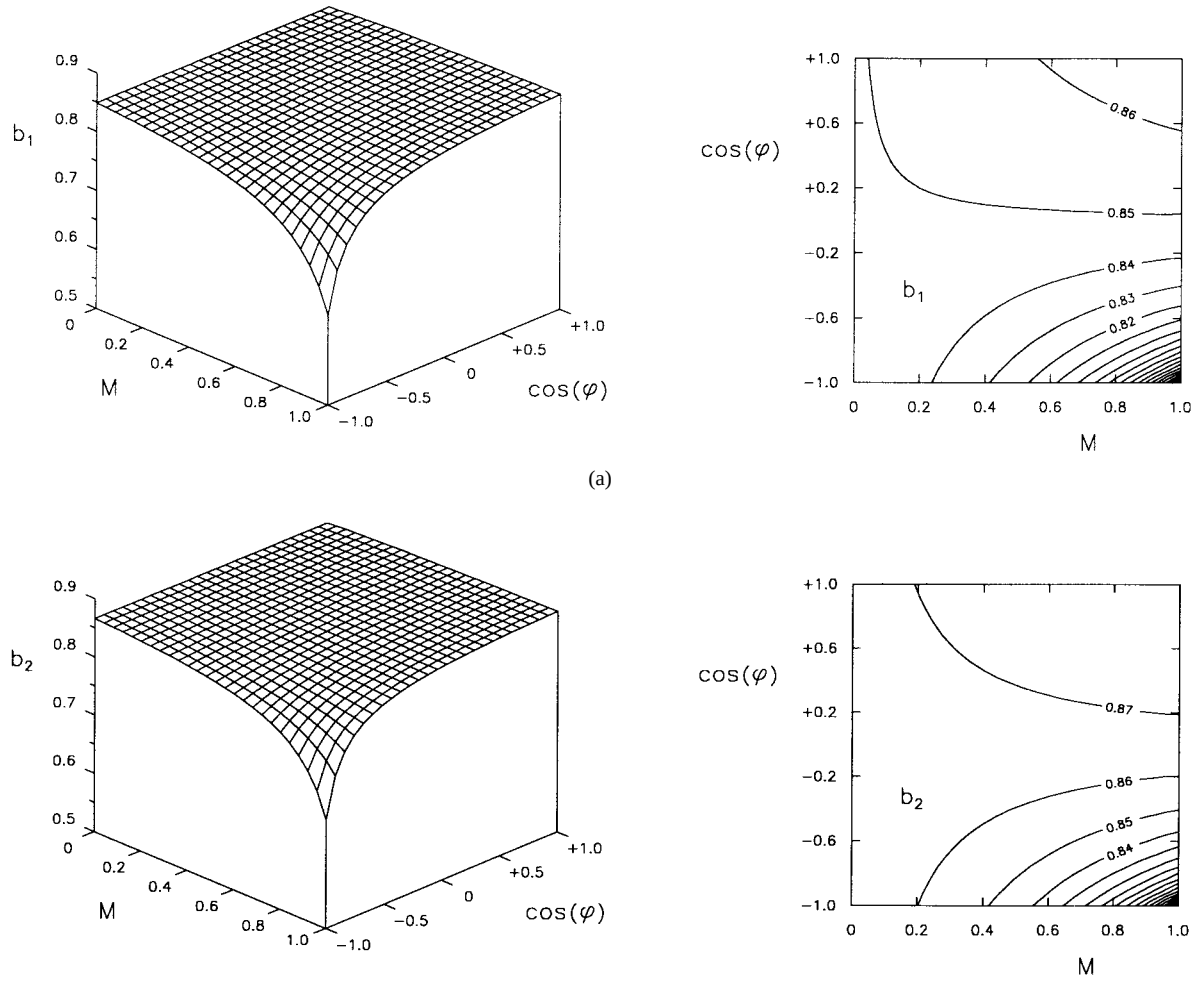


Fig. 3. Dependency of the correction factors: (a) b_1 [see (17)] and (b) b_2 [see (18)] required for the calculation of the effective on-state resistance $R'_{\mathrm{DS(on)}}$ according to (16) on the modulation depth M and on the fundamental power factor $\cos\varphi$.

The task shall be to calculate the on-state losses of a power MOSFET IXTH5N100 for

$$\hat{I}_N = 10\,\mathrm{A}$$
$$\cos\varphi = 0.7$$
$$M = 0.9$$
$$T_j = 110\,^{\circ}\mathrm{C}.$$

This operating point is typical for the application of the transistor in a voltage dc-link PWM inverter structure. The dependency of the on-state resistance of the power MOSFET on the current is shown in Fig. 2.

Remark: The junction temperature T_j is determined by the total conduction and switching losses of the transistor. For the sake of clarity, this will be not treated in detail here. Instead, $T_j = 110\ ^{\circ}\mathrm{C}$ is assumed directly.

The calculation has to be performed in the following steps:

1) determination of $R_{\mathrm{DS(on)},0}$ and of the coefficients a_1 and a_2 of the quadratic approximation (11) of the relationship $R_{\mathrm{DS(on)}} = R_{\mathrm{DS(on)}}\{I_T\}$, according to Fig. 2;
2) determination of b_1 and b_2 according to (17) and (18) or according to Fig. 3(a) and (b);
3) calculation of the effective on-state resistance $R'_{\mathrm{DS(on)}}$ according to (16);
4) calculation of the on-state resistance for the actually given junction temperature (Fig. 2 is based on a junction temperature of $T_j = 25\ ^{\circ}\mathrm{C}$);
5) calculation of the rms value of the transistor current according to (10) and, finally, of the on-state losses according to (15).

The value of $R_{\mathrm{DS(on)},0}$ can be taken directly from Fig. 2; there follows

$$R_{\mathrm{DS(on)},0} = 1.88\,\Omega.$$

For the calculation of a_1 and a_2 the pairs of characteristic parameters $i_{T,1}/R_{\mathrm{DS(on)},1} = 10\ \mathrm{A}/2.6\ \Omega$ and $i_{T,2}/R_{\mathrm{DS(on)},2} = 5\ \mathrm{A}/2.1\ \Omega$ (see Fig. 2) are applied. By insertion into (11) and rearranging the resulting relations

$$a_1 = \frac{1}{i_{T,2}} \frac{\dfrac{i_{T,2}^2}{i_{T,1}^2}\left(\dfrac{R_{\mathrm{DS(on)},1}}{R_{\mathrm{DS(on)},0}} - 1\right) - \left(\dfrac{R_{\mathrm{DS(on)},2}}{R_{\mathrm{DS(on)},0}} - 1\right)}{\left(\dfrac{i_{T,2}}{i_{T,1}} - 1\right)} \quad (19)$$

and

$$a_2 = \frac{1}{i_{T,1}^2} \frac{\frac{i_{T,1}}{i_{T,2}}\left(\frac{R_{\mathrm{DS(on)},2}}{R_{\mathrm{DS(on)},0}} - 1\right) - \left(\frac{R_{\mathrm{DS(on)},1}}{R_{\mathrm{DS(on)},0}} - 1\right)}{\left(\frac{i_{T,2}}{i_{T,1}} - 1\right)} \quad (20)$$

the following results are obtained:

$$a_1 = 0.00851\ \mathrm{A}^{-1}$$
$$a_2 = 0.000\,298\ \mathrm{A}^{-2}.$$

Application of (17) and (18) yields, furthermore,

$$b_1 = 0.8609$$
$$b_2 = 0.8760.$$

This leads to the effective on-state resistance (for $T_j = 25\ ^\circ\mathrm{C}$) according to (16)

$$R'_{\mathrm{DS(on)}}|_{T_j=25\ ^\circ\mathrm{C}} = 2.45\ \Omega.$$

(As mentioned before, this value could be taken also directly from Fig. 2 with sufficient accuracy for $i_T \approx 0.87\hat{I}_N = 8.7$ A.)

If one would assume $I_{T,\mathrm{rms}}$ to be characteristic for the on-state resistance (as might look obvious for a superficial consideration), i.e., if the value of $R_{\mathrm{DS(on)}}$ associated with

$$I_{T,\mathrm{rms}} = 4.38\ \mathrm{A}$$

[see (10)] would be taken from Fig. 2, there would follow

$$R_{\mathrm{DS(on)}}|_{T_j=25\ ^\circ\mathrm{C}} = 2.06\ \Omega$$

(this is shown only to demonstrate inaccuracy). Now, for $T_j = 110\ ^\circ\mathrm{C}$ the on-state resistance has to be increased by a factor of 1.75 according to the data sheet; then, there results

$$R'_{\mathrm{DS(on)}}|_{T_j=110\ ^\circ\mathrm{C}} = 4.29\ \Omega$$

and with this we finally obtain for the on-state losses

$$P'_T = 82.2\ \mathrm{W}.$$

If one would use for the calculation of the losses the value of the on-state resistance for $I_{T,\mathrm{rms}}$ ($R_{\mathrm{DS(on)}}|_{T_j=25\ ^\circ\mathrm{C}} = 2.06\ \Omega$ or $R_{\mathrm{DS(on)}}|_{T_j=110\ ^\circ\mathrm{C}} = 3.6\ \Omega$, respectively) and if the current dependency of the on-state resistance would not be considered, on-state power losses of

$$P_T = 69.1\ \mathrm{W}.$$

would follow. The resulting error of ≈16% as compared to the actual losses P'_T, which would increase the dimensioning uncertainity substantially, can be avoided with a minor calculation effort, as shown.

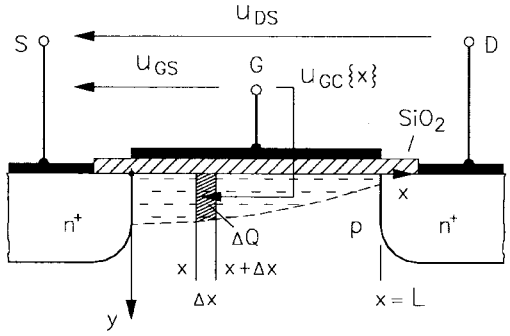


Fig. 4. Cross section through a lateral n-channel MOSFET structure; D drain, S source, G gate, C conductive channel between drain and source for $U'_{\mathrm{GS}} > 0$ formed by free electrons (also called inversion layer because the n-conductivity of the channel is inverse with respect to the basic p-doping of the substrate).

V. Conclusions

In this paper, a simple procedure has been given for consideration of the current dependency of the on-state resistance for dimensioning of power MOSFET's as applied in PWM converter systems.

It is shown that the effective on-state resistance within a wide operating region (characterized by the modulation index M and phase shift φ between the fundamentals of the output current i_N and the fundamental of the output voltage u_U of a bridge leg) is defined by a current value $I'_T \approx 0.87\hat{I}_N$ greater than the rms value of the output current $I_{N,\mathrm{rms}} \approx 1/\sqrt{2}\hat{I}_N \approx 0.7\hat{I}_N$. This is true despite the current flow in the power transistor which is: 1) limited to half a fundamental period and 2) has only a rectangular pulse shape. Therefore, it is not valid for inverter operation to apply the resistance value related to $I_{T,\mathrm{rms}}$, as one could possibly assume without a detailed analysis of the problem.

Appendix

In the following, we will try to give a clear explanation for the physical background of the dependency of the on-state resistance of a MOSFET on the value of the drain current. For the sake of clarity, a very much simplified model is used. In particular, the consideration is limited to the channel of the transistor. Therefore, the contribution of the drift region (being essential especially for power MOSFET's with high blocking voltage) to the on-state resistance (see [9, p. 588, Fig. 22-15]) is not considered. Furthermore, a lateral (see Fig. 4) transistor structure (and not a vertical, as being characteristic for power MOSFET's) is considered. In spite of these facts, the device behavior is described qualitatively correctly by the selected model.

In Fig. 4, a cross section of a lateral n-channel MOSFET structure is shown. The p-doped substrate extends up to the SiO_2 gate isolation. Drain and source are formed by two highly n-doped islands. If the gate-source voltage, $U_{\mathrm{GS}} = 0$, and a positive drain–source voltage, U_{DS} is applied, no drain current will flow because there exists no continuous n-conducting region between the n^+-doped drain and source islands.

Only by application of a sufficiently high positive gate-source voltage $U_{GS} > U_{GS(th)}$ will free electrons gather at the isolator/semiconductor junction, due to the electrical field (see [9, p. 577, Fig. 22-5]. This results in the formation of a very thin n-conducting channel. The gate-source voltage being just necessary for forming this inversion channel is called threshold voltage $U_{GS(th)}$. For the part of the gate voltage exceeding $U_{GS(th)}$ (the effective gate voltage), we use

$$U'_{GS} = U_{GS} - U_{GS(th)} \tag{21}$$

in the following.

If a small drain–source voltage U_{DS} is now applied, a drain current I_D results if $U'_{GS} > 0$. Then, the channel is seen as (ohmic) resistance $R_{DS(on)}$ connecting the drain and source regions. If U_{DS} is increased further, an increase of I_D will follow. However, the ratio between U_{DS} and I_D deviates increasingly from the constant on-state resistance as given for small values of U_{DS} (and/or for small currents I_D). This is due to the fact that the voltage U_{GC} across the oxide layer and, therefore, also the thickness of the inversion layer are reduced in the direction of the x axis according to $U_{GC}\{x\} = U_{GS} - U_{CS}\{x\}$ (see Fig. 4). This reduction in the direction of the x axis, in turn, is caused by the voltage drop $U_{CS} = U_{CS}\{x\}$ (channel-to-source voltage) in the direction of the channel (coordinate x) due to the current flow. This (current-dependent) reduction of the thickness of the inversion layer leads to an increase of the effective channel resistance and, therefore, also of the total on-state resistance of the power MOSFET with increasing drain current.

This explanation of the current dependency of the on-state resistance $R_{DS(on)} = R_{DS(on)}\{I_D\}$ (on which this paper is based), of a MOSFET, can also be based on a mathematical treatment in a simple manner, as shown in the following.

C_G shall denote the gate-channel capacitance and $x = L$ the length of the channel of a MOSFET cell, as shown in Fig. 4. For the capacitance of a part of the channel of infinitesimal length dx one can write then

$$dC = C_G \frac{dx}{L}. \tag{22}$$

For the electrical charge determining the current flow in the part dx of the channel there follows then

$$\begin{aligned} dQ &= dC(U'_{GS} - U_{CS}\{x\}) \\ &= C_G(U'_{GS} - U_{CS}\{x\})\frac{dx}{L} \end{aligned} \tag{23}$$

where U_{CS} describes the dependency on the location of the channel voltage related to the source terminal (as described before). From the field strength in x-direction dU_{CS}/dx and of the charge per length unit dQ/dx one can now determine the channel current which is independent on x (for dc processes the total current I_D is free of sources). With the velocity of the charge carriers

$$v_n = \mu_n \frac{dU_{CS}}{dx} \tag{24}$$

(where μ_n is the electron mobility, assumed constant) we have

$$I_D = \frac{dQ}{dt} = \frac{dQ}{dx}\frac{dx}{dt} = \frac{dQ}{dx}v_n = \frac{C_G}{L}\mu_n(U'_{GS} - U_{CS})\frac{dU_{CS}}{dx}. \tag{25}$$

With the boundary conditions

$$U_{CS}|_{x=0} = 0 \quad \text{and} \quad U_{CS}|_{x=L} = U_{DS} \tag{26}$$

we obtain by integrating (25)

$$I_D \int_{x=0}^{x=L} dx = \mu_n \frac{C_G}{L} \int_{U_{CS}=0}^{U_{CS}=U_{DS}} (U'_{GS} - U_{CS})\, dU_{CS} \tag{27}$$

$$I_D = \mu_n \frac{C_G}{L^2}\left(U'_{GS}U_{DS} - \frac{1}{2}U_{DS}^2\right). \tag{28}$$

The limit of the validity of this relation is reached for almost complete pinchoff of the channel at $x = L$, i.e., for $U_{GD} = U_{GS(th)}$ or $U_{DS} = U'_{GS}$, respectively. For $U_{DS} > U'_{GS}$ the device leaves the resistive region, as being of importance for power electronic applications, and enters the active region of the I_D, U_{DS} plane. Then, I_D will be only dependent on U_{GS}.

For the desired current dependency of the on-state resistance there follows, from (28)

$$R_{DS(on)} = \frac{U_{DS}}{I_D} = \frac{L^2}{\mu_n C_G}\frac{1}{\left(U'_{GS} - \frac{1}{2}U_{DS}\right)} = R_{DS(on)}\{I_D\} \tag{29}$$

(the dependency on U_{DS} can be transferred into a dependency on I_D if (28) is considered). Then, the nonlinear dependency of the on-state resistance on the value of the drain current becomes clear, as being approximated in (16) by a Taylor series of the second order. Thus, the assumption of Ohm's law as being valid for the volume element of length dx [see (24)] is no longer true for the terminal quantities I_D and U_{DS} of the device.

For $U_{DS} \ll U'_{GS} > 0$ (29) can be linearized. According to

$$R_{DS(on)} \approx \frac{L^2}{\mu_n C_G}\frac{1}{U'_{GS}} \tag{30}$$

then the MOSFET represents an ohmic resistance being independent of the current and being controllable by U'_{GS}, as already mentioned in the explanation given above.

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