Novel Single-Phase Buck+Boost PFC Rectifier with Integrated Series Power Pulsation Buffer

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Abstract—This paper introduces a novel integrated series power pulsation buffer (iSPPB) concept for a single-phase AC-to-DC two-switch buck+boost PFC rectifier to compensate the fluctuating power mismatch between the AC input and the DC output. Accordingly, the DC-link capacitance can be drastically reduced and an electrolytic-capacitor-less PFC rectifier system featuring a higher power density and an increased lifetime is obtained. The proposed iSPPB concept consists of a simple full-bridge circuit with a buffer capacitor and is placed in series with the buck-boost inductor, thus no additional inductive component is required for the iSPPB realization. The basic operating principle of the buck+boost PFC rectifier with iSPPB is investigated and the characteristic waveforms are presented. As shown in the analysis, due to the employment of the iSPPB also the maximum buck+boost inductor current is reduced, which compared to the conventional rectifier system without iSPPB allows to further downsize the inductive component. Consequently, the major drawbacks of conventional single-phase PFC rectifiers are eliminated. Furthermore, the control structure is presented and the proper operation is verified based on a closed-loop circuit simulation. Finally, the proposed buck+boost PFC rectifier with iSPPB and a conventional two-switch implementation employing electrolytic capacitors are quantitatively compared by means of simple performance indices.

I. INTRODUCTION

The number of DC loads in industrial applications, e.g. electric vehicle (EV) charging stations [1], data centers [2] or distributed DC buses for variable speed drive systems [3], [4] is continuously increasing. Such loads with a power level of several kilowatts are typically connected to a common DC bus, which is often supplied from a single-phase mains in order to keep the grid interface as simple as possible or to benefit from the advantages of a phase-modular rectifier system [5]. Consequently, a single-phase rectifier with PFC functionality [6], i.e. a rectifier system drawing an input current proportional to the sinusoidal input voltage, is required to convert the single-phase AC input voltage into the DC bus output voltage and to keep the harmonic distortion as well as the reactive power in the grid at a minimum. In addition, in order to enable compatibility with a wide range of DC loads, the DC-link voltage level should be freely selectable, which means that it could be either below or above the grid peak voltage. This wide output voltage range capability is, for example, required for EV battery charging systems in order to cope with the wide variation of the battery voltage [7], and is also beneficial for the aforementioned drive applications, as the DC-link voltage can be decreased at low speeds reducing the switching losses of the subsequent inverter and leading to an overall efficiency improvement [8].

All these requirements can be accomplished e.g. by means of a buck+boost PFC rectifier [9], [10], whose two-switch implementation [11] is shown in Fig. 1(a). Advantageously, to step the DC-link voltage up or down, this structure can be operated in exclusive buck or boost mode, where either only the buck or only the boost half-bridge is high-frequency modulated [12].

However, as common to all single-phase PFC converters, the unity power factor operation leads to a pulsating input power $P_G$ with twice the mains frequency $2f_G$, while at the output mainly a constant power $P_N$ is drawn by the DC load. Hence, the instantaneous power mismatch between the input and the output power has to be buffered somewhere. This is typically done by employing large DC-link capacitors, usually electrolytic capacitors in the mF-range (for rated rectifier output power in the kW-range), which are either absorbing the excessive input energy or delivering the excessive output energy [13]. Consequently, this results in a certain DC-link voltage ripple $\Delta v_{PNP}$, which is often limited to a certain percentage of the average DC-link voltage $v_{PN}$. A lower voltage ripple can be achieved by installing a DC bus buffer capacitance, which further increases the volume and the cost of the system. Furthermore, as shown in the literature [14], [15], electrolytic capacitors also limit the converter lifetime.

In the course of the Google Little Box Challenge [16], [17] various active power pulsation buffer (PPB) concepts have been proposed, from which e.g. the parallel PPB [18], [19] and the series PPB [20], [21] would also be applicable for the buck+boost PFC rectifier. However, besides the buffer capacitor and the additional half- (or full-) bridge, these concepts also require an additional inductive component, which is unfavorable especially concerning volume and costs. In the literature [22], [23] also PPB concepts without an additional inductor, i.e. integrated into a boost-type PFC rectifier are proposed, however, to also step down the DC-link voltage below the peak AC input voltage a subsequent buck converter is needed, introducing another magnetic component.

Therefore, in this paper an integrated series PPB (iSPPB) concept for a single-phase two-switch buck+boost PFC rec-
A rectifier is proposed, which covers the inherent input power pulsation of the single-phase grid by means of a controllable source in series to the buck-boost inductor. The iSPPB is implemented as asymmetric full-bridge with DC side buffer capacitor as shown in Fig. 1(b). The full-bridge of the iSPPB could be also implemented with four switches, however, due to the unidirectional power flow defined by the input diode rectifier as well as the asymmetric buck-boost bridges also the inductor current is unidirectional, thus only two switches are needed. In contrast to the large DC-link capacitor which has to maintain the DC-link voltage rather constant, a large voltage ripple of the buffer capacitor can be accepted which means that the input power pulsation can be covered with a significantly smaller buffer capacitance value and/or capacitor volume. Accordingly, the needed output capacitance is drastically reduced and as a result of the adopted modulation scheme, a lower maximum inductor current and a more compact inductor realization is obtained.

In literature, the proposed iSPPB structure was already used, e.g. to implement an ideal smoothing inductor in the context of a passive three-phase bridge rectifier [24], where the iSPPB has to buffer a power pulsation with six-times the mains frequency. The symmetric iSPPB with four switches was also employed on the AC-side of a three-phase wind energy conversion system [25], where in series to each phase one buffer is inserted in order to compensate the reactive power demand due to the generator inductance and/or to increase the maximal transferable power. Moreover, the unipolar implementation of the buffer structure, i.e. only one half-bridge with a capacitor, was employed in a cycloconverter-based single-phase rectifier [26]. Most similar to this paper, the proposed iSPPB is utilized in a single-phase buck-type rectifier [27], where the circuit clearly benefits from the advantages of the iSPPB, however, its output voltage range is limited to only half of the peak input voltage. In contrast, the two-switch buck-boost PFC rectifier proposed in this paper, enables a wide output voltage range only limited by the maximum blocking voltage of the used semiconductors and therefore also benefits from the iSPPB, i.e. shows a smaller output capacitor volume and a much lower inductor peak current. Furthermore, due to the synergistic control with seamless transition between buck and boost operation, the efficiency in both cases is kept high, since only either the buck or the boost stage is high-frequency pulse width modulated.

In Section II, the operating principle and the characteristic waveforms of the proposed rectifier topology with the iSPPB are investigated. Subsequently, the control structure implementing the PFC and the iSPPB operation is explained in Section III, and the proper operation of the system is verified in Section IV for a 8 kW PFC rectifier system with closed loop control using circuit simulations. Finally, in Section V, the proposed system is evaluated and compared to the conventional implementation by means of simple performance indices. Section VI summarizes the main findings of the work and gives an outlook towards future research.

II. iSPPB OPERATING PRINCIPLE

In the following, first the operating principle of the conventional two-switch buck-boost PFC rectifier (cf. Fig. 1(a)) is shortly explained, which serves as a basis for a clear understanding of the iSPPB operating principle. The conventional single-phase two-switch buck-boost PFC is operated from the single-phase grid \( v_G \) with voltage amplitude \( \hat{v}_G \) and frequency \( f_G \), i.e. \( v_G = \hat{v}_G \cdot \cos 2\pi f_G \). In order to consider the most general case, \( v_{PN} \) is assumed to be lower than \( \hat{v}_G \) as shown in Fig. 2(a), since in this case the rectifier has to be operated in buck (BU) and boost (BO) mode within one mains half period (cf. Fig. 2(b)). In both operating modes, the buck-boost PFC rectifier is able to draw a sinusoidal input current \( i_G \), which is proportional and in phase to the grid voltage \( v_G \), while the DC-link draws the local average load current \( \langle i_{PN}\rangle_{T_{SW}} = \int_{t_0}^{t_0 + T_{SW}} i_{PN}(\tau) d\tau \), which is almost constant during steady-state, i.e. \( \langle i_{PN}\rangle_{T_{SW}} = i_{PN} \).

If the rectified voltage \( v_R \approx |v_G| \) is smaller than the DC-link voltage \( v_{PN} \), the buck-boost converter has to be operated in boost mode (BO), which means that the buck transistor \( T_A \) is continuously turned on (\( d_A = 1 \)) and only the boost stage is high-frequency (HF) pulse width modulated. Hence, this operation mode actually equals the operation of a conventional boost PFC rectifier, where the duty cycle \( d_B \) for the boost stage is directly derived from the voltage ratio between \( v_R \) and \( v_{PN} \), resulting in a voltage modulation index of \( m_N = v_R/v_{PN} \) (cf. Fig. 2(b)). Furthermore, in order to achieve unity power factor operation, the current \( i_R \) is controlled to be proportional to the rectified voltage \( v_R \), which means that \( i_R \) equals the
rectified input current $i_G$. In the boost mode, where $T_A$ is continuously turned on and thus $i_R$ equals the inductor current $i_L$, the inductor current $i_L$ has to be controlled to be equal to the rectified input current $i_G$ (cf. Fig. 2(b)).

As soon as the rectified voltage $v_R$ exceeds the DC-link voltage $v_{PN}$, the buck+boost converter has to switch to the buck mode (BU), where now the boost transistor $T_B$ is continuously turned off ($d_B = 0$) and only the buck stage with $T_A$ is pulse width modulated. The appropriate buck duty cycle $d_A$ is again derived from the ratio of $v_R$ and $v_{PN}$ (cf. Fig. 2(b)). Furthermore, also during buck operation the current $i_R$ is controlled to be proportional to the rectified voltage $v_R$. However, due to the HF switching of $T_A$, the inductor current $i_L$ is not anymore equal to $i_R$ in buck operation, and thus $i_L$ has to be increased in such a way that still PFC functionality is guaranteed. Hence, the maximum inductor current $i_L$ (equal to twice the average load current $2i_{PN}$) is reached at the grid peak voltage, where both the maximum grid current and the lowest buck duty cycle occur, which mainly defines the dimensioning of the inductor. Consequently, the modulation scheme, i.e. either only buck or only boost operation, is directly deduced from the momentary ratio of the rectified input voltage $v_R$ and the output voltage $v_{PN}$, further denoted as voltage conversion approach.

As shown in Fig. 2(b), the unity power factor operation leads to a pulsating input power with twice the mains frequency $2f_G$, while at the output the DC load draws a constant power. In the conventional PFC rectifier, this instantaneous power mismatch is typically covered by employing a large DC-link capacitor $C_{PN}$, however, still causing a DC-link voltage variation of

$$\Delta v_{PNp} = \frac{\bar{P}_{PN}}{\omega_G} - \frac{1}{\bar{v}_{PN}C_{PN}}$$

with $\omega_G = 2\pi f_G$, which typically must be limited to a certain percentage of the average DC-link voltage $\bar{v}_{PN}$ and thus results in a large capacitance value $C_{PN}$.

Instead of using a large DC-link capacitor, in the proposed PFC buck+boost rectifier topology (cf. Fig. 1(b)), the power mismatch is covered by the iSPPB and only the average input power $\bar{P}_{PN}$ is transferred to the output. Consequently, the DC-link capacitor $C_{PN}$ does not have to cover any low-frequency current or power mismatch and therefore $C_{PN}$ can be very small. Assuming a lossless converter system ($\bar{p}_G = \bar{p}_{PN}$), the input current $i_G$, the rectified grid current $i_R$ and the output
current \((i_B)_{T_{SW}}\) can be immediately calculated for a given output power \(P_{PN}\), input voltage \(v_C\) and output voltage \(v_{PN}\) as shown in Fig. 2(c). The DC-link voltage \(v_{PN}\) is again chosen to be below the grid peak voltage \(v_G\).

The iSPPB actually acts as a controllable voltage source which is connected in series to the buck-boost inductor and in the simplest case is realized as an asymmetric full-bridge with a buffer capacitor \(C_C\) (cf. Fig. 1(b)). For the iSPPB basically four conduction paths are possible. In a first case, where both switches \(T_{C1}\) and \(T_{C2}\) are turned off, the inductor current \(i_L\) must flow through the two diodes \(D_{C1}\) and \(D_{C2}\) as well as through the buffer capacitor \(C_C\) in positive direction \((i_{CC} = i_L)\), which means that \(C_C\) is charged, i.e. the excessive input power is stored in the iSPPB. This switching state can also be understood as inserting a positive power pulsation buffer voltage \(v_{PPB} = v_C\) in series to the inductor. On the other hand, if both switches \(T_{C1}\) and \(T_{C2}\) are turned on, the inductor current \(i_L\) is forced through the switches and through the buffer capacitor \(C_C\) in negative direction \((i_{CC} = -i_L)\), thus \(C_C\) is discharged which means that energy which is stored in the iSPPB is transferred to the output, or in other words a negative power pulsation buffer voltage \(v_{PPB} = -v_C\) is added in series to the inductor. In the other two switching states, either only \(T_{C1}\) or only \(T_{C2}\) is turned on which bypasses the capacitor \(C_C\) \((i_{CC} = 0A)\) and therefore no energy is stored or released by the iSPPB. Hence, also no voltage is inserted in series to the buck-boost inductor. The switches of the iSPPB now have to be modulated in such a way that the input power pulsation is fully covered. Advantageously, a full-bridge modulation strategy is used where only one half-bridge is operated with a high switching frequency, while the second half-bridge is used to select the polarity of the inserted power pulsation buffer voltage \(v_{PPB}\). Concerning the buffer capacitor voltage \(v_C\) it should be mentioned that for \(C_C\) the voltage ripple requirement \(\Delta v_{PP,max}\) is much less stringent than for the DC-link capacitor \(C_{PN}\) of the conventional system. In addition, the averaged buffer voltage \(v_C\) is beneficially chosen high enough, since the energy stored in the capacitor is proportional to the voltage squared. Consequently, the buffer capacitance \(C_C\) is much smaller than \(C_{PN}\) and can be realized with e.g. ceramic or foil capacitors.

As already mentioned, the operation principle of the conventional buck-boost PFC rectifier was directly deduced from the momentary ratio of the rectified input voltage \(v_R\) and the output voltage \(v_{PN}\) \((\text{voltage conversion approach})\), however, due to the insertion of the iSPPB the operation of the proposed converter is beneficially explained with the \textit{current conversion} ratio between the rectified current \(i_R\) and the local average output current \((i_B)_{T_{SW}}\). This ratio actually equals the current modulation index

\[
m_l = \frac{i_R}{(i_B)_{T_{SW}}},
\]

which finally defines the operation mode with the corresponding buck duty cycle \(d_A\) and boost duty cycle \(d_B\).

In analogy with a conventional buck+boost PFC converter, in boost mode only the boost half-bridge \((T_{B}, D_{B})\) is HF pulse width modulated and \(T_A\) of the buck half-bridge is continuously turned on \((d_A = 1)\), which means that the inductor current \(i_L\) equals the rectified current \(i_R\). This inductor current \(i_R\) now has to be converted to an output current \(i_{BO}\), whose local average value \((i_B)_{T_{SW}} = (i_{PN})_{T_{SW}}\) due to the PWM operation of the boost half-bridge is always smaller than the inductor current \(i_L\). This is also obvious from the power balance \((i_B)_{T_{SW}} \cdot i_L = (i_{BO})_{T_{SW}} \cdot (i_{BO})_{T_{SW}}\) where a smaller voltage \((i_B)_{T_{SW}}\) is converted in a larger voltage \(v_{PN}\) and therefore the current \((i_B)_{T_{SW}}\) must be smaller than \(i_L\). Consequently, independently of the ratio of the voltages \(v_R\) and \(v_{PN}\), the proposed converter topology is always operated in boost mode \((\text{BO})\), when the rectified input current \(i_R\) is larger than the local average output current \((i_B)_{T_{SW}}\), i.e. \(m_l > 1\) (cf. Fig. 2(c)).

In contrast, during buck mode operation the buck half-bridge \((T_A, D_A)\) is HF pulse width modulated and \(T_B\) is continuously turned off \((d_B = 0)\). The inductor current \(i_L\) is then equal to the output current \(i_B\) instead of the rectified input current \(i_R\). In analogy to the boost mode, this inductor current \(i_L\) now has to result in an input current \(i_A\), whose local average equals the rectified sinusoidal input current \(i_R = (i_A)_{T_{SW}}\) and due to the PWM operation of the buck half-bridge is also always smaller than the inductor current \(i_L\). Again, this can also be deduced from the power balance \(v_R \cdot (i_A)_{T_{SW}} = v_{BO} \cdot (i_{BO})_{T_{SW}}\) and it is found that independent of the voltage ratio \(v_R\) to \(v_{PN}\), the proposed converter topology is always operated in buck mode \((\text{BU})\) when the rectified input current \(i_R\) is \((i_A)_{T_{SW}}\) smaller than the local average output current \((i_B)_{T_{SW}}\), i.e. \(m_l < 1\) (cf. Fig. 2(c)).

Hence, for the proposed topology, the current ratio instead of the voltage ratio defines whether the PFC rectifier is operated in exclusive buck or boost mode. Accordingly, the inductor current \(i_L\) equals the rectified grid current \(i_R\) in case \(i_R > (i_B)_{T_{SW}}\) \((\text{BO})\) and the average load current \((i_{BO})_{T_{SW}}\) in case \((i_B)_{T_{SW}} > i_R\) \((\text{BU})\) and thus, \(i_L\) is always given by the maximum of \(i_R\) and \((i_B)_{T_{SW}}\) \((i.e. i_L = \max(i_R, (i_B)_{T_{SW}}))\), which depending on the operating point is below or at least equal to the maximum inductor current \(i_L\) obtained with the conventional solution (cf. Fig. 2(b)).

Furthermore, the current ratio or modulation index \(m_l\) also directly defines the buck duty cycle \(d_A\) and the boost duty cycle \(d_B\)

\[
d_A = \min(m_l, 1) \in [0, 1]
\]

\[
d_B = 1 - \min\left(\frac{1}{m_l}, 1\right) \in [0, 1]
\]

(cf. Fig. 2(c)), and in turn also determines the ratio between the local average switch node voltage \((v_{BO})_{T_{SW}}\) and the output voltage \(v_{PN}\) during boost mode, or the local average switch node voltage \((v_A)_{T_{SW}}\) and the input voltage \(v_R\) during buck mode. However, in boost mode the local average switch node voltage \((v_{BO})_{T_{SW}}\) is not necessarily equal to the rectified input voltage \(v_a = v_R\), while in buck mode the
local average switch node voltage \( \langle v_A \rangle_{T_{SW}} = d_A v_R \) is not necessarily equal to the output voltage \( v_B = v_{PN} \), which would lead to a resulting local average voltage across the inductor \( L_{BB} \) and thus to a change in the inductor current \( i_L \), e.g. if the iSPPB is bypassed \( v_{PPB} = 0 \) V.

In order to achieve a voltage balance at the inductor’s terminals and to avoid any undesired change in the inductor current, the iSPPB has to insert a voltage \( v_{PPB} \) in such a way that \( \langle v_A \rangle_{T_{SW}} = \langle v_{PPB} \rangle_{T_{SW}} + \langle v_B \rangle_{T_{SW}} \) is fulfilled. Since for both operation modes, the switch node voltages \( \langle v_A \rangle_{T_{SW}} \) and \( \langle v_B \rangle_{T_{SW}} \) are given by the modulation index \( m_t \), the needed iSPPB voltage can directly be calculated as

\[
\langle v_{PPB} \rangle_{T_{SW}} = d_A v_R - (1 - d_B) v_{PN},
\]

and based on the iSPPB capacitor voltage \( v_C \) the overall buffer duty cycle \( d_C \) is given as the ratio

\[
d_C = \frac{\langle v_{PPB} \rangle_{T_{SW}}}{v_C} \in [-1, 1],
\]

as shown in Fig. 3. In addition, the maximum needed iSPPB voltage \( \langle v_{PPB} \rangle_{T_{SW}} \) directly determines the minimum buffer capacitor voltage \( v_C \), since \( v_C \) must always be larger than \( |\langle v_{PPB} \rangle_{T_{SW}}| \) as \( d_C \) is restricted to values between \(-1\) and \(1\).

The worst case operating point is given at the grid voltage zero crossing, where the rectified voltage \( r_R \) is zero and thus the iSPPB has to counterbalance the DC-link voltage \( v_{PN} \), which means that \( v_C \) must always be larger than \( v_{PN} \).

From the overall duty cycle \( d_C \), the duty cycles \( d_{C1} \) and \( d_{C2} \) of the two buffer half-bridges have to be obtained. As can be noted from Fig. 3, the overall duty cycle \( d_C \) oscillates with twice the mains frequency and is in phase with the power pulsation \( p_{CC} \). This is essentially logical, since a positive duty cycle \( d_C \) means that the buffer capacitor \( C_C \) is connected in the positive direction in series to the inductor \( (T_{C1} \) and \( T_{C2} \) are opened) and thus the excessive input power is stored in the iSPPB, while with a negative \( d_C \) the buffer capacitor \( C_C \) is connected in the negative direction in series to the inductor \( (T_{C1} \) and \( T_{C2} \) are closed) and thus transfers stored energy to the output.

Consequently, a possible modulation scheme is to use one half-bridge (e.g. \( T_{C1} \) and \( D_{C1} \) ) to select the polarity of the iSPPB voltage \( \langle v_{PPB} \rangle_{T_{SW}} \), which means that for a positive duty cycle \( d_C \) or positive iSPPB voltage \( \langle v_{PPB} \rangle_{T_{SW}} \) the switch \( T_{C1} \) is permanently turned off \( (d_{C1} = 0) \) and for a negative duty cycle \( d_C \) the switch \( T_{C1} \) is continuously turned on \( (d_{C1} = 1) \). The other half-bridge then has to be HF pulse width modulated in order to control the amount of energy which has to be either released or stored in the iSPPB, whereas its duty cycle is calculated as \( d_{C2} = 1 - d_{C1} - d_C \) (cf. Fig. 3).

Finally, it should be mentioned again that the iSPPB can only buffer the input power pulsation, which is also given by the product of the buffer voltage \( \langle v_{PPB} \rangle_{T_{SW}} \) and the inductor current \( i_L \), and no net power is processed by the iSPPB. This is achieved by the fact that the input and output currents are calculated in such a way that the average input and output power are equal (cf. Fig. 2). Based on the ratio of the currents \( i_R \) and \( \langle i_B \rangle_{T_{SW}} \), then the duty cycles \( d_A \) and \( d_B \) for the buck and boost half-bridge are found.

The duty cycles \( d_{C1} \) and \( d_{C2} \) for the iSPPB are then deduced from the needed iSPPB buffer voltage \( \langle v_{PPB} \rangle_{T_{SW}} \) to eliminate the resulting voltage across the inductor and the capacitor voltage \( v_C \). It also should be mentioned that the time behavior of the capacitor voltage \( v_C \) cannot be controlled, but is a consequence of the input power which has to be buffered and the selected capacitor value \( C_C \). Hence, in theory, the capacitor voltage \( v_C \) will fluctuate around a certain average value \( \bar{v}_C \) if no net power (losses generated in the iSPPB) is drawn from the iSPPB.

### III. Control Structure

In conventional PFC rectifiers typically the output voltage \( v_{PN} \) and the inductor current \( i_L \) have to be controlled [9]. For the proposed converter system this control structure is now extended by a control block keeping the average buffer voltage \( \bar{v}_C \) at its nominal voltage level \( V_C^* \). Furthermore, the control loops of the output voltage \( v_{PN} \) and the inductor current \( i_L \) have to be slightly modified. As illustrated in Fig. 4, the converter control is structured in a cascaded fashion and consists of the three main control blocks, i.e. a DC-Link Voltage Control, a Buffer Voltage Control and a PFC.
Buffer Voltage Control

DC-Link Voltage Control

PFC Modulator and Inductor Current Control

Modulator and Inductor Current Control, which are step by step explained in the following.

A. DC-Link Voltage Control Block

A major objective of a PFC rectifier is to provide a constant output voltage \( v_{PN} \) to the supplied DC load, which is achieved with the DC-Link Voltage Control block. Thereby, the measured DC-link voltage \( v_{PN} \) is compared with the reference DC-link voltage \( V_{PN}^* \), which results in the DC-link voltage error \( \delta v_{PN} \). Then, the DC-link voltage controller \( R_{VPN} \) translates this voltage error into a reference DC-link capacitor current \( i_{CPN}^* \), which should either charge or discharge the DC-link capacitor \( C_{PN} \) to the desired reference DC-link voltage \( V_{PN}^* \). This current \( i_{CPN}^* \) actually equals the needed output current \( i_{CC}^* \) plus the feed-forward value of the load current \( i_{PN,FF} \), which would improve the dynamic behavior of the converter during load steps.

The current \( i_{B}^* \) is then passed to the PFC Modulator and Inductor Current Control block, which on the one hand uses \( i_{B}^* \) to calculate the buck and boost stage duty cycles \( d_A \) and \( d_B \) and on the other hand to determine the reference inductor current \( i_L^* \).

B. Buffer Voltage Control Block

As already mentioned, for the proposed converter structure the average voltage \( \bar{v}_C \) of the iSPPB has to be controlled, while the time behavior of \( v_C \) cannot be influenced and is given by the basic operation. Thus, the buffer voltage \( v_C \) contains a distinctive harmonic component at twice the grid frequency \( 2\omega_G \). Therefore, the measured buffer voltage \( v_C \) first must be filtered by a low-pass filter \( F_{VC} \) to obtain its average value \( \bar{v}_C \). However, the low-pass filter drastically limits the dynamic performance, e.g. during a load step, and as only one specific frequency component at twice the grid frequency, has to be eliminated, a Notch-filter [28],

\[
G_{\text{Notch}}(s) = \frac{s^2 + \omega_0^2}{s^2 + \frac{\omega_0^2}{2} s + \omega_0^2}, \quad \text{with} \quad \omega_0 = 2\omega_G \tag{7}
\]

is recommended for an enhanced dynamic performance.

In accordance to the DC-link voltage control block, the average value \( \bar{v}_C \) is then compared with the reference value \( V_C^* \). The error voltage \( \bar{v}_C - V_C^* \) is then processed by the voltage controller \( R_{VC} \), whose output again equals the average buffer current \( i_{CC}^* \), which is needed to charge or discharge the capacitor \( C_C \) to its reference voltage \( V_C^* \). The demand of the needed buffer current \( i_{CC}^* \) can also be translated into an average or net power demand \( \bar{P}_{CC} \) of the iSPPB by multiplying \( i_{CC}^* \) with the reference buffer voltage \( V_C^* \). This average or net power demand \( \bar{P}_{CC} \) of the iSPPB has to be delivered from the input side, i.e. the mains. Furthermore, the mains also has to provide the needed output power \( \bar{P}_B \), which in the same way can be determined as the average power of the iSPPB, i.e. by multiplying the reference current \( i_{B}^* \) with the reference DC-link voltage \( V_{PN}^* \). The sum of the average buffer power \( \bar{P}_{CC} \) and the output power \( \bar{P}_B \) equals the needed average input power \( \bar{P}_C \).
output power $p_B^G$ also contains certain low and high frequency components, which could generate distortions at the input, the needed output power $p_B^G$ is first low-pass filtered by $F_{PB}$ to obtain the averaged reference output power $p_B^G$ before it is added to the averaged buffer power $p_{CC}^B$. Beneficially, these frequency components are then covered by the power pulsation buffer and are therefore confined in the converter system.

Based on the needed average input power $p_C^G$ and the measured input voltage $v_G$, the sinusoidal reference input current $i_G^R$ can be calculated as it is also typical done for conventional PFC rectifier systems. The current $i_G^R$ is then also forwarded to the PFC Modulator and Inductor Current Control block, which then together with $i_B^L$ is used to calculate the buck and boost stage duty cycles $d_A$ and $d_B$ and the reference inductor current $i_L^B$, as explained in the following.

**C. PFC Modulator and Inductor Current Control Block**

In the PFC modulator block the ratio of the reference currents $i_R^B$ and $i_B^L$ directly determines the current modulation index $m_1$ and therefore the buck and boost stage duty cycles $d_A$ and $d_B$. Furthermore, the maximum value of either $i_R^B$ or $i_B^L$ serves as reference value of the inductor current $i_L$ and actually also defines the operation mode of the converter.

The difference of the reference current $i_R^B$ and the measured inductor current $i_L^B$, i.e. the current control error $\delta_{IL}$, is then processed by the most inner (and therefore fastest) inductor current controller $R_{IL}$, whose output equals the reference inductor voltage $v_{IL}^B$ which is needed to ramp the actual inductor current $i_L^B$ up or down. Since based on the calculated buck and boost stage duty cycles $d_A$ and $d_B$, also the switch node voltages $v_A$ and $v_B$ are defined, this reference inductor voltage $v_{IL}^B$ can only be controlled with the iSPPB voltage $v_{PPB}$, whereas its reference value is determined as $v_{PPB} = v_A - v_B - v_{IL}^B$. Finally, in combination with the measured actual capacitor voltage $v_C$, the full-bridge duty cycle $d_C$ can be calculated.

**D. PWM Unit**

The PWM unit now converts the buck and boost duty cycles $d_A$ and $d_B$ into the switching signal of the buck and boost half-bridge $S_A$ and $S_B$, and the ISPDPB duty cycle $d_C$ into the switching signals $S_{C1}$ and $S_{C2}$ of the low- and high-frequency half-bridge of the iSPPB. As discussed in Section II, the low-frequency half-bridge defines the polarity of the inserted iSPPB voltage $v_{PPB}$, which means that for a positive duty cycle $d_C$ the switch $T_{C1}$ is permanently turned-off ($d_{C1} = 0$) and for a negative duty cycle $d_C$ the switch $T_{C1}$ is continuously turned-on ($d_{C1} = 1$). The other half-bridge is then HF pulse width modulated according to the needed magnitude of the iSPPB voltage $v_{PPB}$. Consequently, only two half-bridges, i.e. one half-bridge of the iSPPB and either the buck or the boost half-bridge, are simultaneously operated at the desired switching frequency. The relative phase shift of the two half-bridge carriers is a degree of freedom and is chosen such that the current ripple is minimal.

**IV. System Verification**

In the following, the proper operation of the proposed topology including the corresponding control structure are verified by means of a circuit simulation. As an application example, one single-phase rectifier cell of a grid connected Δ-rectifier [29] is selected. The considered single-phase rectifier cell is supplied from the 400 Vrms line-to-line voltage of the 50 Hz three-phase grid and is rated to deliver an output power of 8 kW to a 400 V DC bus. Consequently, a single-phase PFC rectifier with buck+boost functionality is required, where the proposed system is a suitable solution avoiding electrolytic capacitors. The switching frequency of the rectifier is selected to be 72 kHz (second harmonic is still below the starting frequency of the conducted noise emission EMI standards at 150 kHz) to further reduce the size of the passive components and to increase the power density. The system specifications are listed in Tab. I and the circuit parameters summarized in Tab. II.

<table>
<thead>
<tr>
<th>Description</th>
<th>Parameter</th>
<th>Nominal Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Power</td>
<td>$P_{IN}$</td>
<td>8 kW</td>
</tr>
<tr>
<td>DC-Link Voltage (L-L)</td>
<td>$V_{IN}$</td>
<td>400 V</td>
</tr>
<tr>
<td>Grid Voltage</td>
<td>$V_{Grms}$</td>
<td>400 V</td>
</tr>
<tr>
<td>Grid Frequency</td>
<td>$\omega_G$</td>
<td>2·50 Hz</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>$f_{SW}$</td>
<td>72 kHz</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Description</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Buck-Boost Inductor</td>
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<td>$100 \mu$H</td>
</tr>
<tr>
<td>Input Capacitor</td>
<td>$C_F$</td>
<td>3.5 mF</td>
</tr>
<tr>
<td>Power Pulsation Buffer Capacitor</td>
<td>$C_C$</td>
<td>81 mF</td>
</tr>
<tr>
<td>DC-Link Capacitor</td>
<td>$C_{PN}$</td>
<td>8.2 mF</td>
</tr>
</tbody>
</table>

The simulated waveforms for the steady state operation at the given operating point are shown in Fig. 5. As can be noticed, there is a smooth transition between the operation modes (BU) and (BO), which leads to a sinusoidal grid current $i_G$ and a low THD of 1.4%. Furthermore, the input current is in phase with the grid voltage $v_G$ and thus, the desired PFC operation is achieved. It can be seen that the average of the inductor current $i_L$ nicely follows its reference, which is also the rectified grid current or the average output current. The maximum inductor current ripple occurs in the vicinity of the grid voltage zero crossing and has a peak-to-peak value of $\Delta i_{Lpp} = 25$ A. The buffer voltage $v_C$ fluctuates with twice the grid frequency around its reference; the maximum and minimum voltages are 897 V and 419 V, respectively. Furthermore, also the output voltage tracks the reference and verifies the operation of the iSPPB. As can be noticed, the limited control bandwidth causes a LF fluctuation of the DC-link voltage of $\Delta v_{PPLFB} = 9.7$ V, which could be even further reduced with a higher control bandwidth and higher switching frequency. In order to keep the voltage ripple at the same...
The conduction losses of a transistor are proportional to the square of the \( I_{rms} \) current, while the conduction losses of a diode mainly depend on the diode’s \( I_{avg} \) current. For this reason, the conduction losses can be assessed based on the sum of the squared \( I_{rms} \) transistors \( P_{DC} \approx \sum_k I_{rms,k}^2 \) and the sum of the average diode currents \( P_{DC} \approx \sum_k I_{avg,k} \).

The result of the quantitative comparison between the conventional and the proposed topology is summarized graphically in Fig. 6, where a better performance results in a shorter bar. The performance index for the switching losses \( \sum_k (v_{T,k} i_{T,k}) \) is 11 kVA for the conventional system and is mainly defined by the switching losses of the buck stage resulting in an index of 9 kVA compared to the switching losses generated in the boost half-bridge with a switching loss index of 2 kVA. Compared to the conventional system, for the proposed buck+boost system with the employed iSPPB, the operation regimes of the BU and BO mode are swapped within the mains period (cf. Fig. 2), and thus the buck half-bridge is operated at a lower input voltage and a lower inductor current, resulting in a reduced switching loss index of only 2 kVA. In contrast, the boost half-bridge is now operated in the vicinity of the peak inductor current and as the DC-link voltage remains the same, the corresponding loss index increases to 5 kVA. Consequently, the total switching loss index of the buck and the boost half-bridge is reduced to 7 kVA but the iSPPB is continuously operated at a buffer voltage which is above the output voltage, and thus contributes the major part of the switching losses with a loss index of 15 kVA, leading to a total loss index of 22 kVA, which is twice the benchmark of the conventional system.

Considering the conduction loss measure of the transistors \( \sum_k I_{rms,k}^2 \), it has to be noted that due to the fundamental input current component \( i_q \) the LF \( I_{rms} \) current loss index of the buck transistor is directly given with \( I_{rms}^2 = 400 \text{ A}^2 \) for both topologies. In addition, for the conventional system the HF \( I_{rms} \) current component loss index of the buck transistor is given with 100 \text{ A}^2 and the \( I_{rms} \) current loss index of the boost transistor is 15 \text{ A}^2, thus the total value of the performance index is given with 515 \text{ A}^2. Consequently, for the conventional system, the major conduction losses are again contributed by the buck half-bridge. For the proposed topology, however, the HF \( I_{rms} \) current component loss index of the buck transistor is reduced to 30 \text{ A}^2, while the \( I_{rms} \) current loss index of the boost transistor is increased to 70 \text{ A}^2. Furthermore, the iSPPB introduces additional \( I_{rms} \) currents resulting in an additional loss index contribution of 307 \text{ A}^2, and finally in a total conduction loss index of \( \sum_k I_{rms,k}^2 = 1007 \text{ A}^2 \), which again is approximately twice the value of the conventional system.

The sum of the average diode currents \( \sum_k I_{avg,k} \) mainly depends on the rectifier diodes (9 A per rectifier diode) and the boost diode current, which equals the DC-link current of 20 A. The sum of the diode currents is given with 60 A for the conventional system and is increased to 84 A due to the additional diodes employed in the iSPPB.

Comparing now the system volumes, the volume of the

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**V. COMPARATIVE EVALUATION**

In the following, the proposed single-phase buck+boost PFC rectifier with iSPPB is evaluated and compared to a conventional buck+boost implementation with electrolytic output capacitor concerning losses and volume by means of simple performance indices [30]. These indices are based on fundamental waveforms, which result from the modulation scheme, but are independent of the component selection and the electric parameters (e.g. the switching frequency and the inductor current ripple). For the comparison, the same system specifications as listed in Tab. I and the circuit parameters summarized in Tab. II are used. Typically, in power electronic converters, the losses are dominated by the semiconductor losses, i.e. switching and conduction losses, while the volume is mainly given by the passive components.

For the loss comparison, it is assumed in a first approximation that the hard switching losses of a transistor linearly depend on both the switched voltage \( v_T \) and the switched current \( i_T \), thus the product \( v_T i_T \) averaged over one grid period \( T_G \) is a good measure for the switching losses. In order to compare both topologies, the average product is summed up over all HF operated transistors, not considering the clamped transistors, resulting in \( P_{T,S} \sim \sum_k (v_{T,k} i_{T,k}) T_G \).

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Comparing now the system volumes, the volume of the
The buck+boost inductor can be related to an area product \( L_{BB} I_{Lms} V_{IL} \), which results from fundamental scaling laws and only takes the LF waveforms into account. The relation of the inductor volume and the area product is approximated by \( V_{IL} \sim \left( L_{BB} I_{Lms} V_{IL} \right)^{3/4} \). In order to compare the volumes of the EMI filter, the differential mode (DM) noise at the AC input side is used as a measure, which is mainly given by the discontinuous current through the buck transistor during buck operation. This current actually corresponds to the HF \( I_{Lrms} \) current in the input capacitor \( C_{Frms} \), and therefore is used for the EMI filter volume estimation. In a first approximation it is assumed that the filter volume of the LC-filter scales with the square root of the required attenuation such that \( V_{EMI} \sim \left( L_{BB} I_{Lms} V_{IL} \right)^{1/2} \). The volume of the capacitive energy storage, i.e. either the DC-link capacitor \( C_{PB} \) of the conventional system or the iSPPB capacitor \( C_{iPB} \) of the proposed system, is considered to be proportional to the maximum of the stored energy, and thus is a good measure for the volume comparison \( V_{PB} \sim E_{PB,max} = \frac{1}{2} C_{PB} V_{PB,max}^2 \).

As already highlighted in previous sections, the employment of the iSPPB reduces the inductor peak current \( i_L \) and the inductor \( I_{Lrms} \) current from 40 A to 28 A and from 25 A to 23 A, respectively. Based on the circuit simulation and for comparison purpose, the inductance value is chosen to be 100 \( \mu \)H for both topologies. Thus, the proposed topology enables a reduction of the inductor volume index \( L_{BB} I_{Lms} V_{IL} \sim 3/4 \) from 0.18 \( (HA^2)^{3/4} \) to 0.13 \( (HA^2)^{3/4} \) (cf. Fig. 6), which means that the inductor is downsized by 28 \%. As already mentioned, the \( I_{Lrms} \) current of the input capacitor \( I_{Frms} \) is mainly given by the operation of the buck half-bridge. As the proposed system features a lower inductor current during buck operation (cf. Fig. 2), compared to the conventional system, the square root of the current stress reduces from 3.1 A\(^{1/2} \) to 2.4 A\(^{1/2} \), resulting in an EMI-filter volume reduction of 23 \% (cf. Fig. 6). Concerning the capacitive energy storage, in the conventional system, the output capacitor has to be designed for a small voltage ripple, resulting in a bulky DC-link capacitor. Based on the results obtained from the circuit simulation, i.e. a capacitance value of 6.6 m\( \mu \)F and a maximum output voltage of 405 V, the maximum stored energy is given with \( E_{PB,max} = 541 \) J (Ws). As already mentioned, in order to keep the volume of the DC-link capacitor small, it is typically realized with electrolytic capacitors featuring a high energy density, however, also showing a limited lifetime. In case of the iSPPB operation, the buffer voltage ripple is increased, enabling the utilization of a much smaller capacitance of 81 \( \mu \)F and is operated up to 900 V. Due to this large voltage swing and/or lower capacitance requirement, the iSPPB buffer capacitor can be implemented with either ceramic or film capacitors, which tolerate a higher current stress. The maximum stored energy in the buffer capacitor is given with \( E_{PB,max} = 33 \) J, which is a drastic reduction by a factor of 16 compared to the conventional system (cf. Fig. 6). However, for comprehensive comparison also the energy density ratio of the different capacitor technologies has to be taken into account.

Finally, the heatsink volume could be deduced from the Cooling System Performance Index (CSPi) [31] and mainly the semiconductor losses, which would require loss models of the components. By increasing the chip area for a given semiconductor technology, the conduction losses are reduced at the cost of elevated (capacitive) switching losses. Thus, a minimum semiconductor losses with the optimal distribution between switching and conduction losses can be found and compared for both topologies. However, in order to conduct a comparison only based on the fundamental waveforms, as mentioned at the beginning, neither the optimal chip area nor the corresponding heatsink volume is determined, but as the loss indices of the semiconductors are increased by a factor of two, it can be assumed in a first step, that the heatsink volume also scales with this factor.

In summary, it can be said that for the proposed system compared to the conventional system, the major semiconductor losses are transferred from the buck stage to the iSPPB, while the total losses are approximately doubled. However, the employment of the iSPPB results in a downsizing of all passive components, especially of the capacitive energy storage, enabling an electrolytic-capacitor-less PFC rectifier system and/or ensuring extended lifetime.

VI. CONCLUSION

In this paper, a novel integrated series power pulsation buffer (iSPPB) concept covering the input power pulsation of a single-phase AC-to-DC two-switch buck+boost PFC rectifier is introduced. The proposed converter and control structures are explained in detail, and are verified by simulations for a 8 kW single-phase PFC rectifier system. The iSPPB does not require a further inductor and its buffer capacitor is operated with a large voltage swing, which drastically reduces the energy storage requirement of the DC-link output capacitor by a factor of 16. Furthermore, with the proposed modulation scheme, which preserves the exclusive operation of the buck and the boost half-bridge, also the peak current of the buck-boost inductor as well as the high-frequency current component at the AC input are reduced. Consequently, also the inductor and required EMI-filter volume are decreased by 28 \% and 23 \%, respectively.
Hence, the proposed topology overcomes the limitations of the conventional buck+boost PFC rectifier, and therefore is a promising solution to strongly improve the power density of the PFC rectifier system and to avoid electrolytic capacitors, which also increases the converter’s lifetime. However, the high power density and extended lifetime are obtained at the expense of higher total semiconductor losses.

ACKNOWLEDGMENT

The authors would like to express their sincere appreciation to Nabtesco Corp., Japan, for the financial and technical support of research on Advanced Mechatronic Systems at the Power Electronic Systems Laboratory, ETH Zurich. Furthermore, inspiring technical discussions with K. Nakamura are especially acknowledged.

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