Power Electronic Systems
Laboratory

IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 5, No. 1, pp. 213-232, March 2017

Optimum Number of Cascaded Cells for High-Power Medium-Voltage AC–DC Converters

J. Huber,
J. W. Kolar

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Optimum Number of Cascaded Cells for High-Power Medium-Voltage AC–DC Converters

Jonas E. Huber, *Student Member, IEEE*, and Johann W. Kolar, *Fellow, IEEE*

***Abstract*— For power electronic systems to interface medium-voltage grids, e.g., in future electric ships, usually cascaded cells converters need to be employed, whereby either few cells featuring power semiconductors with high blocking voltage capability or a larger number of cells using low-voltage (LV) semiconductors can be used. As shown in this paper, physics-inspired empirical models of the dependence of Insulated-Gate Bipolar Transistor (IGBT) power modules' loss-relevant characteristics on the blocking voltage enable an analytic optimization of the efficiency of a cascaded H-bridges (ac–dc) converter, which is complemented by a full efficiency versus power density $\eta\rho$-Pareto optimization. For a 10-kV grid, 1200 V or 1700 V are identified as optimum blocking voltages, resulting in a suitable trade-off between efficiency and power density. Significant efficiency and power density gains can be realized by replacing silicon IGBTs by LV silicon carbide (SiC) devices in multi-cell systems, whereas single-cell designs based on high-voltage SiC devices suffer from the high dv/dt and di/dt values required to limit switching losses. Reliability is analyzed considering redundancy, showing that the reliability of designs based on lower blocking voltages can be comparable with that of designs using higher blocking voltages, and hence fewer cells, if similar effort concerning additionally installed power capability is considered.**

***Index Terms*— Multilevel systems, Pareto optimization, power semiconductor devices, reliability.**

I. Introduction

THERE are many applications, both, well established and emerging ones, that require power electronic systems to interface medium-voltage (MV) grids. An exciting example for the latter is the planned electrification of both, future navy warships [1] as well as future civilian ships, such as cruise liners [2], where local MVAC and/or MVDC grids will be employed for on-board power distribution. Other examples comprise, e.g., high-power drive systems, STATCOMs, MVDC transmission, and, at the interface between MV and low-voltage (LV) systems, solid-state transformers (SSTs), which will serve as an example system in this paper.

SSTs can be defined as power electronic systems that interface to an MV system on their input side and to an LV system on their output side, ensure galvanic isolation between the input and the output by means of medium-frequency (MF) transformers, and provide controllability of their input and output voltages and currents. The first proposal of an "electronic transformer" featuring a high-frequency (HF) ac link for isolation purposes dates back to 1970 [3], [4]. Because an increase in the transformer operating frequency allows to reduce its size and especially its weight, the concept has been pursued for traction applications [5]. Recent advantages in power semiconductor technology have laid the basis for a major revival of the "electronic transformer" around the turn of the millennium, where, initially, again traction applications have been of main interest [6]–[8]. Following the then-emerging smart grid paradigm and its requirement for adding controllability to the distribution grid, the SST was put in the focus also for distribution grid applications, i.e., for supplying LV (400 V in Europe) loads from an MV grid [9]–[12].

In order to interface, e.g., a 10-kV MV grid, either series connections of power semiconductors or multilevel converters have to be employed [11]. The latter avoids issues with voltage sharing among individual switches and can generate multilevel output voltage waveforms with improved harmonic performance, and hence reduced filtering requirements compared with a conventional two-level approach [13]. Therefore, single-cell three-level diode-clamped [14] and capacitor-clamped topologies [15] have found widespread application in the MV drives industry; however, these concepts cannot be scaled to higher voltage levels easily without resorting again to a direct series connection of power semiconductors, because even though topology variants with more than three voltage levels are possible, such configurations increase the system complexity, yet do not provide modularity.

Paralleling [16] or series connecting [17] converter *cells* instead of the power semiconductors is a well-known alternative approach. A typical example using a series connection of converter cells is the cascaded H-bridges (CHB) topology [see Fig. 1(a)], which has been patented already in the 1970s [18]. In theory, this modular approach can cope with any grid voltage by increasing the number of cascaded cells. Since the cells' potentials with respect to ground change constantly due to the switching operations of the other cells in the stack, the dc-side supply or dc-side load of each cell requires galvanic isolation (notable exceptions being the modular multilevel converter [19], [20], or battery storage applications [21]). Realizing these isolation stages by means

Manuscript received May 18, 2016; revised August 16, 2016; accepted August 29, 2016. Date of publication September 2, 2016; date of current version January 31, 2017. Recommended for publication by Associate Editor Rui Li.

The authors are with the Power Electronic Systems Laboratory, ETH Zurich, 8092 Zürich, Switzerland (e-mail: huber@lem.ee.ethz.ch).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JESTPE.2016.2605702

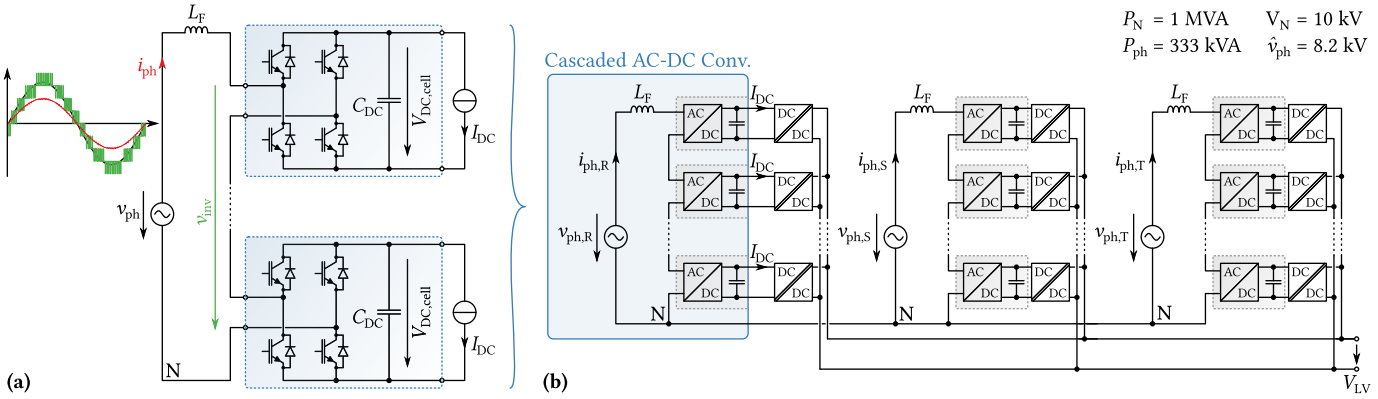

Fig. 1. (a) Single-phase CHB converter structure with the dc-side supply/loads modeled as dc current sources as considered throughout this paper, including key waveforms. (b) Exemplary application of this CHB structure in a three-phase ac–dc SST.

of isolated dc–dc converters featuring an MF transformer, and then connecting the LV dc outputs of all these dc–dc converters in parallel to a common LVDC bus, i. e., employing an input-series output-parallel (ISOP) configuration, results in a typical multi-cell MVAC-LVDC SST topology [6]–[8], [22], which is shown in Fig. 1(b) in a three-phase configuration. (Remark: In a single-phase traction application, only one phase stack would be required.)

Cascading of converter cells is thus a feasible approach to interface power electronic systems, such as SSTs, to the MV grid. Considering recent advances in high-voltage (HV) silicon-carbide (HV SiC) power semiconductor technology, which have resulted in 4H–SiC IGBTs with blocking voltages of 15 kV and beyond [23], [24], SSTs based on 10 kV [25] or 15 kV [26] devices and conventional single-cell two-level or three-level converter topologies could be alternatively considered. However, only LV SiC power modules with blocking voltages up to 1700 V are currently available as products [27]–[29]. Therefore, especially in heavy-duty industrial applications, silicon IGBT power modules will prevail in the foreseeable future and might be gradually complemented by LV SiC solutions. In either case, the blocking voltages of industrially available semiconductor modules are limited to several kV (e. g., to 6.5 kV for silicon IGBTs). Furthermore, only about 50 %–60 % of the devices' rated blocking voltage can be utilized in an application in order to limit the susceptibility to cosmic-ray-induced failures [30], [31].

Thus, a cascaded cells system can be realized using few cells employing, e. g., 6.5-kV IGBTs, but also using many cells based on, e. g., 600-V IGBTs. This paper comprehensively discusses the trade-offs that have to be considered for the selection of the number of cells in order to identify the optimum number of cascaded cells for a given grid voltage (or, equivalently, the optimum semiconductor blocking voltage), considering efficiency, power density, and also reliability aspects.

Initial analyses of the trade-offs affected by the number of cascaded cells have been addressed in [32] for IGBTs with 3.3-kV blocking voltage and higher, and in [21], where due to the employed low switching loss modulation scheme basically only conduction losses have been considered. Therefore, first, an analytic loss analysis based on physics-inspired models of IGBT parameters' dependences on the blocking voltage, covering the full range from 600 V to 6.5 kV, is introduced in Section II. Subsequently, a full efficiency versus power density $\eta\rho$-Pareto analysis [33] is performed in Section III, whereby also modern LV SiC power modules are considered in Section IV, and finally, fundamental reliability aspects of multi-cell systems are discussed in Section V.

II. Basic Considerations on the Optimum Number of Cascaded Converter Cells

In the following, a single CHB phase stack, as shown in Fig. 1(a), will be considered. In order to obtain generic results that are applicable to cascaded cells converters in general, the cascaded cells' dc side sources or loads are modeled as dc current sources. Depending on the application, these might represent isolated dc–dc converters (SSTs) or passive diode rectifiers fed by a grid-frequency multiwinding transformer (drive systems); in the case of a STATCOM application, or for a modular multilevel converter, no current sources would be present. In addition to the variable number of cascaded converter cells that can generate an output voltage waveform with multiple levels, a filter inductor, L_F, is required to limit the current harmonics injected into the grid.

Fig. 2 shows an overview of the trade-offs affected by the number of cascaded converter cells. If the number of cells is high, the required semiconductor blocking voltage is low. By using Pulse-Width Modulation (PWM) modulation with phase-shifted carriers [34], [35] and many cascaded cells, the number of voltage levels and the effective switching frequency seen by the filter inductor are increased, and hence the required switching frequency per cell and the filtering effort, i. e., L_F, can be reduced. However, the conduction losses increase because the phase current passes through more (bipolar) power semiconductors in series, i. e., the total voltage drop increases. In addition, reliability concerns might arise if the number of cells is high. On the other hand, using only few cascaded cells employing devices with higher blocking voltages reduces the number of available voltage levels, which requires either a larger filter, L_F, and/or higher switching frequencies to

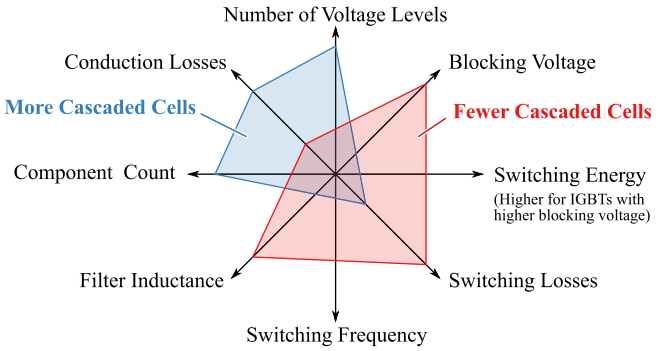

Fig. 2. Overview of the trade-offs that are affected by the number of cascaded converter cells.

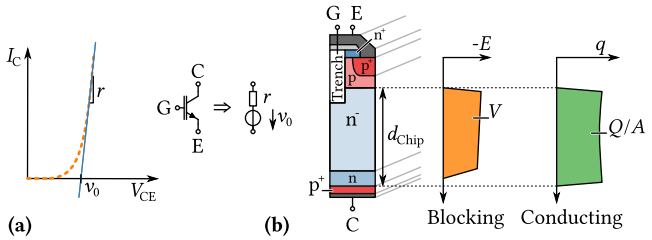

Fig. 3. (a) Approximation of an IGBT (or diode) forward characteristic by v_0 and r. (b) Schematic cross section (not to scale) of a trench/field-stop IGBT with qualitative drift region field distribution in the blocking state and qualitative charge carrier concentration in the conducting state [36]. The integral of the electric field corresponds to the applied reverse voltage, and the integral of the charge carrier density along d_{Chip} gives the stored charge per chip area.

keep the harmonic content of the grid current within limits. However, since the switching energies of IGBTs increase with blocking voltage, high switching losses are generated if high switching frequencies are needed. Therefore, designs based on devices with higher blocking voltages are dominated by switching losses, whereas designs based on lower blocking voltages are dominated by conduction losses. This trade-off regarding semiconductor losses will be analyzed in detail in the following.

A. Blocking Voltage Scaling of IGBT and Diode Characteristics

In order to investigate how the device blocking voltage affects the trade-off between conduction and switching losses, the scaling of the relevant parameters of IGBTs and diodes with blocking voltage and rated current needs to be investigated and approximated, which is done in the following by fitting physics-inspired models to empirical data of modern IGBT modules (Infineon IGBT3/IGBT4 types featuring a trench/field-stop design, considering the data for a junction temperature of $T_{\mathrm{j}} = 125\,^{\circ}\mathrm{C}$). The raw data, the corresponding fits, and resulting model parameters can be found in the Appendix. These models allow to estimate the conduction and switching loss characteristics of a *virtual* power module with arbitrary rated blocking voltage, V_{B}, and rated current, I_{N}.

1) Conduction Losses: In general, the v_{CE} versus i_{C} (or, for diodes, v_{F} versus i_{F}) characteristic of bipolar power semiconductors can be approximated by a linear model $v_{\mathrm{CE}}(i_{\mathrm{C}}) = v_{\mathrm{CE},0} + r \cdot i_{\mathrm{C}}$, as shown in Fig. 3(a). The total forward voltage drop at rated current, $v_{\mathrm{CE}}(I_{\mathrm{N}})$, thus, consists of two parts, $v_{\mathrm{CE},0}$ and $v_{\mathrm{CE,r}} = r \cdot I_{\mathrm{N}}$. From semiconductor physics [37] it is expected that the total forward voltage drop at rated current, and hence $v_{\mathrm{CE},0}$ and $v_{\mathrm{CE,r}}$ scale with the blocking voltage roughly as

$$v_{\mathrm{CE},0}(V_{\mathrm{B}}) = A_{\mathrm{v0}} \cdot \log(B_{\mathrm{v0}} \cdot V_{\mathrm{B}} + C_{\mathrm{v0}}) \tag{1}$$

and

$$v_{\mathrm{CE,r}}(V_{\mathrm{B}}) = r \cdot I_{\mathrm{N}} = A_{\mathrm{r}} \cdot \log(B_{\mathrm{r}} \cdot V_{\mathrm{B}}) \tag{2}$$

implying

$$r(V_{\mathrm{B}}, I_{\mathrm{N}}) = \frac{1}{I_{\mathrm{N}}} \cdot A_{\mathrm{r}} \cdot \log(B_{\mathrm{r}} \cdot V_{\mathrm{B}}). \tag{3}$$

These functions can be fitted (parameters A_{v0}, B_{v0}, C_{v0}, A_{r}, and B_{r}) with good accuracy to empirical data as is shown in the Appendix. Note that r is inversely proportional to the rated current (chip area) for a given blocking voltage. This can be explained considering that the maximum loss density in a chip is limited, corresponding to a maximum permissible current density at rated current [38]. Therefore, the chip area in a module must be $A_{\mathrm{Chip}} \propto I_{\mathrm{N}}$, and hence $r \propto 1/A_{\mathrm{Chip}} \propto 1/I_{\mathrm{N}}$.

2) Switching Losses: In order to express the dependence of switching losses on the blocking voltage with low complexity, the switching energies of a given device are approximated to scale linearly with the switched current and also with the applied dc voltage, i.e., the blocking voltage utilization, $u = V_{\mathrm{dc}}/V_{\mathrm{B}}$. Then, the switching losses of a specific device can be expressed by a normalized switching energy $K_{\mathrm{sw}} = E_{\mathrm{sw}}(I_{\mathrm{N}})/I_{\mathrm{N}}$ for $u = 0.5$ (as typically specified in datasheets) and with $[K_{\mathrm{sw}}] = \mathrm{mJ/A}$. The switching energy of a certain transition can then be calculated from K_{sw} as

$$E_{\mathrm{sw}} = K_{\mathrm{sw}} \cdot i_{\mathrm{sw}} \cdot \frac{u}{0.5} \quad \text{with} \quad [E_{\mathrm{sw}}] = \mathrm{mJ}, \tag{4}$$

where u denotes the actual application's blocking voltage utilization, which might be different from $u = 0.5$ for which K_{sw} is specified. Note that three individual K exist for turn-OFF, turn-ON, and diode recovery losses, i.e., K_{OFF}, K_{ON}, and K_{rec}.

Fig. 3(b) shows a schematic cross section of a modern field-stop IGBT with a trench-gate structure together with the field distribution across the n^- drift region in the blocking state and the charge carrier density distribution across the n^- drift region in the conducting state. Switching energies of bipolar power semiconductors are roughly proportional to this stored charge that needs to be removed during the turn-off process, and to the reapplied voltage, i.e., $E_{\mathrm{sw}} \propto Q \cdot u \cdot V_{\mathrm{B}}$ [39]. Assuming an approximately rectangular field profile in the blocking state, the chip thickness, d_{Chip}, is proportional to the blocking voltage, i.e., $d_{\mathrm{Chip}} \propto V_{\mathrm{B}}$. Assuming further an approximately rectangular charge density profile in the conduction state, the stored charge per chip area is proportional to the chip thickness, i.e., $Q/A_{\mathrm{Chip}} \propto d_{\mathrm{Chip}} \propto V_{\mathrm{B}}$. Hence, since the chip area is proportional to the rated current, the normalized switching energies are expected to scale with the square of the blocking voltage, i.e., $K_{\mathrm{sw}} \propto V_{\mathrm{B}}^2$. These considerations inspire the following models for the scaling of normalized turn-off,

turn-on, and diode recovery losses with the rated blocking voltage:

$$K_{\mathrm{OFF}}(V_{\mathrm{B}}) = A_{\mathrm{OFF}}V_{\mathrm{B}}^2 + B_{\mathrm{OFF}}V_{\mathrm{B}} + C_{\mathrm{OFF}} \quad (5)$$

$$K_{\mathrm{ON}}(V_{\mathrm{B}}) = A_{\mathrm{ON}}V_{\mathrm{B}}^2 + B_{\mathrm{ON}}V_{\mathrm{B}} + C_{\mathrm{ON}} \quad (6)$$

$$K_{\mathrm{rec}}(V_{\mathrm{B}}) = A_{\mathrm{rec}}V_{\mathrm{B}}^2 + B_{\mathrm{rec}}V_{\mathrm{B}} + C_{\mathrm{rec}}. \quad (7)$$

Note that the approximated normalized switching energies are modeled without a dependence on the current rating, i.e., the chip area, which is in accordance with findings from [40]. Again, the Appendix provides the fit results and model parameters (A_{i}, B_{i}, C_{i} with $i = \mathrm{OFF}, \mathrm{ON}, \mathrm{rec}$).

3) Thermal Resistance: The thermal resistance from junction to heat sink, $R_{\mathrm{th,JH}}$, (in datasheets specified per device, i.e., per individual IGBT or diode) is expected to be roughly inversely proportional to the chip area, while other factors, such as the package, also have an influence. The chip area, in turn, is proportional to the current rating, but depends also on the blocking voltage because $v_{\mathrm{CE}}(I_{\mathrm{N}})$ and hence also the allowable maximum current density for a given loss density limit show this dependence (see the Appendix). Therefore, and to account for the observed increase of package size with rated blocking voltage, the thermal resistances are modeled as

$$R_{\mathrm{th,JH}}(V_{\mathrm{B}}, I_{\mathrm{N}}) = A_{\mathrm{Rth}} \cdot (V_{\mathrm{B}} \cdot I_{\mathrm{N}})^{-B_{\mathrm{Rth}}} \quad (8)$$

which fits the empirical data well, as is shown in the Appendix.

B. Analytical Derivation of the Optimum Blocking Voltage

The models for semiconductor parameters as functions of the blocking voltage and current rating derived in Section II-A facilitate the calculation of conduction and switching losses of a cascaded cells converter system according to Fig. 1(a) with an arbitrary cell number, which will be discussed in the following, whereby unity power factor operation and a power flow from ac to dc (i.e., rectifier mode) are assumed without loss of generality.

1) System Quantities: The required total dc voltage of a phase stack (i.e., the sum of the cell's dc voltages) is given by

$$V_{\mathrm{dc,total}} = \frac{\hat{v}_{\mathrm{ph}}}{M_{\mathrm{N}}} = \sqrt{\frac{2}{3}}\frac{V_{\mathrm{N}}}{M_{\mathrm{N}}}, \quad (9)$$

where $M_{\mathrm{N}} = \hat{v}_{\mathrm{ph}}/V_{\mathrm{dc,total}}$ denotes the nominal modulation index and V_{N} is the nominal grid voltage (line to line). This total dc link voltage is split among the cascaded converter cells. With V_{B} denoting the blocking voltage of the power semiconductors used and with u being the blocking voltage utilization, the dc voltage of a single cell is given by $V_{\mathrm{dc}} = u \cdot V_{\mathrm{B}}$, and hence the required number of cascaded cells follows directly as

$$n_{\mathrm{cell}} = \frac{V_{\mathrm{dc,total}}}{u \cdot V_{\mathrm{B}}}. \quad (10)$$

Equation (10) illustrates the equivalence of looking at the optimum number of cascaded converter cells and at the optimum semiconductor blocking voltage. Note that in actual implementations of course only a discrete number of cells could be used, i.e., $n_{\mathrm{cell,actual}} = \lceil n_{\mathrm{cell}} \rceil$.

The amplitude of the phase current, $\hat{i}_{\mathrm{ph}}$, can be calculated as

$$\hat{i}_{\mathrm{ph,pk}} = 2 \cdot \frac{P_{\mathrm{ph}}}{\sqrt{2/3}V_{\mathrm{N}}}, \quad (11)$$

and its rms value and the rectified average value follow then directly as

$$\tilde{i}_{\mathrm{ph}} = \frac{1}{\sqrt{2}}\hat{i}_{\mathrm{ph}} \quad \text{and} \quad \overline{i}_{\mathrm{ph}} = \frac{2}{\pi}\hat{i}_{\mathrm{ph}}. \quad (12)$$

2) Conduction Losses: The current flowing into one of the cascaded converter cells equals the phase current and flows through two power semiconductors per cell at any instant in time. Assuming here in a first step that the conduction loss characteristics of IGBTs and diodes are the same, the total conduction losses of a phase stack based on power semiconductors with a certain blocking voltage, V_{B}, and a certain rated current, I_{N}, can be calculated as

$$P_{\mathrm{cond}}(V_{\mathrm{B}}, I_{\mathrm{N}}) = 2n_{\mathrm{cell}} \cdot \left(v_{\mathrm{CE},0}(V_{\mathrm{B}}) \cdot \overline{i}_{\mathrm{ph}} + r(V_{\mathrm{B}}, I_{\mathrm{N}}) \cdot \tilde{i}_{\mathrm{ph}}^2\right), \quad (13)$$

where n_{Cell} has been given in (10). Note that $n_{\mathrm{Cell}} \propto 1/V_{\mathrm{B}}$, and hence, since the reduction of the forward voltage drop with the blocking voltage is not very pronounced (see the Appendix), high conduction losses must be expected for designs based on lower blocking voltages.

3) Required Switching Frequency: The required switching frequency (per cell) depends strongly on the number of cascaded converter cells. Let l_{f} denote the filter inductance in per unit, whereby

$$Z_{\mathrm{B}} = \frac{V_{\mathrm{N}}^2}{P_{\mathrm{N}}} = \frac{\tilde{v}_{\mathrm{ph}}^2}{P_{\mathrm{ph}}} = \frac{(V_{\mathrm{N}}/\sqrt{3})^2}{P_{\mathrm{N}}/3} \quad \text{and} \quad L_{\mathrm{B}} = \frac{Z_{\mathrm{B}}}{2\pi f_{\mathrm{g}}} \quad (14)$$

are the reference impedance and inductance, respectively. Let further $\delta i_{\mathrm{pp}} = \Delta i_{\mathrm{pp}}/\hat{i}_{\mathrm{ph}}$ denote the allowable maximum relative peak-to-peak ripple of the phase current. Then, since for a single two-level H-bridge inverter operated with unipolar PWM, where the output frequency of the full-bridge is already twice the device switching frequency, i.e., $f_{\mathrm{S,eff}} = 2 \cdot f_{\mathrm{S}}$, due to interleaved operation of the two bridge legs, the maximum current ripple during a half-period of the grid current occurs when the modulation index is $M = 1/2$. Thus, the required switching frequency for a given maximum peak-to-peak current ripple can be calculated as

$$f_{\mathrm{s,2L}} = \frac{V_{\mathrm{dc,total}}}{8 \cdot L_{\mathrm{F}} \cdot \Delta i_{\mathrm{pp}}} = \frac{V_{\mathrm{dc,total}}}{8 \cdot l_{\mathrm{F}} L_{\mathrm{B}} \cdot \delta i_{\mathrm{pp}} \hat{i}_{\mathrm{ph}}}. \quad (15)$$

If more than one cell is connected in series and if phase-shifted PWM [34], [35] is used, the magnitude of the steps in the output voltage [see Fig. 1(a)] is reduced to $V_{\mathrm{dc,total}}/n_{\mathrm{Cell}}$, and the effective switching frequency seen by the filter inductor is increased by a factor n_{Cell} (i.e., to $f_{\mathrm{S,eff}} = 2 \cdot n_{\mathrm{Cell}} \cdot f_{\mathrm{S}}$). Therefore, solving

$$\Delta i_{\mathrm{pp}} = \frac{V_{\mathrm{dc,total}}}{8 \cdot L_{\mathrm{F}} \cdot f_{\mathrm{s,2L}}} \stackrel{!}{=} \frac{V_{\mathrm{dc,total}}/n_{\mathrm{Cell}}}{8 \cdot L_{\mathrm{F}} \cdot n_{\mathrm{Cell}} f_{\mathrm{s}}} \quad (16)$$

reveals that the switching frequency *per bridge leg*, f_s, that is required to achieve the same current ripple in the same filter inductor is reduced according to

$$f_s = \frac{1}{n_{Cell}^2} \cdot f_{s,2L}, \tag{17}$$

that is, it decreases with the number of cascaded converter cells *squared,* which is in accordance with the findings reported in [41].

4) Switching Losses: Each bridge leg in a cell is operated at a fixed switching frequency f_s from above. For normal PWM operation where the ratio between switching frequency and fundamental frequency is quite high, and since a linear dependence between switched current and resulting switching energies is assumed [see (4)], e. g., the turn-off losses during half a grid period can be estimated based on the bridge leg's average current, $\overline{i}_{ph}$, as

$$P_{OFF,leg}(V_B) = K_{OFF}(V_B) \cdot \frac{1}{1000} \cdot \overline{i}_{ph} \cdot \frac{u}{0.5} \cdot f_s, \tag{18}$$

where the factor $1/1000$ is required to compensate for the mJ/A unit of K_{OFF}. Each of the three switching energies is dissipated once per bridge leg during one switching cycle (although not in the same device). The overall switching losses of a phase stack based on power semiconductors with a certain blocking voltage, V_B, can thus be calculated from

$$P_{sw}(V_B) = 2n_{Cell} \cdot \left(K_{sw}(V_B) \cdot \frac{1}{1000} \cdot \overline{i}_{ph} \cdot \frac{u}{0.5} \cdot f_s \right) \tag{19}$$

with $K_{sw}(V_B) = K_{OFF}(V_B) + K_{ON}(V_B) + K_{rec}(V_B)$ and with f_s given in (17). Inserting some of the relationships discussed earlier, $P_{sw}(V_B) \propto V_B^3$ is found, indicating high switching losses for designs employing semiconductors with high blocking voltages.

5) Optimum Blocking Voltage: The above derivations, especially (13) and (19), allow to calculate conduction and switching losses, and hence the total semiconductor losses of a CHB system, as shown in Fig. 1(a), employing IGBT modules with arbitrary blocking voltage ratings. Considering now an example system with a grid voltage of $V_N = 10\,\text{kV}$ (line to line), a nominal (three-phase) power of $P_N = 1\,\text{MVA}$, and hence a nominal power of $P_{ph} = 333\,\text{kVA}$ for the phase stack, the blocking voltage utilization is chosen as $u = 0.55$, and the nominal modulation index as $M_{nom} = 0.8$. The filter inductance is set to $l_F = 10\,\%$, and the allowable relative peak-to-peak current ripple to $\delta i_{pp} = 1\,\%$, since the filter inductor current corresponds to the grid current, and therefore strict limits on its harmonic content apply, e. g., IEEE 519 [42]. In order to establish a fair comparison, the total silicon area should be the same for all considered designs. Thus, aiming for a high overall efficiency of above 99 %, for a reference blocking voltage, e. g., $V_{B,ref} = 1700\,\text{V}$, the target for the relative semiconductor losses is set to 2/3 % in order to account for additional losses, e. g., in the filter inductor. Solving

$$\frac{P_{cond}(V_{B,ref}, I_N) + P_{sw}(V_{B,ref})}{P_N/3} \overset{!}{=} \frac{2}{3} \cdot 0.01 \tag{20}$$

for I_N with $V_{B,ref} = 1700\,\text{V}$ results in a required current rating of $I_{N,1700\,V} \approx 150\,\text{A}$. The rated current specified in datasheets is typically such that the nominal loss density in the IGBT chips of a module, i. e., $v_{CE}(I_N) \cdot J_N = v_{CE}(I_N) \cdot I_N / A_{Chip}$, does not exceed a limit of, e. g., $150\,\text{W/cm}^2$, resulting in a decrease of the nominal current density, J_N, with increasing blocking voltage [38] (see also the Appendix). Hence, the total silicon area used in a design based on these 1700 V/150 A devices is approximately

$$A_{Si,1700\,V} = n_{Cell}(1700\,\text{V}) \cdot 8 \cdot \frac{I_{N,1700\,V}}{J_N(1700\,\text{V})}, \tag{21}$$

where the factor 8 comes from the fact that there are four IGBT/diode combinations per cell, each consisting of two devices (IGBT and diode, where, as stated before, equal characteristics are assumed here). In order to keep the total silicon area constant for all considered blocking voltages, the nominal currents of the devices considered for other blocking voltages can be found using [see Fig. 4(b)]

$$I_N(V_B) = I_{N,1700\,V} \cdot \frac{n_{Cell}(1700\,\text{V})}{n_{Cell}(V_B)} \cdot \frac{J_N(V_B)}{J_N(1700\,\text{V})}. \tag{22}$$

With I_N defined as a function of V_B such that in all cases the same *total* silicon area is used, the conduction and switching losses of designs based on different blocking voltages can be calculated using (13) and (19), respectively, which is shown in Fig. 4(a). As expected, conduction losses dominate for designs based on IGBTs with lower blocking voltage ratings, whereas switching losses clearly dominate when devices with higher blocking voltages are employed, because, as a consequence of the lower number of cascaded cells, high switching frequencies are required in order to fulfill the current ripple specification, as can be seen from Fig. 4(d), and because, additionally, the normalized switching energies increase with the blocking voltage. Therefore, an optimum blocking voltage resulting in the lowest overall losses can be identified as (theoretically) 1710 V, where then 10.9 cells would be required. Note that the optimum is quite flat, and hence, considering common blocking voltages, either 1200 V or 1700 V devices should result in the lowest overall losses.

The losses generated in the semiconductors must be removed by means of a cooling system, i. e., a heat sink. For each combination of V_B and I_N, the thermal resistance from junction to heat sink per IGBT can be approximated using (8). From that, the temperature T_{HS} that the heat sink would need to maintain such that the devices operate at a junction temperature of $T_j = 125\,^\circ\text{C}$ can be calculated as

$$T_{HS} = T_j - R_{th,JH}(V_B, I_N) \cdot \frac{P_{cond}(V_B, I_N) + P_{sw}(V_B)}{8 \cdot n_{Cell}(V_B)}, \tag{23}$$

including a factor 8 again, since $R_{th,JH}$ is specified per device, i. e., per IGBT or per diode. As can be seen from Fig. 4(c), designs that feature very low losses can tolerate very high heat sink temperatures. This means that a lower total chip area could be used from a loss dissipation point of view, however, while this would increase the thermal resistances from junction to heat sink, $R_{th,JH}$, and hence reduce the allowable heat sink temperature, it would also increase the losses, which is not feasible if an efficiency specification shall

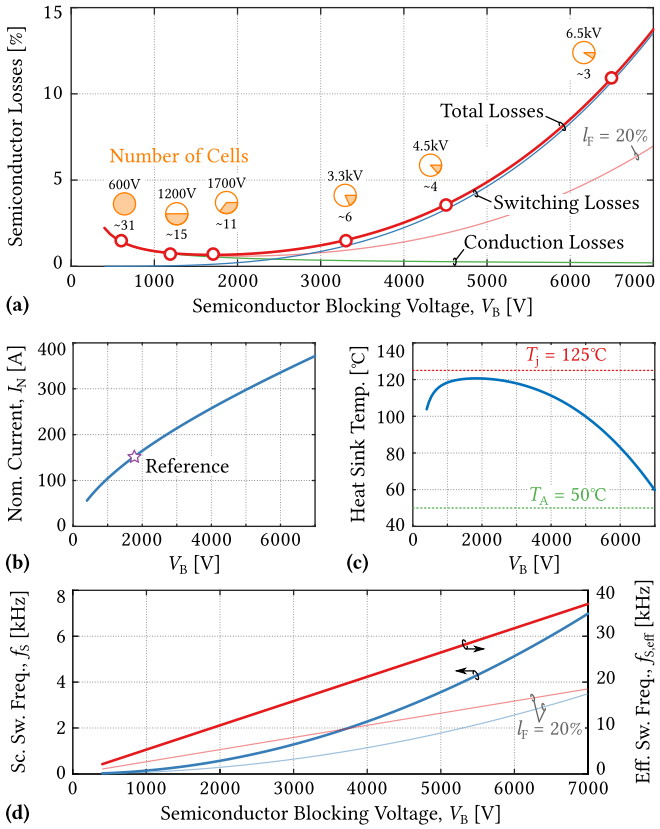

Fig. 4. (a) Normalized semiconductor losses as a function of the cells' blocking voltage in a 1 MVA CHB system interfacing a 10-kV grid. The total silicon area is kept constant for all designs, and the required number of cascaded cells is indicated for common IGBT blocking voltages. The main loss curves are for $l_F = 10\,\%$ and $\delta i_{pp} = 1\,\%$, and additionally, the total losses for the case of an increased $l_F = 20\,\%$ are shown. (b) Nominal device currents for a constant total silicon area as a function of the blocking voltage. (c) Heat sink temperature that is required to dissipate the losses indicated in (a) with $T_j = 125\,°C$. (d) Required switching frequencies per semiconductor and resulting effective switching frequencies of the output multilevel voltage waveforms, $f_{S,eff} = 2 \cdot n_{Cell} \cdot f_S$.

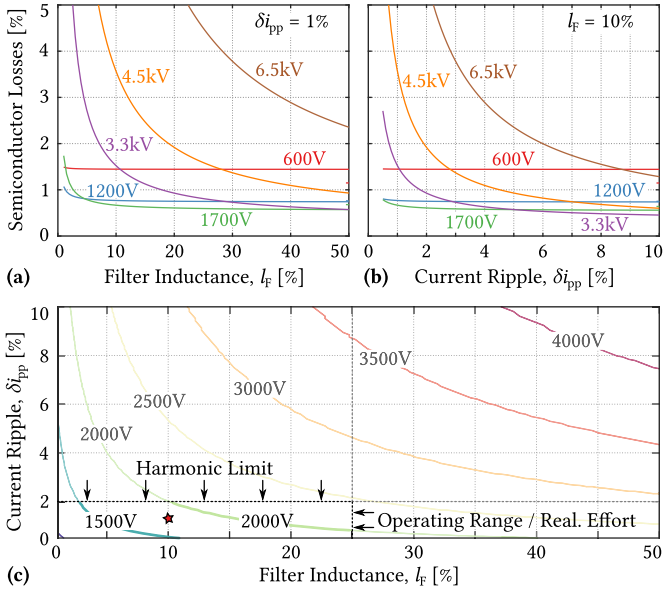

Fig. 5. Sensitivity of the semiconductor losses to variations of (a) filter inductance, l_F, and (b) allowable grid current ripple, δi_{pp}, and (c) corresponding dependence of the optimum blocking voltage on these parameters, where the basic limitations of feasible values are indicated.

be met. In contrast, designs with higher losses require lower heat sink temperatures, implying a larger volume of the heat sink. Note that an increase of the silicon area for designs with higher blocking voltages would enable higher heat sink temperatures, i. e., smaller heat sinks; however, since the losses of these designs are dominated by switching losses, which do not depend on the nominal current (chip area), this measure would not improve the efficiency of these designs significantly. An increase of the total chip area would reduce the thermal resistances of the devices and the conduction losses, i. e., slight efficiency improvements could be expected for designs based on lower blocking voltages, since these are dominated by conduction losses, and hence the optimum blocking voltage would be shifted to slightly lower values. On the other hand, for designs based on higher blocking voltages, only the cooling would be simplified, whereas the losses would not be reduced significantly.

Fig. 5(a) and (b) show the sensitivity of the semiconductor losses on the filter inductance, l_F, and on the allowable current ripple, δi_{pp}. It can be seen that designs employing devices with lower blocking voltages do not benefit from an increase of either of these parameters, because the required switching frequencies are anyway low as a result of the high number of voltage levels [see also Fig. 4(d)], and hence these designs are dominated by conduction losses. If these are low, the switching frequencies could be increased, which would increase the semiconductor losses, but, on the other hand, allow to reduce the size of the filter inductor, and potentially its losses, and hence favorably affect the total system losses and/or volume. In contrast, designs based on devices with higher blocking voltages do benefit from an increased filtering effort and/or current ripple, because lower switching frequencies can be used [see again Fig. 4(d)], thereby reducing the total semiconductor losses. Such an increase of the filter inductance or the current ripple corresponds to a shift of the optimum blocking voltage toward higher values, as can be seen in Fig. 5(c). Note, however, that an increase of the current ripple is constrained by harmonic limits, and that an increase of the filter inductance is constrained by output voltage capability requirements, as will be discussed later, and also by the realization effort of the inductor, resulting in comparatively low values of the optimum blocking voltage.

Thus, changes of the filter inductance value affect the losses in the semiconductors (and hence the optimum blocking voltage) but also losses in the filter inductor itself, and, through the size of the required heat sinks and the size of the inductor, also the power density, ρ, of the system, which is another interesting performance characteristic in addition to the efficiency, η. Furthermore, a frequency-independent current ripple specification is a simplification only, since current harmonics are limited by standards such as IEEE 519 [42], which consider a variation of the limits with frequency. A detailed treatment of these aspects is beyond the possibilities of the simplified analytic analysis presented here, and

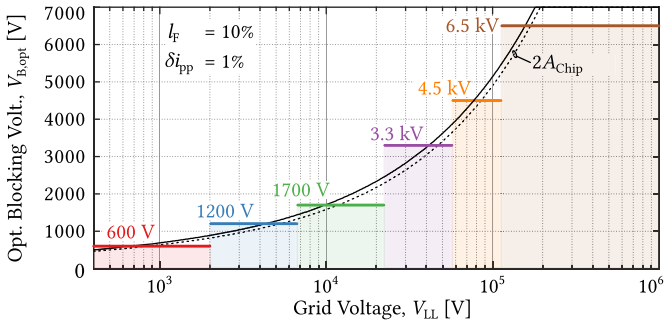

Fig. 6. Optimum blocking voltage as a function of the grid voltage (line to line); the theoretical curve is overlaid by bars indicating the most suitable IGBT voltage rating. The results consider $l_F = 10\,\%$ and $\delta i_{pp} = 1\,\%$. The optimum blocking voltage is slightly lowered if the available silicon chip area is doubled.

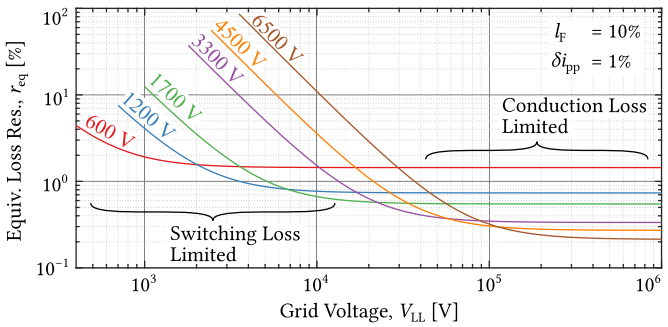

Fig. 7. Semiconductor losses expressed as an equivalent loss resistance, r_{eq}, for $l_F = 10\,\%$ and $\delta i_{pp} = 1\,\%$, showing the silicon multilevel limits, i.e., the switching loss limited region and the conduction loss limited region.

will therefore be addressed comprehensively by means of an efficiency versus power density, i.e., $\eta\rho$-Pareto optimization in Section III.

C. Optimum Blocking Voltage for Other Grid Voltages

The above calculations can be repeated for grid voltages other than the 10 kV considered so far. The phase current is kept constant, while the grid voltage (and hence the required number of cells, and so on) is varied, thereby scaling the system power proportionally to the grid voltage. The devices' current rating is kept constant, and therefore the same chip area is used for all designs at a given grid voltage. In addition, the filter inductance value in per unit is kept constant, i.e., the actual inductor value, L_F, scales with the nominal power and the grid voltage. Fig. 6 shows the optimum blocking voltage for a wide range of grid voltages, considering $l_F = 10\,\%$ and $\delta i_{pp} = 1\,\%$. Each of the common IGBT blocking voltages suits a certain range of grid voltages best. Note, however, that the optima are quite flat (see Fig. 4), and that a variation of l_F and/or δi_{pp} might shift these optima as indicated by Fig. 5. Furthermore, an increase of the total chip area, i.e., of $I_{N,1700\,V}$ from above, lowers the optimum blocking voltage for a given grid voltage, because the trade-off between conduction and switching losses is shifted in favor of conduction losses as discussed above, allowing to use more cascaded cells and hence lower blocking voltages for a given grid voltage.

D. Silicon Multilevel Limits

For (unipolar) power semiconductor technology, diagrams showing the achievable specific on-state resistance versus the device blocking voltage on a log–log scale are used to indicate material and technology limits. By expressing the losses of a cascaded cells system as an equivalent normalized loss resistance,

$$r_{eq} = \frac{R_{eq}}{Z_B} = \frac{P_{cond} + P_{sw}}{\tilde{i}_{ph}^2} \cdot \frac{1}{Z_B}, \tag{24}$$

a similar diagram can be shown in Fig. 7, showing the achievable r_{eq} for each blocking voltage as a function of the grid voltage. Note that the region where a certain blocking voltage provides the lowest r_{eq} coincides with the corresponding bar indicated in Fig. 6.

Here, in contrast to the initially mentioned semiconductor technology limit diagram, *two* different limits can be identified. Note that again l_F and δi_{pp} are fixed, and that the same total chip area is used for all designs at a given grid voltage. Then, there is a switching loss limit for low grid voltages, because for a given blocking voltage, the number of required cells becomes small and hence the required switching frequency increases. For a given filter inductance, the switching loss limit can be overcome by choosing a design with a *lower* blocking voltage, and hence more cascaded cells that can operate at a lower switching frequency. On the other hand, there is a conduction loss limit when higher grid voltages are considered. Then, the number of cells is high, and hence the required switching frequency and the switching losses are low. The conduction loss limit can thus be overcome by choosing a design with a *higher* blocking voltage and hence fewer cascaded cells. Note, however, that the conduction loss limit is a consequence of the voltage drop across the semiconductor junction of the bipolar power semiconductors considered here, i.e., $v_{CE,0}$. In the case of unipolar devices, such as MOSFETs, using more cells with a lower blocking voltage results in theory in lower conduction losses, also if the total chip area is kept constant [43], because the specific on-state resistance of MOSFETs scales roughly as $r_{ON} \propto V_B^{2.5}$ [37].

III. $\eta\rho$-Pareto Optimization of the Number of Cascaded Converter Cells

As has been discussed in Section II, the trade-off between switching and conduction losses is affected by the choice of the filter inductance, which is a passive component showing both losses and, as a second characteristic, a considerable volume that affects the system's power density. In addition, the cooling system required to maintain the semiconductor junction temperature at the assumed $T_j = 125\,°C$ contributes a volume that depends on the losses to be removed from the power modules. To include both these dimensions, efficiency *and* power density, and their mutual coupling, into the determination of the optimum number of cascaded cells, a multi-objective efficiency versus power density $\eta\rho$-Pareto analysis

TABLE I

NUMBER OF CASCADED CELLS AND SEMICONDUCTOR BLOCKING VOLTAGE UTILIZATION FOR $V_{\mathrm{dc,total}} = 10.3\,\mathrm{kV}$ AND NOMINAL CURRENTS I_{N}, CORRESPONDING TO A CONSTANT TOTAL CHIP AREA AMONG THE DESIGNS, WHERE $I_{\mathrm{N,1700\,V}} = 150\,\mathrm{A}$ SERVES AS REFERENCE

V_{B}	n_{Cell}	u	I_{N}	V_{B}	n_{Cell}	u	I_{N}
600 V	29	0.592	81 A	3300 V	6	0.520	217 A
1200 V	15	0.572	124 A	4500 V	4	0.572	292 A
1700 V	11	0.551	150 A	6500 V	3	0.528	343 A

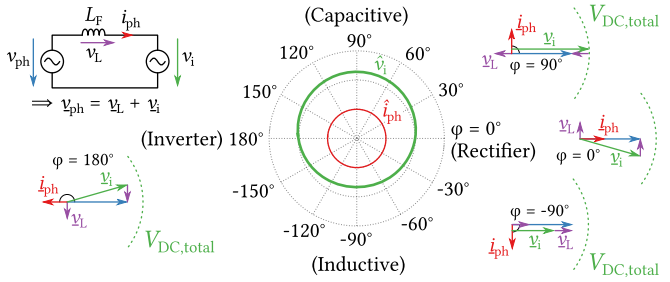

Fig. 8. Dependence of the required inverter output voltage amplitude $\hat{v}_{\mathrm{i}} = M \cdot V_{\mathrm{dc,total}}$ on the desired phase angle between grid voltage and current, φ. The capacitive operating point ($\varphi = 90°$) limits the maximum feasible filter inductance, L_{F}, for a given total dc voltage.

of the CHB system shown in Fig. 1(a) is performed in the following.

A. System Modeling and Optimization Procedure

As shown in Fig. 1, the grid voltage (line to line) of the considered example system is $V_{\mathrm{N}} = 10\,\mathrm{kV}$ and the nominal (three phase) power is $P_{\mathrm{N}} = 1$ MVA. Note that due to the phase-modular nature of the three-phase configuration, it is sufficient to confine the analysis to one phase stack with a nominal power of $P_{\mathrm{ph}} = 333$ kVA.

1) Blocking Voltage Utilization and Number of Cells: The analytic discussion before indicated that the optimum blocking voltage would be 1710 V, corresponding to 10.9 cascaded cells. However, in reality of course IGBT modules are only available with discrete blocking voltages, and only an integer number of cascaded cells can be used. Hence, if the blocking voltage utilization, u, was set to the equal value for all blocking voltages, the total dc link voltages would differ between the designs, and hence their output voltage capabilities would be different. Therefore, the total dc link voltage is set to be equal for all designs according to (9) with $M_{\mathrm{nom}} = 0.8$, resulting in $V_{\mathrm{dc,total}} = 10.3\,\mathrm{kV}$. Then, the number of cascaded cells featuring devices with a certain blocking voltage is chosen such that the blocking voltage utilization lies within $u = 0.55 \pm 0.05$. Table I shows the resulting number of cascaded cells and utilizations for the considered blocking voltages.

2) Filter Inductance Value: Fig. 8 shows a fundamental frequency equivalent circuit of the phase stack, comprising the grid phase voltage, v_{ph}, the filter inductance, L_{F}, and the inverter voltage, v_{i} (i. e., the output voltage generated by the cascaded cells phase stack). Considering a constant phase current amplitude, the required inverter voltage amplitude varies with the power factor, i. e., with the phase angle between the phase voltage and the phase current, because of the voltage drop across the filter inductance, v_{L}. As shown in Fig. 8, the worst case operating point, i. e., the highest inverter voltage amplitude requirement, occurs in the capacitive operating point ($\varphi = 90°$). Since the inverter voltage is limited by the total dc voltage, i. e., $\max(\hat{v}_{\mathrm{i}}) \leq M_{\max} \cdot V_{\mathrm{dc,total}}$, there is an upper limit for the filter inductance, L_{F}. If the capacitive operating point should be reachable at nominal current and $M_{\max} = 1$, the filter inductance is constrained by

$$L_{\mathrm{F}} \leq L_{\mathrm{F,max}} = \frac{V_{\mathrm{dc,total}} - \sqrt{2/3}V_{\mathrm{LL}}}{2\pi f_{\mathrm{g}} \hat{i}_{\mathrm{ph}}} \approx 26.1\,\%\,\mathrm{pu}. \quad (25)$$

3) Filter Inductance Modeling: The losses and volume of a filter inductor with a certain inductance, L_{F}, and stressed by a certain phase current, i_{ph}, are obtained from a local $\eta\rho$-Pareto optimization, which sweeps the dimensions of the inductor's core as well as the number of turns over wide ranges to obtain a large number of inductor designs. For each of these inductor designs, winding losses are calculated for round solid copper wires, neglecting HF losses in the winding, which is a feasible approximation since the inductor current equals the grid current, where harmonics above 1 kHz are limited to below 1 % by IEEE 519 [42], i. e., the squares of the rms current components at frequencies above 1 kHz are limited by $i_{\mathrm{rms}}(f > 1\,\mathrm{kHz})^2 < (0.01)^2 \cdot i_{\mathrm{rms}}(f_{\mathrm{g}})^2 = 0.0001 \cdot i_{\mathrm{rms}}(f_{\mathrm{g}})^2$. Therefore, even if the ac resistance at the harmonic frequencies would be a factor of 100 larger than at the fundamental (grid) frequency, the loss contribution of the current harmonics would be below $0.0001 \cdot i_{\mathrm{rms}}(f_{\mathrm{g}})^2 \cdot 100 \cdot R_{\mathrm{ac}}(f_{\mathrm{g}}) = 0.01 \cdot i_{\mathrm{rms}}(f_{\mathrm{g}})^2 R_{\mathrm{ac}}(f_{\mathrm{g}})$, i. e., only around 1 % of the losses at the grid frequency. Core losses are calculated for laminated silicon steel cores (M165-35S material). HF core losses are considered using the iGSE approach [44], because the core losses of this type of material are quite sensitive to flux components at high frequencies. The thermal limit is observed by assuming a surface heat transfer coefficient of $15\,\mathrm{W/(m^2K)}$ (typical value for natural convection in air [45]), an ambient temperature of 50 °C, and a maximum allowable surface temperature of 100 °C. Designs that generate losses that cannot be dissipated under these conditions are discarded. In addition, all designs that cannot carry twice the rated current without saturation of the core are discarded in order to ensure that the inductor can contribute to current limiting during fault situations, e. g., overcurrent or grid overvoltage surges [46]. Finally, four designs from the resulting $\eta\rho$-Pareto front of the inductor are chosen: the most efficient one, the one with the highest power density, and two trade-off designs which are identified by allowing for a 25 % volume increase over the smallest design and then selecting the most efficient one within this volume range, or by allowing for a 25 % loss increase over the most efficient design and then selecting the smallest one within this efficiency range, resulting typically in designs close to the "knee" of the Pareto front.

4) Semiconductor Losses: The losses of the power semiconductors are calculated using either virtual devices for a certain V_{B} and I_{N} rating as discussed in Section II, where I_{N} can

again be chosen such that the total silicon area is equal for all designs, leading to the values shown in Table I. Alternatively, it is also possible to directly use datasheet conduction loss and switching loss characteristics of specific devices. Note that here, in contrast to the analytical approach described in Section II, the losses of the IGBTs and diodes are calculated individually, i. e., separate loss models are used for IGBTs and diodes, whereby the device currents of a specific converter cell can be obtained from the phase current and the modulation function.

5) Heat Sink Modeling: To remove these losses from the semiconductors and to ensure a junction temperature of $T_j = 125\,°C$, appropriate heat sinks are required. Considering a single heat sink per cell, the thermal resistances from junction to heat sink of the individual power devices, i. e., IGBTs and diodes, obtained from the models discussed in Section II, $R_{th,JH,i}$, together with the individual losses, $P_{loss,i}$, allow to calculate the maximum allowable heat sink temperature as

$$T_{HS,max} = \min_i (T_j - P_{loss,i} \cdot R_{th,JH,i}). \tag{26}$$

The cooling system performance index (CSPI) [47], which characterizes the capability of certain cooling methods in terms of power dissipation capability per volume and temperature difference, i. e., [CSPI] = W/(K dm^3), is then used to estimate the volume of the heat sink according to

$$V_{HS} = \frac{1}{\text{CSPI} \cdot R_{th,HS}} \quad \text{with} \quad R_{th,HS} = \frac{T_{HS,max} - T_A}{\sum_i P_{loss,i}}, \tag{27}$$

where T_A denotes the ambient temperature (50 °C). For a typical forced air cooling system, CSPI = 10 W/(K dm^3) is assumed here [47]. If for a certain design the required $R_{th,HS}$ becomes negative due to excessive losses, the design is discarded.

6) DC Link Capacitors: The dc link capacitances of the converter cells are chosen such as to result in a peak-to-peak voltage ripple of 10 %. This is mainly a ripple at twice the grid frequency, because the difference between the ac-side power that is $\propto \sin(2\pi f_g t)^2$ and the dc-side power which is constant needs to be buffered. Note that, therefore, the total energy buffering capability of a phase stack at twice the grid frequency does not depend on the number of cells, while of course additional current components at the respective switching frequency might cause slight differences in the capacitance requirements for designs based on different blocking voltages. The capacitor current of a specific cell can be calculated from the phase current, the modulation function, and the (constant) dc current, which leads directly to the required capacitance value for a given voltage ripple criterion. The capacitor volume is then estimated from the capacitance value and the dc voltage by assuming a constant volume per stored energy of 6.3 cm^3/J, which has been found by averaging the datasheet values of polypropylene foil capacitors of various capacitance and voltage ratings (600 V to 1300 V), and from different manufacturers. This value corresponds to an energy density of 0.16 J/cm^3, which is in agreement with data reported in [48].

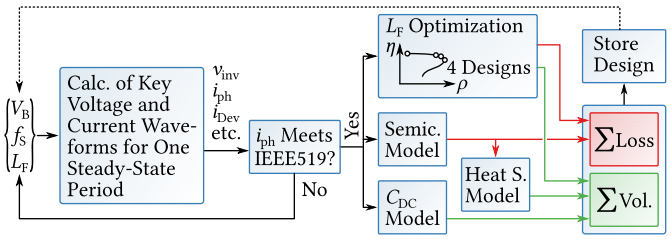

Fig. 9. Flowchart illustrating the optimization procedure used to calculate many design points allowing for the $\eta\rho$-Pareto fronts in Fig. 10(a) to be extracted. The component models and the overall optimization procedure are described in Section III-A.

7) Optimization Procedure: Considering here again full-load operation in ac–dc rectifier mode with unity power factor, for each of the common IGBT blocking voltages, V_B, the cell switching frequency, f_s, and the filter inductance, L_F, are swept over wide ranges (200 Hz…30 kHz and 1 µH…80 mH < $L_{F,max}$, respectively). As shown in Fig. 9, for each tuple $\{V_B, f_s, L_F\}$, the main converter waveforms can be numerically calculated for one steady-state period at full-load operation, whereby PWM modulation with phase-shifted carriers [34], [35] is considered. The superposition of the switched ac output voltage waveforms of all converter cells yields together with the grid voltage and the filter inductor the output phase current. If a design's phase current spectrum does not comply with IEEE 519, the design is discarded. Else, the loss and volume contributions of the main components are calculated as described above, resulting in an efficiency, η, and a power density, ρ, for each $\{V_B, f_s, L_F\}$. The power density is obtained from the sum of the main component volumes, and is then scaled with a factor $C_p = 0.7$ in order to account for spacing between components, etc., as suggested in [33].

B. Pareto Optimization Results and Discussion

Each $\{V_B, f_s, L_F\}$ combination can be plotted as a point in the $\eta\rho$-plane, and these points can then be grouped by blocking voltages to obtain the Pareto fronts shown in Fig. 10(a), where, as in the analytic calculations in Section II, virtual semiconductors with rated currents, I_N, corresponding to equal total silicon area for all designs have been considered to model the semiconductor losses. The current ratings are therefore obtained with (22), where the $v_{CE}(I_N)$ characteristics of IGBTs and a reference design employing 1700 V semiconductors with $I_{N,1700\,V} = 150$ A are considered. Table I shows the resulting current ratings for all blocking voltages.

All in all, the outcome of the Pareto optimization indicates that designs based on 1200 V or 1700 V devices offer the most suitable trade-off between efficiency and power density for the considered system, whereas designs based on devices with higher blocking voltages are not competitive. This confirms the results from the analytical considerations of Section II.

The shape of the Pareto fronts can be explained as follows: starting from very low power densities, an increase of the switching frequency allows reducing the inductance and hence the size of the filter inductor, while still meeting the current

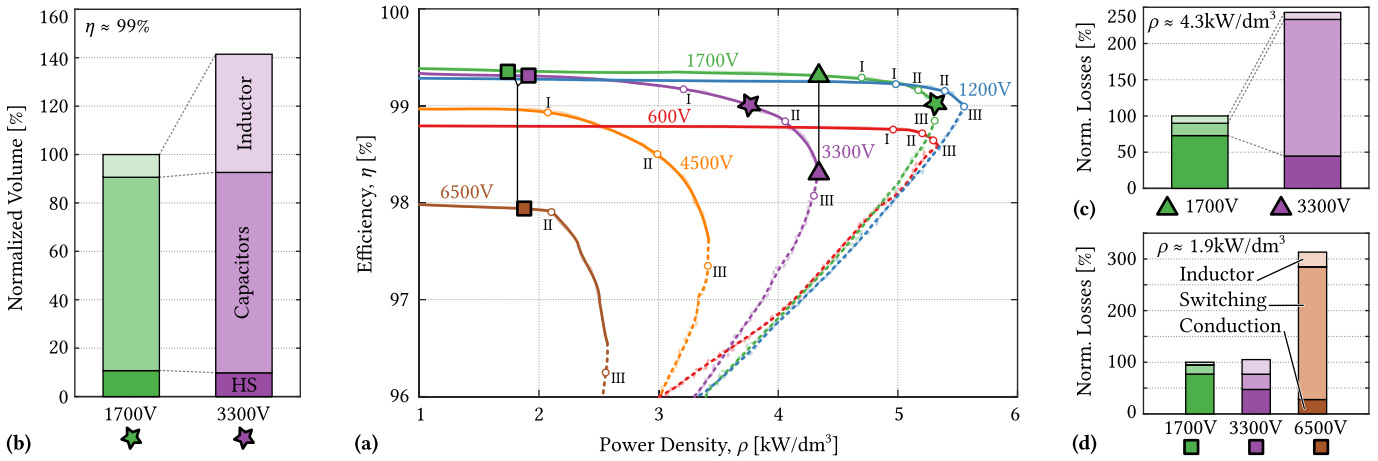

Fig. 10. (a) Results of the $\eta\rho$-Pareto optimization of a 1 MVA system (operating in ac–dc rectifier mode with unity power factor) connected to the 10-kV grid and based on virtual IGBT modules with current ratings, I_N, according to Table I, i. e., with equal total silicon area for all designs. The roman numbers I, II, and III indicate approximate device switching frequencies of I → 500 Hz, II → 1 kHz, and III → 2 kHz; Table II shows the resulting effective switching frequencies of the multilevel output voltage waveforms. (b) Component volume distribution of two designs based on 1700 V and 3300 V IGBTs, respectively, that feature the same efficiency of $\eta = 99\,\%$. (c) Loss distribution of a 1700 V and 3300 V design, featuring the same power density (the maximum power density achievable with 3.3 kV IGBTs). (d) Loss distribution at a much lower power density, also including a 6.5 kV design.

TABLE II

EFFECTIVE SWITCHING FREQUENCIES OF THE OUTPUT VOLTAGE WAVEFORMS FOR DIFFERENT BRIDGE LEG SWITCHING FREQUENCIES, f_S [SEE FIG. 10(A)]. NOTE THAT $f_S = 500$ Hz IS NOT FEASIBLE FOR THE 6.5 kV DESIGNS, BECAUSE THE FILTER INDUCTANCE L_F IS LIMITED.

V_B	n_{Cell}	I $f_S \approx 500$ Hz	II $f_S \approx 1$ kHz	III $f_S \approx 2$ kHz
600 V	29	29 kHz	58 kHz	116 kHz
1200 V	15	15 kHz	30 kHz	60 kHz
1700 V	11	11 kHz	22 kHz	44 kHz
3300 V	6	6 kHz	12 kHz	24 kHz
4500 V	4	4 kHz	8 kHz	16 kHz
6500 V	3		6 kHz	12 kHz

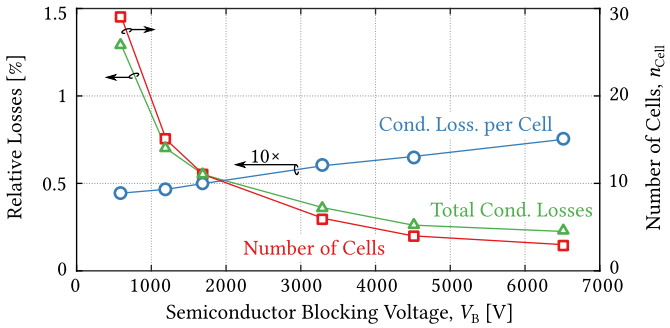

Fig. 11. Conduction losses per cell and total conduction losses, and number of cells used in the Pareto optimization as a function of the blocking voltage. Note that the conduction losses per cell (blue curve) are multiplied by a factor of 10 for better visibility. Even though the losses per cell are increasing with the blocking voltage, the total conduction losses decrease because $n_{Cell} \propto 1/V_B$.

harmonic limits. As the switching frequency increases, so do the switching losses, causing the efficiency to decrease, which is much more pronounced for higher blocking voltages, because both the required switching frequencies (lower number of cells) and the normalized switching energies are higher. For lower blocking voltages, the efficiency does not decrease significantly over a wide range of power densities, because these designs are dominated by conduction losses, as shown in Fig. 11, which shows the dependence of the conduction losses on the blocking voltage: for lower blocking voltages, the conduction losses *per cell* become lower, but only slightly because bipolar devices are considered, whereas the number of cells increases sharply. Thus, the total conduction losses increase for lower blocking voltages, e. g., to more than 1 % for 600 V designs, which is directly reflected by the corresponding Pareto front in Fig. 10(a). Since these losses are independent of the switching frequency, an increase of the filter inductance and thus also the filter inductor size (and hence a decrease of the power density) does simply lead to current harmonics far below the IEEE 519 limits, but cannot significantly improve the system efficiency, which explains the flat shape of the Pareto fronts for designs based on lower blocking voltages. For all designs, the maximum power density point is reached when the decrease of the filter inductance with a further increase of the switching frequency is overcompensated by the increase of the heat sink volume that is required to dissipate the increasing (switching) losses.

To further illustrate these effects, Fig. 10(b) shows the volume distributions among the main components of a 1700 V design and a 3.3 kV design, which both feature $\eta \approx 99\,\%$. As discussed above, the capacitor volume is similar, and due to the high efficiency, the heat sink volume is rather small and almost equal to in both designs. However, in order to achieve this high efficiency with the 3.3 kV design, a very large filter inductor is required to allow a sufficient reduction of the switching frequency and hence the switching losses. This explains the lower power density of the design with higher blocking voltage devices at the same efficiency. In addition, Fig. 10(c) shows the loss distribution of a 1700 V design and a 3.3 kV design, which both feature the same power density of $\rho \approx 4.3\,\text{kW/dm}^3$, corresponding to the maximum power density achievable with designs based on 3.3 kV devices. Whereas the conduction losses are higher in the 1700 V design as discussed above, the switching losses of

the 3.3 kV design are significantly higher as a consequence of the high switching frequency that is required to reduce the size of the filter inductor sufficiently. This explains the higher losses of the design with higher blocking voltage devices at the same power density. Finally, Fig. 10(d) shows the loss distributions at a very low power density for a 1700 V, a 3.3 kV, and a 6.5 kV design. The 1700 V and the 3.3 kV designs achieve a similar efficiency, but by different means: whereas conduction losses dominate in the 1700 V design, the 3.3 kV design shows higher switching losses and higher losses in the filter inductor, which is again a consequence of the higher required switching frequency and/or the increased filtering effort to compensate for the lower number of cells. The 6.5 kV design shows much higher losses due to very high switching losses. Any option to improve the efficiency of designs based on 6.5 kV devices would therefore require higher filter inductance values, which would allow a reduction of the switching frequency. To do so, either the requirement that the capacitive operating point must be achievable at rated current could be relaxed, or, alternatively, the total dc link voltage, and hence the number of cells, could be increased.

Note that in grid-connected systems, considerations regarding the protection against overvoltages, e. g., lightning strikes, and against overcurrents might require a minimum value of the filter inductance, L_F, to limit fault currents [8], [46]. Such a lower bound on L_F would reduce the maximum achievable power densities, which would affect especially the designs based on low blocking voltages, because these can fulfill the current harmonic criteria with very low filter inductances due to the high number of levels and the high effective switching frequencies, resulting in high power densities [see also Fig. 10(b)]. On the other hand, even at lower power densities, these designs still provide an efficiency benefit over designs with higher blocking voltages, as shown in Fig. 10(c).

IV. Silicon Carbide Power Semiconductors

Recent developments in SiC technology point in two directions: first, ever higher blocking voltages, exceeding those achievable with silicon power semiconductors, are aimed for mainly in prototype devices [23], [24], and second, LV SiC MOSFETs with very low on-state resistances have reached maturity and are available in standard power module packages [27]–[29]. HV SiC devices could allow to reduce the number of cells for a given line voltage or even enable single-cell solutions, and LV SiC devices applied in cascaded converter cells are expected to improve efficiency and power density over systems based on silicon IGBTs. Sections IV-A and IV-B discuss these aspects.

A. Low-Voltage SiC Power Modules

Significant improvements can be expected from replacing LV Si devices by their SiC counterparts in cascaded cells systems, as it is now possible to obtain suitable SiC power MOSFETs in standard 62 mm packages with very low on-resistances, e. g., 1200 V/13 mΩ [27], 1200 V/5 mΩ [28], or 1700 V/8 mΩ [29]. This motivates an application of the $\eta\rho$-Pareto optimization procedure described in Section III to

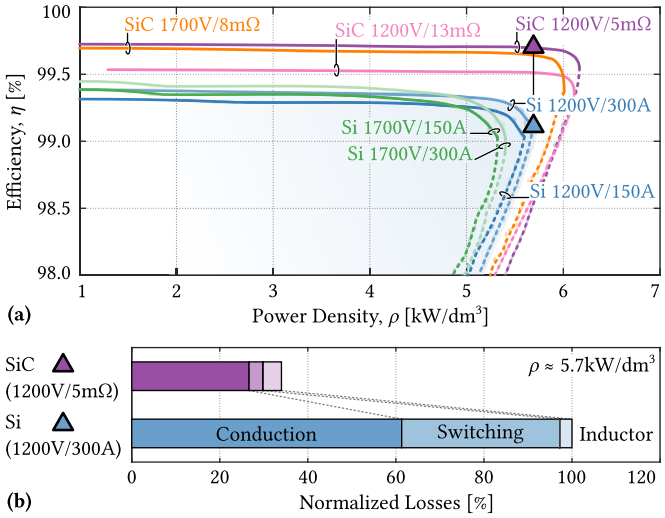

Fig. 12. (a) Comparison of Pareto fronts of designs based on silicon IGBTs (see also Fig. 10) and SiC power MOSFET modules. (b) Loss distribution of a SiC and a Si design featuring the same power density (the maximum power density achievable with Si designs).

designs based on such LV SiC power modules. To account for the higher allowable junction temperatures of SiC devices, $T_{\mathrm{j,SiC}} = 150\,^\circ\mathrm{C}$ is considered, and since SiC devices can cope with higher blocking voltage utilizations [49], [50], $u_{\mathrm{SiC}} \approx 0.7$ is assumed. In addition, the switching frequency search range has been increased up to 100 kHz. The loss characteristics of the SiC semiconductors have been taken directly from the respective datasheets. Because the available SiC power modules are rated at roughly 200 A to 300 A, virtual IGBT modules with nominal currents of 150 A and also of 300 A have been considered for comparison purposes.

Fig. 12(a) shows the resulting Pareto fronts and compares them with the Pareto fronts of the best Si-based designs. It can be seen that both efficiency and power density of cascaded cells systems can be significantly increased if silicon IGBTs are replaced by LV SiC power modules. Considering the same power density, SiC designs show significantly lower losses [see Fig. 12(b)], which reduces the required heat sink volume. This, in turn, allows for a larger inductor, and hence a lower switching frequency in the SiC designs, which, in combination with the superior switching properties, explains the very low switching losses of the SiC design. Note also that the 1200 V SiC solution has a higher efficiency than the 1700 V SiC solution in the region of dominating conduction losses, which is to be expected for unipolar MOSFET devices, where the specific on-state resistance scales roughly as $r_{\mathrm{ON}} \propto V_\mathrm{B}^{2.5}$ [37]. On the other hand, the common-mode ground current issues observed in cascaded cells converter systems [51] worsen with increasing dv/dt values, which are typically higher with SiC than with Si devices. This needs to be considered during the converter design, or especially during retrofitting operations.

B. High-Voltage SiC Devices

The availability of SiC devices with blocking voltages of 15 kV and beyond would in theory allow to interface the 10-kV grid with a single two-level H-bridge converter, i. e.,

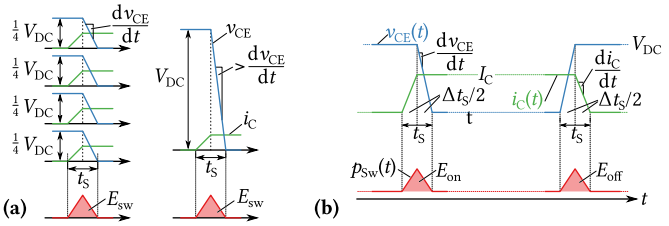

Fig. 13. (a) Increase of required dv/dt to obtain equal switching energies in a single-cell system as in a corresponding multi-cell system. (b) Simplified modeling of turn-on and turn-off losses for the HV SiC devices.

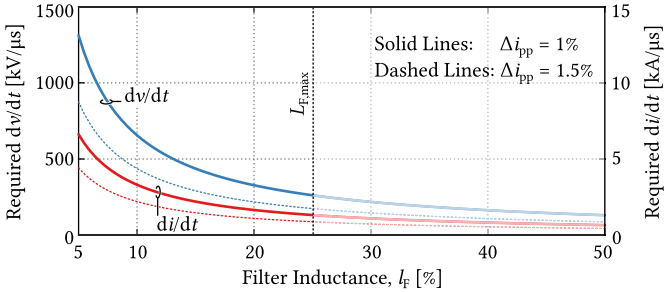

Fig. 14. Required dv/dt and di/dt [see Fig. 13(b)] to obtain relative switching losses of 0.5 % with a single-cell HV SiC solution as a function of the filter inductance and for two different current ripple limits. $L_{F,max}$ is the maximum allowable inductance value if the pure capacitive operating point must be achievable with rated current and $V_{dc,total} = 10.3$ kV.

reducing n_{Cell} to one. However, as discussed earlier, this is associated with a massive increase of the required switching frequency compared with a multi-cell solution. Therefore, the switching characteristics which such devices would require in order to be competitive with multi-cell solutions are investigated in the following.

If a given total dc voltage, V_{dc}, is switched by, e. g., four cascaded converter cells, the total switching energy that results from the overlap of voltage and current for four switching transitions can be approximated as [see Fig. 13(a)]

$$E_{sw} = 4 \cdot \left(\frac{1}{4} V_{dc} \cdot I_C \cdot t_S \cdot \frac{1}{2} \right) = \frac{1}{2} \cdot V_{dc} \cdot I_C \cdot t_S \qquad (28)$$

where t_S denotes the duration of the switching transition. If the same total dc voltage should be switched by a single HV device such that the same switching energy results, the same switching time t_S is required. This, however, corresponds to an increase in dv/dt by a factor of 4 (if, as here, the di/dt is assumed to be the same). Furthermore, the four transitions of the multi-cell system would not occur at the same time, but would be phase-shifted with respect to each other, thereby increasing the effective switching frequency and reducing the magnitude of the voltage steps seen by the filter inductor as discussed earlier. If the single-cell design should provide the same switching *losses*, it therefore would need to achieve even shorter switching transitions and hence higher dv/dt (and di/dt) to compensate the high required switching frequency if the same filter inductor and the same current ripple limit would be considered as in the multi-cell case.

The switching characteristics of an HV SiC device are approximated in dependence of the total switching duration, t_s, as shown in Fig. 13(b), where, taking the example of the turn-off transition, the voltage across the switch rises to the dc voltage, e. g., within $t_S/2$, and where the current decays from its nominal value to zero during the second half of t_S. Therefore, the involved switching characteristics are

$$\frac{di_C}{dt} = \frac{I_C}{t_S/2} \quad \text{and} \quad \frac{dv_{CE}}{dt} = \frac{V_{dc}}{t_S/2}. \qquad (29)$$

Assuming $E_{OFF} = E_{ON} = E_{sw}$, as shown in Fig. 13(b), the total switching losses of the single-cell solution can be approximated as

$$P_{sw} = 4 f_{s,2L} \cdot E_{sw} = 4 f_{s,2L} \cdot \frac{1}{2} t_S \bar{i}_{ph} V_{dc}, \qquad (30)$$

where the required switching frequency, $f_{s,2L}$, can be calculated with (15). Thus, by defining a switching loss budget of 0.5 %, the required switching characteristics in terms of t_S, and thus di/dt and dv/dt, can be calculated directly, whereby the results depend on the filter inductance and the inductor current ripple limit. Fig. 14 shows that extreme dv/dt and di/dt values ranging up into the MV/µs range would be required—while 0.5 % switching losses correspond already to a similar efficiency as can be achieved with silicon multilevel solutions, *including* also conduction and inductor losses (see Fig. 10). Note also that, for example, a dv/dt of 1 MV/µs would result in common-mode current peak values of 10 A even for a very small common-mode capacitance of 10 pF, clearly indicating that the application of HV SiC power devices would pose significant challenges regarding Electromagnetic Interference (EMI) filtering, EMI immunity of control and driving circuits, and also isolation stress. If, on the other hand, dv/dt values must be limited, the switching energies increase, and hence the feasible switching frequencies for a given efficiency target decrease, which must be compensated by a higher filtering effort with an adverse impact on power density.

Although a two-level solution could be designed with very low complexity, especially considering a three-phase system, where also dc capacitance requirements could be reduced when compared with the three individual single-phase stacks, the above considerations clearly indicate that HV SiC technology, at least in the near future, will not supercede the need for cascading converter cells in MV and of course also in HV applications, at least in the case when a high power density is required.

V. Reliability Considerations

The considerations presented in Sections III and IV indicate that designs featuring a comparably high number of cascaded cells achieve favorable performance. However, on the other hand, high component counts are generally associated with reduced reliability. This notion is investigated in the following, whereby the calculations are based on a reliability textbook [52] to which the interested reader is referred for more detailed derivations.

A. Reliability Basics

The reliability of a component can be expressed by its *failure rate*, λ, with $[\lambda] = 1\,\text{FIT} = 1/10^{-9}\,\text{h}$, i. e., 1 FIT (Failure in Time) corresponds to statistically one failure per one billion

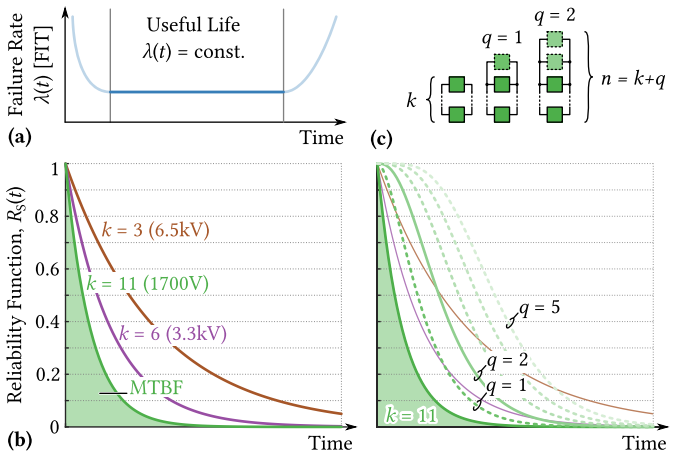

Fig. 15. (a) Typical evolution of a component's failure rate over time ("bathtub curve"). (b) Reliability function dependent on the number of elements (cascaded cells with equal failure rate per cell), where the system-level $\mathrm{MTBF_S}$ is indicated as the area below the reliability function. (c) Improvement of the reliability by adding q redundant cells to the k cells strictly required for system operation.

hours of operation. In general, the failure rate is a function of time with the typical "bathtub" shape, as shown in Fig. 15(a): initially, the failure rate is high as a consequence of production quality fluctuations. These "early failures", however, should be filtered out by manufacturers' quality control measures. During the useful life of a component, the failure rate is approximately constant, which corresponds to a random distribution of failures, e. g., cosmic ray-induced failures in power semiconductors. Toward the end of a component's life time, wear-out failures, e. g., bond-wire lift-off or solder delamination as a consequence of thermal cycling and material fatigue, cause the failure rate to increase again. Wear-out failures could be addressed by preventive maintenance measures. Thus, here only the useful life phase is considered, where $\lambda = \text{const}$. The failure rate, λ_S, of a system consisting of several components that all are required to work for the entire system to be operational can be calculated as the sum of the individual components' failure rates, which simplifies to $\lambda_\mathrm{S} = k\lambda$ if k equal components are considered.

The *reliability function*, $R_\mathrm{S}(t)$, expresses the probability that a system with k components (or, e. g., converter cells), each of which having a failure rate of λ, is still operational after t hours:

$$R_\mathrm{S}(t) = e^{-k\lambda t}. \tag{31}$$

Fig. 15(b) shows the evolution of the reliability function over time for different values of k. Thus, considering a cascaded cells system with k being the number of cells, the probability that a system is still operational after a certain time decays with increasing number of cells. The area below the reliability function equals the *mean time between failures* of the system, $\mathrm{MTBF_S}$,[1] that is

$$\mathrm{MTBF_S} = \int_0^\infty R_\mathrm{S}(t)dt \overset{\lambda=\text{const.}}{=} \frac{1}{k\lambda}. \tag{32}$$

[1]The term MTFB usually refers to systems that are repaired; else, the term MTTF (mean time to failure) is used. However, since both cases are looked at here, only the term MTBF is used to improve readability.

Because of the modular nature of cascaded cells converter systems, *redundancy* can be implemented by adding q additional cells to the k cells that are strictly required for the system to be operational (i. e., to provide enough total dc voltage). Such a configuration features then a total of $n = k+q$ cells, and is called *k-out-of-n-redundant*, because it remains operational as long as k out of n cells are operational. Adding redundant cells to a system improves the reliability, as can be seen from Fig. 15(c), and is therefore a mighty tool to alleviate the impact of a high component count on the system reliability, as has been discussed already in the 1990s for the case of paralleled converter cells [53] and later also for series/parallel structures [54]. In the following, the concept is applied to the cascaded cells system discussed in this paper, whereby also the cost of adding redundant converter cells is taken into account.

B. Reliability of Multi-Cell Systems With Redundancy

There are two different variants of how k-out-of-n redundancy can be implemented on the system level, i. e., with k and n referring to entire converter cells, each of which having a cumulative failure rate of λ_Cell: standby redundancy and active redundancy with load sharing, which will be described in detail after an initial discussion of the cell failure rate, λ_Cell.

A converter cell contains parts whose failure rates can be assumed to not depend on the blocking voltage, e. g., control electronics, and other components whose failure rates do depend on the blocking voltage. In particular, the power semiconductors are falling in this category, since the required semiconductor chip area for the same rated current depends on the blocking voltage (see the Appendix) and the failure rate, in turn, depends on the chip area [31]. Therefore, the cumulative failure rate of a cell is modeled to contain a constant part and a part that depends on the blocking voltage according to

$$\lambda_\mathrm{Cell}(V_\mathrm{B}) = \lambda_\mathrm{B} \cdot (a + b \cdot f(V_\mathrm{B})) \quad \text{with} \quad a + b = 1, \tag{33}$$

where to account for the dependence of the required chip area on the blocking voltage

$$f(V_\mathrm{B}) = \frac{v_\mathrm{CE}(V_\mathrm{B})}{v_\mathrm{CE}(1700\,\mathrm{V})}, \tag{34}$$

if the base fit rate λ_B and the parameters a and b are specified for a 1700 V design. Note that for reasons of simplicity, this implies the same nominal currents for all modules. To give an impression of the order of magnitude of a numerical value for λ_B, typical failure rates for one IGBT module are between 10 FIT and 100 FIT, depending on the operating conditions such as the blocking voltage utilization, and the altitude above sea level due to increased cosmic ray activity [30], [31]. Note that according to field experience information from industry, the failure rate of a combination of an IGBT module and its gate drive unit is dominated by the power module, not the gate drive unit. Considering entire converter cells, Grinberg *et al.* [55] report 1000 FIT for a modular multilevel (M2LC) converter cell containing one 1700 V IGBT module, a dc link capacitor, and control electronics. However, it must be highlighted that λ_B cancels out in the comparative results derived in the following, and hence the actual value assumed for λ_B is not important.

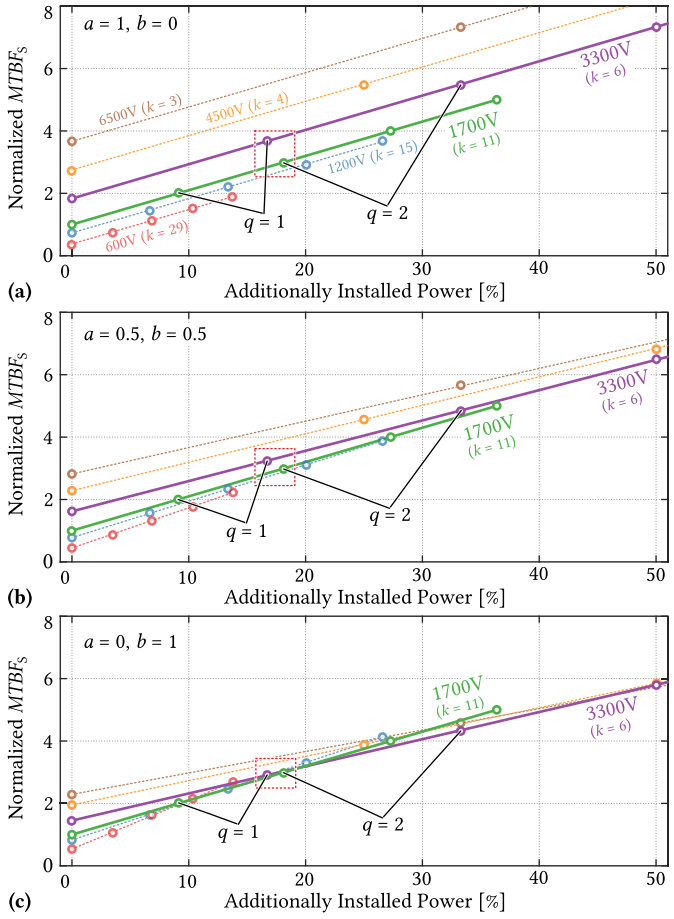

Fig. 16. Standby redundancy: $\mathrm{MTBF_S}$ (normalized to the 1700 V design without redundancy) versus additionally installed power capability for different blocking voltages (and therefore different numbers of required cells, k). (a) Constant failure rate per cell ($a = 1, b = 0$). (b) 1:1 distribution between a constant and a blocking-voltage dependent part of the cells' failure rates ($a = 0.5, b = 0.5$). (c) Only a blocking-voltage dependent part ($a = 0, b = 1$).

1) Standby Redundancy: In this case, the q redundant cells are not active but simply in a ready state, which would allow them to immediately start taking over the power and voltage shares of a failing cell. Since in this reserve state the cells' stress level is significantly lower than that of cells in operation, the failure rate in the reserve state is assumed to be zero. Under these conditions, the $\mathrm{MTBF_S}$ for the complete system (i. e., one phase stack) is given by

$$\mathrm{MTBF_S} = \frac{n-k+1}{k\lambda_{\mathrm{Cell}}(V_{\mathrm{B}})}. \tag{35}$$

Since $n - k = q$ is the number of reserve cells, the $\mathrm{MTBF_S}$ increases with the amount of reserve cells [see also Fig. 15(c)]. However, adding additional cells to a system, i. e., additional power processing capability that is not utilized during normal operation, is associated with costs. Therefore, Fig. 16 shows the normalized $\mathrm{MTBF_S}$ versus the additionally installed power capability for systems based on different blocking voltages, and hence different numbers of required cells, k. Note that $\mathrm{MTBF_S} \propto 1/\lambda_{\mathrm{Cell}}(V_{\mathrm{B}}) \propto 1/\lambda_{\mathrm{B}}$ and that therefore λ_{B} cancels out when the $\mathrm{MTBF_S}$ values are normalized—the results shown in Fig. 16 do not depend on λ_{B}.

Consider the highlighted designs based on 1700 V and 3.3 kV devices. If about the same additionally installed power capability is considered, *two* additional cells can be added to the 1700 V design, whereas only *one* spare cell can be added to the 3.3 kV design—resulting in comparable $\mathrm{MTBF_S}$ values for both configurations, even though the 1700 V design features almost twice as many converter cells. To indicate the sensitivity on the distribution between constant and blocking-voltage dependent parts of the cells' failure rates, results for three different combinations of a and b [$(a = 1, b = 0)$, $(a = 0.5, b = 0.5)$, and $(a = 0, b = 1)$] are shown in Fig. 16(a)–(c), respectively. Although there is an impact, the general conclusion that with similar additionally installed power capability also similar $\mathrm{MTBF_S}$ values can be achieved, regardless of the actual number of cascaded cells, remains valid, especially considering that the case $(a = 1, b = 0)$, i. e., no dependence of λ_{Cell} on the blocking voltage, is rather optimistic, since it seems a reasonable assumption that a cell featuring higher blocking voltage devices and hence also a higher power rating typically would also show a higher complexity and hence a higher failure rate.

2) Active Redundancy With Load Sharing: Instead of keeping the reserve cells in a waiting state, they could also participate in the system operation, which would reduce the power processed per cell, and hence reduce the stress level of all cells, but on the other hand increase the number of cells experiencing this reduced stress. The failure rate of the reserve cells is thus not zero anymore, but equal to that of all the other cells. In addition, the failure rate of the cells depends on how many cells are still operational and share the total stress.

According to [56], the temperature-dependence of the semiconductors' failure rates can be expressed as

$$\lambda(T_{\mathrm{j}}) = \lambda_{100\,^\circ\mathrm{C}} \cdot \pi_{\mathrm{T},i} \quad \text{with} \quad \pi_{\mathrm{T},i} = e^{3480\left(\frac{1}{373} - \frac{1}{T_{\mathrm{j},i}+273}\right)}. \tag{36}$$

Since (36) is valid for power semiconductors only, the case $a = 0$ and $b = 1$ is considered here, i. e., it is assumed that a cell's failure rate is dominated by the power module's failure rate, which depends on the blocking voltage as described above. Assuming further as an approximation that the total system losses were not affected by the number of cells involved in the power processing (for the same blocking voltage) and neglecting the semiconductor losses' dependence on the junction temperature, the losses that need to be dissipated by the power semiconductors of each converter cell depend only on the number of active cells. Let i denote the number of defective cells, i. e., $0 \le i \le n - k$ while the system is still operational. The junction temperature varies then according to

$$T_{\mathrm{j},i} = T_{\mathrm{A}} + \frac{P_{\mathrm{loss,total}}}{n-i} \cdot R_{\mathrm{th,cell}}, \tag{37}$$

showing an increase with each defective cell, and a maximum, $T_{\mathrm{j,max}}$, for $n - i = k$. With that, (37) can be made independent of $P_{\mathrm{loss,total}}$ and $R_{\mathrm{th,cell}}$:

$$T_{\mathrm{j},i} = (T_{\mathrm{j,max}} - T_{\mathrm{a}}) \cdot \frac{k}{n-i} + T_{\mathrm{a}}. \tag{38}$$

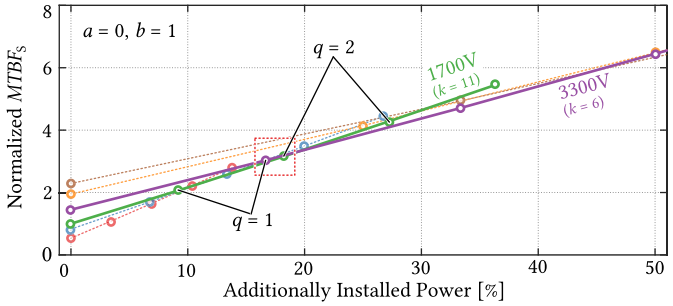

Fig. 17. Active redundancy: $\mathrm{MTBF_S}$ (normalized to the 1700 V design without redundancy) versus additionally installed power capability, considering only a blocking-voltage dependent failure rate ($a = 0$, $b = 1$).

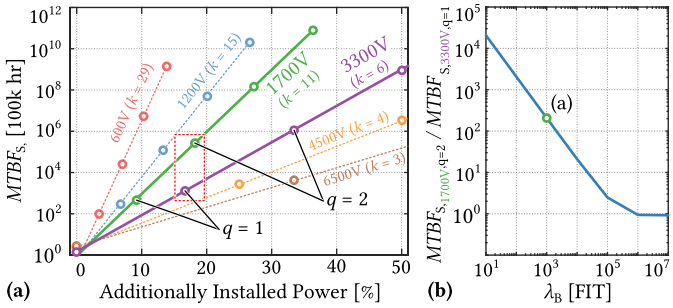

Fig. 18. (a) System-level (one phase stack) $\mathrm{MTBF_S}$ versus additionally installed power capability considering a repairable system with standby redundancy [$\lambda_\mathrm{B} = 1000\,\mathrm{FIT}$, $\mu = 1/(7 \cdot 24\,\mathrm{h})$, $a = 0.5$, $b = 0.5$]. (b) Impact of the base failure rate, λ_B, on the ratio between the $\mathrm{MTBF_S}$ values of a 1700 V design with $q = 2$ and a 3300 V design with $q = 1$.

The system-level mean time between failures becomes then

$$\mathrm{MTBF_S} = \sum_{i=0}^{n-k} \frac{1}{(n-i)\lambda_\mathrm{cell}(V_\mathrm{B})\pi_{\mathrm{T},i}}, \tag{39}$$

which is again $\propto \lambda_\mathrm{B}$. Therefore, the normalized results shown in Fig. 17 do not depend on the base fit rate, λ_B, either. Comparing the results with those for standby redundancy and $a = 0$ and $b = 1$ in Fig. 16(c) reveals only minor differences. Therefore, other factors such as, for example, the feasibility of immediately bypassing a faulty cell and turning on a reserve cell or, most prominently, the non-optimal number of cascaded cells during the nominal operating state with active redundancy should be carefully taken into account regarding decisions on a redundancy concept.

Additional potential lies in the possibility of not only reducing the thermal stress due to a reduction of the processed power per cell but also the voltage stress by reducing the cells' dc voltages as long as more cells than required are operational, since the failure rate of power semiconductors depends strongly on the blocking voltage utilization [30], [31]. However, whether this is possible or not depends on the realization of the cells' dc sources or loads. If, e.g., in an SST application [see Fig. 1(b)] dc–dc converters with a fixed voltage transfer ratio were used [57], the cells' dc voltages could not be changed if the LV dc bus voltage must maintain a certain value.

C. Reliability of Multi-Cell Systems With Redundancy and Repairability

In reality, a faulty cell in a system could be repaired as soon as possible. Depending on the implementation, this can even be possible as a hot-swap operation without service interruption on system level [58]. Repairability is an effective means of increasing the availability of systems with a high component count [59]. Again, based on derivations from [52], the $\mathrm{MTBF_S}$ value of a repairable system can be calculated from the following relations, which hold for the assumptions of there being only a single repair crew, defective cells being repaired while the system remains operational, and no further failures at system down (i.e., failures during the restoration time after the complete system has failed), as

$$\begin{aligned}
\mathrm{MTBF_{S,0}} &= \frac{1}{v_0} + \mathrm{MTBF_{S,1}} \\
\mathrm{MTBF_{S,}}_i &= \frac{1}{v_i + \mu}(1 + v_i \mathrm{MTBF_{S,}}_{i-1} + \mu \mathrm{MTBF_{S,}}_{i+1}) \\
&\qquad \text{for } i = 1, \ldots, n-k-1 \\
\mathrm{MTBF_{S,}}_{n-k} &= \frac{1}{v_{n-k} + \mu}(1 + \mu \mathrm{MTBF_{S,}}_{n-k-1})
\end{aligned} \tag{40}$$

where

$$v_i = k\lambda_\mathrm{cell}(V_\mathrm{B}) + (n-k-i)\lambda_\mathrm{cell,reserve} \tag{41}$$

and where μ denotes the repair rate and $\lambda_\mathrm{cell,reserve}$ is the failure rate for cells in the reserve state. If $\lambda_\mathrm{cell,reserve} = 0$ is considered (standby redundancy), the approximation

$$\mathrm{MTBF_{S,0}} \approx \frac{\mu^{n-k}}{(k\lambda_\mathrm{Cell}(V_\mathrm{B}))^{n-k+1}} \tag{42}$$

can be used, which illustrates directly that a higher failure rate, λ_Cell, can be compensated by increasing the repair rate, μ, accordingly.

Note that here λ_B does not cancel out if again a normalization would be used due to the exponent in the denominator of (42), and therefore, absolute values are given in Fig. 18(a), which shows the $\mathrm{MTBF_S}$ versus additionally installed power for the case of a repairable system with standby redundancy and a repair rate of $\mu = 1/(7 \cdot 24\,\mathrm{h})$, corresponding to a mean time to repair (MTTR) of one week. A base failure rate of $\lambda_\mathrm{B} = 1000\,\mathrm{FIT}$ is assumed [55], and $a = 0.5$ and $b = 0.5$ is considered. In contrast to the nonrepairable cases, now the $\mathrm{MTBF_S}$ value of the 1700 V design with two spare cells is significantly higher than that of a 3.3 kV design with one spare cell (again with about the same amount of additionally installed power capability). In the first case, after a first cell has failed, *two* more would have to fail before the repair of the first one is completed in order for the complete system to fail, whereas in the second case a single additional failure before completion of the repair leads to system down. Under the assumption of independent elements, the latter is much more likely, which corresponds to much lower $\mathrm{MTBF_S}$ values. Changing a and b does not alter this conclusion significantly, whereas λ_B affects the ratio between the $\mathrm{MTBF_S}$ values of

the 1700 V design with two spare cells and the 3.3 kV design with one spare cell, as is shown in Fig. 18(b). For typical failure rates, the 1700 V solution results in a significantly higher $\mathrm{MTBF_S}$, and even for very high λ_B, the ratio saturates close to unity.

All in all, the above discussion indicates that reliability considerations are not preventing the decision for designs with higher number of cascaded cells, especially as such designs can be superior regarding efficiency and power density as shown in Section III. Furthermore, a modular system design using many cascaded cells allows to lower MTTR figures and thus can help to improve the availability [59], for example by allowing for hot-swapping of defective converter cells against replacements stored on-site during full converter operation [58].

However, it should be kept in mind that with increasing number of redundant cells, the other system components, such as the control and communication system, and so on, which might not be fully redundant, are effectively limiting reliability, as discussed in [55]. Such "reliability bottlenecks" must not be neglected when assessing the benefits of redundancy applied to multi-cell systems. In addition, the limitations inherent to reliability figures such as the MTBF should be carefully considered during the design of an actual system, which is covered in [60] using the example of high-power drive systems. A transition to a physics-based reliability design as proposed in [61] is advisable, and in general, reliability aspects need to be included in the design process of power electronic systems at an early stage. Approaches to reliability design based on reliability block diagrams and specialized software tools, such as described in [62] for aircraft system architectures, could be applied to the design of complex converter systems in order to enable a comprehensive reliability assessment.

D. Reliability Versus Power Density

As an example of how reliability considerations could be included in the design of a converter system, in the following the trade-off between (semiconductor) reliability and achievable power density is described. It is well known and considered by relevant standards, such as [63] and [56], that the reliability of power semiconductors depends on the blocking voltage utilization and the junction temperature, T_j. The latter offers the possibility to improve reliability by increasing the capability of the cooling system, e. g., the size of the heat sinks. According to [56], the semiconductor failure rate at $T_\mathrm{j} = 100\,°\mathrm{C}$ has to be scaled by a factor π_T to account for different junction temperatures,

$$\lambda(T_\mathrm{j}) = \lambda_{100\,°\mathrm{C}}\pi_\mathrm{T} \quad \text{with} \quad \pi_\mathrm{T} = e^{3480\cdot\left(\frac{1}{373}-\frac{1}{T_\mathrm{j}+273}\right)}, \qquad (43)$$

that is, as an example, $\lambda(T_\mathrm{j} = 110\,°\mathrm{C}) \approx 1.3 \cdot \lambda_{100\,°\mathrm{C}}$. Using the same optimization routine as described in Section III and considering a real 1700 V/150 A IGBT module (with temperature-dependent loss characteristics from its datasheet [64]), but varying the allowable maximum junction temperature specifications, the $\eta\rho$-Pareto fronts shown in Fig. 19 can be obtained. Each Pareto front is associated with a certain junction temperature, and hence with a certain correction factor, π_T, and a corresponding $\mathrm{MTBF_S}$ value. No redundancy is considered here, and thus the value of $\lambda_{100\,°\mathrm{C}}$ cancels out when normalizing the $\mathrm{MTBF_S}$ values. By reducing the allowable junction temperature, e. g., from 120 °C to 80 °C, the $\mathrm{MTBF_S}$ can be increased by a factor of 2.7, however, at the price of a larger heat sink and/or reduced maximum power density. Note also that the lower junction temperatures provide a slight efficiency benefit due to reduced semiconductor losses.

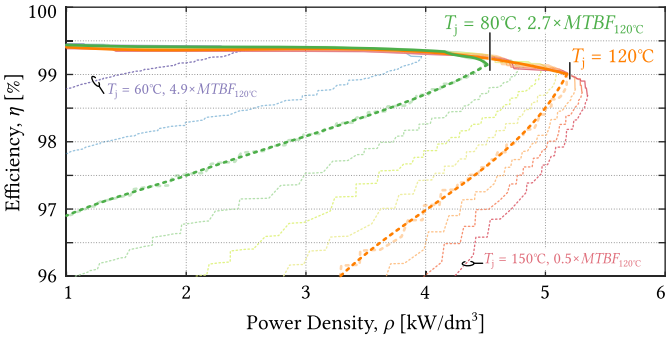

Fig. 19. Reliability versus power density trade-off for a design based on 1700 V/150 A IGBTs; no redundancy is considered.

VI. Conclusion

Cascaded cells converter systems, such as the CHB topology, are a very attractive solution to interface power electronic systems to MV applications. The choice of a number of cascaded cells, or, equivalently, of a semiconductor blocking voltage, affects trade-offs between system efficiency, power density, and also reliability aspects, which have been addressed comprehensively in this paper. By identifying simple, physics-inspired relationships between the loss-relevant characteristics of IGBT power modules and their blocking voltage and current ratings on the basis of empirical data (i. e., datasheet values), an analytic calculation of the optimum blocking voltage in terms of efficiency can be established, providing further insights on how the number of cells affects conduction and switching losses. The results indicate that 1200 V or 1700 V devices (i. e., 15 or 11 cells per phase stack, respectively) are most suitable for a 1 MVA system connected to a 10-kV grid. A full efficiency versus power density $\eta\rho$-Pareto optimization that includes also the loss and volume contributions of the grid filter inductance and the cooling system confirms that designs based on these blocking voltages offer the most suitable trade-off between efficiency and power density, whereby efficiencies above 99 % at a power density of about 5 kW/dm^3 (considering a ratio of 0.7 between the sum of the main component volumes and the boxed volume) are achievable.

Since recent advances in SiC power semiconductor technology have produced devices with very high blocking voltages, it is shown that the switching characteristics that such devices would have to provide in order for a single two-level SiC inverter to be competitive with a silicon multi-cell solution would involve extreme switching speeds, posing significant challenges regarding, e. g., EMI and isolation stress.

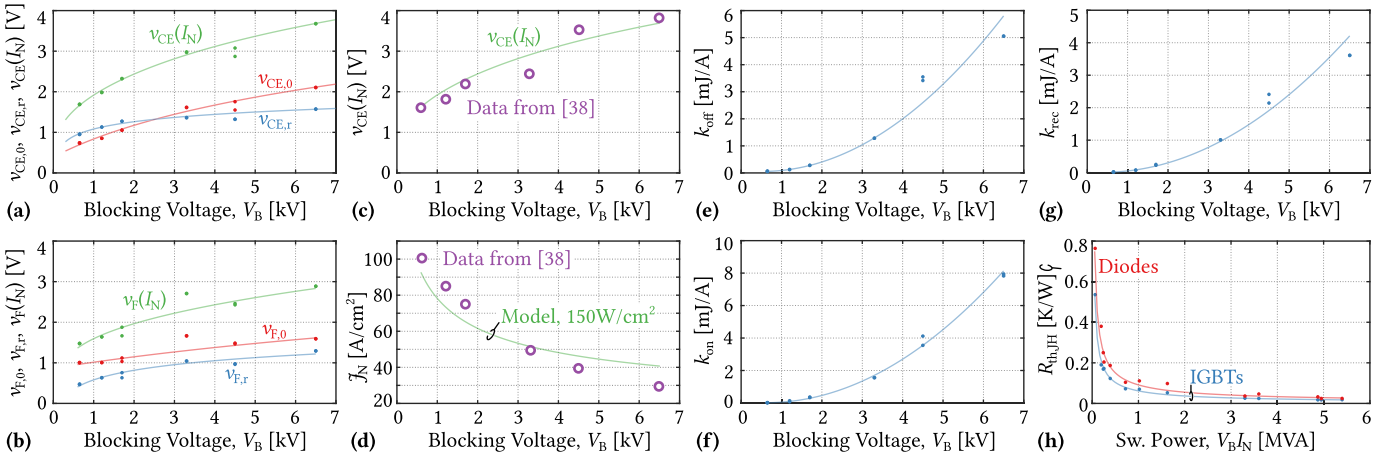

Fig. 20. Datasheet values for the loss-relevant IGBT and diode parameters and fitted analytical approximations for (a) IGBT conduction losses, (b) diode conduction losses, (e) normalized turn-off losses, (f) normalized turn-on losses, (g) normalized diode recovery losses, and (h) thermal resistances from junction to heat sink. (c) Comparison of conduction loss model with typical data for the forward voltage at rated current from [38] and (d) comparison of the same for the corresponding nominal current densities.

In contrast, multi-cell designs employing LV SiC MOSFET power modules are found to yield significant improvements of both, efficiency and power density, compared with designs based on silicon IGBTs. This is a result of the ohmic characteristic of the unipolar SiC devices, which allows to, in theory arbitrarily, reduce the conduction losses by increasing the chip area. Furthermore, the lower normalized switching energies of SiC devices allow for an increase of the switching frequencies, and hence a further reduction of the filter inductor size, corresponding to higher power densities, at least if protection considerations do not set a lower bound for the filter inductance. It is therefore expected that even with a future emergence of HV SiC devices on an industrial scale, the most feasible options might not be single-cell systems, but *fewer*-cell systems featuring cells based on SiC power semiconductors with intermediate blocking voltages, e. g., 3.3 kV, which could offer a suitable trade-off between performance and complexity.

Furthermore, reliability concerns arising from the high number of components in multi-cell systems have been addressed by showing how the addition of redundant cells can improve the system reliability. If similar costs of the redundancy in terms of additionally installed power capability are considered, the resulting reliability of systems based on LV semiconductors and hence many cells is comparable with that of designs based on fewer cells with higher blocking voltages. Reliability considerations do therefore not *a priori* exclude solutions based on LV semiconductors and many cascaded cells, which have been identified before to offer suitable trade-offs between power density and efficiency.

Other aspects that could affect the choice of the number of cells comprise the complexity of the system, i. e., the signal electronics including the potentially required redundancy to fully benefit from increased reliability achieved by means of redundant converter cells, but also the construction complexity, especially if advanced features, such as the capability to hot-swap converter cells, are desired. Furthermore, economic considerations, such as the trade-off between capital expenditure (CAPEX) and operating expenditure (OPEX), e. g., costs caused by energy losses but also by the effort for maintenance and repair, and so on, are important with respect to developing, selling, and servicing of industrial products. The comparatively flat optimum of the blocking voltage and especially also the trade-off between efficiency and power density shown by the Pareto fronts leave room to include such advanced considerations in the selection of the number of converter cells for high-power MV converter systems, and hence to obtain suitable performance in multiple dimensions, not only efficiency and power density, to satisfy specific customer requirements. Further considerations in this direction could be based on the analysis presented here.

Appendix
Empirical Modeling of Power Modules

This Appendix presents the parameters of analytical approximations used to model the IGBT and diode characteristics concerning the dependences on the rated blocking voltage V_B, and the rated current, I_N, and provides some additional remarks. The empirical data has been obtained from the datasheets of modern Infineon IGBT3/IGBT4 trench/field-stop IGBT modules with a wide range of blocking voltage and nominal current ratings. The number of modules considered per blocking voltage has been considered in the fits in order to assign the same weight to each blocking voltage.

A. Conduction Losses

Fig. 20(a) shows the voltage drop at nominal current, $v_{CE}(I_N)$, and its two components, $v_{CE,v0}$ and $v_{CE,r}$, [see Fig. 3(a)] as functions of the blocking voltage, and the fit curves according to (1) and (2); Fig. 20(b) shows the same data for diodes (note that the dependences on the blocking voltage for IGBTs and diodes are quite similar). The resulting model parameters can be found in Tables III and IV.

To further verify the model, Fig. 20(c) shows typical on-state voltages at rated current, i. e., $v_{CE}(I_N)$, for IGBTs with different blocking voltages as published in [38] (note that these

TABLE III
PARAMETERS OF THE IGBT MODEL.

$v_{\mathrm{CE,v0}}(V_{\mathrm{B}})$	A_{v0}	=	1.3862
	B_{v0}	=	$5.0353 \cdot 10^{-4}$
	C_{v0}	=	1.3244
$v_{\mathrm{CE,r}}(V_{\mathrm{B}})$	A_{r}	=	0.2605
	B_{r}	=	0.0635
$K_{\mathrm{off}}(V_{\mathrm{B}})$	A_{off}	=	$1.6097 \cdot 10^{-7}$
	B_{off}	=	$-1.6897 \cdot 10^{-4}$
	C_{off}	=	0.0992
$K_{\mathrm{on}}(V_{\mathrm{B}})$	A_{off}	=	$2.3481 \cdot 10^{-7}$
	B_{off}	=	$-2.9117 \cdot 10^{-4}$
	C_{off}	=	0.1066
$R_{\mathrm{th,JH}}(V_{\mathrm{B}}, I_{\mathrm{N}})$	A_{Rth}	=	1866.7
	B_{Rth}	=	0.7468

TABLE IV
PARAMETERS OF THE DIODE MODEL.

$v_{\mathrm{F,v0}}(V_{\mathrm{B}})$	A_{v0}	=	1.2316
	B_{v0}	=	$2.5990 \cdot 10^{-4}$
	C_{v0}	=	2.0201
$v_{\mathrm{F,r}}(V_{\mathrm{B}})$	A_{r}	=	0.3410
	B_{r}	=	0.0055
$K_{\mathrm{rec}}(V_{\mathrm{B}})$	A_{rec}	=	$1.1240 \cdot 10^{-7}$
	B_{rec}	=	$-8.6844 \cdot 10^{-5}$
	C_{rec}	=	0.0267
$R_{\mathrm{th,JH}}(V_{\mathrm{B}}, I_{\mathrm{N}})$	A_{Rth}	=	2014.2
	B_{Rth}	=	0.7240

data are for IGBT modules from *another* manufacturer). The $v_{\mathrm{CE}}(I_{\mathrm{N}})$ characteristic obtained from the model in (1) and (2) using the parameters given in Table III shows good agreement also with these data, indicating that the objective of modeling the characteristics of a "typical" IGBT is achieved.

As mentioned earlier, the datahseet current ratings are typically chosen such that the loss density in the IGBT chips of a module at rated current, i. e., $v_{\mathrm{CE}}(I_{\mathrm{N}}) \cdot J_{\mathrm{N}} = v_{\mathrm{CE}}(I_{\mathrm{N}}) \cdot I_{\mathrm{N}} / A_{\mathrm{Chip}}$, does not exceed a limit of about $100\,\mathrm{W/cm^2}$ to $150\,\mathrm{W/cm^2}$, resulting in a decrease of the nominal current density, J_{N}, with increasing blocking voltage, as is illustrated again by data taken from [38] in Fig. 20(d). This means that a module with higher blocking voltage rating has a larger chip area for the same rated current. Taking the $v_{\mathrm{CE}}(I_{\mathrm{N}})$ characteristic from the fit model and assuming a loss density limit of $150\,\mathrm{W/cm^{-2}}$ to calculate $J_{\mathrm{N}}(V_{\mathrm{B}})$, again good agreement with the data from [38] can be observed. The deviations indicate that for lower blocking voltages, higher loss densities might be permissible in practical module designs, whereas for higher blocking voltages lower loss densities must be used, which can be attributed to differences in the packaging technologies [38]. Note also that the effective silicon area would in addition also include the chip edge passivations, further increasing the chip areas for higher blocking voltages.

B. Switching Losses

Fig. 20(e)–(g) show the normalized switching energies as functions of the blocking voltage and the corresponding approximations and/or model characteristics. Since, in contrast to the conduction loss case, the raw data obtained from the datasheets span about two orders of magnitudes, it is important to find the model parameters by considering normalized residuals, i. e., by minimizing the function

$$r = \sum_{i=1}^{N_{\mathrm{Devices}}} \left(\frac{K_{\mathrm{sw}}(V_{\mathrm{B},i}) - K_{\mathrm{sw},i}}{K_{\mathrm{sw},i}} \right)^2 \tag{44}$$

with $K_{\mathrm{sw}}(V_{\mathrm{B}})$ as in (5), (6), or (7), respectively. This ensures similar *relative* errors between the model and the data points, and explains why the fit curves in Fig. 20(e)–(g) seem to be very accurate for lower blocking voltages and less accurate for higher blocking voltages.

As an aside, note that the 4.5 kV devices show lower $v_{\mathrm{CE}}(I_{\mathrm{N}})$ and higher K_{sw} than expected. The reason for this is that the available devices in this voltage class are optimized more toward low conduction losses, which is achieved by increasing the high-level life-time of the charge carriers, resulting in an increase of the switching energies [37].

C. Thermal Resistances

Finally, Fig. 20(h) shows the thermal resistances of IGBTs and diodes versus the rated switching power, i. e., $V_{\mathrm{B}} \cdot I_{\mathrm{N}}$, and the corresponding fits, which are obtained in the same way as those for the switching losses.

ACKNOWLEDGMENT

The authors would like to thank Prof. N. Kaminski from the Institute for Electrical Drives, Power Electronics and Devices, University of Bremen, Germany, for interesting discussions concerning multi-cell converter scaling.

REFERENCES

[1] N. Doerry and K. McCoy, "Next generation integrated power system: NGIPS technology development roadmap," Naval Sea Syst. Command, Washington, DC, USA, Tech. Rep., 2007. [Online]. Available: http://www.dtic.mil/cgi-bin/GetTRDoc?AD=ADA519753

[2] D. Bosich, A. Vicenzutti, R. Pelaschiar, R. Menis, and G. Sulligoi, "Toward the future: The MVDC large ship research program," in *Proc. AEIT Int. Annu. Conf. (AEIT)*, Naples, Italy, Oct. 2015, pp. 1–6.

[3] W. McMurray, "Power converter circuits having a high frequency link," U.S. Patent 3 581 212, 1970.

[4] W. McMurray, "The thyristor electronic transformer: A power converter using a high-frequency link," *IEEE Trans. Ind. General Appl.*, vol. IGA-7, no. 4, pp. 451–457, Jul. 1971.

[5] H. Mennicken, "Stromrichtersystem mit Wechselspannungs-Zwischenkreis und seine Anwendung in der Traktionstechnik," (in German), Ph.D. dissertation, Rheinisch-Westfälische Technische Hochschule, Aachen, Germany, 1978.

[6] M. Steiner and H. Reinold, "Antriebssystem für ein Schienenfahrzeug und Ansteuerverfahren hierzu," Germany Patent 196 30 284 A1, Jan. 29, 1998.

[7] M. Steiner and H. Reinold, "Medium frequency topology in railway applications," in *Proc. 12th Eur. Conf. Power Electron. Appl. (EPE)*, Aalborg, Denmark, 2007, pp. 1–10.

[8] C. Zhao *et al.*, "Power electronic traction transformer—Medium voltage prototype," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3257–3268, Jul. 2014.

[9] M. Kang, P. N. Enjeti, and I. J. Pitel, "Analysis and design of electronic transformers for electric power distribution system," *IEEE Trans. Power Electron.*, vol. 14, no. 6, pp. 1133–1141, Nov. 1999.

[10] M. D. Manjrekar, R. Kieferndorf, and G. Venkataramanan, "Power electronic transformers for utility applications," in *Proc. Conf. Rec. IEEE Ind. Appl. Conf.*, Rome, Italy, Oct. 2000, pp. 2496–2502.

[11] L. Heinemann and G. Mauthe, "The universal power electronics based distribution transformer, an unified approach," in *Proc. 32nd Annu. IEEE Power Electron. Specialists Conf. (PESC)*, Vancouver, BC, Canada, Jun. 2001, pp. 504–509.

[12] E. R. Ronan, S. D. Sudhoff, S. F. Glover, and D. L. Galloway, "A power electronic-based distribution transformer," *IEEE Trans. Power Del.*, vol. 17, no. 2, pp. 537–543, Apr. 2002.

[13] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[14] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep. 1981.

[15] T. A. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," in *Proc. 23rd Annu. IEEE Power Electron. Specialists Conf. (PESC)*, Toledo, Spain, Jun./Jul. 1992, pp. 397–403.

[16] C. Keller and Y. Tadros, "Are paralleled IGBT modules or paralleled IGBT inverters the better choice?" in *Proc. 5th Eur. Conf. Power Electron. Appl.*, Brighton, U.K., Sep. 1993, pp. 1–6.

[17] L. Matakas, C. Burlacu, and E. Masada, "The connection of converters instead of semiconductor power devices—A high performance solution for the MVA range of power comverters," *J. Circuits, Syst. Comput.*, vol. 5, no. 3, pp. 503–521, 1995.

[18] W. McMurray, "Power converter circuits having a high frequency link," U.S. Patent 3 517 300, Jun. 23, 1971.

[19] R. Marquardt, A. Lesnicar, and J. Hildinger, "Modulares Stromrichterkonzept für Netzkupplungsanwendung bei hohen Spannungen," (in German), in *Proc. ETG-Fachtagung*, Bad Nauheim, Germany, 2002, pp. 1–7.

[20] A. Lesnicar and R. Marquardt, "A new modular voltage source inverter topology," in *Proc. 10th Eur. Conf. Power Electron. Appl. (EPE)*, Toulouse, France, Sep. 2003, pp. 1–10.

[21] S. Thomas, M. Stieneker, and R. W. De Doncker, "Development of a modular high-power converter system for battery energy storage systems," in *Proc. 14th Eur. Conf. Power Electron. Appl. (EPE)*, Birmingham, U.K., Aug./Sep. 2011, pp. 1–10.

[22] J. E. Huber and J. W. Kolar, "Volume/weight/cost comparison of a 1MVA 10 kV/400 V solid-state against a conventional low-frequency distribution transformer," in *Proc. IEEE Energy Convers. Congr. Expo (ECCE)*, Pittsburgh, PA, USA, Sep. 2014, pp. 4545–4552.

[23] X. Wang and J. A. Cooper, "High-voltage n-channel IGBTs on free-standing 4H-SiC epilayers," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 511–515, Feb. 2010.

[24] S.-H. Ryu *et al.*, "High performance, ultra high voltage 4H-SiC IGBTs," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Raleigh, NC, USA, Sep. 2012, pp. 3603–3608.

[25] T. Zhao, L. Yang, J. Wang, and A. Q. Huang, "270 kVA solid state transformer based on 10 kV SiC power devices," in *Proc. IEEE Electr. Ship Technol. Symp.*, Arlington, VA, USA, May 2007, pp. 145–149.

[26] K. Hatua, S. Dutta, A. Tripathi, S. Baek, G. Karimi, and S. Bhattacharya, "Transformer less intelligent power substation design with 15kV SiC IGBT for grid interconnection," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Phoenix, AZ, USA, Sep. 2011, pp. 4225–4232.

[27] *CAS120M12BM2 Datasheet*, Cree, Inc., Durham, NC, USA, 2014.

[28] *CAS300M12BM2 Datasheet*, Cree, Inc., Durham, NC, USA, 2014.

[29] *CAS300M17BM2 Datasheet*, Cree, Inc., Durham, NC, USA, 2014.

[30] J. Dodge, "Reduce circuit zapping from cosmic radiation," *Power Electron. Technol.*, pp. 20–26, Sep. 2007.

[31] N. Kaminski and A. Kopta, "Failure rates of HiPak modules due to cosmic rays (AN 5SYA 2042-04)," ABB Switzerland Ltd., Lenzburg, Switzerland: Tech. Rep., 2011.

[32] S. Dieckerhoff, S. Bernet, and D. Krug, "Power loss-oriented evaluation of high voltage IGBTs and multilevel converters in transformerless traction applications," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1328–1336, Nov. 2005.

[33] J. W. Kolar, J. Biela, S. Waffler, T. Friedli, and U. Badstuebner, "Performance trends and limitations of power electronic systems," in *Proc. 6th Int. Conf. Integr. Power Electron. Syst. (CIPS)*, Nuremberg, Germany, Mar. 2010, pp. 1–20.

[34] B. Mwinyiwiwa, Z. Wolanski, and B.-T. Ooi, "Microprocessor-implemented SPWM for multiconverters with phase-shifted triangle carriers," *IEEE Trans. Ind. Appl.*, vol. 34, no. 3, pp. 487–494, May 1998.

[35] J. Rodríguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[36] Z. J. Shen and I. Omura, "Power semiconductor devices for hybrid, electric, and fuel cell vehicles," *Proc. IEEE*, vol. 95, no. 4, pp. 778–789, Apr. 2007.

[37] B. Jayant Baliga, *Fundamentals of Power Semiconductor Devices*. New York, NY, USA: Springer, 2008.

[38] B. Jayant Baliga, *The IGBT Device*. Oxford, U.K.: Elsevier, 2015.

[39] J. Huber, G. Ortiz, F. Krismer, N. Widmer, and J. W. Kolar, "$\eta-\rho$ Pareto optimization of bidirectional half-cycle discontinuous-conduction-mode series-resonant DC/DC converter with fixed voltage transfer ratio," in *Proc. IEEE Appl. Power Electron. Conf. (APEC)*, Long Beach, CA, USA, Mar. 2013, pp. 1413–1420.

[40] M. Schweizer, T. Friedli, and J. W. Kolar, "Comparative evaluation of advanced three-phase three-level inverter/converter topologies against two-level systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5515–5527, Dec. 2013.

[41] H. Ertl, J. W. Kolar, and F. C. Zach, "Analysis of a multilevel multi-cell switch-mode power amplifier employing the 'flying-battery' concept," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 816–823, Aug. 2002.

[42] *IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems*, IEEE Standard 519-1992, 1992.

[43] M. Kasper, D. Bortis, and J. W. Kolar, "Scaling and balancing of multi-cell converters," in *Proc. Int. Power Electron. Conf. (ECCE Asia)*, Hiroshima, Japan, 2014, pp. 2079–2086.

[44] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters," in *Proc. IEEE 8th Workshop Comput. Power Electron.*, Jun. 2002, pp. 36–41.

[45] J. Biela and J. W. Kolar, "Cooling concepts for high power density magnetic devices," in *Proc. Power Convers. Conf. (PCC)*, Nagoya, Japan, Apr. 2007, pp. 1–8.

[46] T. Guillod, F. Krismer, R. Färber, C. M. Franck, and J. W. Kolar, "Protection of MV/LV solid-state transformers in the distribution grid," in *Proc. 41st Annu. IEEE Ind. Electron. Soc. Conf. (IECON)*, Yokohama, Japan, Nov. 2015, pp. 003531–003538.

[47] U. Drofenik, G. Laimer, and J. W. Kolar, "Theoretical converter power density limits for forced convection cooling," in *Proc. 26th Int. Conf. Power Electron., Intell. Motion, Power Quality (PCIM)*, Nuremberg, Germany, Jun. 2005, pp. 608–619.

[48] M. März, A. Schletz, B. Eckardt, S. Egelkraut, and H. Rauh, "Power electronics system integration for electric and hybrid vehicles," in *Proc. 6th Int. Conf. Integr. Power Syst. Conf. (CIPS)*, Nuremberg, Germany, Mar. 2010, pp. 16–18.

[49] A. Bolotnikov *et al.*, "Overview of 1.2 kV–2.2 kV SiC MOSFETs targeted for industrial power conversion applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Charlotte, NC, USA, Mar. 2015, pp. 2445–2452.

[50] C. Felgemacher, S. V. Araújo, C. Nöding, and P. Zacharias, "Benefits of increased cosmic radiation robustness of SiC semiconductors in large power-converters," in *Proc. Int. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage. (PCIM Europe)*, Nuremberg, Germany, May 2016, pp. 1–8.

[51] J. E. Huber and J. W. Kolar, "Common-mode currents in multi-cell solid-state transformers," in *Proc. Int. Power Electron. Conf. (IPEC-ECCE-Asia)*, Hiroshima, Japan, May 2014, pp. 766–773.

[52] A. Birolini, *Quality and Reliability of Technical Systems: Theory, Practice, Management*, 2nd ed. Berlin, Germany: Springer, 1997.

[53] J. G. Kassakian and D. I. Perreault, "An assessment of cellular architectures for large converter systems," in *Proc. 1st Int. Power Electron. Motion Control Conf.*, Beijing, China, Jun. 1994, pp. 970–977.

[54] T. Meynard, G. Gateau, and P. Lezana, "Design of series/parallel multi-cell converters for improved power conversion," *Tutorial at the 38th Annu. IEEE Ind. Electron. Soc. Conf. (IECON)*, Montreal, QC, Canada, Oct. 2012.

[55] R. Grinberg, G. Riedel, A. Korn, P. Steimer, and E. Bjornstad, "On reliability of medium voltage multilevel converters," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Denver, CO, USA, Sep. 2013, pp. 4047–4052.

[56] *Reliability Data Handbook*, IEC Standard 62 380:2004(E), 2004.

[57] J. E. Huber and J. W. Kolar, "Analysis and design of fixed voltage transfer ratio DC/DC converter cells for phase-modular solid-state transformers," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Montréal, QC, Canada, Sep. 2015, pp. 5021–5029.
[58] D. Cottet *et al.*, "Integration technologies for a fully modular and hot-swappable MV multi-level concept converter," in *Proc. 26th Int. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage. (PCIM Europe)*, Nuremberg, Germany, May 2015, pp. 1–8.
[59] D. Dujic, F. Kieferndorf, F. Canales, and U. Drofenik, "Power electronic traction transformer technology," in *Proc. 7th Int. Power Electron. Motion Control Conf. (IPEMC)*, Harbin, China, Jun. 2012, pp. 636–642.
[60] P. Wikstrom, L. A. Terens, and H. Kobi, "Reliability, availability, and maintainability of high-power variable-speed drive systems," *IEEE Trans. Ind. Appl.*, vol. 36, no. 1, pp. 231–241, Jan./Feb. 2000.
[61] H. Wang, M. Liserre, and F. Blaabjerg, "Toward reliable power electronics: Challenges, design tools, and opportunities," *IEEE Ind. Electron. Mag.*, vol. 7, no. 2, pp. 17–26, Jun. 2013.
[62] D. Rehage, U. B. Carl, and A. Vahl, "Redundancy management of fault tolerant aircraft system architectures—Reliability synthesis and analysis of degraded system states," *Aerosp. Sci. Technol.*, vol. 9, no. 4, pp. 337–347, Jun. 2005.
[63] "Reliability prediction of electronic equipment," U.S. Dept. Defense, Washington, DC, USA, Tech. Rep. MIL-HDBK-217F, 1995.
[64] *FF150R17KE4 Datasheet*, Infineon Technol. AG, Neubiberg, Germany, 2013.

Jonas E. Huber (S'11) received the MSc degree from ETH Zurich, Zürich, Switzerland, in 2012. He is currently pursuing the Ph.D. degree with the Power Electronic Systems Laboratory, ETH Zurich.

His current research interests include solid-state transformers, focusing on the analysis, optimization, and design of high-power multi-cell converter systems, reliability considerations, control strategies, and applicability aspects, among others.

Johann W. Kolar (M'89–SM'04–F'10) is a Full Professor and the Head of the Power Electronic Systems Laboratory, ETH Zurich, Zürich, Switzerland.

He has published over 650 scientific papers in international journals and conference proceedings and has filed more than 120 patents. He received 21 IEEE Transactions and Conference Prize Paper Awards and the ETH Zurich Golden Owl Award for excellence in teaching. His current research interests include ultra-compact and ultra-efficient SiC and GaN converter systems, wireless power transfer, solid-state transformers, power supplies on chip, and ultra-high speed and bearingless motors.