POTENTIAL-FREE GATE DRIVE CIRCUITS FOR FAST SWITCHING POWER SEMICONDUCTOR DEVICES

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A B S T R A C T

This paper treats the discussion of basic concepts for potential-free gate drive circuits for fast switching power semiconductor devices. The discussion will apply - as a characteristic example - the half bridge leg as used in pulse width modulated (PWM) inverters with isolated gate bipolar transistors (IGBT). Experiences and related investigations are reported where the following problem areas are treated:

- Power Supply:
  - power requirement of the gate driver
  - requirement of negative supply voltages
  - separated transmission of energy and information
- Information Transmission:
  - pulse transformer
  - optocoupler
- Power Stage:
  - voltage amplification
  - driver circuit
- Failure Protection:
  - decentralized - self-protecting driver circuit
  - failure storage unit internally/externally
  - overcurrent protection
  - overvoltage protection
- Turn-On Problems of the Gate Drive Circuit:
  - defined gate voltage during supply voltage start-up

In connection with a 1000V/100A-IGBT half bridge module especially the problem of dv/dt stress of the gate driver is treated in detail. In conclusion the test results of the different concepts of potential separation of control and power circuit are compared and rated.

1. INTRODUCTION

Until a few years ago it was assumed that the development of power electronic switching devices had come to a standstill and that no new and spectacular developments could be expected. Fortunately this opinion had to be revised due to the application of techniques as used originally for VLSI-technology of integrated circuits. This led to some revolutionary new developments in the area of power electronic devices in the recent past.

One of these developments brought the combination of bipolar and FET technology. Thereby the advantages of FETs (high switching speeds, low gating power, etc.) with these of bipolar transistors (low voltage drops in the conduction mode also for high currents, etc.) have been combined. As of 1988 these devices (called IGT, IGBT or COMFET, dependent on the different manufacturers) are available for ratings of up to 1000V/400A as single transistor modules (IGBT plus freewheeling diode), or up to 1000V/200A as complete half bridge module, respectively.

The highest requirement for IGBT gate drive circuits are to be met for PWM-inverters (control of half bridges, see Fig.1).

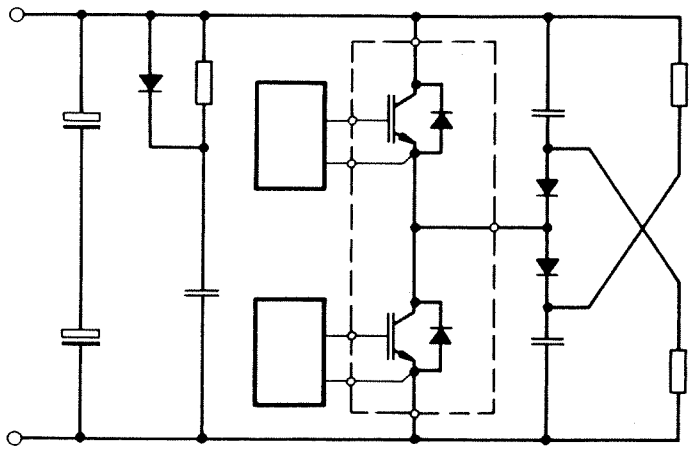
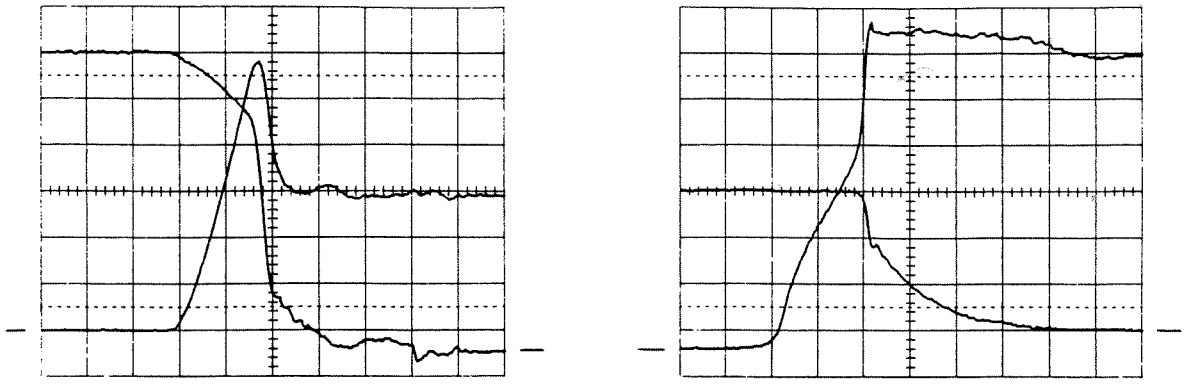


Fig.1 IGBT Inverter Half Bridge and Snubber Circuits

As has been shown by measurements of a 1000V/100A-IGBT half bridge module (TOSHIBA MG100N2YS1; see Figs.2a,b) dv/dt-values of $> 10kV/\mu s$ (corresponds to 1A into 100pF !) and di/dt-values of $> 2kA/\mu s$ (corresponds to 20V across 10nH, as given e.g., by a wire of approximately 1cm !) occur. In spite of using low inductance wiring therefore the RCD circuits shown in Fig.1 as well for the DC link as for the switching devices become necessary. (The low inductance current path can be realized advantageously as "biplanar" connection. This can be realized for low power, e.g., by printed circuit boards.) Due to the selected position of the discharging resistors (reduction of the occurring losses) the RCD circuits do not have the function of a classical RCD snubber; they only serve for the limitation of voltage spikes being greater than the DC link voltage. It has to be mentioned basically that under certain circumstances the actual voltage stress on the semiconductor itself is significantly different

from the voltage stress as can be measured at the device terminals. This is due to the package form taken from bipolar transistors which results in relatively large parasitic inductances between terminals and semiconductor chip.



a) turn-on behavior b) turn-off behavior

Fig.2 Switching Behavior of 1000V/100A-IGBT Half Bridge Module (U_Z=660V, I_L=100A, T_J=100°C, 100V/div, 100A/3div, 200ns/div)

Besides providing floating potential (high dv/dt strength) for the gate drive circuits for the switches of the upper bridge half, these features are also recommended for the transistors of the lower bridge half. A common gate drive unit for all switches of the lower bridge half is not realizable in a reliable manner; this is due to the combined effect of parasitic lead inductances (which always remain even in conventional low inductance circuits) and of the high di/dt rates during commutation (this leads to voltage spikes of some 10V). As compared to the driver stages of the upper half bridge the dv/dt stress of the corresponding driver stages of the lower bridge half lies at relatively uncritical values, due to the substantially lower voltage steps with high dv/dt.

2. CONCEPT OF THE GATE DRIVE CIRCUIT

In the following it is assumed that (according to the reasons given before) each power switch has its own floating driver circuit of equal structure. Figure 3 on one hand gives an overview over its functional parts, on the other hand it shows the incorporation of the driver circuits into a supervisory control unit.

This unit has to guarantee a lockout time (required by the switching time of the power semiconductors) between the upper and lower switch of a bridge leg in order to avoid a bridge short circuit. Within this lockout time the output voltage polarity is determined by the direction of the current flow. In any case this results in a discrepancy between the output voltage behavior and the pulse pattern reference. As detailed in [1], this possibly (dependent on

the control concept used in a drive application) results in a significant output (machine) current distortion. A compensation of this "nonideal" converter operation is only possible by changing from an "open loop" control to a closed loop control of the converter output voltage (interlock delay compensation - see Fig.3). Only then the converter function is incorporated quasi a posteriori into the determination of the gating signals. The voltage-time-area of the converter output voltage then corresponds to the input (reference) pulse pattern - with the exception of deviations due to nonequal voltage drops across the electric valves. A realization of this "voltage-time-area correction" can be achieved fully digitally as shown, e.g., in [2].

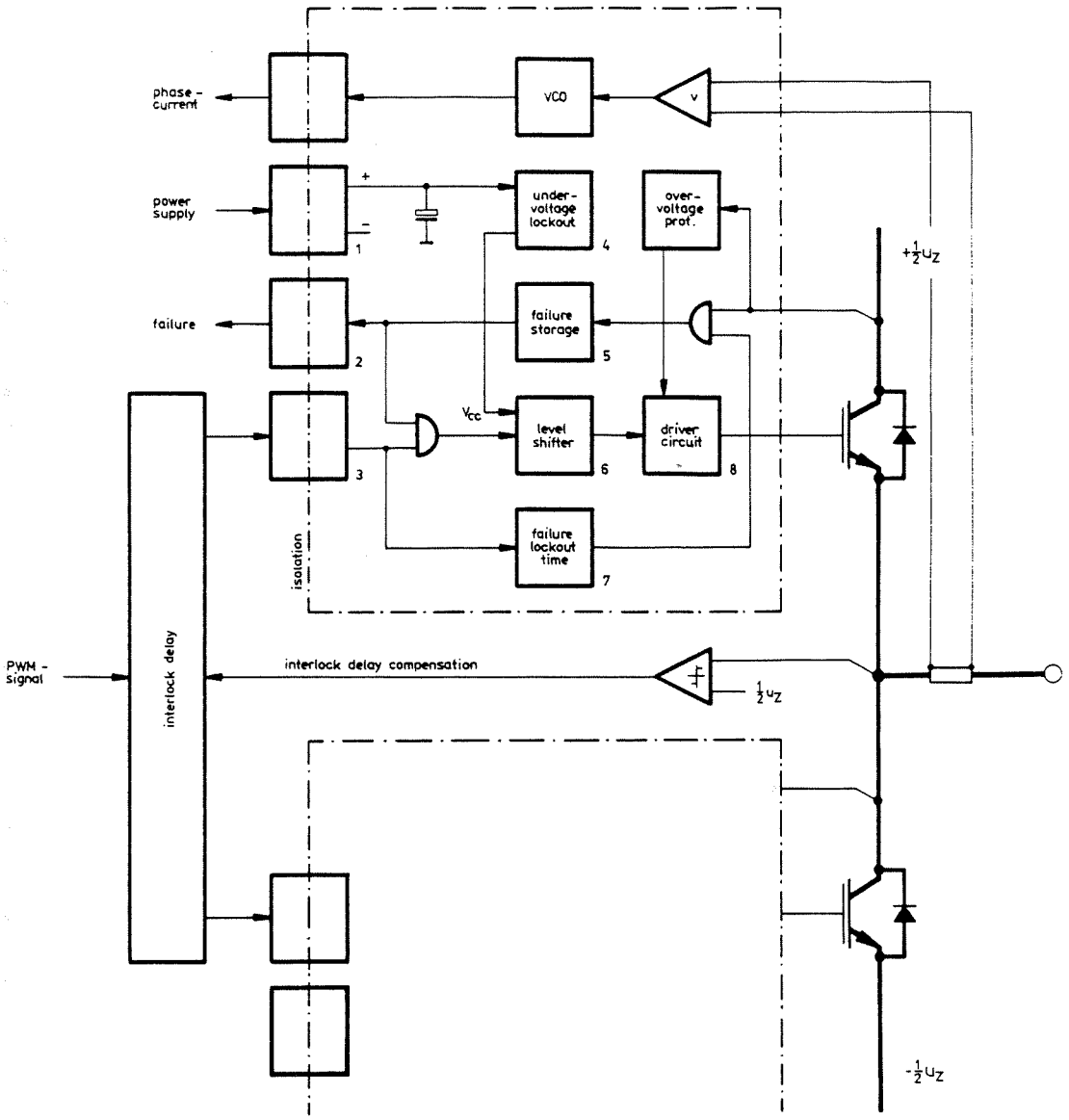


Fig.3 Functional Diagram of an IGBT Control Stage with Integrated Protective Functions

For the sake of completeness we want to discuss furthermore briefly the determination (measurement) of the output currents as is frequently required for incorporation into control concepts. Frequently passive AC current transformers are used for this purpose. However, as most important disadvantage, they show especially a severe bandwidth limitation for lower frequencies. (This imposes a problem for lower output frequencies as encountered in servo drives.) Active current transformers (e.g., "transfoshunts") on one hand make the measurement also of DC currents possible, on the other hand they require a voltage supply, however, as necessary due to the principle of current compensation applied. This results in relatively high transducer and system cost. An alternative is given by inserting a simple low inductance shunt into the output of the converter. This approach, however, is connected with the problem of signal processing at high (and stepwise varying) potential. As can be seen from Fig.3, this can be done simply at the potential of the gating stage of the upper power switch if the signal processing is incorporated into this gating stage. This also makes a separate voltage supply obsolete.

It is recommended to use an integrating measurement principle (where integration time = converter pulse period). This makes it possible to suppress the current harmonics (corresponding to the pulse frequency) to a large extent (simple measurement of the fundamental) according to the comb filter type transfer function of the measurement system. If the current measurement signal is present as frequency, the measurement principle mentioned can be realized simply by a counter (fully digital signal processing). An additional advantage is given by the simple and disturbance proof possibility of measurement signal transfer from the "high" potential of the measurement circuit to the potential of the signal processing electronics. This will be the topic of another paper being in preparation now.

The basic function of the gating and control circuit shown in Fig.3 consists of a floating (potential free) transmission of the gating information (3) and a possibly required following level shifter (6) for the output driver stage (8). Furthermore, the potential free supply of the unit is given by block (1). For avoidance of overcurrents (short circuit currents) in the power switch its collector-emitter-voltage is monitored. (This corresponds to a desaturation monitoring for bipolar transistors.) If an overcurrent (short circuit) occurs, the failure register (5) is set and the power switch is immediately turned off. Furthermore block (2) transfers (optionally) a potential free failure message to a supervisory unit. The reset of the failure register can be effected, e.g., by turning off the supply voltage of the gating stage.

Because for each turn-on of the power switch its collector-emitter-voltage initially shows high values (the opposite free wheeling diode is conducting), this would pretend an overcurrent failure and trigger the failure register. This can be suppressed by disabling the "failure signal" via (7) for a short period of time.

As further protective function one can achieve a limitation of the maximum collector-emitter-voltage via a feedback of the collector potential to the transistor gate being only active during operation of the limitation function. This makes also overvoltages manageable which originate from the mains and occur in the DC link (VDE-pulse) when smaller DC link capacitors are applied. This point of view is not treated in more detail in this paper. A relatively broad discussion of the associated problems can be found in [3] as

applied to MOSFETs.

During supply voltage buildup of the gating circuit one has to guarantee that the gate voltage occurring during this buildup does not exceed the threshold voltage. Otherwise the danger of a bridge short would exist. The level shifter (6) and the driver stage (8) therefore have to be locked by an undervoltage-lockout circuit (4).

3. DEVELOPMENT OF THE GATING/CONTROL CIRCUIT

For the development of the gate drive circuit basically the following problem areas have to be treated:

(A) Power Supply

For this problem one has to determine at first the power requirement for charging and discharging of C_{GE} (and the "Miller"-capacitance C_{CG}). Detailed analysis shows that the power required is below 1W even for today's largest IGBT modules. This leads to the conclusion that the power requirement of the complete stage should not be over a few watts in order to maintain the advantages of the IGBT ("powerless" control). Therefore one has to observe low current consumption for the development of the various building blocks of the gate drive circuit (failure storage, overcurrent protection, start-up circuit, etc.). This is even more important because of the additional power losses in the switched mode power supply which is necessary for floating power supply.

An essential point for the design is the question whether unipolar (+,0) or bipolar (+,-) gate voltage is required. Concerning the device control (where there is a gate rather than a base) the IGBTs behave like a FET. This means that we have a purely voltage controlled element - turn on only requires charging of the gate-emitter capacitance C_{GE} (and discharging of C_{GC}). The only exception is that C_{GE} (C_{GC}) is much larger here as compared to FETs due to the (much) higher switched currents and (therefore) due to the larger chip sizes. Furthermore, some IGBT manufacturers recommend to apply a negative gate voltage during turn-off. This obviously should result in a reliable switching operation and requires - as opposed to FETs - a bipolar control circuit. This naturally leads to a larger complexity of the control stage, however.

Furthermore, one has to ask the question whether the energy and switching information have to be transmitted separately or if this can be done in the same device (pulse transformer). The latter approach would reduce the number of elements subject to high dv/dt by one half. Furthermore one has to make a compromise between the power to be transmitted and the delay of the signal transmission. From a purely technical point of view always a clear separation of the function of the different (sub)assemblys is obvious. Therefore in this paper only the separate transmission of energy and information is treated.

Figure 4 shows various forms of the voltage supply. It is assumed that each control/gating circuit has its own low power switched mode power supply

(SMPS), controlled by a centralized clock. A further approach could be given by replacing these decentralized units by a central SMPS which feeds into a high frequency power bus. Each control/gating circuit then only has to have a transformer and rectifier.

For construction of the SMPS transformer one has to especially observe low coupling capacitance between primary and secondary because of the possibility of high currents flowing through this capacitance due to the usual high dv/dt stress. These currents flow through the gating circuit and could cause malfunctions due to resistive and inductive voltage drops. To prevent this an appropriate layout and/or shielding of the transformer (with direct connection to the power transistor emitter) is required.

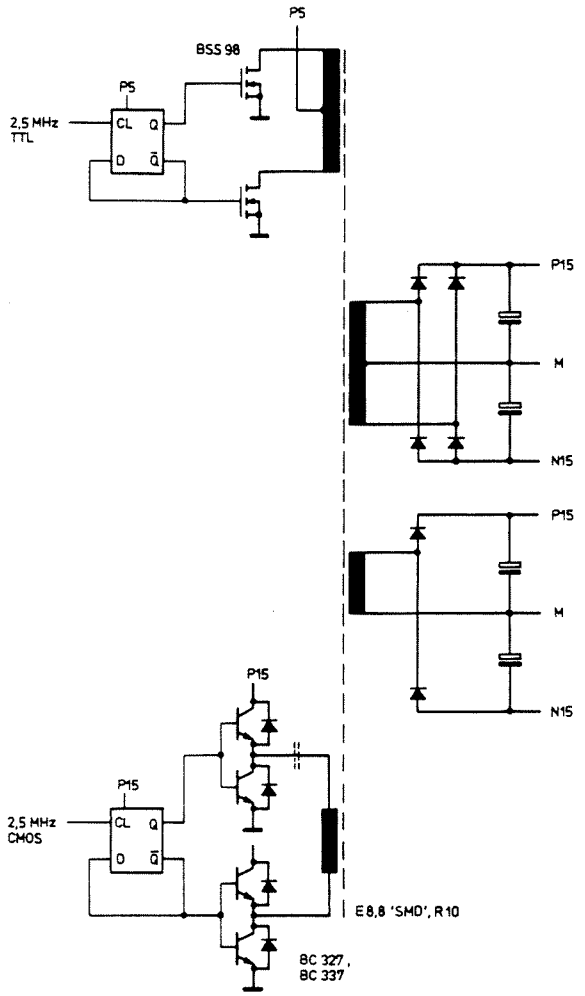


Fig.4 Circuit Alternatives of Primary and Secondary Side of the Gating Circuit Power Supply.

(B) Information Transmission

Information transmission is a crucial point of the control stage. This deals in general with the floating transmission of switching information (gate signal) to the control stage. Furthermore there are frequently other requirements for information transmission, e.g., if the control stage has to transmit

back information (failure detection, measurement signals, etc.) to the central control electronics.

Except for the case of combined energy and switching information transmittal (where a magnetic element (pulse transformer) has to be applied) the means of information transmission can be chosen according to the particular requirements. The alternatives are optocouplers and pulse transformers. The associated problems and their solutions are treated in detail in chapter 4.

(C) Power Stage

For realization of the power stage (i.e. of the stage which really drives the IGBT gate) there exist two major problems. First the power stage has to be able to deliver the relatively high currents which are necessary for the fast charging and discharging of C_{GE} (C_{GC}). Second, for electromagnetic compatibility also after switching has been completed the power stage has to define the gate voltage, e.g., via the low output resistance of a push-pull emitter follower.

Furthermore, the power stage has to contain a voltage amplifier (level shifter). This is necessary because the required voltage levels (especially for bipolar control) cannot be supplied by the controlling logic circuits. The problem of voltage amplification has to be emphasized very much because a high cut-off frequency is necessary to achieve a good pulse behavior, i.e. with little distortion (delay) as compared to the input signal. E.g., a simple amplifier (grounded emitter-circuit) can produce a steep falling edge by ("active") pull-down. The rising edge, however, shows relatively slow behavior because this is produced by charging up of the parasitic collector capacitances via the pull-up resistor. This effect can only be kept small if R_C has low resistance. This implies, however, that there is a high "quiescent" current in the turn-on intervals. Closer research has shown that this leads to much higher power consumption than needed for charging/discharging of the gate. The solution of this problem can be given by an "active" collector resistance (realized by a low power FET - see Fig.5) which is turned into low resistance during the pulse edges. At the other times it has relatively high resistance and causes small power consumption.

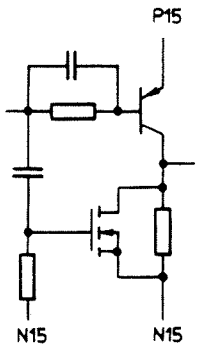


Fig.5 Level Shifter with "Active" Collector Resistor

(D) Protection Concepts

For PWM inverters with bipolar transistor modules in most cases a pro-

tection concept is applied using central overcurrent monitoring and turn-off. This concept is not well suited for IGBTs due to their high switching speed. It serves the purpose better to perform overcurrent monitoring and turn off in the control stage itself. This leads to a "self-protecting" control circuit. Because one can assume that the central control device usually contains current control electronics which can detect and turn off longer existing, relatively low overcurrents, the control stage has only to react to high overcurrents occuring within some µs. This can be, e.g., for inverter bridge short-circuits or for ground short-circuits. A well proven method for detecting such a malfunction is given by monitoring the collector-emitter-voltage (drain-source-voltage) of the IGBT; thereby turn-off is performed when the voltage exceeds the rated maximum voltage (according to the data sheets) for rated current.

Because in the latter case usually there exists a major malfunction, it is not sufficient to turn the transistor off only for this single switching instant. Then rather a failure storage unit (realized either in the control stage or in the central control electronics) has to detect the malfunction and to turn off the entire inverter.

(E) Turn-On Considerations

A special problem associated with control stages is their start-up, e.g. their supply voltage build-up. Modern inverters receive their auxiliary power via a switched mode power supply from the inverter DC-link; this is connected with the fact that the start-up of the supply voltages for the gate or base control circuits is performed when the DC-link capacitor already is (at least partly) charged. This on one hand requires that the power transistors can sustain (block) the DC-link voltage also without negative gate voltage. On the other hand it has to be avoided under all circumstances that the control stage behaves undefined during supply voltage start-up. If this is not taken into account, e.g., a short positive gate pulse can be produced which could lead to a short-circuit of the inverter bridge with devastating results. For safe operation of the control stage in this respect in general one has to introduce special precautions; one possibility is to connect the power (output) stage of the control circuit only after the supply voltage build-up is completed.

4. dv/dt-TEST OF DIFFERENT APPROACHES FOR CONTROL/GATING INFORMATION TRANSMISSION

As mentioned in the introduction the basic problem area of gating/controlling of half bridge circuits is given by the required dv/dt strength of the gating stage. As shown in Fig. 6 for the upper power switch of a bridge leg, high displacement currents flow through the coupling capacitances of the potential-free information transmission system (and also through all other circuit capacitances (distributed capacitances) of the system). These displacement currents can be of high magnitude due to the steep voltage changes when switching of the bridge legs occurs. For information transmission via a pulse transformer these currents can cause disturbances of the output signal if the input and/or output circuits are not symmetric. This is caused in de-

tail by the currents which are capacitively coupled and which flow through primary and secondary and which can result in a net magnetization of the transformer. This means a limited common mode rejection.

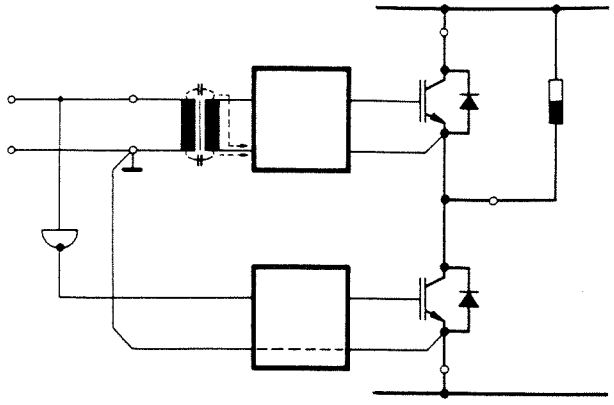


Fig.6 Inverter Bridge Leg and Gating Circuits

For testing various winding schemes relative to their common mode rejection it is advisable to use the actual half bridge module to be controlled as "test generator" (see Fig.7). The upper switch of the bridge leg is permanently locked by a 9V-battery (U_{G2}). For appropriate control of the lower transistor and by using a sufficiently inductive load one can closely reproduce the situation existing for converter operation. The output voltage of high dv/dt is connected to the primary side of the information transmission system under test; its secondary side is connected on one side to the negative pole of the DC link. If one assumes that for the actual application of the pulse transformers tested both terminals of the primary are terminated by the driver stage low resistance, the terminals can also be shorted for the dv/dt test. The interfering voltage appearing on the secondary due to the nonideal coupling (due to the required insulating strength) is monitored by an oscilloscope. Its chassis (ground) is also coupled by a low resistance to the negative bus. The negative bus of the DC link does not have a constant voltage relative to ground because of the combination of high di/dt during switching and the lead inductances L_P. If the oscilloscope gets its voltage supply via a separating transformer, the absence of the charging lead would cause loading of the earth capacitance of the measurement device by the charging currents via the outer line of the probe. This would result in a measured signal disturbance. Placing a differential inductor L_D into the probe line (several turns of the coaxial cable around a ferrite core EC52) improves the effect of the charging lead. For minimizing the inductive coupling of disturbances furthermore probing of the measured signal with the shortest possible ground lead has to be performed. The same reason holds for positioning the charging lead in closest proximity to the probe cable in order to minimize the ground loop formed between them (hatched area in Fig.7). For grounding of the oscilloscope basically the same guidelines have to be followed; the charging lead then also acts as voltage balancing lead.

The simplest version (as shown in Fig.8a) of a pulse transformer has been tested. The coupling capacity between primary and secondary in reality would be a distributed capacitance; for simplicity it shall be approximated by two discrete capacitances. Due to the relatively high resistivity of the termina-

ting resistor we have an asymmetric current distribution in the secondary. This causes, as mentioned, a disturbing signal of untolerably high magnitude (Fig.8b).

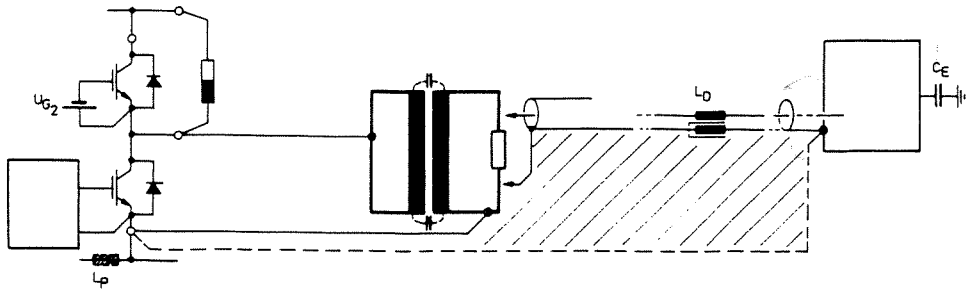


Fig.7 dv/dt-Test Circuit

The currents causing the magnetization compensate each other to a large extent due to the also symmetric capacitive coupling if the impedance relationships on the secondary are symmetric with respect to ground. (For this one has to observe the sense of windings.) This results in a substantial reduction of the disturbing signal (Fig.8d). One version of this circuit is treated, e.g., in [4].

A similar improvement of common mode rejection is achievable by the circuit shown in Fig.8e. The second part of the secondary winding of Fig.8c is formed here by a "screen"-winding which is bifilar and wound together with the actual secondary winding and which is left open on one side. The measurement result obtained herewith is shown in Fig.8f.

If the transformer core is connected to the ground of the secondary side one can achieve a further common mode rejection improvement according to Fig.8g (for the circuit of Fig.8a) or, according to Fig.8h (for the circuit of Fig.8c), respectively. The reason for this is that then, as shown in Fig.8i, a capacitive coupling of the primary and secondary side via the core is avoided. (One has to keep in mind that the windings are located close to the core in order to minimize the leakage inductances; this, however, tends to increase the coupling capacitances C_{S1K}, C_{S2K} of Fig.8i.) The remaining coupling capacitance C_{S12} can be kept low by a sufficient distance between the winding systems.

Besides the magnetic transmission of the gating/control information treated so far, also the optical transmission via optocouplers has to be investigated (Fig.9). Due to the high dv/dt values one has to apply a "HIGH-CMR" type (with screen) under all circumstances. However, the resulting common mode transient immunity is highly dependent on the common mode transient amplitude applied. For the voltage range existing here it shows typical values of about 1kV/µs. As can be seen from Figs.10a-d, the application is not possible here. However, a disturbance of the high-level signal of the optocouplers only occurs for a rising edge of the converter output voltage. (Vice versa, of the low-level signal for the falling edge.) This makes a gating circuit thinkable which would not be disturbed by a switching action of the power transistor controlled by this gating circuit.

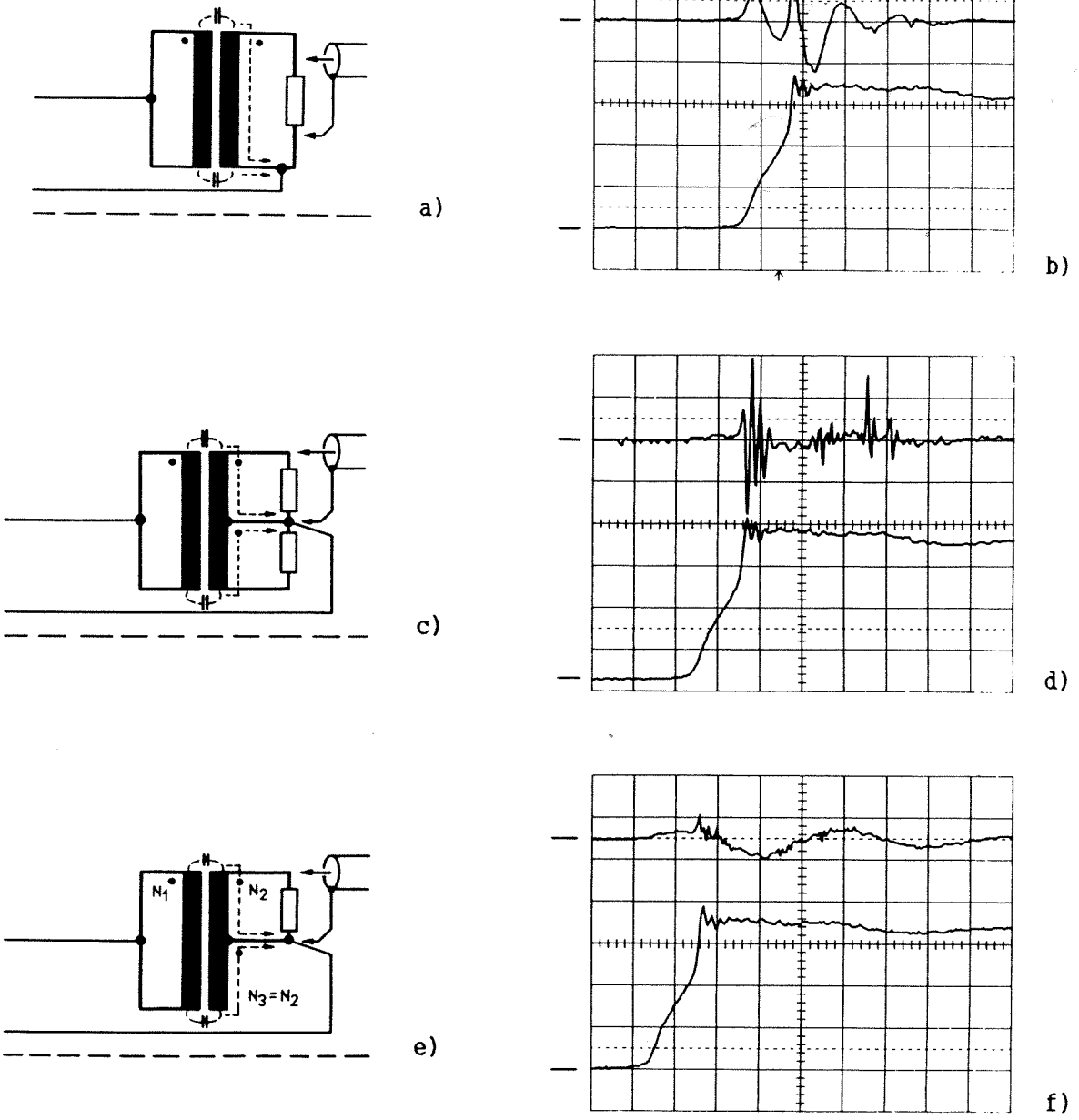
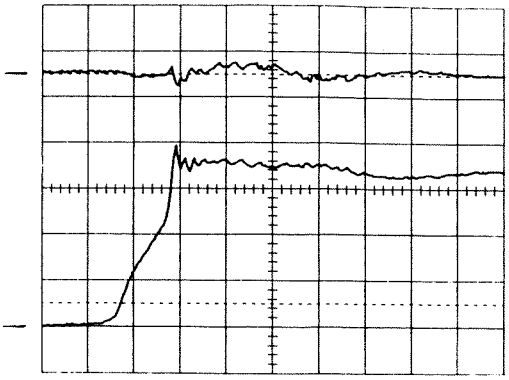
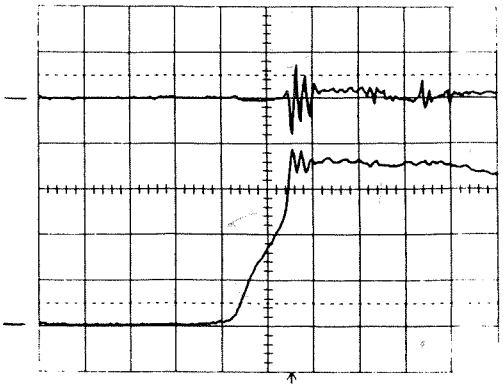


Fig.8 dv/dt-Test of Pulse Transformers

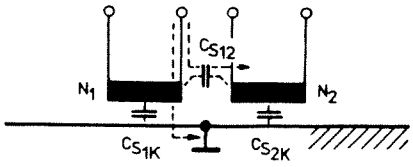
a) testing circuit for simple pulse transformer
b) upper trace: pulse transformer output voltage
(5V/div, 200ns/div)
lower trace: inverter output voltage
(200V/div, 200ns/div)
c) pulse transformer with center-tapped secondary
d) measurement result for c) (0.1V/div, 200ns/div)
e) "shielded" pulse transformer
f) measurement result for e) (0.5V/div, 200ns/div)



g)



h)



i)

Fig.8 dv/dt-Test of Pulse Transformers (continued)

g) as f) but with i)
h) as d) but with i)
i) magnetic core connected to secondary ground

As a more detailed analysis shows, however, both edges of the converter output voltage appear for the same gating signal level. This is due to the current flow through the free wheeling diodes of the bridge leg (or due to the lockout times). Therefore, a disturbance of the gating circuit is unavoidable. (The application of this principle therefore would be possible only for one single high side switch (buck-converter)).

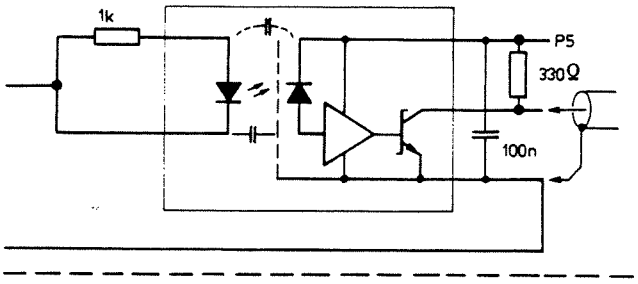


Fig.9 dv/dt-Test of Optocoupler

The application of optical coupling devices therefore is only possible when fiber optic links are applied (e.g., SIEMENS SFH750/SFH250). There the circuit for processing the signal of the receiver diode requires a certain effort. The closer treatment of this solution certainly would be of technical/scientific interest. However, this shall not be persued here in more detail due to the limited scope of this paper.

5. CIRCUIT PROPOSAL FOR AN IGBT-GATING/CONTROL STAGE

Figure 10 shows a possible realization of an IGBT-control/gating stage including the functional parts described before. Basically there exists a

limited maximum turn on time for transmission of control pulses via pulse transformers due to the limited saturation voltage-time-area of the magnetic core. (Matching to the primary signal level, e.g., TTL, can be achieved by an appropriate turns ratio.) It is of advantage therefore to only transmit the information of the switching status change (switching edges) and to "reconstruct" the actual control signal by a bistable circuit connected in series. A fundamental disadvantage of this solution consists of the fact that even a short disturbing pulse can lead to a permanent change of the switching status (generally equivalent to a bridge short). Furthermore one has to guarantee that the bistable circuit is kept well defined in the turn-off state of the power switch while the power supply is being built up after the system start-up.

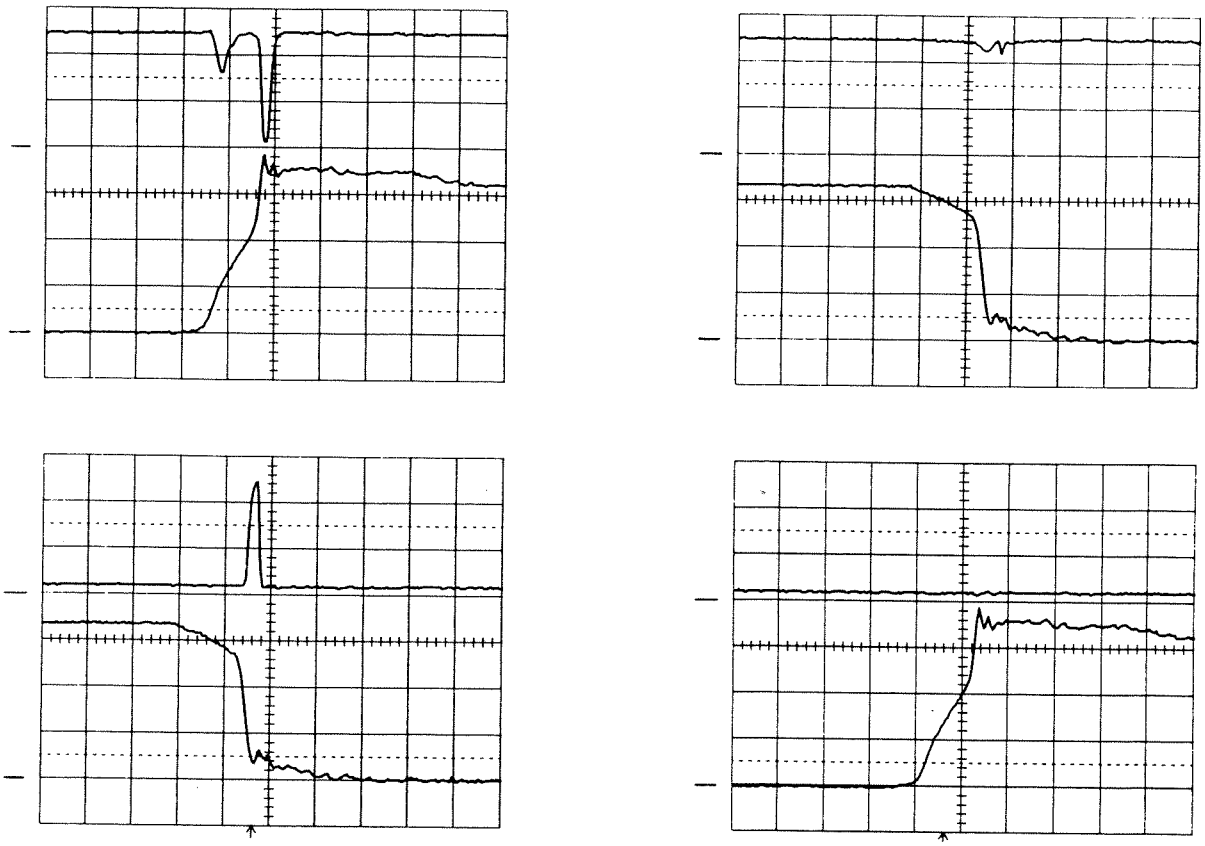


Fig.10 Test of HCPL-2602 optocoupler

upper trace: output signal of the optocoupler
(2V/div, 200ns/div)
lower trace: inverter output voltage
(200V/div, 200ns/div)

This bistable circuit can be realized, e.g., as shown in Fig. 11 (3), by feedback of two CMOS gates via the secondary side of the pulse transformer. Figures 12a,b show the behavior of voltage u_T which is characteristic for the circuit function for turn-on and turn-off of the power transistor; u_T appears at the lower end of the pulse transformer with respect to ground. Due to the switching action a voltage step of about twice the supply voltage appears du-

ring the pulse transmission due to the switching of the stage. One can see from Fig. 12 the excellent disturbance immunity of the system (even for gating the upper transistor) and the total switching delay of gating circuit and power switch. (The gate resistance is 12 Ohms according to the manufacturer's recommendations.)

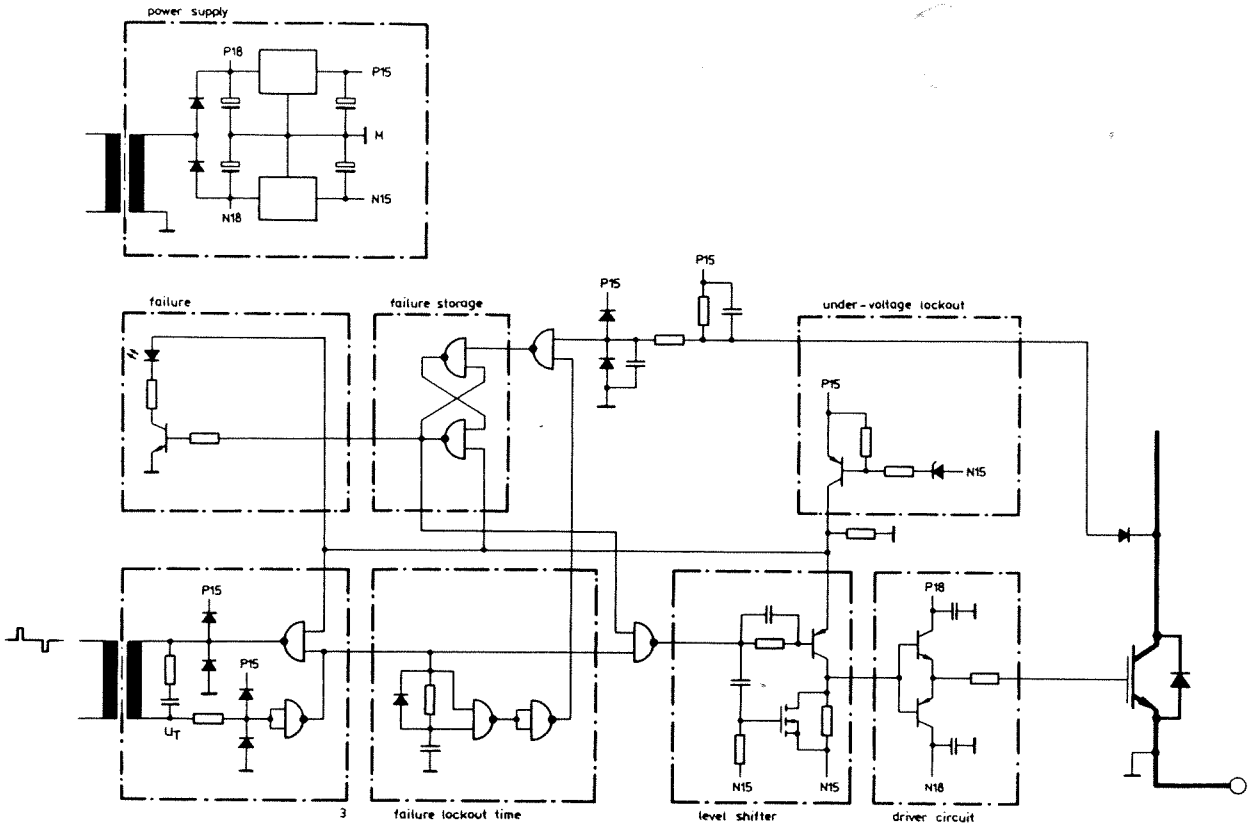
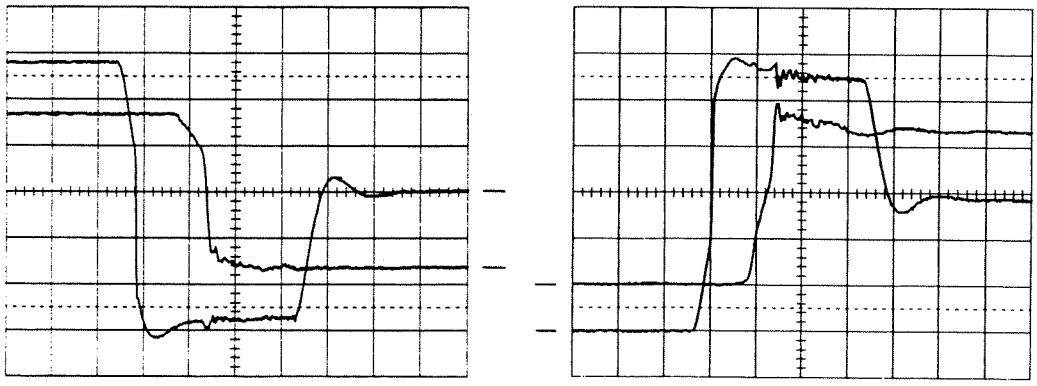


Fig.11 IGBT-Control/Gating Circuit



a) turn-on behavior b) turn-off behavior

Fig.12 Input Signal u_T of the Bistable Circuit (5V/div), Converter Output Voltage (200V/div, 500ns/div)

The under voltage lockout shown in Fig.11 suppresses the turn-on of the power transistor during supply voltage build-up. This is achieved by resetting the bistable circuit as described before and by turning off the level shifter. Additionally, the voltage supply of the failure message circuit (overcurrent sensing) is routed via the under voltage lockout. Therefore, a failure signal is initiated also for a certain supply voltage decrease.

Basically one can use a relatively slow (low cost) optocoupler for the failure message. This is due to the fact that the short circuit current turn-off is performed within the gating/control stage ("self-protecting" driver stage) and that the supervisory monitoring unit only has to react when output currents appear which lie a little above the rated value.

The final stage of the gating circuit most advantageously receives its voltage supply from the nonstabilized supply voltage. This results in relieving the voltage stabilizers. Figure 13 shows a realization of the gating/control circuit. The print area required thereby amounts to 15 cm^2. A further reduction by application of SMD technology is obviously possible.

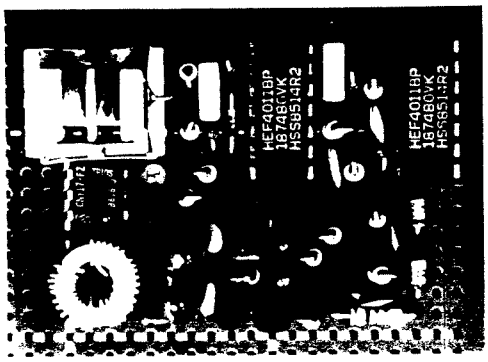


Fig.13

6. CONCLUSIONS AND FUTURE ASPECTS

This paper shows that the realization of an IGBT gating/control circuit with integrated protective functions is possible with justifiable effort. Under retention of the functions described a reduction of the circuit complexity is possible if functional parts of the gating/control circuit are transferred into a central control and monitoring unit. E.g., the failure register can then be realized by evaluation of the interlock delay compensation signal while the system remains self-protecting (automatic turn-off of short-circuit currents). A comparison of this signal (derived from the actual converter output voltage) to the reference pulse pattern results in an information that a turn-off possibly (or likely) linked to an overcurrent has taken place. This makes the avoidance possible of a repetitive turn-on when a short circuit exists. This concept is especially convincing because it allows the inclusion of the failure register into the pulse pattern processing ("interlock delay", see Fig.3) which can be realized purely digitally (e.g., by ASICs). Figure 13 shows a basic circuit for a control/gating circuit which is based on this principle. The bistable circuit mentioned is realized here by including the power switch. Furthermore, a unipolar gating only of the IGBT is assumed. This supposes, however, an appropriate specification of the power switch (which

cannot be fulfilled by all semiconductor manufacturers today). It results in a substantial reduction of the circuit complexity (the level shifter is not necessary.). A more detailed analysis of this gating/control circuit shown in Fig.14 and of the associated pulse pattern processor will be the topic of a future paper.

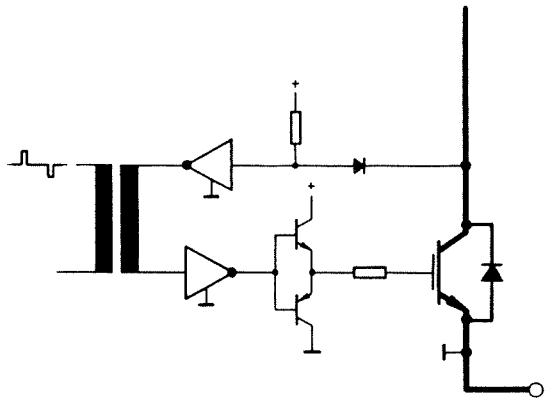


Fig.14 Basic Circuit of a Self-Protecting Low-Cost IGBT Control/Gating Circuit.

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