Comparative Theoretical and Experimental Evaluation of Bridge Leg Topologies of a Three-Phase Three-Level Unity Power Factor Rectifier

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Abstract. In this paper a theoretical and experimental analysis of the voltage stress on the power semiconductors employed in a bridge leg of a unidirectional three-phase three-level PWM (VIENNA) rectifier is given. Furthermore, a new turn-on snubber is proposed which does improve the rectifier efficiency by 0.3% as verified by an experimental analysis and a detailed loss breakdown.

1 INTRODUCTION

For the realization of unidirectional three-phase unity power factor PWM rectifier systems, the bridge leg topology depicted in **Fig.1**(a) was proposed in [1]. (With reference to the total number of power diodes and power switches this bridge leg topology is designated as *6D1S* in the following). Assuming a positive mains phase voltage in the turn-on state of the power transistor S (phase switching function s=1) a positive input current is flowing via the mains diode D_{N+}, the power transistor S and the center point diode D_{M-} against the capacitive output voltage center point M. Turning the power transistor S off, the input current, which is impressed by the input inductor L, commutates into the free-wheeling diode D_{F+} and the positive output voltage rail (cf. **Figs.1**(b) and (c)). So a sinusoidally varying local average value $u_{U,avg}$ (averaging over one pulse period) of the input voltage u_U can be achieved at input b of a bridge leg with reference to M by pulse width modulation (PWM) and results in connection with the mains phase voltage u_N (being applied to a, cf. **Fig.1**(a)) in a sinusoidal shape of the input current i_N and/or in an ohmic fundamental mains behavior of the rectifier system.

The advantages of the bridge leg topology shown in **Fig.1** are:

- The formation of the converter input voltage $u_{U,avg}$ is by switching between three voltage levels, i.e. between the output voltage center point M and the positive output voltage rail (for $u_{U,avg}>0$) or between M and the negative output voltage rail (for $u_{U,avg}<0$) and not like for conventional two-level PWM rectifier systems by directly changing over between the two output voltage rails [2]. Consequently, as compared to a two-level topology the three-level structure shows for equal inductance of the input inductor L a significantly lower value of the input current ripple. This is due to the lower deviation of the rectifier input voltage u_U from the ideal sinusoidal shape;
- Positive and negative phase currents are flowing across the same power transistor S and not via different devices. Therefore, the utilization of the power transistor is higher and the transistor conduction losses are decreased (for equal total transistor silicon area). Also, only a single drive circuit has to be provided per bridge leg.
- According to the three-level structure, the voltage stress on all power semiconductors is defined by only half the output voltage. In contrast, the valves of the two-level topology are stressed with the total output voltage value. The lower value of the turn-off and turn-on voltage and the lower reverse recovery time of diodes with half voltage rating (D_{F+} and D_{F-}) results in considerably lower switching losses.

However, as a more detailed analysis shows, no direct limitation of the blocking voltage stress on the components S, D_{N+} and D_{N-} to half the output voltage is given. If we assume according to **Fig.1**(c) a conducting diode D_{F+} the source potential of S theoretically could be pulled down to the negative output voltage rail what would result in stressing S (and also D_{N-}) with the total output voltage. There no limitation of the overvoltage is provided by the diodes D_{M-} or D_{F-}. Up to now, this issue has not been treated in the literature and therefore shall be analyzed in detail in this paper (cf. **section 2**). Furthermore, a simple implementation of a passive turn-on snubber (avoiding auxiliary switches) will be discussed in order to further improve the high efficiency of the energy conversion (cf. **section 3**). **Section 4** shows the analysis of the transistor switching behavior with turn-on snubber in comparison to hard switching. The efficiency improvement is proven in **section 5** by a loss breakdown of a 10kW rectifier prototype (input voltages: 320, 400, 480V_{rms} line-to-line, output voltage: U_O=800Vdc, pulse frequency f_P=25kHz) which shows that the elimination of the power transistor turn-on switching losses would result in a reduction of the total switching losses by about ½ [3] and/or in an increase of the efficiency by ≈ 0.3% to 97.6%.

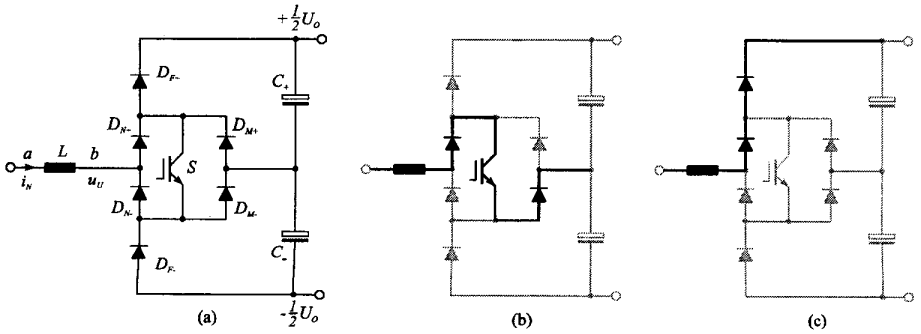

Fig.1: Structure of the bridge leg of a three-phase/level unity power factor PWM (VIENNA) rectifier according to Fig.9 in [1] (cf. **(a)**) and conduction states for $i_N>0$ and s=1 (cf. **(b)**) and s=0 (cf. **(c)**). For the sake of brevity, this topology is designated in the present paper as *6D1S* with reference to the number of power diodes and power transistors employed.

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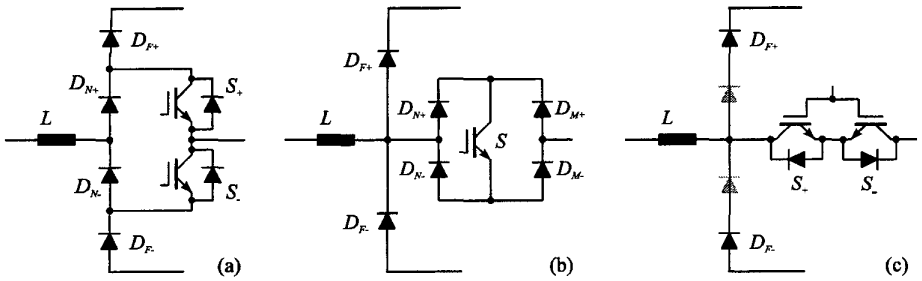

Fig.2: Implementations of a bridge leg of a three-phase/level PWM rectifier as proposed in [2] (cf. **(a)**) and [3] (cf. **(b)** and **(c)**). For the bridge leg topology shown in (c) a single diodes or a series connection of two diodes with lower blocking capability and/or lower reverse recovery time could be employed for realizing D_{F+}, D_{F-}.

2 ANALYSIS OF THE VOLTAGE STRESS ON THE POWER SEMICONDUCTORS

The results of an experimental analysis of the bridge leg *6D1S* are shown in **Fig.3** for hard switching as implemented in a 10kW prototype of the three-phase three-level unity power factor rectifier. The voltage stress of the power semiconductors is defined by half of the total rectifier output voltage U_O. Therefore, for a rectifier system with a total output voltage of U_O=800V power semiconductor components with a voltage rating of 600V can be employed. It is necessary to point out, that although it seems that the mains diodes D_N and the center point diodes D_M are stressed with switching frequency (cf. Figs.3 (c) and (d)) they can be realized by a conventional single-phase bridge rectifier module. The diodes are in blocking state during half of the mains time period where the blocking voltage is varying with switching frequency. For the free-wheeling diodes D_F and the center point diodes D_M the voltage stress is well defined. This is because of the series connection of the diodes D_F and D_M which does limit the voltage stress on each device to the voltage being present across the partial output capacitor C_+ and/or C_-. The voltage stress on the power transistor S and on the mains diodes D_N is not clearly defined by the circuit structure. In the turn-on state of the power transistor S a positive input current i_N>0 is flowing via the mains diode D_{N+} and continuing via the power transistor S and via the center point diode D_{M-} against the capacitive output voltage center point M. (cf. Fig.1(b)). Turning the power transistor S off, the input current, which is impressed by the input inductor L, commutates into the free-wheeling diode D_{F+} (cf. Fig.1(c)) and into the positive output voltage rail. In this point of time the collector of the power transistor is clamped to the positive rail voltage. A transient overvoltage exceeding the partial output voltage u_{C+} being present across C_+ would force the center point diode D_{M-} in the blocking state. However, since D_{M-} is realized by a conventional mains rectifier diode with relatively slow reverse recovery behavior, the emitter of the power transistor effectively is connected to the output voltage center point immediately after turn off. Accordingly, the voltage stress on the power transistor is limited to the partial output voltage u_{C+} (with the exception of switching overvoltages due to parasitic wiring and output capacitor inductances). For applications where one could not rely on the reverse recovery property of the center point diodes a low-power overvoltage limitation circuit, such as a DRC snubber or a Zener-clamp, could be provided for the power transistor. In case this overvoltage limitation circuit is active the power transistor emitter or collector is clamped to M via D_{M+} or D_{M-} and transistor voltage limitation is taken over by D_{F+} or D_{F-}. As soon as the voltage stress of the power transistor is defined also the voltage stress of the mains diodes D_{N+} and D_{N-} is defined precisely because of the conducting series connected diode D_{N-} or D_{N+}.

It should be pointed out, that the question concerning extra measures for defining the voltage stress on the power semiconductors also does exist for the components of alternative realizations of the bridge leg topology (cf. D_{N+} and D_{N-} in **Fig.2**(a) and diodes D_{N+}, D_{N-}, D_{M+} and D_{M-} as well as the power

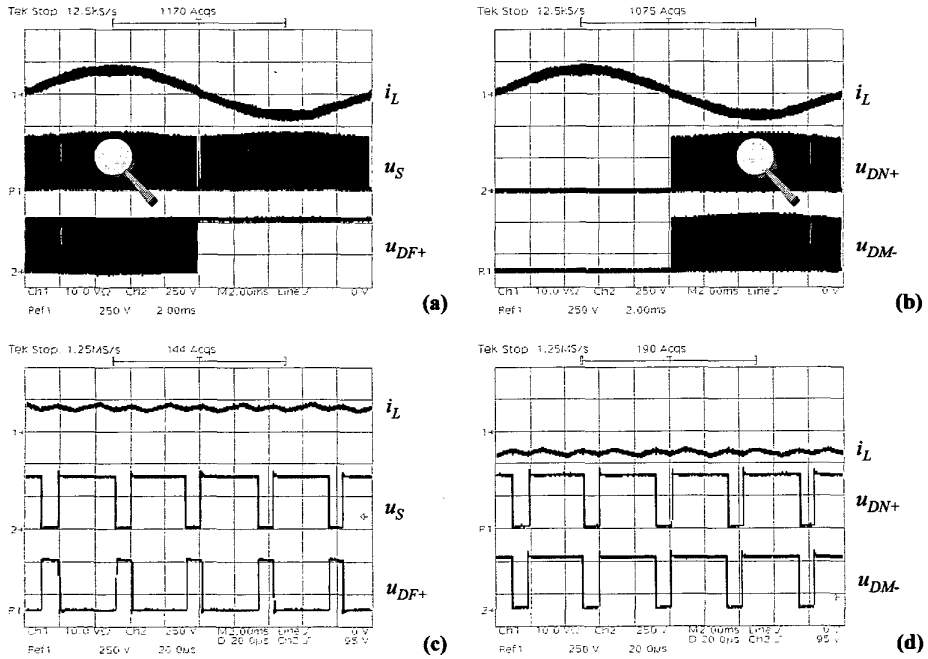

Fig.3: Demonstration of the voltage stress of the power semiconductors of a bridge leg according to Fig.1(a) employed in a 10kW prototype of the rectifier system. Operational conditions: Input voltage $U_{N,LL}$=480V, output voltage U_O=800V, output power P_O=4kW. Shown are the input inductor current i_L (10A/div) and the voltage stresses (250V/div) of the power transistor u_S, the free-wheeling diode u_{DF+} (cf. **(a)**, **(c)**), the mains diode u_{DN+} and the center point diode u_{DM-} (cf. **(b)**, **(d)**) in a mains time period (cf. (a), (b)) and in detail (delayed trigger instant indicated by the magnifying glass in (a) and (b)) in a switching time scale (cf. (c), (d)).

transistor S in **Fig.2**(b) [1]). Only the bridge leg topology depicted in **Fig.2**(c) provides a clear definition of the voltage stress on all components, but with a lower utilization of the total power transistor silicon (current flow for s=1 and i_N>0 only via S_+, for i_N<0 only via S_-). However, there the free-wheeling diodes D_{F+} and D_{F-} have to show a high blocking capability as determined by the total output voltage value U_O. Accordingly, a relatively higher reverse recovery time and/or significantly higher turn-on losses as compared to the bridge topology *6D1S* (cf. Fig.1(a)) does occur. This problem could be solved as proposed in [4] for single-phase boost-type unity power factor rectifiers by replacing D_{F+} and D_{F-} by a series connection of two diodes of lower blocking capability or by employing a turn-on snubber.

3 PRINCIPLE OF OPERATION OF THE NOVEL TURN-ON SNUBBER

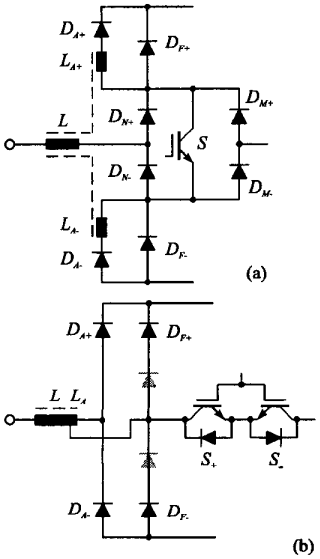

Fig.4: Turn-on snubber circuit based on the concept proposed in [5] for bridge leg topology *6D1S* (cf. **(a)**) and alternative realization for the bridge leg topology shown in Fig.2(c) (cf. **(b)**).

A new turn-on snubber circuit which is based on a concept proposed in [5] for a single-phase unity power factor rectifier is depicted in **Fig.4**(a) [6] for the bridge leg topology *6D1S*. The snubber does not (!) increase the turn-off overvoltage of the power transistor and can be employed in modified form also for the bridge leg topology shown in Fig.2(c) (cf. **Fig.4**(b)). For the sake of brevity the principle of operation is discussed in the following only for bridge leg *6D1S*. The auxiliary components facilitating the turn-on loss reduction are D_{A+} and L_{A+} for i_N>0 and D_{A-} and L_{A-} for i_N<0. Assuming a positive input current i_N>0 at the turn-off of the power transistor S, the input current directly commutates to D_{F+} (cf. **Fig.5**(a)), i.e. no overvoltage due to L_{A+} does occur. Now due to the magnetic coupling of L_{A+} and of the input inductor L a voltage is generated (cf. **Fig.5**(b)) across L_{A+} which does divert the input current flow from the diode D_{F+} to the series connection of D_{A+} and L_{A+}. If now the winding ratio N_A/N (L_{A+}~N_A^2, L~N^2) and the magnetic coupling k of L_{A+} to L is chosen in a way, that the current in D_{F+} does reach zero within the off-time of the power transistor S the free-wheeling diode D_{F+} is already biased in blocking direction at the following turn-on of the power transistor S. Accordingly, only a low reverse recovery current of the auxiliary diodes D_{A+} will occur in a point in time where the power transistor voltage is already close to zero. The reverse recovery current is low due to the relatively low rate of change of the current in D_{A+} as defined by the stray inductance $L_{A\sigma+}$= $(1\text{-}k^2)L_{A+}$ (cf. Figs.8(c) and (g) and (1)).

At hard switching the transistor current rate of rise is $(di_S/dt)_{max}$ ≈1A/ns (cf. Figs.8(a) and (e)). In order to reduce the transistor voltage to low values immediately after turn-on we therefore have to provide a minimum effective inductance of the turn-on snubber of

$$L_{A\sigma,\min} = 2...3.\frac{\frac{1}{2}U_O}{(di_S/dt)_{\max}}. \qquad (1)$$

In the case at hand there results $L_{A\sigma,min}$≈1µH for ½U_O=400V.

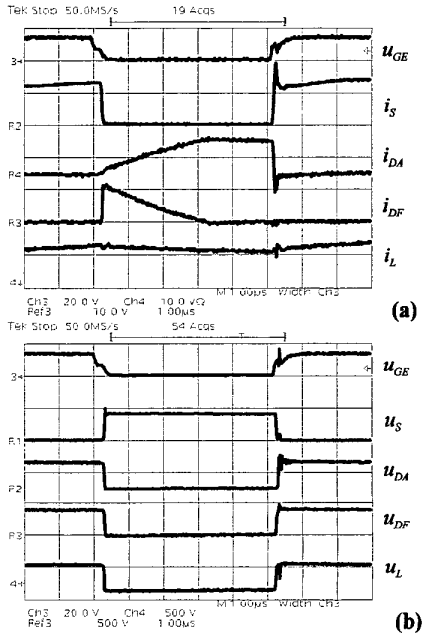

Fig.5: Principle of operation of the turn-on snubber depicted in Fig.4(a). Shown are the gate-emitter voltage u_{GE} (20V/div), the current (10A/div) and the voltage (500V/div) of the power transistor S (i_S and u_S), the current and voltage of the auxiliary diode D_A (i_{DA} and u_{DA}), of the free-wheeling diode D_F (i_{DF} and u_{DF}) and of the input inductor L (i_L and u_L). Operational conditions (cf. Fig.6): input voltage $U_{R\text{-}M}$=300V, output voltage ½U_O=400V.

Unfortunately, the turn-on snubber circuit (cf. Fig.4(a)) does not operate in the whole mains voltage and current range, e.g. with high mains phase voltage and high current values the voltage difference applied to the input inductor L is too small to generate a sufficient voltage in the coupled winding L_A to force the free-wheeling diode current completely into D_A within the free-wheeling interval. Also with very low input voltages the free-wheeling interval would be too short in time for commutating the free-wheeling current into the auxiliary diode D_A despite the relatively high voltage appearing across L withing the turn-off interval. This deficiency however is alleviated by the ohmic mains behavior of the rectifier where the current to be commutated shows low values at low mains voltages (low turn-off times); accordingly, any remaining switching losses will be negligible in a first approximation. Therefore, the behavior at low input voltages is not analyzed in more detail in this paper.

In order to fully commutate the free-wheeling current i_{DF} into the auxiliary diode D_A during turn-off a minimum slope of the auxiliary diode current of

$$\frac{di_{D_A}}{dt} = \frac{i_{D_F}}{(1-\delta)T} = \frac{\frac{N_2}{N_1}(\frac{1}{2}U_O - u_N)}{L_{A\sigma}} \quad (2)$$

(δ denotes the transistor turn-on duty cycle, T denotes the switching frequency period) with

$$L_{A\sigma} = L_A(1-\frac{M^2}{L_A L}) \quad (3)$$

by proper selection of $L_{A\sigma}$ and N_2/N_1 (M denotes the mutual inductance of L_A and L which also could be characterized by a coupling factor $k=M/\sqrt{L_A L}$ and/or a stray coefficient $\sigma = 1-k^2$, $L_{A\sigma}=\sigma L_A$; u_N denotes the mains phase voltage).

Remark: For (2) the influence of the switching state of the other two phases of the three-phase rectifier on the voltage appearing across L has been neglected for the sake of clearness.

Assuming zero fundamental voltage drop across L

$$u_N = (1-\delta)\tfrac{1}{2}U_O \quad (4)$$

is valid. Combining (2) and (4) there results for the duty cycle limits

$$\delta_{1/2} = \frac{1}{2} \pm \sqrt{\frac{1}{4} - \frac{L_{A\sigma}\frac{N_1}{N_2} i_{D_F}}{T\frac{1}{2}U_O}} \,. \quad (5)$$

For a practical realization of a converter system with $T=1/f_P=40\mu s$, $\frac{1}{2}U_O=400V$, $N_1=72$Wdg., $N_2=4$Wdg., $i_{DF}=20A$ and a stray inductance $L_{A\sigma}=1.6\mu H > L_{A\sigma.min}$ (cf. (1)), the resulting duty cycle limits are $\delta_1=96.3\%$ and $\delta_2=3.7\%$, where δ_1 is not considered further as already mentioned. The number of turns $N_2=4$ of the concentrated auxiliary winding on the input inductor toroidal core has been determined by experiments. The resulting turns ratio $N_1/N_2=18$ does match well with the dimensioning guideline $N_1/N_2 = 5 \ldots 20$ given in [5].

4 Analysis of the Switching Behavior With and Without Turn-On Snubber

In **Fig.6** the schematic of the measurement setup for the analysis of the switching behavior is depicted. The measurement circuit is realized on a standard double-sided printed circuit board which has been designed for a 2-U high power density (ρ = 3kW/l) rectifier unit. All the measurements are done without using any overvoltage limitation (DRC) circuits or RC snubbers across the power semiconductor components.

Table 1 shows a detailed listing of the components used for the experimental analysis described in this paper. The power transistor S is driven with a pulse sequence having a low pulse width and a repetition rate of only f_P≈1Hz. The power semiconductor components are mounted on an aluminum carrier. The temperature of the carrier is controlled to a constant value of 25°C or 125°C by means of heating resistors. The carrier temperature does define the power semiconductor junction temperature with respect to the low frequency and low pulse width of the pulse sequence depicted in **Fig.7**. The input inductor current i_L is increased up to an adjustable threshold level where the power transistor is turned off for 4µs. Subsequently the power transistor is turned back on for again 4µs. The detailed investigation of the switching behavior is done using this final turn-on pulse.

The results of the experimental investigation of the turn-on and turn-off behavior are depicted in **Figs.8**(a) ... (h) for a transistor current of i_S=20A and for junction temperatures of T_j =25°C and T_j=125°C with and without turn-on snubber circuit. The turn-on snubber circuit does considerably reduce the transistor turn-on switching losses, e.g. for a junction temperature of T_j=125°C and i_S=20A from w_S=55.32/0.0968=571µJ to w_S=8.295/0.0968=86µJ (= −85%, cf. Fig.8(e) and (g)).

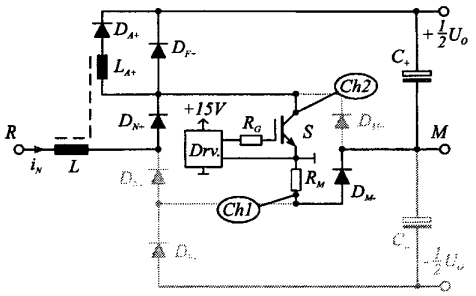

Fig.6: Measurement setup for the of the turn-on snubber employing the power transistor S (Int. Rect. IRG4PC50W) in combination with the free-wheeling diode D_{F+} and the auxiliary diode D_{A+} (both of type Int. Rect. HFA15TB60). The components shown in gray are not placed on the evaluation board.

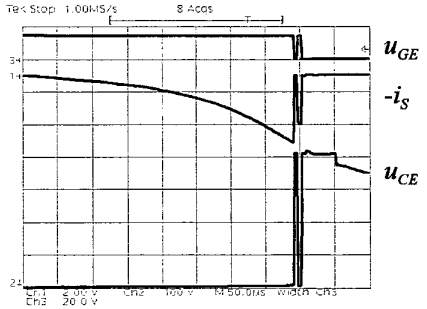

Fig.7: Pulse sequence employed for the analysis of the turn-on snubber circuit. Top: u_{GE} @ 20V/div; middle: $-i_S$ @ 20A/div; bottom: u_{CE} @ 100V/div. The detailed investigations are done at the end of the sequence (last turn-on and turn-off).

The transient turn-off overvoltage shows a maximum value of 508V (cf. Fig.8(h)) at a partial output voltage of $\frac{1}{2}U_O$=400V and a

Part	Type / Value
S	Int. Rect. IRG4PC50W
D_{N+}, D_{M-}, D_{F+}, D_{A+}	Int. Rect. HFA15TB60
C_+	2x 150µF / 450V + 220nF / 630V
L	700µH, iron powder core
R_M	T&M Research SDN-414-10 0.0968Ω, 2GHz, 2W
R_G	15 Ohm, SMD MiniMelf
Drv.	Optocoupler drive Agilent HCPL 3120
Ch1	Tektronix TDS 544A 500MHz 1.0m coaxial cable
Ch2	Tektronix TDS 544A 500MHz 1:10 voltage probe 350 MHz
R-M	Input voltage, 55VDC
$+\frac{1}{2}U_O$	Half output voltage, 400VDC

Tab.1: List of components and equipment employed in the measurement setup.

switched transistor current of i_S=20A and T_j=125°C. Although the switching speeds are comparably low [7] the overshoot of the transistor voltage is relatively high. This is due to the disadvantageous shape of the switched current which does not decrease linearly but step-like at a point in time where the voltage applied to the transistor is already on an elevated level. It therefore cannot be not recommended to operate this type of switch with higher currents without any overvoltage limitation circuit.

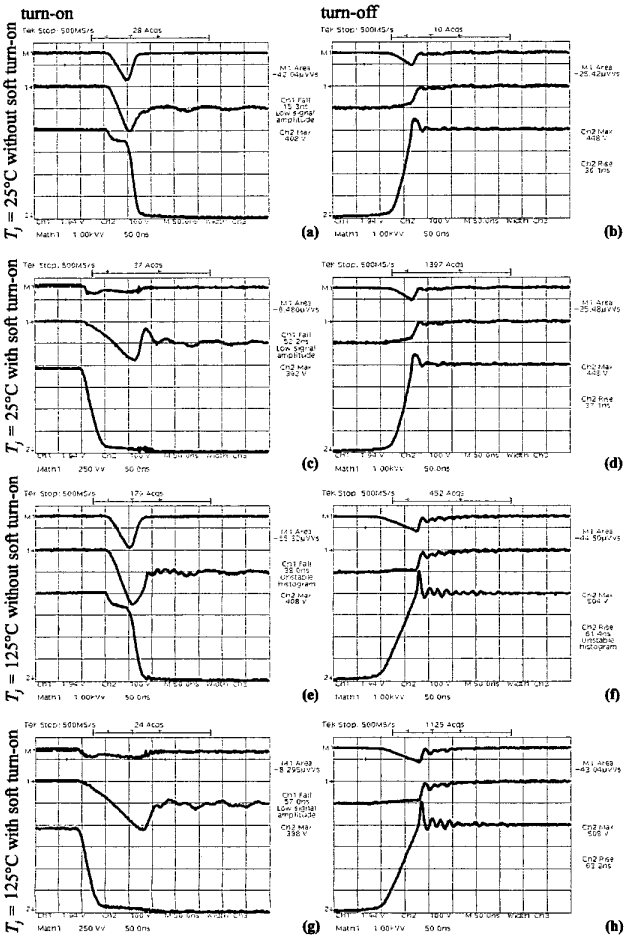

Fig.8: Experimental analysis of the switching behavior of the power transistor IRG4PC50W (warp speed IGBT) in connection with the ultrafast free-wheeling diode HFA15TB60 for application in a three-phase/switch/level PWM (VIENNA) rectifier system with and without turn-on snubber. Test parameters according to Table 1. **(a)** ... **(d)**: junction temperature T_j=25°C; **(e)** ... **(h)** T_j=125°C; **(a)** and **(e)**; turn-on of the power transistor *S* without turn-on snubber, **(c)** and **(g)**: turn-on of the power transistor *S* with turn-on snubber, **(b)** and **(f)**; turn-off of the power transistor *S* without turn-on snubber, **(d)** and **(h)**: turn-off of the power transistor *S* with turn-on snubber. Power transistor current being switched i_S=20A. Top trace: negative switching power loss $-p_s$ (10kW/div except (c) and (g): 2.5kW/div), middle: negative power transistor current $-i_S$ (20A/div), bottom: power transistor collector emitter voltage u_{CE} (100V/div). The turn-on snubber circuit does reduce the transistor turn-on switching losses for T_j=125°C and i_S=20A from w_S=571µJ to w_S=86µJ (= –85%).

Remark: For determining the switching power losses with sufficient accuracy a high bandwidth of the voltage and current measurement is required with respect to the high switching speed without turn-on snubber. In the case at hand a coaxial shunt with a nominal value of 0.1Ω with a bandwidth of 2GHz has been employed (cf. **Fig.9**, [8]) for measuring the transistor current.

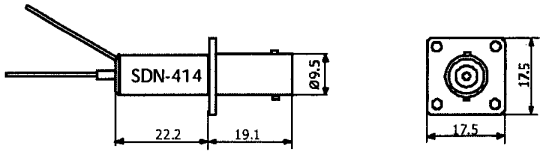

Fig.9: Shunt employed for transistor current measurement [8].

5 Analysis of the Power Losses With and Without Turn-On Snubber

Table 2 shows a detailed listing of the loss components at different input voltages (U_N = 320V, 400V, 480V line-to-line) of a 25kHz rectifier system employing three bridge legs like shown in Fig.1. The current values are calculated according to [3], the switching loss values according to $P_S=f_P k|I_N|_{avg}$ with k_{on}=28.5µJ/A at turn-on and k_{off}=22.9µJ/A at turn-off as resulting from the switching loss measurements for a junction temperature of T_j=125°C (Fig.8). The diodes are modeled as ideal diodes with a forward voltage drop

Input power	P_N=	11000	11000	11000	W
Input voltage	$U_{N,l\text{-}l}$=	320	400	480	V
Input current	$I_{N,rms}$=	19.85	15.88	13.23	A
Output voltage	U_O=	800	800	800	V
IGBT current (IRG4PC50W)	$I_{S,rms}$=	13.25	8.80	5.43	A
$U_{CE,sat}$=0.9V, $R_{CE,on}$=0.03Ω	$I_{S,avg}$=	8.70	5.13	2.75	A
Conduction loss @125°C	$P_{S,C}$=	13.1	6.94	3.35	W
Turn on (f_P=25kHz, k_{on}=28.5µJ/A)	$P_{S,on}$=	12.74	10.19	8.49	W
Turn off (f_P=25kHz, k_{off}=22.9µJ/A)	$P_{S,off}$=	10.25	8.20	6.83	W
3x IGBT total losses	P_S=	108.2	76.0	56.0	W
Free-wheeling diode current	$I_{DF,rms}$=	10.45	9.35	8.53	A
U_{DF0}=1.18V, R_{DF}=24mΩ	$I_{DF,avg}$=	4.58	4.58	4.58	A
6x Free-wheeling diode losses	P_{DF}=	48.2	45.0	42.9	W
Mains diode current	$I_{DN,rms}$=	14.03	11.23	9.36	A
U_{DN0}=0.85V, R_{DN}=12mΩ	$I_{DN,avg}$=	8.93	7.15	5.96	A
6x Mains diode losses	P_{DN}=	59.7	45.5	36.7	W
Center point diode current	$I_{DM,rms}$=	9.37	6.22	3.84	A
U_{DM0}=0.85V, R_{DM}=12mΩ	$I_{DM,avg}$=	4.35	2.56	1.37	A
6x Mains diode losses	P_{DM}=	28.5	15.9	8.1	W
Total power semiconductor losses		244.7	182.4	143.7	W
3x Input choke (R_L=65mΩ, P_{FE}=5W)	P_L=	91.8	64.2	49.1	W
Output capacitor current	$I_{CO,rms}$=	12.9	9.7	6.9	A
4x Output capacitor (R_{ESR}=0.233Ω)	P_{CO}=	38.6	22.0	11.0	W
Auxiliary power (housekeeping, fans)	P_{aux}=	30.0	30.0	30.0	W
Snubbers, PCB, var. distributed losses	P_{add}=	50.0	50.0	50.0	W
Total power losses	P=	455.0	348.6	283.9	W
Efficiency	η=	95.9	96.8	97.4	%
Efficiency with turn-on snubber	η_s =	96.2	97.1	97.6	%

Tab.2: Listing of the partial losses of a 10kW/25kHz rectifier system. The improvement of the overall efficiency in case a turn-on snubber is employed is in the range of 0.2 ... 0.3% in correspondence with the relatively low system switching frequency (f_P=25kHz).

U_D and a (differential) series resistance R_D. The iron losses of the input inductors are assumed to show a constant value of P_{FE}≈5W (a calculation would require a consideration of the nonlinear property of the iron powder core and of the frequency spectrum of the input current which does changes with input voltage what is out of the scope of this paper). Also the auxiliary power which contains housekeeping and fans (P_{aux}=30W) as well as an additional share of the power losses for the snubber losses, PCB resistance and various other distributed power losses (P_{add}=50W) are assumed to be of constant value. The main shares of the losses are shown in graphical form in **Fig.10** for three different input voltages.

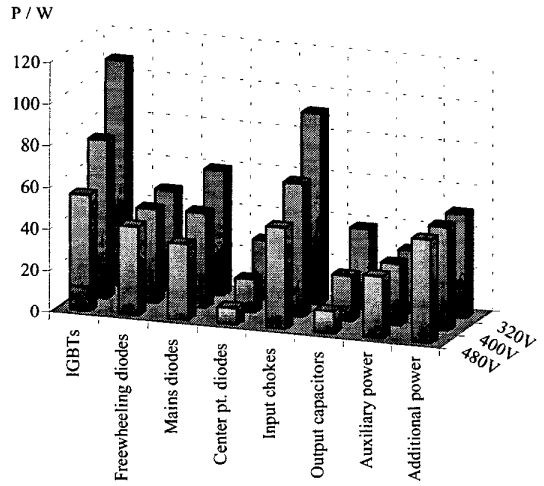

Fig.10: Component power losses as given in Table 2 for different input line-to-line voltages.

6 CONCLUSION

The total efficiency of the converter system with a switching frequency of f_P=25kHz can be improved by 0.2 ... 0.3% by applying the proposed turn-on snubber technique. This corresponds to a reduction of the losses of the power semiconductors of 15% and of the total losses of up to 10%. This improvement is achieved also in case free-wheeling diodes and auxiliary diodes being not of ultra fast recovery type are employed. Accordingly, the practical realization of the rectifier does not require special power semiconductor devices which could be available only from a single source.

A further improvement of the efficiency could be achieved by replacing the Warp-Speed IGBTs by CoolMOS power transistors of type number SPW47N60C2 [7], [9] and by increasing the switching frequency by a factor of 2 or 3. There, due to the decreasing inductance of the input inductors the parasitic winding resistance of the input chokes would be reduced and the resulting efficiency of the total rectifier system could be 98.0% for a mains voltage of 480V line-to-line. The analysis of a further improvement of the rectifier performance by active or passive turn-on *and* turn-off snubbers is in the scope of the continuation of the research on converter systems of ultra high power density at the ETH Zurich.

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