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Protection of MV Converters in the Grid: The Case of MV/LV Solid-State Transformers

T. Guillod,
F. Krismer,
J. W. Kolar

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

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Thomas Guillod, *Student Member, IEEE*, Florian Krismer, *Member, IEEE*, and Johann W. Kolar, *Fellow, IEEE*

***Abstract*— Solid-state transformers (SSTs) are a promising technology as they provide new functionalities and services enabling future smart grids. An SST establishes the interface between an MV ac grid and an LV (ac or dc) grid or load. The SST must provide high reliability even in the event of certain grid faults, where the SST is subject to exceptional electrical stresses. In addition, the MV and LV grids are exposed to failures of the SSTs. Spurred by such challenging requirements, this paper defines the different relevant stresses, identifies the corresponding protection needs, and proposes adequate protection circuitries and devices. The protection mechanisms that are currently used for low-frequency transformers are analyzed and an adapted version is proposed for SSTs. MV short circuits and overvoltages are identified as the most critical situations and are analyzed in detail. From the presented in-depth investigation, guidelines are extracted for designing robust SSTs and are applied to a 1 MVA, 10 kV SST.**

***Index Terms*— Power distribution faults, power electronics, power transformers, power-electronic transformers, solid-state transformers (SSTs), substation protection, surge protection.**

I. Introduction

CURRENTLY, interfacing between the different voltage levels in the grid is done with *low-frequency transformers* (LFTs). The need to integrate renewable energy sources into LV ac or dc grids and the progress of the semiconductor technology has led to the idea of *solid-state transformers* (SSTs) where the power conversion is realized with a medium-frequency link [1]–[3]. SSTs are typically aimed to interface the MV ac grid (6–36 kV) with LV ac or dc grids (48–400 V). SSTs have been proved to achieve a high efficiency conversion from ac to dc [4] and allow for power flow control, active filtering, reactive power compensation, energy storage integration, and so on [3], [5]. In order to use these new features, different applications that have been proposed and examined for SSTs are as follows.

1) SSTs used as distribution transformers (as a replacement for an LFT) in a traditional distribution grid. In this case, the power flow is mainly directed from MV to LV and no monitoring or control of the loads is possible [4].
2) SSTs forming the interface between the MV grid and smart microgrids with renewable energy production and control capabilities [3].
3) An SST employed to directly connect renewable energy plants (for example, PV plants) to the MV ac grid [3].
4) Industrial grids where SSTs could be used as unidirectional power supplies connected to the MV grid (datacenters, power-to-gas systems, etc.) [6].
5) SSTs used as a part of a locomotive power supply chain in order to replace LFTs [7], [8]. In this case, the SST does not form the interface with a distribution grid. Therefore, this application is not considered further in this paper.

All these applications require the SST to be integrated into the grid. The SST, therefore, is subject to perturbations that originate from the grid or the loads. The control of SSTs in the grid has already been examined [3], [9] while the protection of SSTs in the grid has so far not been covered in the literature and remains a widely open topic [10]–[12]. From the above list of possible applications of SSTs, the first item, i.e., the usage of SSTs in a traditional three-phase distribution grid, leads to the largest stresses due to the lack of monitoring and control capabilities of the surrounding system. For this reason, this application will be further considered. Yet, the presented results can be easily adapted to the alternative applications.

The recent literature identifies different converter topologies suitable for the realization of SSTs, depending on particular needs, e.g., single-cell or multicell realizations and unidirectional or bidirectional energy conversion [2], [14], [15]. The multicell variant with independent phase legs, depicted in Fig. 1, is very popular as it allows the use of semiconductors with lower blocking voltages and features a bidirectional modular structure [4], [7], [13], [16]. The different cells are coupled in an *input series, output parallel* (ISOP) structure. In this paper, the following ratings are considered (based on the MEGAlink concept currently under research at the ETH Zurich): 10 kV/400 V (phase-to-phase RMS voltage), 1 MVA, and 50 Hz [4].

As shown in Fig. 2, this SST is employed in a distribution substation where it interfaces with the MV and LV grids. The different abnormal operating conditions considered in this paper are classified as follows.

1) *Internal Fault:* A fault inside the transformer can produce a significant stress for the grid due to the resulting short or open circuits [17], [18].
2) *Lightning Surge:* Direct or indirect atmospheric discharges are quite frequent in MV grids and cause massive overvoltages [18]–[21].

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The authors are with the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology Zurich, 8092 Zurich, Switzerland.

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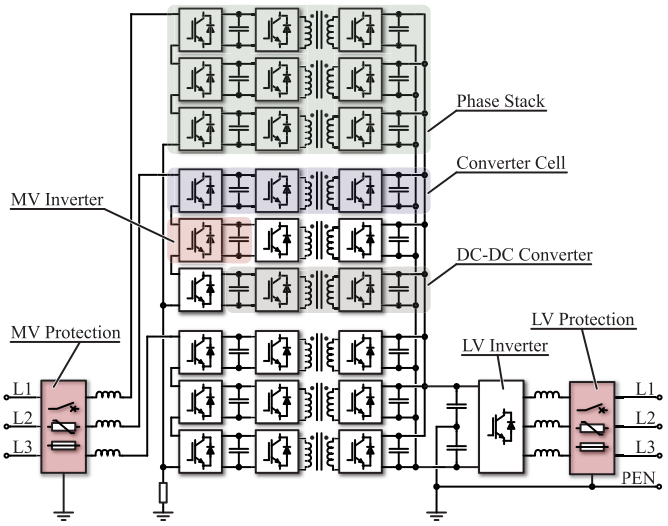


Fig. 1. Structure of a three-phase ac-ac SST, according to [4] and [13], including the protection devices. The ac–dc MV inverters of the SST are composed of stacked single-phase inverters and are coupled via dc–dc converters in an ISOP configuration.

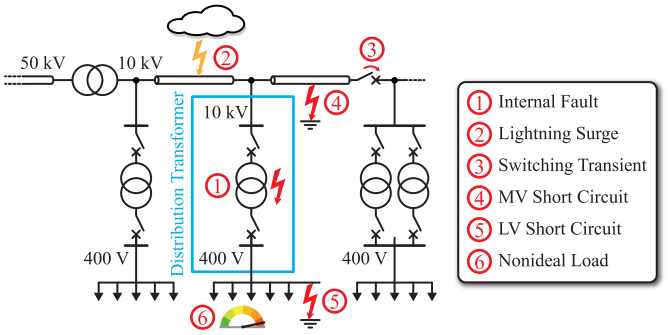


Fig. 2. Typical three-phase MV/LV distribution grid topology with three MV/LV substations. The relevant transformers, lines, and loads are shown schematically. The encircled numbers indicate the different faults considered for the highlighted transformer.

3) *Switching Transient:* Switching transients (overvoltages and overcurrents) occur when a fault is cleared or, more commonly, when a switch is opened or closed for a grid topology reconfiguration [19], [22].
4) *MV Short Circuit:* In a three-phase grid, different types of short circuits are possible and lead to transient overcurrents and overvoltages [17], [18], [23], [24].
5) *LV Short Circuit:* Short circuits in the LV grid are similar to the MV short circuits. The main difference is that LV grids have a neutral conductor, which provides a solid earthing [17], [18], [25].
6) *Nonideal Load:* In addition to the above-mentioned faults, nonideal loads, e.g., overloads, load steps, asymmetric loads, and nonlinear loads drawing a distorted current, can also represent a relevant stress for the transformer [17], [18], [25].

Most of the above-mentioned faults are only acceptable during short time intervals without leading to a partial blackout of the grid and/or the destruction of devices. The grid is thus a hostile environment for a transformer and, in this context, LFTs are much more robust than SSTs, which are composed of filters, power electronic devices, capacitors, sensors, etc. For this reason, this paper proposes models for the aforementioned fault situations in order to allow a detailed examination of the protection of SSTs that are operated between MV and LV grids. The required models could be developed based on the results obtained from transient simulations of the MV and LV grids. However, transient simulations of the grid impose the definition of a specific grid type (e.g., industrial and residential) and topology, which are typically subject to changes over time. This strongly limits the generality of such analysis. With increasing complexity of the considered models, it is, in addition, increasingly difficult to clearly identify critical implications of the different faults on the components of the SST in order to extract comprehensible design rules. Therefore, this paper employs comprehensive and scalable models, which do not require the modeling of the complete grid, to identify the measures needed to provide adequate protection of the SST and to evaluate the implications of these protection measures on the SST properties, e.g., volume and efficiency.

The paper is organized as follows. Section II analyzes the general protection requirements and Section III reviews the protection scheme used for LFTs. In Section IV, this scheme is adapted for SSTs and the impact of short circuits and overvoltages is examined in more detail. Section V, finally, proposes guidelines for the design of a reliable SST.

II. Protection Requirements

The role of the protection system is to protect the transformer from a grid fault, the grid from a fault in the transformer, the MV grid against the LV grid, and the LV grid against the MV grid. The quality of a protection system can be evaluated with the following criteria [18], [25], [26].

1) *Selectivity:* The action of the protection system should be coordinated with the other components in the grid in order to minimize or suppress the impacts of the faults for the end customers.
2) *Sensitivity:* The protection devices should be able to detect all the faults, even those with small magnitudes.
3) *Security:* The protection devices should not trip in case of small disturbances or if another device is responsible for clearing the fault (nuisance tripping).
4) *Safety:* The protection devices should prevent hazards during a fault and allow an isolation of the system for maintenance or inspection.
5) *Speed:* The faults should be handled as fast as possible in order to maximize safety and to minimize perturbations in the grid and exceedingly high stresses applied to the devices.
6) *Reliability:* The protection devices offer reliable operation during a fault even if they are not in use except for the fault events.
7) *Losses:* The protection system should not have significant losses during rated operation.
8) *Cost:* The protection system costs should be reasonable compared to the price of the equipment to be protected.

Some conflicts exist between these goals. Nuisance tripping, for example, may happen more likely for a system with very sensitive or fast protection devices. Therefore, the design of the

TABLE I
DIFFERENT SHORT CIRCUIT TYPES IN AN MV OR LV GRID [17], [27]

Identifier	Description	Sym.	Earth
3p	Three-phase symmetric fault	yes	yes/no
2p	Phase-to-phase fault	no	no
1pg	Single phase-to-ground fault	no	yes
2pg	Double phase-to-ground fault	no	yes

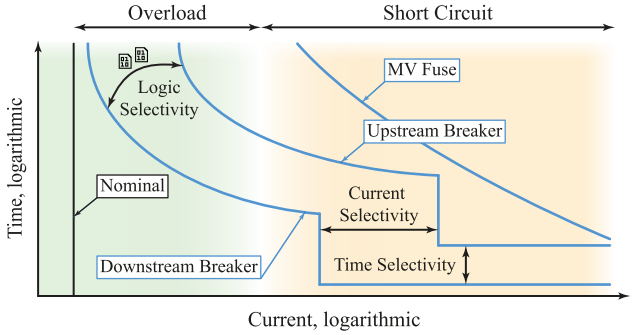


Fig. 3. Qualitative time–current characteristics (selectivity) of the typical protection devices placed near a transformer (MV fuses, LV fuses, and LV breakers) [25], [26].

protection scheme is a tradeoff between the protection of the transformer and the reliability of the grid. Now, these general principles will be applied to the different faults involving a transformer (see Fig. 2).

A. Short Circuits

A short circuit can be caused by an insulation failure, a flashover, an incorrect configuration of the grid topology, etc. Short circuits can be classified as follows: faults produced by an internal failure, faults located upstream, and faults located downstream.

Table I defines different types of short circuits and the corresponding abbreviations, for both the MV and the LV side [17], [27], [28]. These faults can be divided into several categories: symmetric faults (3p), asymmetric faults without earth connection (2p), and asymmetric faults with earth connection (1pg, 2pg). The magnitudes of the overcurrents depend on the impedances of the grid components and on the type of fault. As most short circuits are not self-extinguishing, the protection devices must be able to interrupt the short-circuit currents in the case of a grid fault or to isolate the transformer after an internal fault.

The most important concept for achieving a reliable short circuit protection is the *selectivity* as it minimizes or suppresses the impacts of the faults for the end customers [25], [26]. This is achieved by selecting more sensitive and faster downstream (toward LV, low power) protection devices. Fig. 3 schematically depicts typical time–current characteristics of the overcurrent protection devices.

The *current selectivity* defines lower fault current limits near the end customers. The *time selectivity* adds delays for tripping the protection in the direction of the MV/HV grids. These time delays also help in the identification of a fault and, thus,

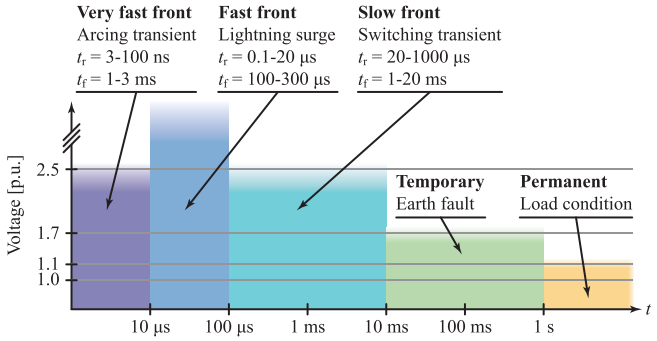


Fig. 4. Time–voltage characteristics of overvoltages in the MV grid (normalized with respect to the nominal phase-to-earth peak voltage). The times t_r and t_f represent the rise time and the total duration of the surges where some overlaps exist between the different overvoltage types. The given levels are only typical values that can vary between grids [19], [30], [31].

to avoid nuisance tripping. Finally the *logic selectivity* is based on communication between the different protection devices and is used to localize the fault [17], [25].

One implication of the selectivity is that the MV/LV transformer should be able to carry an important fault current for a defined time. In the case of an LV short circuit, the MV/LV transformer should be the last device to trip in the whole LV grid. The current threshold is typically increased by 25% per protection stage and the time delay can be more than 1 s for short circuit currents at the transformer [17], [18], [29].

B. Overvoltages

Overvoltages have a critical impact on the *insulation coordination* of the transformer [30]. Fig. 4 depicts typical time–voltage characteristics of different overvoltage conditions in the MV grid [19], [31]. A similar diagram also exists for LV grids [21], [25]. Due to the impedances of the cables and the different components, overvoltage transients also produce temporary overcurrents.

Very fast front surges are mostly created by arcing, extinguish, and restrike processes in switchgears and carry relatively low energies. *Lightning surges* generate the largest overvoltages in the grid. MV overhead lines and renewable energy plants may be subject to direct lightning strikes. Indirect strikes or transmitted surges (from higher voltage level grids) may also occur in grids with underground cables. The enormous current injected by a lightning surge (typically in the range of several 10 kA) produces a massive overvoltage (up to several MVs) during a short time interval [31]–[35].

Switching transients result from the energization/de-energization processes (short circuit interruption, transformer turn-on inrush current, load connection, etc.). The inductances and capacitances present in the distribution grid abet ringing, which typically appears in the kHz range and fades away after some milliseconds [22], [31], [32].

Temporary overvoltages mostly occur during earth faults (see Table I). Depending on the earthing policy of the system), the phase-to-phase voltage can appear in place of the phase voltage during an earth fault [20], [28]. Due to the time selectivity requirement (see Section II-A), these types of short

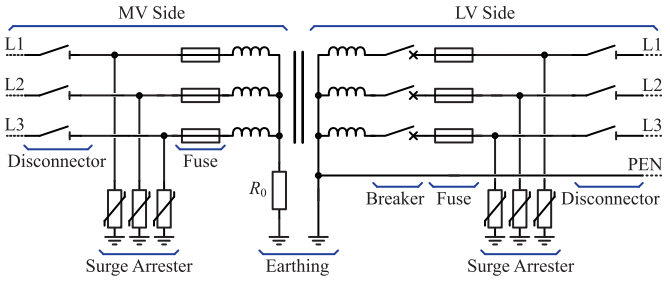


Fig. 5. Star–star distribution LFT with typical protection devices. The MV side of the LFT is earthed with a resistor and the LV side has a solid earth connection (with a TN-C earthing concept) [17], [18], [25].

circuits can be present for hundreds of milliseconds. The permanent allowed overvoltage (voltage control tolerance) for a typical distribution grid is 10%–20% [20], [36].

III. Protection of LFTs

With known policies related to the dimensioning of the protection devices and the discussion of critical overcurrent and overvoltage situations in Section II, the state-of-the-art protection scheme for an MV/LV LFT is analyzed in this section.

A. LFT Capabilities and Protection Scheme

Relevant IEC/IEEE norms require the LFT itself (without external protection devices) to be robust with respect to overvoltages and overcurrents. For a 1 MVA LFT connected to the 10 kV grid (phase-to-phase RMS nominal system voltage [36]), the following limits apply.

1) *Highest Voltage for Equipment:* 12 kV maximum operating voltage, it excludes transient overvoltages [31], [36].
2) *Short Duration Power Frequency Voltage:* 20 kV dielectric withstand value for 1 min [31].
3) *Lightning Impulse Voltage:* 60–75 kV dielectric withstand against lightning surges (ca. 50 μs, MV side) [31], [32].
4) *Short Circuit Impedance:* 5.0% minimum impedance in order to limit the short circuit current flowing in the phase conductors of the LFT [31].
5) *Overload Capabilities:* This is dependent on the LFT type (cooling, insulation, etc.) but the following estimations can be taken for oil insulated LFTs: 25× the rated current for 2 s, 11× for 10 s and 3× for 300 s [37].

A comparison of these ratings with the requirements defined in Section II indicates that additional protection devices are required. A simplified scheme of a typical MV/LV LFT is shown in Fig. 5 [17], [18], [25] and is detailed in Sections III-B–III-D.

B. Short Circuits, Overload, and Isolation

The LFT itself is not able to interrupt a short circuit. Therefore external protection devices are required in order to clear the faults. In the protection scheme presented in Fig. 5, different devices are capable of interrupting the line currents (MV and LV sides) as follows [18], [22], [25].

1) *Disconnector:* Disconnectors are used to disconnect the LFT from the MV and LV grids in order to allow proper earthing for voltage free maintenance. These devices can only switch currents that are considerably lower than the nominal current.
2) *Fuse:* Fuses exist for the MV and LV sides and provide irreversible overcurrent protection. MV fuses are not able to break currents below the minimum breaking current, which is larger than the nominal current. Therefore, typical MV fuses provide only protection against short circuits and not against overloads, while LV fuses can also provide protection against overload (see Fig. 3).
3) *Breaker:* Breakers are able to break a short circuit current. The total breaking time of a breaker is typically 50–100 ms (without additional delays required by the time selectivity). For ac systems, the break event occurs at or close to the zero crossing of the respective phase currents. This device is expensive compared to a load switch or a fuse.
4) *Load Switch:* A load switch is only able to break nominal and overload currents but not short circuit currents. In Fig. 5, load switches could be used in place of breakers for basic substations, which, however, is less flexible, as the fuse is responsible for clearing short circuit currents [17].

For a standard distribution substation, breakers are only present at the LV side and are responsible for LV short circuit and overload protections (see Fig. 5) [25], [29]. As breakers are complex devices, LV fuses are also present in order to improve the reliability of the system (or to interrupt fault currents exceeding the capabilities of the breakers) [25], [29].

The LV breakers cannot clear all short circuits, i.e., in the case of an internal failure of the transformer. Therefore, MV fuses are also required to disconnect the transformer from the MV grid (see Fig. 5). Complex substations may employ additional breakers or load switches at the MV side [17].

C. Overvoltages

For the overvoltage protection, the insulation levels defined in Section III-A (short duration power frequency voltage and lightning impulse voltage) are sufficient for handling switching overvoltages and power frequency overvoltages. The surge arresters depicted in Fig. 5 limit the maximum phase-to-earth voltages during lightning surges. State-of-the-art transformers use metal-oxide surge arresters on the MV and LV sides [18], [20].

A metal-oxide arrester features a highly nonlinear and voltage-dependent resistance, which enables it to clamp the applied voltage to a certain (device-specific) clamping voltage, which is typically between two and three times the continuous operating voltage [20]. The transformer can withstand this increased voltage, as the resulting clamping voltage is still less than the lightning impulse voltage the transformer is designed for. As the thermal rating of a surge arrester only allows short pulses (lightning, switching surges), the device should not

TABLE II
ADVANTAGES AND LIMITATIONS OF THE DIFFERENT EARTHING CONCEPTS USED FOR MV DISTRIBUTION GRIDS [20], [38]

Features	$R_0 \to \infty$	$R_{0,\text{high}}$	$R_{0,\text{low}}$	$R_0 = 0$
Overcurrent	low	low	med.	high
k_I	< 0.01	< 0.05	$0.05 - 0.5$	$0.5 - 1.7$
Overvoltage	high	high	med.	low
k_V	1.7	$1.4 - 1.7$	$1.2 - 1.4$	$1.1 - 1.3$
Device protection	low	high	med.	med.
Service continuity	high	low	low	low
Max. fault duration	long	3.0 s	1.0 s	< 0.5 s

conduct in the event of temporary overvoltages (see Fig. 4). For this reason and depending on the earthing concept, each surge arrester may need to be dimensioned for the phase-to-phase instead of the phase-to-earth voltage [20], [28].

D. Earthing

The earthing of the LFT is an important aspect: according to Fig. 5, the earthing of star-points is different for the LFT's LV and MV sides. This has a decisive impact on the short circuit currents and voltages. The LV side of an LFT has a solid earth connection for safety reasons and in order to provide a protective earth neutral conductor (PEN) [26], [38]. This implies that only the impedances of lines and transformers limit the short circuit currents on the LV side. On the MV side, only three conductors are distributed, which enables the realization of different earthing concepts as follows [23], [25], [38].

1) *Solid Earthing ($R_0 \approx 0$):* Solid earthing is usually not used in the case of a three-phase distribution system. Transient overvoltages are limited, however, short circuit currents are very high during a 1pg fault (see Table I). Therefore, the usage of solid earthing is limited to grids with reduced short circuit power.
2) *Unearthed ($R_0 \to \infty$):* The star-point is only connected to the earth through parasitic capacitances or no star-point is present (delta winding). The advantages of this earthing concept are the limited earth short circuit currents and the possibility to operate the grid with a 1pg fault (see Table I). The main drawbacks are the difficulty to detect earth faults without additional monitoring and that overvoltages appear at the star-point during asymmetric faults.
3) *Resistance Earthing (R_0):* A resistor is placed between the star-point and the earth for limiting the short circuit currents. This variant is a compromise between limiting the short circuit currents and the overvoltages. The resistance also damps oscillations during fault transients. For these reasons, this is the typical earthing method for MV grids.

Table II summarizes the advantages and the limitations of different earthing concepts where the given values can vary between grids (voltage level, short circuit power, etc.) and are here given only as typical examples. The fault current is expressed by the factor k_I, which is defined as the ratio between the single phase-to-earth (1pg) fault current and the three-phase symmetrical 3p fault current (3p), which is often taken as a reference value [17], [24], [28]. The factor k_I, together with the overcurrent capability of the LFT, determines the maximum acceptable duration of a 1pg fault.

During a 1pg fault, the star-point of the SST is shifted with respect to earth (see [10]). As a consequence, one or more phase-to-earth voltages exceed their nominal values. This effect is quantified by the *earth fault factor* k_V, which is the ratio of the phase-to-earth voltages during a 1pg fault with respect to nominal conditions. Even with a solid connection to earth, the earth fault factor is greater than one due to the earth resistance.

Therefore, the choice of the MV earthing concept is a tradeoff between short circuit currents and overvoltages. In any case, the earthing should be matched between the different devices composing the grid [10], [24]. Therefore, earthing is a grid policy which can vary between countries [38].

IV. PROTECTION OF SSTs

The disturbances occurring in grids and the protection scheme of an LFT have been examined in Sections II and III, respectively. With this, a protection scheme is derived for SSTs and the impact of LV and MV faults (short circuits and overvoltages) is analyzed in this section.

A. SST Capabilities

As shown in Fig. 1, the SST is a complex device and, as a consequence, a multitude of different failure modes are possible, e.g., semiconductor failures, thermomechanical failures, control errors, or insulation breakdowns (particularly critical for the MV side converter [7], [16]). Moreover, SSTs have limited current and voltage overload capabilities, where the employed semiconductors are identified to mainly restrict the SST's overload capabilities. However, the high complexity of SSTs can be compensated for with redundancy, as often done for multicell SST topologies (see Fig. 1), in order to increase the mean time between failures [7], [13].

With regard to overcurrent capabilities, thermal time constants in the range of several seconds apply for the packages of power semiconductor switches and milliseconds for the chips, which dramatically limit the allowable durations of overcurrents. For an SST, the typical maximum allowable overcurrent ratios are in the range of $1.5\times$ for some minutes and $4\times$ for some milliseconds [4], [12], [39], [40]. In addition, the input filter inductor saturates at exceedingly high currents, which also limits the maximal allowed current of the SST.

Further particular challenges include robustness against overvoltages, as semiconductors may not withstand voltages that exceed their maximum blocking voltage capability. Due to cosmic ray-induced failures and transient overvoltages during switching, the voltage utilization of power devices is usually between 40% and 70% [4], [41], leaving a margin for handling faults with short durations of up to some hundred milliseconds. Moreover, the passive components (input filter, dc-link capacitor), where increased breakdown voltages apply for pulses with short durations, provide a smoothing effect for

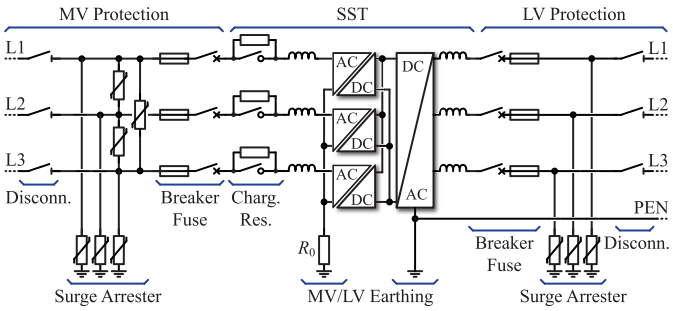


Fig. 6. Proposed protection scheme for an SST based on classical protection devices. Earthing of the MV side is realized with a resistor and the LV side is solidly earthed.

the surges [22], [42]. As a consequence, possible worst case characteristics of transient overvoltages are not only linked to a selection of appropriate protection devices and semiconductor blocking voltages, but also to a suitable design of the input filter and the dc-link capacitor.

The main feature of an SST is its ability to control phase currents and voltages. The SST is also capable to operate under nonideal operating conditions, e.g., in the presence of a voltage dip, asymmetrical loads, nonlinear loads, and so on [3], [43]. The dc-links of the SST offer decoupling between the MV and LV grids. This means that disturbances are not transmitted from one grid to another grid [5], [39], [44]. Moreover, the SST features highly dynamic current control properties (LV and MV sides), allowing the interruption of phase currents in some milliseconds [3], [44], [45]. This implies that an SST can be shut down very quickly and without opening a mechanical breaker. Finally, SSTs feature advanced monitoring capabilities. The current and voltage measurements that are required for the control of the SST can be used for identifying faults and overload situations [3], [44].

B. Proposed Protection Scheme

As SSTs are considerably more sensitive to overcurrents and overvoltages than LFTs, external protection devices are required. In Fig. 6, an adapted version of the discussed LFT protection scheme (see Fig. 5) is proposed for SSTs. The functional principle of the proposed protection scheme is explained based on the following listed events.

1) *Overvoltage:* Metal-oxide surge arresters are placed at the MV and LV sides in order to clamp large overvoltages. As the overvoltage capabilities of SSTs are limited, surge arresters are also placed between the phases in order to achieve better clamping [20].
2) *Overcurrent:* Fuse/breaker combinations are used on the MV and LV sides for interrupting the phase currents. MV breakers are required, due to the SST's limited overcurrent capability and for disconnecting the SST after an MV short circuit or an internal failure [12], [17], [40]. Fuses are also present as a last resort grid protection. Due to the current control capabilities of SSTs, short circuit current breaking is only required in the case of an internal failure of the SST. The probability of an internal failure is low and, in this case, a fast overcurrent protection is no more required. This implies that the breakers could be replaced by a less expensive fuse/load switch combinations.
3) *Isolation:* Disconnectors are present on both the sides in order to allow for voltage free maintenance [17], [25].
4) *Startup:* The MV side inverters of an SST most commonly act as diode rectifiers during the startup procedure (see Fig. 1), making precharging resistors and bypass load switches necessary in order to limit the inrush currents [7], [46]. Similar devices are required at the LV side for starting the SST from the LV grid.

As explained in Section III-D for LFTs, the LV side requires a solid earthing and different choices are possible for the MV side. The multicell SST with separated phase stacks (see Fig. 1) features a star-point, allowing the earthing via a resistor R_0 [20], [38]. This protection scheme is analyzed in more detail in Sections IV-C–IV-F. Thereafter, in Section IV-G, an advanced protection scheme based on solid-state devices is presented.

C. LV Faults

On the LV side, the expected overvoltages strongly depend on the loads (switching overvoltages) and on whether overhead lines are present (lightning surges). A large variety of LV surge protection devices with low clamping voltages are readily available, e.g., surge arresters and breakover diodes [17], [21], [25]. Furthermore, protection concepts already detailed for solar inverters and grid connected rectifiers can be used [25], [47], [48]. For these reasons, the LV overvoltage protection is not further discussed in this paper.

The control capabilities of SSTs allow the compensation of nonideal loads in a wide range and an effective overload protection [3], [18], [43], [44]. In the case of LV short circuits, the presence of a neutral conductor allows a fast identification of the fault (see Table II). The SST is able to interrupt the current immediately, which, however, violates the selectivity policy discussed in Section II-A, because the downstream breakers or fuses do not trip. In this case, all the LV loads would experience a blackout. In order to avoid this situation, the SST needs to inject short circuit current in the LV grid until the following occur [3], [44].

1) A downstream breaker or a fuse interrupts the fault. Afterward, the SST restores the voltage for the remaining loads.
2) The downstream breakers or fuses cannot interrupt the fault (for example, if the fault is located at the output of the SST). After some seconds, the SST reduces the current to zero and conducts a shutdown.
3) If neither the downstream breakers nor the SST are able to interrupt the fault (failure of the LV side of the SST), then the LV breakers (see Fig. 6) will open in order to interrupt the fault current supplied by the LV grid.

For these three cases, the short circuits are not transmitted to the MV grid as the SST decouples the MV and LV grids. Another important question is the required current that the SST should inject in order to trip the downstream protection devices, which is dependent on the power ratings of the LV downstream fuses. Tripping a 1 MVA LV side fuse of

a 1 MVA SST, for example, requires 12 s at 5× the rated current while a 500 kVA fuse will still need 20 s at 2× the rated current [49]. As stated in Section IV-A, a typical SST can deliver only up to 1.5× of the rated current which, thus, is insufficient for breaking the fuse of the SST or a large load [18], [25]. Fulfilling this requirement would therefore require a substantial overrating of the LV inverter.

A possible alternative solution considers more sensitive LV breakers [12], [18]. As the SST is able to limit the fault current, load switches can be used instead of breakers in the LV grid. In the case of a smart grid environment, the improved logic selectivity allows a rapid identification of the fault and the SST does not have to inject a large short circuit current [3], [9], [43]. In any case, the LV grid selectivity and the SST overcurrent capability need to be matched.

D. MV Side Characteristic Properties

In order to extract figures of merit for SSTs with different voltage and power levels, all the characteristic electrical parameters are scaled by means of a per-unit system. The following scaling is defined:

$$\hat{v}_\mathrm{p} = \frac{\sqrt{2}}{\sqrt{3}}V, \quad \hat{i}_\mathrm{p} = \frac{\sqrt{2}}{\sqrt{3}}\frac{S}{V}, \quad Z_\mathrm{b} = \frac{V^2}{S} \tag{1}$$

where $\hat{v}_\mathrm{p}$ is the peak phase-to-earth voltage, $\hat{i}_\mathrm{p}$ the peak phase current, and Z_b the phase impedance. These values are used to scale voltages, currents, and impedances, respectively. In (1), V is the rated phase-to-phase RMS voltage and S the rated three-phase power.

The *short circuit ratio* (*SCR*) is the ratio between the nominal phase current and the symmetric three-phase short circuit current (3p fault, see Table I) and can be expressed as (for LFT and SST) [17], [31]

$$SCR = \frac{Z_{SCR}}{Z_\mathrm{b}}, \quad \underline{Z}_{SCR} = Z_{SCR}\mathrm{e}^{j\arctan(XR)} = \underline{SCR}Z_\mathrm{b} \tag{2}$$

where $\underline{Z}_{SCR}$ is the short circuit impedance and *XR* the ratio between the reactance and the resistance. For an SST, the *SCR* characterizes the input filter impedance (see Fig. 1) where a purely inductive filter (without saturation and without capacitors) is employed [4], [12].

The MV earthing resistor (for LFT and SST) is scaled with respect to the base impedance of the system and forms the *earthing impedance ratio* (*EIR*)

$$EIR = \frac{R_0}{Z_\mathrm{b}}. \tag{3}$$

For the modeling of the ac–dc inverters, the energy stored in the dc-links and the maximum applied voltage at the ac port are considered for basic fault considerations. The modeling of the multilevel ac voltage is not required. This implies that the multicell structure (see Fig. 1) can be reduced to an equivalent virtual single-cell structure with a dc-link consisting of the series connection of all MV dc-links of the corresponding phase [13]. With this transformation, the aforementioned properties remain unchanged. The dc-link voltage and capacitance of this virtual single-cell structure are scaled and form the *capacitor voltage ratio* (*CVR*) and the *capacitor energy ratio* (*CER*), respectively

$$CVR = \frac{V_{\mathrm{DC},0}}{\hat{v}_\mathrm{p}}, \quad CER = \frac{\frac{C_\mathrm{DC}\,V_{\mathrm{DC},0}^2}{2}}{\frac{S/3}{2f}} = C_\mathrm{DC}CVR^2\,Z_\mathrm{b}2f \tag{4}$$

where $V_{\mathrm{DC},0}$ is the nominal dc-link voltage and f the grid frequency. The *CER* is the ratio between the energy stored in the dc-link capacitor and the energy consumed by one phase during a grid half-period.

The analysis assumes the MV side of the SST to be fed by a standard HV/MV LFT with the same power rating (50 Hz grid). The SST depicted in Fig. 1 is chosen [4] and Table III summarizes the parameters used for the corresponding MV models. The short circuit power of the feeder will increase for an MV feeder with a larger power rating. However, the required short circuit impedance is larger for high power LFTs such that the increase in the short circuit power is limited [31].

TABLE III
PARAMETERS USED FOR THE MV MODELS [4], [13]

Parameters	Values
LFT, $V = 10\,\mathrm{kV}$, $S = 1\,\mathrm{MVA}$	$\hat{v}_\mathrm{p} = 8.2\,\mathrm{kV}$, $\hat{i}_\mathrm{p} = 82\,\mathrm{A}$, $Z_\mathrm{b} = 100\,\Omega$
$SCR_\mathrm{LFT} = 5\,\%$, $XR_\mathrm{LFT} = 10$	$L_{SCR,\mathrm{LFT}} = 16\,\mathrm{mH}$, $R_{SCR,\mathrm{LFT}} = 500\,\mathrm{m}\Omega$
EIR_LFT	open design parameter
SST, $V = 10\,\mathrm{kV}$, $S = 1\,\mathrm{MVA}$	$\hat{v}_\mathrm{p} = 8.2\,\mathrm{kV}$, $\hat{i}_\mathrm{p} = 82\,\mathrm{A}$, $Z_\mathrm{b} = 100\,\Omega$
$SCR_\mathrm{SST} = 8\,\%$, $XR_\mathrm{SST} = 100$	$L_{SCR,\mathrm{SST}} = 25\,\mathrm{mH}$, $R_{SCR,\mathrm{SST}} = 80\,\mathrm{m}\Omega$
$CVR_\mathrm{SST} = 1.3$, $CER_\mathrm{SST} = 1.0$	$V_{\mathrm{DC},0} = 10.6\,\mathrm{kV}$, $C_{\mathrm{DC,SST}} = 60\,\mu\mathrm{F}$
EIR_SST	open design parameter

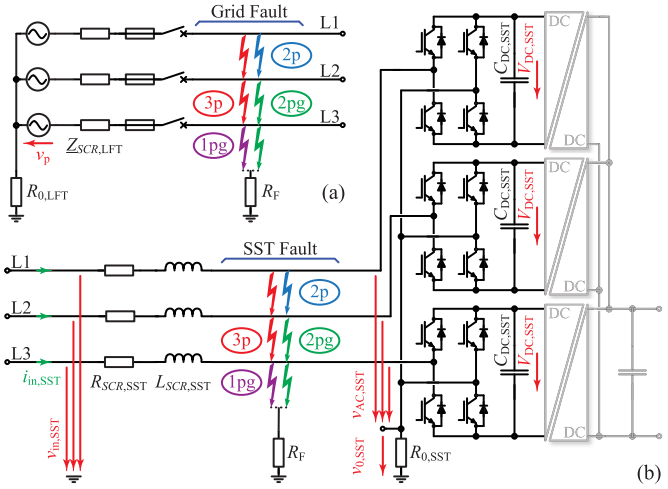


Fig. 7. (a) Equivalent circuit of the LFT feeder where the possible grid short circuits are highlighted. (b) MV equivalent circuit of the SST with the considered internal short circuit faults. The multicell structure is replaced by a virtual single cell per phase.

E. MV Short Circuits

1) Modeling: The presented short circuit analysis is based on the model presented in Fig. 7. The length of the connection between the LFT feeder and the SST is assumed to be zero (back-to-back connection), as this configuration leads to

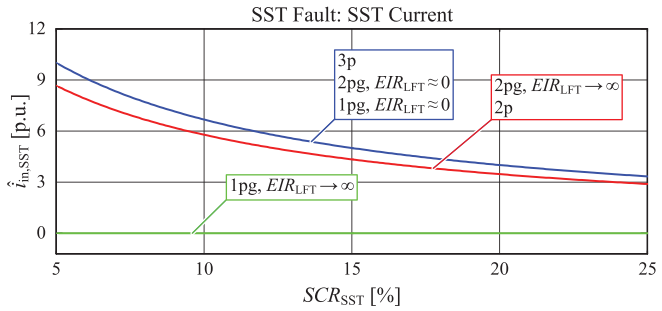


Fig. 8. Converter fault currents ($\hat{i}_{\text{in,SST}}$) during internal SST faults. Different SST *SCR* values are considered with a solidly earthed and an unearthed MV feeder. Currents (maximum over the three phases) are normalized to the phase peak current $\hat{i}_{\text{p}}$ [see (1)].

the largest fault current [24]. The resistance R_{F} (earth fault resistance) is 0.1% of the base impedance Z_{b} (low ohmic fault). This paper considers two possible cases for an SST that is subject to an MV short circuit.

1) *SST Internal Fault:* Due to an internal failure, the SST causes a short circuit after the filter inductor. In case the switches are still operational, the MV ac–dc stages shut down, i.e., opens all switches, but a current is still present at the input ($i_{\text{in,SST}} \neq 0$ in Fig. 7).
2) *Grid Short Circuit:* A short circuit occurs between the MV feeder and the SST. The SST shuts down the MV ac–dc stages. After a short initial transient, the input current of the SST is zero ($i_{\text{in,SST}} = 0$ in Fig. 7).

2) SST Internal Fault: Internal failures can be located after the filter, inside the ac–dc inverters, at the dc buses, etc. DC bus faults have already been examined in [12]. The highest steady-state short circuit currents inside the SST occur during a fault placed after the filter (see Fig. 7(b)), and therefore this case is further considered.

During an internal failure of the SST, the SST is not anymore able to interrupt the MV current and the MV breakers will clear the fault. However, due to the reaction time of the MV breakers and due to selectivity, short circuit currents still flow into the SST. In order to limit the short circuit currents, an *SCR* of at least 5.0% is required by the IEC norms [31].

Fig. 8 depicts the steady-state amplitudes of the fault currents ($\hat{i}_{\text{in,SST}}$ in Fig. 7) flowing into the SST owing to different internal failures. Different SST short circuit impedances and two differently earthed MV feeders are considered (EIR_{LFT}). The earthing of the SST (EIR_{SST}) has no impact on the computed currents as the fault occurs before the ac–dc inverters, which are turned off. For this reason, no current flows through the star-point of the SST. A fault occurring inside the ac–dc inverters (between the ac terminals) leads to smaller fault currents, due to the current limiting effect of EIR_{SST}. This implies that the faults chosen in Fig. 8 are the worst cases.

The 3p fault produces the largest current, independent of the type of earthing. By contrast, the 1pg fault current is zero in the case of an unearthed MV feeder (no current path exists). Globally, it can be seen that the value of the fault current can be adjusted by a proper choice of the *SCR* of the SST (defined by the MV side filter inductor). The maximum fault current (3p fault), can be easily computed as

$$\hat{i}_{\text{in,SST}} = \hat{i}_{\text{p}} \left| \frac{1}{\underline{SCR}_{\text{LFT}} + \underline{SCR}_{\text{SST}}} \right|. \tag{5}$$

A low-frequency current component appears during the initial fault transient (superimposed on the steady-state sinusoidal current). This can lead to a peak current of up to twice the steady-state value [17], [28], [31]. This low-frequency component is damped by the earthing resistor and the *XR* ratio and converges (typically in less than 50 ms) toward the values shown in Fig. 8 [17], [27].

From the presented results, it can be seen that an *SCR* of less than 10% will lead to very large fault currents, greater than 7 p.u., in the filter. A lower *SCR* value would lead to important fault currents in the grid and to hazardous currents inside the SST [7]. Moreover, the filter impedance limits the initial current during failures of the ac–dc inverters, which prevents the instantaneous transfer of the energy stored in the dc-links into the grid. It can be further concluded that the filter inductor needs to be capable of carrying the short circuit current until a breaker clears the fault, which can take more than a hundred milliseconds. Furthermore, a decrease in the filter inductance at high currents due to saturation also needs to be considered in the course of the design of the SST. However, this current is only flowing in the case of an internal failure of the SST and, thus, does not have an implication on the current ratings of the ac–dc inverters.

3) Grid Short Circuit: During an MV grid short circuit, the SST tries to actively control the fault current [5], [9], [11]. However, this requires a fast identification of the fault in order to react appropriately. Furthermore, the SST control strategy aims to avoid a mismatch between the MV and LV power flows, which causes a rapid change in the dc-link voltages. If the SST is not able to control the current, the ac–dc inverters (and the dc–dc converters) initiate a shutdown. This last case is considered in this paper, as it has been identified to represent the worst case.

During a grid earth fault, the amplitudes of one or more phase-to-earth voltages at the input of the SST increase and may, in the worst case, reach the amplitude of the phase-to-phase voltage (see Section III-D) [20], [24]. Depending on the EIR_{LFT} and EIR_{SST}, this may lead to an increase in the ac voltages applied to the SST's input inverters, i.e., $v_{\text{AC,SST}}$ in Fig. 7. If the instantaneous input voltages are greater than the dc-link voltages, an effective shutdown of the SST is not possible as the shutdown ac–dc inverters act as diode rectifiers. Fig. 9 depicts the charging process of the MV dc-links during a 1pg fault with a resistance earthing. The dc-link voltage of the faulted phase is not affected, while the voltage rises for the remaining phases. In the presented simulation, the MV breakers interrupt the increase of the dc-link voltages after 80 ms [27], [29].

The applied steady-state overvoltage ($\hat{v}_{\text{in,SST}}$ in Fig. 7) is shown in Fig. 10(a) for different earthing of the MV feeder and fault types. The identified worst-case scenario is the single phase-to-earth fault (1pg) and the derivation of the

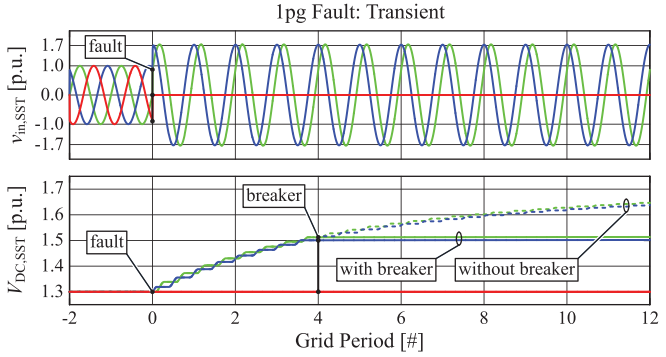


Fig. 9. Input phase-to-earth voltages $v_{\mathrm{in,SST}}$ and dc-link voltages $V_{\mathrm{DC,SST}}$ during a 1pg short circuit interrupted after 80 ms by the MV breakers. Voltages are normalized to $\hat{v}_{\mathrm{p}}$ [see (1)]. The following earthing applies: $EIR_{\mathrm{LFT}} = EIR_{\mathrm{SST}} = 5.0$. The dotted line represents the overvoltage that would appear without breakers.

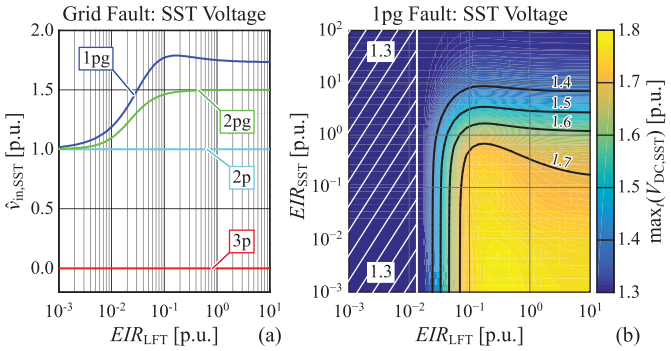


Fig. 10. (a) Maximum phase-to-earth voltages ($\hat{v}_{\mathrm{in,SST}}$) applied to the SST during grid short circuits in dependence of the *EIR* of the MV feeder. (b) Maximal MV dc-link voltages if the fault is interrupted after 80 ms with a breaker. The hatched domain represents the zone where $\hat{v}_{\mathrm{in,SST}}$ increases to less than $V_{\mathrm{DC,0,SST}}$. Voltages (maximum over the three phases) are normalized with respect to $\hat{v}_{\mathrm{p}}$ [see (1)].

corresponding expression gives

$$\hat{v}_{\mathrm{in,SST}} = \hat{v}_{\mathrm{p}} \left| \mathrm{e}^{\frac{j2\pi}{3}} - \frac{EIR_{\mathrm{LFT}}}{SCR_{\mathrm{LFT}} + EIR_{\mathrm{LFT}} + (R_{\mathrm{F}}/Z_{\mathrm{b}})} \right| . \quad (6)$$

The voltage stress reaches the phase-to-phase voltage (1.7 p.u.) with an unearthed LFT, which corresponds to the earth fault ratio defined in Section III-D [24], [28]. However, these analytical computations are only valid in steady state.

If the short circuit duration is small, this upper bound (see Fig. 9) will never be reached. Fig. 10(b) shows the dc-link overvoltage for different grid earthing, given that the fault is cleared after 80 ms by the MV breakers. During the charging process, the phase currents remain less than the nominal current such that no overcurrents occur. It has to be noted that these overvoltages are only critical for SSTs with independent phase legs where the dc-link voltage is related to the phase-to-earth voltage [2], [50]. The depicted overvoltages are relevant with respect to the selection of the semiconductor blocking voltages and can be minimized based on the following design choices.

1) Using an MV feeder with a solid or low-ohmic earth connection (see Fig. 10(b)).
2) Selection of a large EIR_{SST} (unearthed SST). In this case, no current path for charging the dc-link exists. However, adequate insulation coordination is required, as the SST experiences the phase-to-phase voltage [16].
3) Slowing down the rise in the voltage by increasing SCR_{SST} and/or CER_{SST} values, which, however, impairs the volume, efficiency, and cost of the SST.
4) Interrupting the fault with MV breakers to quickly stop the charging of the dc-link capacitors.

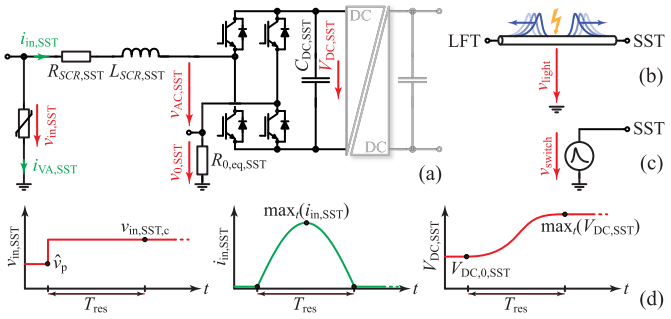


Fig. 11. (a) Single-phase MV equivalent circuit for the simulation of surge propagation. (b) Lightning and (c) switching surge models. (d) Input current $i_{\mathrm{in,SST}}$ and dc-link voltage $V_{\mathrm{DC,SST}}$ during a step response of the input voltage $v_{\mathrm{in,SST}}$.

F. MV Overvoltages

1) Modeling: The investigation of MV overvoltage is limited to switching and lightning surges. The remaining overvoltages are either absorbed by the input filter of the SST (e.g., in the case of very fast front or low-energy overvoltage pulses [51]) or, in the case of enduring overvoltage conditions, like short circuit failures, require the SST to be rated for these (see Section IV-E).

Fig. 11(a) shows the used model for surge simulations in SSTs. A single-phase and, according to Section IV-D, virtual single-cell can be used for basic assessment of the overvoltages and overcurrents inside the SST, where $R_{0,\mathrm{eq,SST}} = R_{0,\mathrm{SST}}$ for a common-mode (CM) surge and $R_{0,\mathrm{eq,SST}} = 0$ for a differential-mode (DM) surge. Lightning surges are typically CM surges while switching transients are commonly DM [31], [52]. More complex models (including the stray capacitive couplings which depend on the geometries of the components) would provide more accurate results but are not scalable and, thus, less suitable for initial identification of meaningful design criteria [39], [53].

A simple figure of merit for evaluating the robustness of an SST during an overvoltage situation is the response to a voltage step, as shown in Fig. 11(d), where the arrester limits $v_{\mathrm{in,SST}}$ to $v_{\mathrm{in,SST,c}}$. In order to get a simple model, $R_{0,\mathrm{SST}} = 0$ is assumed, the impact of the *XR* ratio [see (2)] is neglected, and the initial input current is assumed to be zero. The input voltage step causes the input current and the dc-link voltage to oscillate. The characteristic properties of the relevant first half-cycle of this oscillation can be derived as

$$\frac{\max_t(V_{\mathrm{DC,SST}})}{\hat{v}_{\mathrm{p}}} = 2\frac{v_{\mathrm{in,SST,c}}}{\hat{v}_{\mathrm{p}}} - CVR \quad (7a)$$

$$\frac{T_{\mathrm{res}}}{1/(2f)} = \frac{\sqrt{\pi}}{CVR}\sqrt{CER\,SCR} \quad (7b)$$

$$\frac{\max_t(i_{\mathrm{in,SST}})}{\hat{i}_{\mathrm{p}}} = \frac{\sqrt{\pi}}{CVR}\sqrt{\frac{CER}{SCR}}\left(\frac{v_{\mathrm{in,SST,c}}}{\hat{v}_{\mathrm{p}}} - CVR\right) \quad (7c)$$

where T_{res} is the duration of the current half-cycle resonance (assuming a non-saturating filter inductor), which is also the time where the maximum dc-link overvoltage is reached. Due to resonance, the maximum dc-link voltage is larger than the clamping voltage of the MV side surge arrester. The duration T_{res} is useful in order to assess the immunity of the SST against short duration overvoltages.

For the chosen SST (see Table III) and a typical clamping voltage of $v_{in,SST,c} = 2.6\,\hat{v}_p$ (see Section IV-F3), the following results are obtained: $T_{res} = 3.8$ ms, maximum voltage of 4.0 p.u., and maximum current of 6.5 p.u. According to Fig. 4, however, the durations of lightning and of some switching surges are less than T_{res}. Therefore, the maxima calculated in (7) are actually not reached and further investigations are required, which are given in the following.

2) Lightning Surge, Propagation: The lightning overvoltage test of LFTs is normalized in the IEC norm as a CM/DM voltage surge with a rise time of 1.2 µs and a 50% fall time of 50 µs (the test is made without surge arresters). This test, however, is not suitable for an SST, which is an active device with energy storage. For this reason, the following procedure is proposed. The input filter (standalone, without the ac–dc inverters) and the insulation of the dc–dc converters can be tested with a standard IEC surge test (75 kV for an SST connected to the 10 kV grid) in order to assess dielectric strengths [31], [32]. This first test, which is done in standby condition (zero initial currents and voltages), corresponds to the test condition of LFTs, and, therefore, this procedure is not further discussed.

Afterward, the complete SST is tested with a CM voltage surge, which reproduces overvoltages and overcurrents appearing inside the SST. This second test, which is done with the protection devices, aims to assess the propagation of the surge inside the SST and not only dielectric strengths. The amplitudes and durations of the voltage surges are statistically distributed and depend on whether a direct, an indirect, or a transmitted strike applies [19], [33], [34]. For the following analysis, a direct strike is assumed. The resulting overvoltage has been approximated as an IEC 1.2/50 µs surge with an amplitude of 25 p.u., which is similar to the typical voltage surge described in [54].

The SST is connected to the HV/MV LFT feeder by a 2 km long MV cable ($Z_0 = 30\ \Omega$, $v_p = 200$ m/µs) and the lightning strikes in the middle of the line, as shown in Fig. 11(b) (single-phase model) [55]. The continuous operating voltage of the arrester is $1.2\,\hat{v}_p$, the SST is solidly earthed ($R_{0,SST} = 0$), and the ac–dc inverters and the dc–dc converters are shut down (passive diode rectifier). The surge is triggered at the peak of the grid voltage and current (worst case). Different types of earthing and SST operating conditions are examined in Sections IV-F3 and IV-F4.

The surge voltage and the resulting input current and dc-link voltage of the SST are depicted in Fig. 12. The input voltage, $v_{in,SST}$, is clamped by the surge arrester but as the clamping voltage is higher than the dc-link voltage, $V_{DC,0,SST}$, a charging process starts and leads to an overcurrent in the ac–dc inverter and an overvoltage in the dc-link [see (7)]. The duration of the overcurrent, $i_{in,SST}$, is larger than the duration

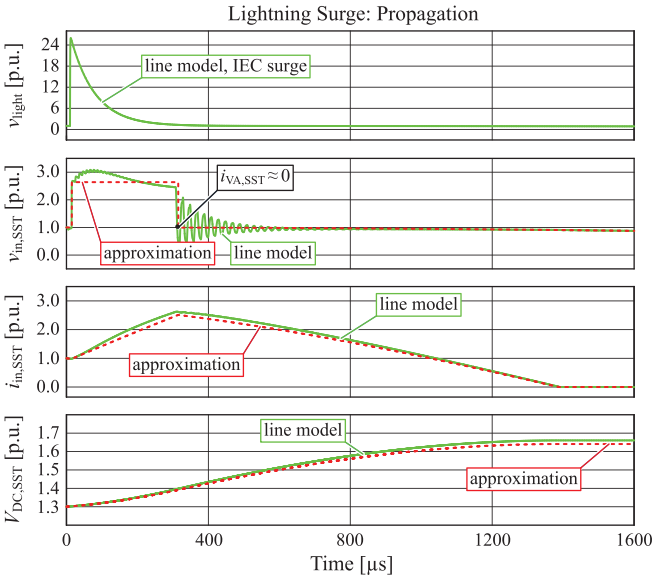


Fig. 12. Single-phase lightning surge propagation in the MV grid and inside the SST. An approximation of the surge by a rectangular voltage for $v_{in,SST}$ is also shown. Currents and voltages are normalized to $\hat{i}_p$ and $\hat{v}_p$ [see (1)].

of the lightning surge, v_{light}, due to electric and magnetic energy stored in the SST and in the cable.

Fig. 12 compares the simulation results obtained with the line model with the results obtained with a simplified model based on a rectangular approximation of the surge for $v_{in,SST}$, which is found to provide a very good approximation of the surge propagation inside the SST. The identified duration of 300 µs is also similar to the results presented in [35]. For this reason, in the rest of this paper, the lightning surge is approximated as a 300 µs rectangular surge with a voltage equal to the arrester clamping voltage, $v_{in,SST,c}$, which is accepted to be 2.2 times the peak continuous operating voltage of the arrester (at 5 kA surge current, $i_{VA,SST}$) [20].

3) Lightning Surge, Earthing: Lightning surges are mostly CM overvoltages, implying that the earthing of the MV feeder and of the SST are important parameters. Moreover, the continuous operating voltage of the arrester should be greater than the overvoltage that appears during a 1pg grid fault (see Fig. 10(a)). This constraint arises from the limited energy dissipation capability of the arrester, which is not compatible with the duration of short circuit faults. Therefore, the continuous operating voltages of the arresters are scaled with respect to the earthing of the MV feeder.

1) *Solid Earthing:* The continuous operating voltage of the arrester is $1.2\,\hat{v}_p$ ($v_{in,SST,c} = 2.6$ p.u.), which is based on the phase-to-earth voltage and would allow the operation in a solidly earthed grid or a grid where earth faults are immediately interrupted. The factor 1.2 takes permanent and temporary overvoltage conditions into account [20], [34].
2) *Unearthed:* The continuous operating voltage of the arrester is $(\sqrt{3}/1.2)\,\hat{v}_p$ ($v_{in,SST,c} = 3.2$ p.u.), which is based on the phase-to-phase voltage and would allow for operation in an unearthed grid. The thermal derating

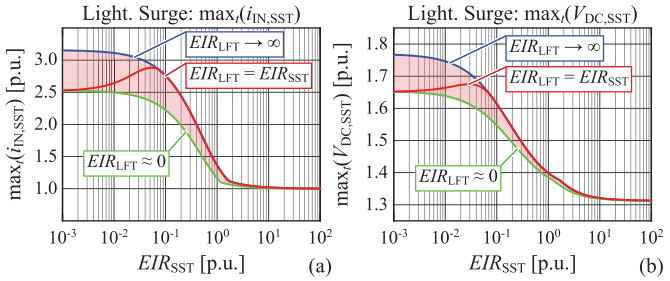


Fig. 13. (a) Maximum input current and (b) maximum dc-link voltage caused by a lightning surge. Different earthing policies are considered. Currents and voltages are normalized to $\hat{i}_p$ and $\hat{v}_p$ [see (1)].

factor 1.2 allows the operation with a 1pg fault during approximately 10 s [20], [34].

3) *Resistance Earthing:* For a resistance earthing the continuous operating voltage is scaled between the values chosen for the solidly earthed and the unearthed grid. Between these two extrema, the scaling is done with the curve for the 1pg fault depicted in Fig. 10(a).

Fig. 13 shows overcurrents and overvoltages in the SST in the event of a lightning surge and for different realizations of the MV feeders and the SST's earthings. The lightning surge is modeled according to Section IV-F2. If the SST is unearthed, the overvoltage is applied between the star-point of the SST and the earth (CM surge). In this case the complete SST reference potential is shifted, which has an impact on the insulation coordination but not on the ac–dc inverters [16]. However, the rapid shift on the star-point potential can produce capacitive disturbances inside the SST [39], [53]. As it is found that the stress is larger for a solidly earthed SST, where no shift of the star-point is possible, only this case will be further considered, together with a solidly earthed MV feeder.

4) Lightning Surge, Converter State: Until now, the ac–dc inverter has been considered as a passive diode rectifier. However, an SST features an active inverter that can provide a voltage, $v_{AC,SST}$, between $\pm V_{DC,SST}$ at its ac port. If the applied voltage $v_{AC,SST}$ has the same sign as the surge voltage $v_{in,SST}$, the voltage across the input inductor will be moderate [39], [40]. In the case of opposite signs, a large voltage is applied to the input inductor, leading to a rapid increase in the input current. A passive diode rectifier will always produce the best possible voltage, $v_{AC,SST}$, in order to minimize the impact of the surge.

Fig. 14 illustrates the impact of the inverter state on the surge propagation inside the SST. The worst possible case ($v_{AC,SST} = -V_{DC,SST}$, given that $v_{in,SST} > 0$) is presented and compared to the case of a passive rectifier (with two different initial currents). The active inverter is programmed to shut down when the input current $i_{in,SST}$ reaches twice the nominal peak current $\hat{i}_p$. Thereafter, the inverter is also operated as a diode rectifier. The lightning surge and the SST are modeled according to Section IV-F3 (solid earthing).

The shapes of the current and voltage waveforms do not change fundamentally between active and passive rectifiers. For an SST in standby, the overvoltage and overcurrent are less critical as the initial current is zero. With the nominal

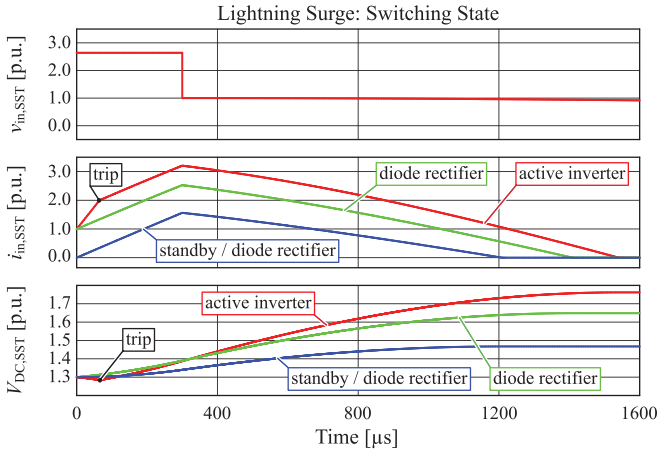


Fig. 14. Impact of the initial converter state on the propagation of a lightning surge inside the SST. The worst case scenario (active inverter) is presented together with the case of a passive diode rectifier (with two different initial currents). Currents and voltages are normalized to $\hat{i}_p$ and $\hat{v}_p$ [see (1)].

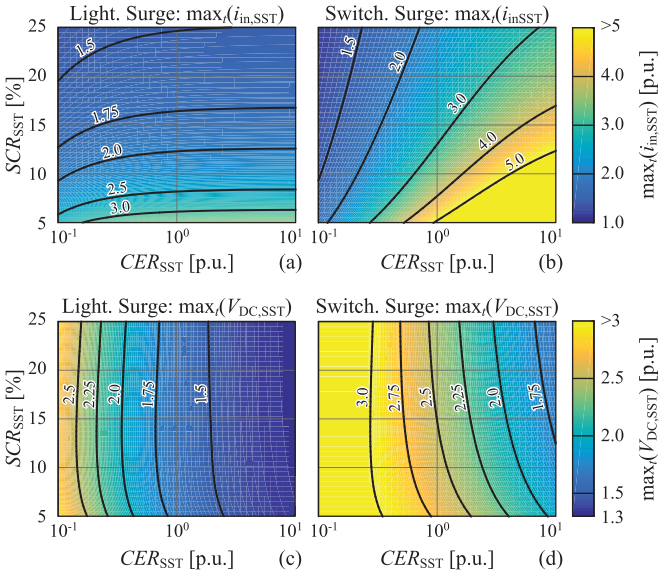


Fig. 15. Maximum input current during (a) lightning and (b) switching surges. Maximum dc-link voltage during (c) lightning and (d) switching surges. Different values of SCR_{SST} and CER_{SST} are considered. Currents and voltages are normalized to $\hat{i}_p$ and $\hat{v}_p$ [see (1)].

current as initial condition, the stress is higher for the case of an active inverter compared to a passive rectifier. The maximal input current increases from 2.5 to 3.2 p.u. and the dc-link voltage from 1.65 to 1.75 p.u. However, the detection of the surge can be drastically improved if the derivative of the input current, $i_{in,SST}$, is considered. In this case, the overcurrents and overvoltages are similar to those obtained with a passive rectifier. For this reason, the state of the inverter will not be further considered in Sections IV-F5 and IV-F6.

5) Lightning Surge, SST Properties: Fig. 15(a) and (c) shows the maximal input current and dc-link voltage owing to a lightning surge for different values of SCR_{SST} and CER_{SST}. The lightning surge and the SST are modeled according to Section IV-F3 (solid earthing).

The maximum input current mainly depends on the SCR_{SST}, which is explained by the fact that the dc-link voltage remains approximately constant during the fast current rise (as long as the surge duration is much smaller than the duration of the half-cycle resonance, see (7)). Furthermore, the dc-link overvoltage mainly depends on the value of CER_{SST}. It can be seen that the overcurrents produced by a lightning surge are acceptable (see Section IV-A), while $CER_{SST} > 1.0$ p.u. is sufficient to maintain the dc-link voltage below 1.7 p.u., which is also compatible with the voltage utilization of semiconductors defined in Section IV-A.

6) Switching Surge, SST Properties: The switching surge test of LFTs is normalized in the IEC norm as a DM voltage surge with a rise time of 250 μs and a 50% fall time of 2500 μs [31], [32]. However, this test is only specified for grid voltages above 115 kV. In this paper, an adapted model for the MV grid is assumed: a DM 250/2500 μs surge is triggered at the peaks of the grid voltage and current. The maximum phase-to-phase voltage reaches $(2.5\sqrt{3})\,\hat{v}_p$ [56], [57]. The factor 2.5 defines the maximum voltage that can be applied without being effectively clamped by the surge arresters placed between the phases (see Section IV-F3).

As the earthing does not play a fundamental role during a DM surge, a single-phase model is used (with $R_{0,eq,SST} = 0$, see Fig. 11(a)). The source of the surge is located at the input of the SST as shown in Fig. 11(c) and v_{switch} equal to half the phase-to-phase voltage (maximum voltage of $(2.5\sqrt{3}/2)\,\hat{v}_p$). The inverter is modeled as a passive diode rectifier.

Fig. 15(b) and (d) illustrates the input current and dc-link voltage owing to a switching surge for different values of SCR_{SST} and CER_{SST}. The results show that switching surges are much more critical than lightning surges due to their longer durations. This holds particularly true for the input current, where large RMS currents during the surge can damage the ac–dc inverter [12], [39], [40]. This current is flowing in the antiparallel diode of the switches after the shutdown of the ac–dc inverters, implying that the current rating of the diodes has to be considered. The filter inductance, represented with SCR_{SST}, needs to be large enough to avoid high inrush currents, in particular in the case of large dc-link capacitance [see (7)]. The saturation current of the filter should be selected appropriately or a possible decrease in the filter impedance due to the partial saturation should be taken into account. Furthermore, for small CER_{SST}, the dc-link overvoltage is higher than the surge peak voltage due to resonance [see (7)].

For the chosen SST (see Table III), the overcurrent is 4.0 p.u. while the dc-link voltage reaches 2.6 p.u., which would require a large overrating of the SST. Even a more robust SST ($SCR_{SST} = 10\%$, $CVR_{SST} = 1.5$, $CER_{SST} = 2.0$), will still experience an overcurrent of 3.0 p.u. and an overvoltage of 2.3 p.u.. This implies that the switching surge is the most critical event for an SST connected to the MV grid with classical protection devices.

G. Advanced Protection Schemes

Different approaches are possible to circumvent the need for high values of CER_{SST}, CVR_{SST}, and SCR_{SST}. A first solution is the suppression or mitigation of the transients in the MV grids. For example, switching transients can be almost suppressed if the breaker's actions are synchronized with the phase of the grid voltages [58]. However, transients due to lightning or unpredictable faults cannot be avoided. A second solution is the use of advanced protection devices, which offer better protection at the MV side as follows.

1) An ultrafast *solid-state breaker* can be employed to immediately disconnect the SST from the MV grid during a short circuit or an overvoltage condition [12], [45], [59]. The main drawbacks of this solution are increased conduction losses, cost, and high complexity of the protection scheme.
2) A *solid-state current limiter* can be installed in the MV grid in order to increase the short circuit impedance during a fault [59], [60].
3) For the mitigation of overvoltages, *surge capacitors* placed at the input of the SST are a common solution to smooth the surges [42], [61]. However, the reactive power consumption of the capacitors has to be compensated for by the SST and, therefore, increases the losses.
4) A *spark gap*, placed in parallel with the surge arrester, can be used for providing a crowbar protection at the input of the SST [62]. The main drawback is the created short circuit and the fact that the breakdown voltage is not well-defined for fast transients.
5) A *dc brake chopper* (or TVS diodes, varistors) can be used to clamp the dc-link voltages [63], [64]. This solution limits the dc-link overvoltages but increases the inrush currents through the ac–dc converters, which are already critical (see Section IV-F6).
6) An *ac crowbar* is inserted between the filter and the inverter [65]. This solution prevents overcurrents through the ac–dc converters without adding losses during nominal operation. The main drawback is that the grid will experience a short circuit during a half-grid period.

Among these solutions, the solid-state breaker and the ac crowbar seem to be the most promising concepts and are part of the advanced protection scheme depicted in Fig. 16(a). The solid-state breaker is realized by an antiseries connection of two switches. The breaker has to commutate an inductive current and, therefore, the voltage across the semiconductors is clamped by a parallel varistor [45], [59]. As the breaker should be able to isolate voltages of up to $\sqrt{3}\hat{v}_p$ (see Fig. 10), the varistor will clamp at approximately $2.2\sqrt{3}\hat{v}_p$. In order to achieve the corresponding blocking voltage, a series connection of many devices is required (IGBTs or MOSFETs), which, however, could be optimized for low conduction losses. The ac crowbar consists of two antiparallel thyristors with a series resistor (or inductor). The resistor limits the current, however, the maximal voltage drop needs to be less than the dc-link voltage [see (5), (7)], in order to ensure zero input current of the inverter.

These two protection devices are evaluated during an MV lightning surge according to Section IV-F3 (solidly earthed LFT and SST). A lightning surge has been taken as this fault leads to the fastest transients and, thus, requires the

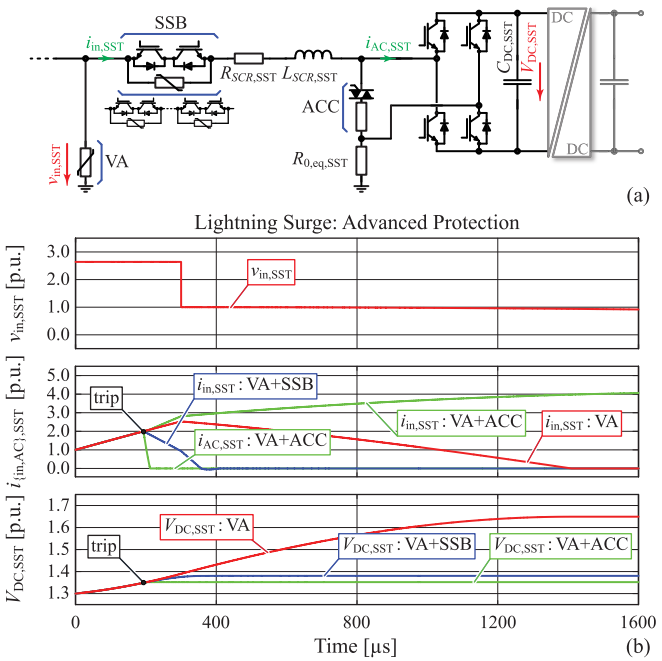


Fig. 16. (a) Advanced protection schemes for the MV side including a surge arrester (VA), an solid-state breaker (SSB), and ac crowbar (ACC). (b) Lightning surge propagation inside the SST with the classical (VA) and advanced (VA + SSB, VA + ACC) protection schemes. Currents and voltages are normalized to $\hat{i}_p$ and $\hat{v}_p$ [see (1)].

fastest protection devices. The resulting waveforms can be seen in Fig. 16(b) for the classical and the advanced protection schemes. The solid-state protection devices are triggered once the input current reaches 2 p.u.

The solid-state breaker cannot immediately interrupt the input current because voltage across the breaker is limited by the parallel varistor and the remaining voltage is applied to filter and inverter. However, as the current commutation occurs in less than 150 µs, the SST is sufficiently protected against overvoltages. With the crowbar protection device, the current commutates immediately, as the ac–dc inverter path is low inductive and the dc-link voltage stops to rise. However, due to the resulting filter short circuit, the input current continues to rise (see Section IV-E2). The resulting fault will be cleared at the next zero crossing of the grid current. This can be avoided if bidirectional turn-off switches are used in place of thyristors.

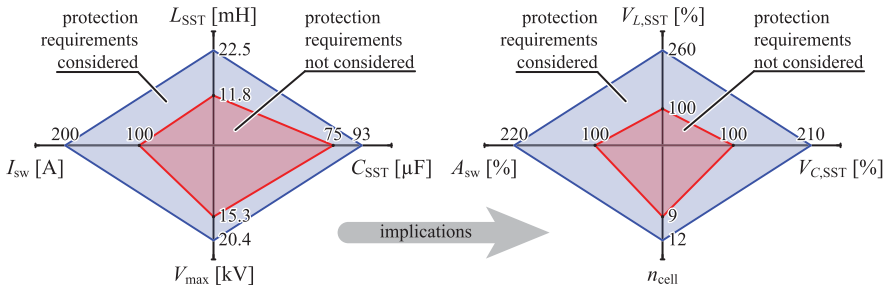
V. Design Guidelines

A. General Guidelines

From the presented analysis of the 10 kV, 1 MVA SST shown in Fig. 1, some design guidelines can be extracted (protection scheme according to Fig. 6). These guidelines may be subject to modifications if different ratings, converter topologies, or usages in the grid (industrial, residential, etc.) are considered. The following fault situations must be considered and are modeled as follows.

1) The LV inverter needs to inject enough fault current in order to trip the downstream protection devices (see Section IV-C). An overcurrent capability of 3× the rated current for some seconds should be considered for tripping a sensitive breaker, while a fuse will require even larger currents. For the complete SST (MV and LV sides), an overload capability of 1.5× for some minutes is typical (see Section IV-A).
2) The internal failure of the MV side of the SST is modeled with a 3p fault placed right after the filter of the SST (see Section IV-E2). An LFT with the same power rating feeds the SST. Related investigations indicate that a minimum short circuit impedance of $SCR_{SST} \approx 10\%$ is required, which is larger than the minimum specified by the IEC norm. The filter inductor should be able to withstand a short circuit for some hundred milliseconds. As a consequence, sufficiently high saturation currents and/or the reduction of the filter impedance due to partial saturation need to be considered.
3) MV grid short circuits are modeled with a 1pg fault (see Section IV-E3). The SST, which is turned off, is fed by an LFT with the same power rating. For some earthing policies (low EIR_{SST} and large EIR_{LFT} (see Fig. 10)), the dc-links and the semiconductors should be rated for the phase-to-phase voltage. A high ohmic MV earthing of the SST is preferred if such an earthing is compatible with the MV grid policies.
4) The dielectric strengths of the different components (filter, medium-frequency transformers, etc.) are tested with a standard IEC 1.2/50 µs impulse voltage (see Section IV-F2). This test is done without protection devices.
5) Lightning surges are modeled with a 300 µs CM rectangular pulse with a voltage equal to the arrester clamping voltage (see Section IV-F2). The test is done for the complete SST under nominal operating conditions. This leads to the following requirements: the MV power semiconductors need to be capable to block 1.8× the nominal phase-to-earth peak voltage, the MV dc-link capacitances and the filter inductance should be sufficiently large (e.g., $CER_{SST} > 1.0$ and $SCR_{SST} > 5\%$), and the voltage applied to the insulation can reach 3× the nominal phase-to-earth voltage. However, a high ohmic MV earthing reduces the impact of CM overvoltages on the SST (see Section IV-F3).
6) Switching surges are modeled with an IEC 250/2500 µs DM pulse with a peak voltage equal to 2.5× the phase-to-phase voltage (see Section IV-F6). The test is done for the complete SST under nominal condition. Compared to lightning surges, this type of overvoltage is critical and imposes $SCR_{SST} > 7\%$ and $CER_{SST} > 1.75$. A large dc-link capacitance, however, demands for a sufficiently high filter inductance to avoid large inrush currents. Moreover, the MV inverters (i.e., the power devices) should be able to accept at least 4× the rated current and 2.5× the nominal phase peak voltage for some milliseconds, which is also larger than the values obtained for lightning surges.

Similar derating factors have been found for SSTs in traction applications [7]. For the cases where the SST cannot reasonably reach these requirements, advanced protection devices need to be considered (see Section IV-G). The solid-state breaker offers a complete protection against short circuits and



param.	without. prot.	with. prot.
V	10 kV	10 kV
S	1 MVA	1 MVA
f	50 Hz	50 Hz
f_{sw}	1.0 kHz	1.0 kHz
C_{SST}	±6% ripple	$CER = 2.0$
L_{SST}	IEEE 519	$SCR = 7\%$
IGBTs	1700 V / 100 A	1700 V / 200 A
n_{cell}	9	12
$V_{DC,cell}$	1200 V	1000 V

Fig. 17. Impact of the protection requirements on the SST MV side characteristic properties. The following figures of merit are shown: I_{sw}, the current rating of the MV ac–dc inverters' semiconductors, V_{max}, the blocking voltage of the MV ac–dc inverters (of all cells, per phase), L_{SST}, the inductance of the filters (per phase), C_{SST}, the dc-link capacitance (of all cells, per phase), A_{sw}, the total chip area, n_{cell}, the number of cells per phase, $V_{L,SST}$, the volume of the filter inductors, and $V_{C,SST}$, the volume of the dc-link capacitors (of all cells).

overvoltages at the expense of increased losses and complexity and the ac crowbar represents a cheaper and lossless solution, which, however, creates a short circuit for one half-grid period.

B. Case Study: 10 kV/1 MVA *Multicell SST*

The multicell SST depicted in Fig. 1 is considered with the following ratings: 10 kV, 1 MVA, and 50 Hz [4]. A first design, without protection considerations, is chosen, which consists of nine cells (per phase) based on 100 A/1700 V IGBTs operated at 1 kHz and 1200 V (ac–dc inverters). The dc-link capacitance is determined by the voltage ripple requirement and the filter inductance by the IEEE 519 standard [66], as described in [13]. In a second step, this design is adapted for meeting the aforementioned protection requirements, which, due to the great number of available degrees of freedom (the number of cells, the switching frequency, the modulation index, etc.), can be achieved by different means and is subject to further design objectives, e.g., high power density or efficiency. In a straightforward manner, the first design can be modified according to tradeoffs given in [4] and [13]. The corresponding result is shown in Fig. 17 for the MV sides of the unmodified (unprotected) and the adapted designs.

The filter inductance value required for the protection of the SST is about twice the value required for harmonics filtering. This has, together with the required overcurrent rating, a decisive impact on the volume of the inductor, which is computed with the scaling laws presented in [67]. This drastically limits the incentive of increasing the switching frequency or the number of levels. Furthermore, the bandwidth of the current control loop, which is inversely proportional to the inductance of the filter, is reduced by the protection requirements [68]. The required dc-link capacitance is also higher than the value prescribed by the voltage ripple limit. This, together with the increased blocking voltage, increases the volume of the dc-link capacitors. In order to meet the overvoltage and overcurrent requirements, 12 cells based on 200 A/1700 V devices have to be considered (or 7 cells based on 200 A/3300 V devices), which increases the complexity of the SST. This infers that the chip area is approximately twice the value required for nominal operation, which has a direct impact on the cost of SSTs [4]. It is thus concluded that the protection requirements have a nonnegligible impact on the volume, weight, and costs of SSTs.

VI. Conclusion

This paper proposes a protection scheme for ac–ac distribution-type SSTs. Design criteria and limitations with respect to current and voltage stresses are investigated, in particular, with respect to robust operation in the MV grid. In this context, different short circuit failure types and overvoltage scenarios are analyzed with the result that MV phase-to-earth short circuits and MV slow front overvoltage situations are particularly critical. Furthermore, the MV side earthing of the grid is found to have a decisive impact on the stresses in the case of short-circuit failures and overvoltages. On the low voltage side, the main challenge is not to protect the SST itself but to respect the selectivity of the downstream protection devices.

The required overcurrent and overvoltage capabilities need to be taken into account for the design of an SST and have an impact on the achieved efficiency, power density, volume, and cost. It can be concluded that the key design parameters of an SST are not primarily influenced by the rated operation of the system, but by the operation during faults. In this context, a high switching frequency may not reduce the volume required for the protective circuits and the MV side filter of the SST. The impact will be particularly important for designs with low power rating, high switching frequency, or high voltage utilization of power devices. Alternatively, a less robust SST may be considered if advanced protection devices, such as solid-state circuit breakers, are used. In any case, the protection scheme and the corresponding derating of the SST have to be considered for the optimization and design procedures.

The presented results indicate that SSTs may be better suited for operation inside a smart or industrial grid than for operation as classical distribution transformers. Inside a smart grid or industrial grid, the dynamics of the sources and loads are known, which reduces the stresses applied to the SSTs. Furthermore, a central protection unit can be used at the interconnection point between the smart/industrial grid and the distribution/transmission grid. Yet, the presented investigations demonstrate the feasibility of the protection of SSTs and can be further developed with respect to the protection

of SSTs for specific applications, e.g., SSTs operated inside dc or smart grids. In the case of a well-defined application, a more accurate modeling of faults, in particular by means of electromagnetic transient simulation may be feasible. This will enable the extraction of more detailed and granular design rules for a particular SST.

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Thomas Guillod (S'14) was born in Neuchâtel, Switzerland, in 1989. He received the M.Sc. degree in electrical engineering and information technology from ETH Zurich, Zürich, Switzerland, in 2013, with a focus on power electronics, numerical analysis, and field theory. In 2013, he joined the Power Electronic Systems Laboratory, ETH Zurich, as a Ph.D. student.

His current research interests include MV converter design, MF transformer optimization, insulation coordination, and numerical methods.

Florian Krismer (M'12) received the Dipl.-Ing. degree in electrical engineering with a specialization in automation and control technology from the Vienna University of Technology, Vienna, Austria, in 2004, and the Ph.D. degree in electrical engineering from the Department of Information Technology and Electrical Engineering, ETH Zurich, Zürich, Switzerland, in 2010.

He is currently a Research Associate with PES, where he has co-supervised Ph.D. students and has continued with his research in the field of power electronics. He has conducted research related to the filtering of conducted electromagnetic emissions and collaborated in the littlebox-challenge with respect to the hardware realization. He has authored or co-authored numerous conference and peer-review publications and has received two awards for his publications. His current research interests include the analysis, design, and general optimization of power converter systems, e.g., the weight optimization of a bi-directional dc-dc converter for an airborne wind turbine.

Johann W. Kolar (F'10) is currently a Full Professor and the Head of the Power Electronic Systems Laboratory at the Swiss Federal Institute of Technology, ETH Zurich, Zürich, Switzerland. He has proposed numerous novel pulsewidth modulation converter topologies, and modulation and control concepts and has supervised over 60 Ph.D. students. He has authored over 750 scientific papers in international journals and conference proceedings, three book chapters, and has filed more than 140 patents. His current research interests include ultra-compact and ultra-efficient SiC and GaN converter systems, wireless power transfer, solid-state transformers, power supplies on chip, as well as ultra-high speed and ultra-light weight drives, bearingless motors, and energy harvesting.

Dr. Kolar has presented over 20 educational seminars at leading international conferences and has served as an IEEE PELS Distinguished Lecturer from 2012 to 2016. He was a recipient of 25 IEEE TRANSACTIONS and Conference Prize Paper Awards, the 2014 IEEE Power Electronics Society R. David Middlebrook Achievement Award, the 2016 IEEE William E. Newell Power Electronics Award, and the ETH Zurich Golden Owl Award for excellence in teaching. He initiated and/or is the Founder of four ETH Spin-off companies.