Highly Compact Isolated Gate Driver With Ultrafast Overcurrent Protection for 10 kV SiC MOSFETs

Daniel Rothmund, Dominik Bortis, and Johann W. Kolar

Abstract—Silicon Carbide (SiC) semiconductor technology offers the possibility to manufacture power devices with unprecedented blocking voltages in the range of 10…15 kV and superior switching characteristics, enabling switching frequencies beyond 100 kHz. To drive these 10 kV SiC devices, the power supply and the gate signal of the (high-side) gate driver require an appropriate galvanic isolation featuring a low coupling capacitance and a high dv/dr ruggedness. Since at the moment no commercially available gate drivers for these specifications exist, a customized isolated gate driver is developed, which, in order to simplify the use of the high-voltage SiC devices, is intended to be integrated into a future intelligent MV SiC module. For this purpose, a highly compact isolated gate driver with an isolation voltage rating of 20 kV is implemented and tested. The realized isolation transformer of the isolated power supply shows a volume of only 3.1 cm³ and a coupling capacitance of only 2.6 pF, and has been successfully tested at 20 kV DC. Furthermore, an ultrafast overcurrent protection (OCP) circuit is implemented to protect the expensive SiC modules from destruction due to overcurrents, which e.g. could result from false turn-on of both transistors of a bridge-leg or from short circuits of the load. The OCP circuit reacts within 22 ns to a fault and measurements prove that it can successfully clear both, a hard switching fault (HSF) and even a flashover fault (FOF), where one of the two switches of a bridge-leg configuration is subject to a flashover, in less than 200 ns for a DC-link voltage of 7 kV.

Index Terms—10 kV SiC MOSFET, isolated gate driver, isolation transformer, overcurrent protection, short circuit.

I. INTRODUCTION

M
deum-voltage (MV) SiC devices with blocking voltages of 10…15 kV have gained significant interest in the recent years [1]–[9], since they enable the simplification of MV-connected power electronics by reducing the number of switches and associated isolated gate drivers compared to modular MV converters based on lower voltage devices [10], [11]. Therefore, possible applications for MV SiC MOSFETs and IGBTs are, besides HVDC, e.g. Solid-State Transformers (SSTs) for future data center power supplies [12]–[14], high-power electric vehicle battery charging facilities [15], [16], traction applications [17], [18], naval or marine on-board MV-
The driver power supply is to use inductive power transfer (IPT) with a common AC-bus has been presented and is intended for a relatively compact current-transformer-based solution. Currents, partial discharges or even dielectric breakdowns. In the International Standard IEC 60950-1 [36]). Furthermore, creepage distances required in air (40 mm for 10 kV according to the isolation transformer module shown in Fig. 1. This can be explained by the large volume of the isolation transformer. Consequently, the volume of the isolation transformer \( V_{iso} \) has to be minimized, which is one of the main objectives of the following considerations.

In literature, most commonly air or tape-insulated transformers with discrete windings [29]–[34] or PCB windings [35] are used to isolate the power supplies of gate drivers employed in MV SiC applications. In some cases however, these transformers are up to 10 times larger than the 10 kV SiC module shown in Fig. 1. This can be explained by the large creepage distances required in air (40 mm for 10 kV according to the International Standard IEC 60950-1 [36]). Furthermore, these isolation transformers must be placed in safe distance from other converter circuit components in order to not risk creepage currents, partial discharges or even dielectric breakdowns. In [37] a relatively compact current-transformer-based solution with a common AC-bus has been presented and is intended for the supply of several gate drivers at the same time.

Another possibility to realize the galvanically isolated gate driver power supply is to use inductive power transfer (IPT) coils [38]–[41]. However, since the electric breakdown field strength of air is comparably small, a large air gap and large creepage paths are necessary, i.e. the overall IPT system will be large and hence is not suited for an integration in a highly compact module.

A further method to supply electric energy to a floating gate driver circuit is to use an optical fiber [42]. Thereby, a powerful laser (e.g. 3…10 W optical power) feeds an optical fiber, which is connected to the laser receiver on the gate driver side converting the laser power back into electric energy. The advantage of this concept is the theoretically infinite dv/dt immunity, since apart from the remaining intrinsic capacitance of the physical components, the coupling capacitance of the optical fiber is basically zero. Furthermore, no creepage distances to the laser receiver are required, such that compact gate driver circuits could be realized with this concept. However, it has to be mentioned that the laser transmitter is very large (e.g. 220 mm \( \times \) 197 mm \( \times \) 143 mm (8.66 in \( \times \) 7.75 in \( \times \) 5.63 in) for 3…20 W optical power, cf. [43]) and thus is difficult to accommodate. The low receiver efficiency of only 25% and the high costs are further disadvantages.

Therefore, a highly compact and cost-effective solution for the galvanically isolated power supply of the high-side gate driver circuits for 10…15 kV SiC MOSFETs must be developed, which could be integrated in a future intelligent MV SiC power module.

Furthermore, the gate driver circuit should be equipped with an OCP in order to protect the 10 kV SiC devices (Wolfspeed CPM3-10000-0350) from destruction due to overcurrents and/or short circuits. A typical fault scenario is the shoot-through of a bridge-leg configuration, i.e. both switches are erroneously turned on, e.g. due to incorrect or distorted gate signals. For the switch turning on while the complementary switch is already in on-state, this type of fault is called hard switching fault (HSF). In contrast, the switch which is already in the on-state experiences a so-called fault under load (FUL) [44], [45]. However, in MV applications, faults due to isolation and/or flashover failures are especially critical due to their extremely fast transients. These so-called flashover faults (FOF) are much more challenging to handle, and to also protect the MV SiC MOSFETs in this worst-case scenario, an OCP with FOF clearing capabilities is developed.

The most common method for the implementation of an OCP is a desaturation detection circuit, which measures the device on-state voltage and compares it to a certain threshold voltage [42]. However, during the turn-on transition a large blanking time is required until the device is in full on-state, the fault detection time is relatively high and potentially hazardous for the 10 kV SiC devices due to the high instantaneous power dissipation in the chip during e.g. an FOF. Furthermore, the drain voltage has to be sensed and blocked by several series-connected diodes, which have to be separated from the rest of the gate driver circuit by a certain creepage distance, which increases the gate driver volume [46]. As an alternative, the current could be measured with a shunt in the source path, or, if a Kelvin source contact is available (which is not the case for the 10 kV SiC modules at hand, cf. Fig. 1), the voltage

![Fig. 2. Concept of a future intelligent 10 kV SiC module which also contains the isolated DC/DC converter for the supply of the (high-side) gate driver stage and a fiber optic receiver for the gate signal. Furthermore, an overcurrent protection (OCP) circuit is integrated, which in case of a fault safely turns off the MOSFET and sends an optically isolated FAULT signal to the supervisory control.](image-url)
the windings and capacitance can only be realized by large distances between the windings in standard isolation transformer designs, a low coupling factor is required. However, a customized isolated power supply featuring a sufficient electrical isolation voltage rating is needed to feature a sufficient electrical isolation voltage rating. Furthermore, the common-mode (CM) currents through the parasitic isolation transformer coupling capacitance must be reduced by roughly a factor of 10 in order to keep the peak CM current in the same operating point, the transformer leakage inductance is compensated by the resonance capacitors and the system is operated at the unity-gain operating point where the output voltage is independent of the load. Consequently, a comparably low magnetic coupling factor is required and hence a relatively large leakage inductance results, which, if not compensated, leads to a load-dependent voltage drop and hence to a load-dependent output voltage of the gate driver supply. To still obtain a stable secondary-side voltage, a feedback-control would be necessary, which would, however, require an isolated transmission of the measured output voltage signal across the isolation barrier, i.e. additional effort which would further increase the risk of failure of the supply.

In order to provide sufficient isolation, the isolated power supply has to provide electric energy to the driver circuit of the power MOSFET, which features galvanic isolation, a high bandwidth, and does not require a connection to the drain potential. The measured current is subsequently processed by a high-speed analog circuit, which reacts to a fault within 22 ns and safely turns off the device.

In the following, first the galvanically isolated power supply and the realization of the isolation transformer with minimum volume and coupling capacitance will be discussed (Section II). Subsequently, the ultrafast OCP circuit is described in Section III and it is experimentally proven that it is able to safely clear both, an FO and a HSF for a DC-link voltage of 7 kV. Finally, conclusions of the main findings are drawn in Section IV.

II. The Isolated Power Supply

The isolated power supply has to provide electric energy to the driver circuit of the power MOSFET, which in the case of the high-side switch is referenced to the switch-node potential, i.e., in the case of 10 kV SiC MOSFETs to a floating rectangular voltage of e.g. 7 kV with a frequency of > 100 kHz, and \( \frac{dv}{dt} \) values of up to 100 kV/µs. Therefore, besides providing the isolated +20 V/-5 V driving voltages, the power supply needs to feature a sufficient electrical isolation voltage rating. Furthermore, the common-mode (CM) currents through the parasitic isolation transformer coupling capacitance must be kept sufficiently low in order not to disturb the proper operation of the gate driver and the protection circuits. Commercially available isolated power supplies, e.g. for 3.3 kV and 6.5 kV IGBTs, feature coupling capacitances in the range of 20...25 pF and a size of typically 50 mm × 50 mm × 20 mm [49], [50], whereby MV IGBTs are switching with rather low \( \frac{dv}{dt} \) values in the range of 10 kV/µs [51], which is 10 times slower than in the case of 10 kV SiC MOSFETs. Consequently, in a 10 kV SiC MOSFET-based converter, \( C_{CM} \) must be reduced by roughly a factor of 10 in order to keep the peak CM current in the same range as in an Si IGBT-based converter. Although there are devices such as [52] featuring an insulation voltage of 12 kV for one minute and a coupling capacitance of only 3 pF, the actual allowed operating voltage according to [36] is only 7.2 kV and due to the missing \( \frac{dv}{dt} \) and CM frequency ratings, also these devices are unsuitable for MV SiC MOSFET applications. Therefore, a customized isolated power supply featuring appropriate insulation ratings has to be realized. However, with standard isolation transformer designs, a low coupling capacitance can only be realized by large distances between the windings and between the windings and core, whereas on the other hand a significant downsizing is necessary for the integration of the transformer (cf. Fig. 2). To achieve both, a special transformer concept must be developed (cf. Section II-B).

The power consumption of the gate driver circuit at hand is 600 mW at most during operation (including the optical fiber transceivers). In order to provide a sufficiently large margin (e.g. if several 10 kV SiC MOSFETs should be operated in parallel), the isolated power supply is rated for a power of \( P_{max} = 2 \) W. TABLE I lists the specifications of the power supply as a basis for the design.

### A. Isolated Power Supply Topology

Due to the high isolation voltage requirement of 20 kV, a certain isolation distance is required between the transformers’ primary and secondary windings. Consequently, a comparably low magnetic coupling factor \( k \) and hence a relatively large leakage inductance results, which, if not compensated, leads to a load-dependent voltage drop and hence to a load-dependent output voltage of the gate driver supply. To still obtain a stable secondary-side voltage, a feedback-control would be necessary, which would, however, require an isolated transmission of the measured output voltage signal across the isolation barrier, i.e. additional effort which would further increase the risk of failure of the supply.

To overcome this problem, a topology with a load-independent voltage transfer ratio, namely the series-series compensated resonant converter shown in Fig. 3 is selected. It consists of an H-bridge inverter, a 1 : 1 isolation transformer (i.e. the lowest rms currents) of the resonant system is achieved and hence beneficial in terms of low high-frequency (HF) losses due to skin-effect and proximity-effect, since no higher current harmonics are present. Consequently, the device current could be measured galvanically isolated with a Rogowski coil [48], which is, however, sensitive to external electric and magnetic fields and could therefore lead to false triggering.

In order to avoid the disadvantages of the mentioned OCP methods and to ensure a highly robust and fast protection, a high-speed analog circuit, which reacts to a fault within 22 ns and safely turns off the device.

In the following, first the galvanically isolated power supply and the realization of the isolation transformer with minimum volume and coupling capacitance will be discussed (Section II). Subsequently, the ultrafast OCP circuit is described in Section III and it is experimentally proven that it is able to safely clear both, an FO and a HSF for a DC-link voltage of 7 kV. Finally, conclusions of the main findings are drawn in Section IV.

<table>
<thead>
<tr>
<th>Property</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltages</td>
<td>( U_{DC1}, U_{DC2} )</td>
<td>+20 V, -5 V</td>
</tr>
<tr>
<td>Max. output power</td>
<td>( P_{max} )</td>
<td>2 W</td>
</tr>
<tr>
<td>Max. coupling capacitance</td>
<td>( C_{CM,max} )</td>
<td>3 pF</td>
</tr>
<tr>
<td>Isolation voltage</td>
<td>( U_{iso} )</td>
<td>20 kV</td>
</tr>
</tbody>
</table>
B. Isolation Transformer

In conventional isolation transformers, the primary and the secondary windings are placed on the same magnetic core and are galvanically isolated from each other by means of insulation material between the primary winding and the core, the secondary winding and the core, and between the primary and secondary windings. In the case of the application at hand, the differential mode voltage applied to both transformer windings is < 50 V and hence, no further isolation between the primary winding and the core (which in this case would be tied to GND potential) would be necessary. However, the secondary winding would have to be isolated from both, the core and the primary winding since it is floating on the switched potential of e.g. 7 kV. Consequently, the winding window and therewith the size of the entire magnetic core has to be chosen sufficiently large, such that the secondary winding can be separated from the core and from the primary winding by approximately 1.6 mm of insulation material thickness to each side, if an (average) electric field strength of 4.5 kV/mm is allowed and the transformer is potted in a suitable insulation material. Since the transformer’s power rating is only $P = 2$ W but the isolation distances do not scale with the power but are defined by the isolation voltage, the required winding window would be large compared to the dimensions of a typical 2 W HF transformer without MV isolation and hence, this transformer concept is not suitable for achieving a low volume.

To overcome this limitation and to minimize the volume of the isolation transformer, as many isolation barriers as possible have to be omitted. Therefore, the primary winding and the secondary winding are wound on separate ferrite E-core halves without any isolation distance between the winding and the core. Fig. 4(a) shows a drawing of one of the core halves with its corresponding winding. Thereby, the core consists of several stacked E-cores to achieve the desired form factor. The two core halves with their respective windings are then separated by a certain distance $d = 1.6$ mm to keep the average electric field strength below 4.5 kV/mm in the case of 7 kV CM voltage, similar to the air gap in a conventional transformer [54], [55].

The isolation distance between the two core halves is ensured by mounting them in a 3D-printed enclosure as shown in Fig. 4(b). In operation, the primary winding is on GND potential, whereas the secondary winding floats on the switch-node potential. To also define the potential of the ferrite cores, they are connected to one end of the corresponding winding as shown in Fig. 4(c) and are covered with a thin layer of semiconductive graphite spray (cf. Fig. 4(d)) to tie the surface of the entire core halves to the potential of the respective winding. The surface resistance of the graphite spray (Kontakt Chemie Graphit 33) is $< 2000 \Omega$/sq, which is sufficiently low to define the potential of the surface and at the same time is sufficiently high such that no significant eddy current losses are generated by the magnetic field [56]. As an alternative, semiconductive tape could be used to create an equipotential surface.

Consequently, this transformer arrangement can be regarded as plate capacitor from an electric field point of view, which allows to estimate the coupling capacitance of the transformer as

$$C_{cm} = \frac{\varepsilon_r \varepsilon_0 A}{d},$$
where $A$ is the surface area of the core halves and the windings (cf. Fig. 4(a)) and $d$ is the separation distance between the core halves. Since $d$ is already fixed to $d = 1.6$ mm, the remaining geometry parameter to minimize the coupling capacitance is the surface area $A$. With a relative permittivity of $\varepsilon_r = 4.12$ of the selected insulation material (cf. Section II-B1), the surface area must be lower than 132 mm$^2$ to keep the coupling capacitance below the desired value of $C_{CM,max} < 3$ pF, which is roughly 10 times lower than the coupling capacitance of commercially available isolation transformers. To fulfill this condition, four stacked E8.8 ferrite cores (material N30) are used ($x = 9$ mm (0.35 in), $y = 8$ mm (0.31 in), $z = 4.1$ mm (0.16 in), cf. Fig. 4(a)), which results in an almost square-shaped form factor of the core surface, a surface area of $A = 108$ mm$^2$ (including the winding heads), and a theoretical coupling capacitance of $C_{CM} = 2.5$ pF.

In order to analyze the electric field in the isolation transformer, a FEM simulation has been implemented and the simulated electric field distribution is shown in Fig. 5. As can be seen, the windings are field-free due to the shielding effect of the graphite coating. Furthermore, a high electric field only occurs between the limbs of the ferrite cores and is slightly lower between the windings (due to the slightly larger distance). To decrease the maximum electric field strength, the edges and corners of the ferrite cores have been rounded off and the maximum value of the electric field (6 kV/mm) is still a factor of four lower than the breakdown field strength of the used silicone encapsulant and therefore uncritical.

As can be noticed from the dimensions of the cores, the isolation gap is comparably large and hence, a rather low magnetic coupling factor $k$ will result. Thus, the transformer acts similar to a pair of inductive power transfer (IPT) coils. Thereby, larger primary-side and secondary-side inductance values are beneficial for ensuring a higher quality factor [57] and lower magnetization current, and for this reason the number of turns wound on the two core halves should be as high as possible while the thermal limit has to be considered at the same time. Therefore, a maximum current density of $J_{max} = 15$ A/mm$^2$ is defined. In order to keep the high-frequency losses due to the skin and proximity effect to a moderate level, litz-wire has to be employed for the primary and secondary windings. For a maximum expected operating frequency of $f_{max} = 1$ MHz, a skin-depth in copper of $\delta_{Cu} = 65 \mu$m results. Hence, as a compromise between the copper filling factor and the HF losses, a strand diameter of $d_s = 71 \mu$m is selected and with an assumed total copper filling factor of 25% (i.e. 50% litz-internal and a 50% ratio between the winding area and the available core window area), the maximum achievable number of turns is 34. For practical reasons, a $6 \times 71 \mu$m litz wire and $N = 32$ turns is selected, resulting in a DC-resistance of $R_{DC} = 620 \Omega$.

To check the feasibility of the transformer design, the magnetic flux density in the ferrite core is determined, whereby it is assumed that the operating frequency is in the range of $[f_{min}, f_{max}] = [100$ kHz, $1$ MHz]. Furthermore, due to the series-series compensation of the leakage inductance, the peak value of the sinusoidal voltage applied to the magnetizing inductance of the transformer is approximately equal to the fundamental component of the rectangular voltage applied from the primary-side, i.e.
\[ u_n = \frac{4}{\pi} \cdot u_p , \]  

Consequently, with the magnetic cross section area \( A_m \) of the core, the peak magnetic flux density can be calculated as

\[ \tilde{B} = \frac{1}{\pi} \frac{\tilde{u}_m}{N^2 A_m} \int_0^T \sin(2\pi f_t) \cdot dt = \frac{2u_p}{\pi^2 N A_m f} , \]

resulting in \( \tilde{B} = 3.2 \text{ mT} \ldots 32 \text{ mT} \) for the assumed frequency range, which indicates that the ferrite cores are operated far below the saturation limit and hence the design is feasible from a magnetic perspective.

1) Thermal Model & Selection of the Insulation Material:

For a prediction of the temperature distribution inside the transformer and especially in the insulation material which plays a central role for the transformer at hand, a thermal FEM simulation is conducted. As a basis for the simulation, the different loss components, i.e. winding losses, core losses, and dielectric losses are calculated first.

For an estimation of the worst case winding losses, the AC winding resistance at the highest expected transformer operating frequency \( f_{\text{max}} = 1 \text{ MHz} \) is calculated. Considering the skin-effect and the proximity effect, the winding losses can be calculated according to [58] as

\[ P_{\text{Cu}} = R_{\text{AC}} (F_h \tilde{B}^2 + G_h \tilde{B}^2) , \]

where \( F_h \) and \( G_h \) are the factors describing the skin-effect and the proximity-effect, and \( \tilde{B} \) depicts the temporal peak value of the magnetic field, which shows a triangular spatial distribution across the winding window width \( w_w = 1.65 \text{ mm} \) (cf. Fig. 4(a)) and a spatial rms value of [59]

\[ \tilde{B}_{\text{rms}} = \frac{N \tilde{I}}{\sqrt{3} w_w} . \]

By combining (9) and (10), the ratio between the effective AC resistance \( R_{\text{AC}} \) and the DC resistance \( R_{\text{DC}} \) can be derived [58]. For \( f_{\text{max}} = 1 \text{ MHz} \), this factor is \( R_{\text{AC}}/R_{\text{DC}} = 4.5 \), i.e., the effective AC resistance is \( R_{\text{AC}} = 2.8 \Omega \) for each of the two windings. With the calculated primary- and secondary-side currents (cf. Section II-A), the highest expected winding losses are \( P_{\text{Cu}} = 415 \text{ mW} \) and \( P_{\text{Cu}} = 138 \text{ mW} \).

Furthermore, a calculation of the core losses with the Steinmetz parameters for N30 ferrite \( (k_c = 15.88, \alpha = 1.31, \text{ and } \beta = 2.45 \) [60]) and the determined values for the magnetic flux density leads to 4 mW at \( f = 100 \text{ kHz} \) and 0.3 mW at \( f = 1 \text{ MHz} \), respectively, i.e. the core losses can be neglected.

Due to the comparably high electric field in the isolation transformer and the high switching frequency of the 10 kV SiC MOSFET bridge, the insulation material between the two core halves is exposed to a high dielectric stress and therefore, dielectric losses might become significant and would have to be considered. According to [61], the dielectric losses generated in a capacitance \( C_{\text{Cu}} \) by a rectangular voltage with bottom value 0 V, top value \( U_{\text{DC}} \), frequency \( f_{\text{sw}} \) and 50% duty cycle can be calculated as

\[ P_{\text{d}} = \frac{\delta \cdot C_{\text{CM}} U_{\text{DC}}^2 \cdot 2 f_{\text{sw}}}{\pi} \ln \left( \frac{2e^\gamma f_{\text{sw}}}{f_{\text{rise}}} \right) , \]

where \( \gamma \approx 0.57 \) is the Euler-Mascheroni constant, and

\[ f_{\text{rise}} = \frac{1}{2 \pi^2 \ln \left( \frac{0.9}{0.1} \right)} \]

is the corner frequency (cf. [61]). Furthermore, \( t_{\text{rise}} \) is the 10 %...90 % rise time of the switch-node voltage. Thereby, it is important to note that not only the fundamental frequency component of the switch-node voltage but also the higher order harmonics contribute to the dielectric losses. (11) already includes the effect of the harmonics and as can be seen, the total dielectric losses are proportional to the dissipation factor \( \tan \delta \), the switching frequency \( f_{\text{sw}} \), and the square of the voltage, or the electric field, respectively. To show that it is important to select a suitable insulation material, the dielectric losses are first calculated for a typical epoxy-based insulation material, e.g., Damisol 3418 whose dissipation factor is strongly frequency and temperature dependent [61] and is assumed to be \( \tan \delta = 1.2 \% \) for the following calculations. With a switch-node voltage of 7 kV, a switching frequency of \( f_{\text{sw}} = 125 \text{ kHz} \) and a rise time of \( t_{\text{rise}} = 100 \text{ ns} \), dielectric losses of \( P_{\text{d}} = 430 \text{ mW} \) occur in the insulation material, which is very high compared to the rated power of the isolation transformer. Furthermore, epoxy resins typically feature a rather low thermal conductivity \( 0.3 \text{ W/(m K)} \) in this case), which means that the extraction of the heat generated by the dielectric losses is impeded and therefore could lead to a thermal runaway.

Fig. 6(a) shows the simulated temperature distribution inside the isolation transformer in the case of epoxy resin as insulation material and a fixed housing temperature of 50 °C. As can be seen, due to the dielectric losses in the insulation material and the low thermal conductivity of the epoxy resin, a hot spot between the two core halves and a temperature rise of 44 K occurs. Since epoxy resins typically show a significant increase of their dielectric dissipation factor \( \tan \delta \) which can reach values of \( \tan \delta > 25 \% \) at higher temperatures in the region of their glass transition temperature [61]–[63], a thermal runaway is very likely to happen (especially when a higher power of the isolation transformer. Furthermore, epoxy resins typically feature a rather low thermal conductivity \( 0.3 \text{ W/(m K)} \) in this case), which means that the extraction of the heat generated by the dielectric losses is impeded and therefore could lead to a thermal runaway.

In contrast, silicone composites typically feature a very low and stable \( \tan \delta \) up to temperatures beyond 200 °C. However, pure silicone rubber typically shows only a low thermal conductivity, which would potentially lead to an undesired heat accumulation similar to Fig. 6(a). To increase this value, thermally conductive micro or nanoparticles can be added to the pure silicone, which, on the other hand, leads to an...
increasing dielectric dissipation factor [64]. Therefore, a compromise between a low tan δ and a high thermal conductivity has to be made. The utilized material for the encapsulation of the isolation transformer at hand is the two-component silicone compound Dow Corning TC-4605 HLV and the properties of this material are listed in TABLE II. With this insulation material, the dielectric losses are only \( P_d = 300 \text{ mW} \).

Fig. 6(b) shows the associated temperature distribution inside the isolation transformer and as can be seen, the temperature increase in the hot spot, which is now located inside the primary-side winding, is only 12 K due to the lower dielectric losses and the higher thermal conductivity. This shows that the selection of a proper insulation material is crucial for the functionality of a highly compact isolation transformer and consequently, with the selected material, the isolation transformer can be operated inside an intelligent 10 kV SiC module with an assumed baseplate temperature, i.e. transformer surface temperature of 100 °C, which would lead to a hot spot temperature of 112 °C inside the transformer.

For a reliable operation of the isolation transformer, the insulation material must be free of air-cavities or other impurities, which could lead to partial discharges and a degradation of the material over time. Therefore, a vacuum pressure potting (VPP) process is used, i.e. the silicone is devolatilized and the transformer is potted under vacuum (30 mbar) before the pressure is increased again to compress possible air or vacuum cavities. The still liquid silicone compound is then cured at a temperature of 120 °C for several hours. More details on the VPP process and the insulation material are given in [14].

In order to provide a sufficiently large creepage distance between the primary-side and secondary-side litz wires at the outside of the transformer, a silicone tube is covering the primary-side litz wire (on GND potential) and is also potted in the silicone insulation material such that there is no other creepage path than the one along the silicone tube. The finalized isolation transformer is shown in Fig. 4(e).

2) Determination of the Transformer Properties:

Besides the inductances and the magnetic coupling factor \( k \), which are required to determine the optimum operating frequency, also the parasitic capacitance \( C_{CM} \) between the primary-side and the secondary-side is measured. For this purpose, a HP 4294A Precision Impedance Analyzer is used.

The measured value of the coupling capacitance is \( C_{CM} = 2.6 \text{ pF} \), which matches very well with the calculated value of 2.5 pF. Considering the small transformer dimensions, this capacitance value is very low and ensures that the parasitic CM currents stay in a reasonable range even in the case of high \( \frac{dv}{dt} \) values of up to 100 kV/µs.

The measurement of the primary-side and the secondary-side inductances leads to \( L_p = 23.7 \mu\text{H} \) and \( L_s = 23.4 \mu\text{H} \) and together with a measured leakage inductance of \( L_{\nu} = 22 \mu\text{H} \), the magnetic coupling factor (referenced to the primary-side) can be calculated as

\[
k = \sqrt{1 - \frac{L_{\nu}}{L_p}} = 0.27. \tag{13}
\]

With these values, the optimum operating frequency \( f_0 = 713 \text{ kHz} \), and the values of the resonance capacitors \( C_{r1} = C_{r2} = 2.88 \text{ nF} \), can be determined with (1) and (2), respectively.

C. Experimental Verification of the Isolated Power Supply

For the experimental verification of the isolated gate driver power supply, different stress tests have been performed. To test the DC isolation rating of the designed transformer, a
20 kV DC voltage (which is almost three times higher than the maximum operating voltage of 7 kV) has successfully been applied between the transformer’s primary and secondary windings for one hour without breakdown, temperature increase or measurable current flow through the isolation. This proves that the isolation concept is properly working and well overdimensioned to guarantee a long lifetime.

Furthermore, to also test the complete gate driver circuit and the isolation transformer under real operating conditions, a 10 kV SiC-MOSFET-based half-bridge inverter has been designed as shown in Fig. 7. It consists of a PCB which incorporates the low-side and the high-side MOSFETs together with their respective gate driver and isolated power supply circuits. As can be seen, the isolation transformers are placed on the bottom side of the PCB and enable the construction of a highly compact half-bridge due to their small dimensions. As already mentioned, the silicone tube provides a 60 mm creepage distance to the primary-side driving circuit of the isolation transformer (not shown), which only consists of a MAX13256 H-bridge IC, an adjustable clock generator IC, and two ceramic DC buffer capacitors.

To expose the isolation transformer to a very high stress, the half-bridge has been operated with a DC-link voltage of 7 kV and a switching frequency of 125 kHz for one hour. Thereby, an inductor has been used as load to enable ZVS and therewith to minimize the switching losses of the 10 kV SiC MOSFETs [22]. During this test, the CM current of the high-side isolation transformer has been measured. The corresponding circuit diagram and the according voltage and current waveforms during a rising voltage transition are shown in Fig. 8. It can be seen that a dv/dt of 82 kV/µs leads to a peak CM current of 300 mA. To obtain this peak current from the measured voltage slope, a coupling capacitance of 4.1 pF (which is 1.5 pF larger than the measured coupling capacitance of the isolation transformer) must be present. The additional capacitance can be explained by parasitic capacitances of the connection of the PCB to the isolation transformer and/or additional cable capacitances.

During the 7 kV, 125 kHz operation of the entire circuit with a load of 2 W, the steady-state surface temperature of the isolation transformer (cf. Fig. 9) reaches 50 °C (at an ambient temperature of 25 °C and for natural convection cooling), and as already shown by the thermal FEM simulation in Fig. 6(b), the hot spot temperature is estimated to be around 62 °C.

III. ULTRAFAST OVERCURRENT PROTECTION (OCP)

In MV applications, it is highly recommended to implement an overcurrent and/or short circuit protection for the MV semiconductors due to the high voltages and the corresponding high energies in e.g. the DC-link capacitors, which could lead to serious damage of the hardware in case of a fault. Furthermore, MV SiC devices with blocking voltages of 10...15 kV are still very expensive and are up to now only available as prototype devices.

It is shown in [65] that single 10 kV SiC MOSFETs can survive approximately 8.5 μs under a full short circuit with 6 kV DC-link voltage. However, in [66], a clear relation between the degradation of the MOSFET-chip (i.e. increased \( R_{DS,on} \)) and the short circuit duration is apparent, since the degradation is an effect of the high temperature of the chip and its metallization.
In the configuration shown in Fig. 10, the current transformer is placed below the gate and source contacts of the driver stage, which ensures that only the drain current $i_d$ is measured. The secondary-side of the current transformer is connected to a burden resistor $R_b = 1 \, \Omega$ and the entire circuit is powered from the $0 \, \text{V} / -5 \, \text{V}$ rails. Since the drain current of the 10 kV SiC device can also be negative, one terminal of the current transformer is connected to a locally generated $-2.5 \, \text{V}$ potential, allowing a voltage swing of $\pm2.5 \, \text{V}$ across $R_b$, which corresponds to a drain current of $\pm75 \, \text{A}$. In case of a fault, where much higher currents can occur, the diodes $D_{1...n}$ start conducting and clamp the voltage across $R_b$ in order to protect the input of the subsequent comparator from overvoltages. The advantage of diode strings compared to a single TVS or zener diode per direction is the steeper characteristic of pn diodes, i.e. the clamping voltage is less current dependent. The type and the number of serial diodes is selected such that a clamping voltage of 2.5 V results.

For the detection of an overcurrent, the voltage at the upper rail of $R_b$ is compared to the threshold voltage $U_{\text{lim}} = -2.5 \, \text{V}$ of the ultrafast comparator. Once the threshold is exceeded, the comparator sets its output to HIGH ($0 \, \text{V}$) and the subsequent D-latch changes state and latches its output state when $E_{\text{lim}} = 2.5 \, \text{V}$. The FAULT signal (cf. Fig. 10) is connected to the enable input EN of the gate driver IC $UCC27531-Q1$ from $T_{\text{H}}$, which then initiates a turn-off of the 10 kV SiC MOSFET. The delay caused by the logic ICS and the gate driver IC adds up to $T_{\text{on}} = 22 \, \text{ns}$ between the detection of the overcurrent and the reaction of the gate voltage. Since the gate driver IC does not provide a sufficiently high gate current (but undervoltage lockout, which is the reason to use an IC at all), a BJT totem-pole stage is used to provide a sufficiently high gate current. The gate resistors for turn-on and turn-off are $R_{\text{on}} = 20 \, \Omega$ and $R_{\text{off}} = 10 \, \Omega$, respectively, according to [22]. Alternatively, a soft turn-off circuit could be implemented, which, in case of a fault, turns off the device with a larger gate resistor as it is done for IGBTs to limit the voltage overshoot. Furthermore, the FAULT signal is also transmitted back to the supervisory control. During a short circuit. Additionally, in the case of 10 kV, 100 A SiC MOSFET modules, a short circuit withstand time of only 3.5 ms at 6 kV has been observed [67]. Therefore, the goal is to realize an ultrafast overcurrent protection (OCP) with a very short reaction time in order to keep the thermal stress on the 10 kV SiC MOSFET chips as low as possible.

In literature, two major types of faults are described, namely the hard switching fault (HSF), where a MOSFET turns on onto a short circuit, and the fault under load (FUL), where a short circuit occurs while the MOSFET is in on-state. In this case, however, the current and voltage slopes are mainly and significantly limited by the switching speed of the turning on MOSFET, whereas in MV applications, flashovers can occur (due to insulation failures e.g. the silica gel in MV semiconductor modules or the insulation material e.g. in the transformer employed in a DC/DC converter) and show extremely fast voltage and current transients, which are much more critical to handle for an OCP. Therefore, the standard HSF and FUL tests are the only measure for the quality of an OCP circuit, since they do not test the worst case scenario, namely an arc flashover across one of the MOSFETs in a bridge-leg configuration while the complementary MOSFET is turned on. Therefore, the term flashover fault (FOF) is introduced and an FOF is applied to a 10 kV SiC MOSFET bridge-leg by using a gas discharge tube (GDT) of type Bourns SA2-7200-CLT-STD in the high-side position, which internally ignites a low-ohmic plasma (i.e. a solid short circuit) when the applied voltage exceeds its breakdown voltage, while the low-side switch is in on-state and has to clear the fault.

### A. Functional Principle of the OCP

For the detection of a fault, the device current is measured by means of an air-gapped current transformer in the source path of the 10 kV SiC MOSFET as shown in Fig. 10. Thereby, the air gap avoids the saturation of the core material due to the DC current component and compared to e.g. a current measurement shunt, the current transformer provides galvanic isolation of the measurement signal and improves the immunity against CM distortions. In the following, the fundamental functionality of the OCP circuit is explained, assuming that the drain current can be measured with a sufficient accuracy with the $1 : 30$ current transformer. The details on the design of the current transformer can be found in the Appendix.

![Circuit diagram of the driver stage and the overcurrent protection.](diagram)

Fig. 10. Circuit diagram of the driver stage and the overcurrent protection. The drain current $i_d$ of the MOSFET is measured via a $1 : N_2 = 1 : 30$ air-gapped current transformer and the subsequent burden resistor $R_b = 1 \, \Omega$. Once the threshold $U_{\text{lim}}$ is exceeded, the comparator and consequently also the D-latch changes state and latches the FAULT state. This signal is fed back to the enable input EN of the driver IC ($UCC27531-Q1$ from $T_{\text{H}}$), leading to a turn-off of the 10 kV SiC MOSFET. The delay of the logic is approximately 22 ns. Furthermore, the FAULT signal is optically transmitted back to the supervisory control.
feedback path to the gate could be implemented for a further reduction of the reaction time.

B. Flashover Fault Simulation

Before the OCP is tested in hardware and has to prove that it is able to safely clear a HSF and an FOF at 7 kV DC-link voltage, a simulation is carried out in order to predict the behavior of the circuit under these extreme conditions. Fig. 11(a) shows the simulation model of the bridge-leg in the case of an FOF, where an ideal switch is located in the high-side MOSFET position and the low-side MOSFET is replaced by a simple equivalent circuit consisting of a voltage controlled current source, the nonlinear parasitic MOSFET capacitances, the antiparallel body diode, and the package inductances [20]. The current source is controlled by the internal gate voltage \( u_{GS,int} \) across the gate-source capacitance \( C_{GS} \) via

\[
\begin{aligned}
\bar{i}_{G,0} &= g_m (u_{GS,int} - u_{D,0}),
\end{aligned}
\]

where \( u_{D,0} \) is the threshold voltage of the MOSFET and \( g_m \) is its transconductance. In the simulation, the ideal switch is closed at \( t = 0 \) while the low-side MOSFET is already turned on, i.e., \( u_{Driver} = 20 \text{ V} \). Furthermore, it is assumed that the overcurrent protection will react 30 ns after the fault and will force the driver output voltage \( u_{Driver} \) to \(-5 \text{ V} \) within another 15 ns.

Fig. 11(b) shows the simulated waveforms under these assumptions. Initially, the drain current \( i_D \) rises with a very high \( di/dt \), which in turn induces a high positive voltage \( u_{GS} \approx 140 \text{ V} \) across the source inductance \( L_S \). The relatively large gate-source capacitance \( C_{GS} \) however keeps its voltage \( u_{GS,int} \) constant and therefore, the external gate-source voltage \( u_{GS} \) closely follows the induced voltage \( u_{GS} \) with a 20 V offset, while the effect of the gate inductance \( L_G \) can be neglected in this case. Since also the driver voltage \( u_{Driver} \) is still clamped to 20 V, the difference of \( u_{GS} - u_{Driver} \approx 140 \text{ V} \) peak is applied to the turn-off gate resistor \( R_G = 10 \Omega \), forcing a part of the MOSFET channel current through \( C_{GS} \) and leading to a negative gate current of \( \bar{i}_G = (u_{GS} - u_{Driver}) / R_G = -14 \text{ A} \) peak (when the gate inductance \( L_G \) is neglected). The reader should note that the gate resistors and the diodes should be well dimensioned to withstand the high peak current. Consequently, \( C_{GS} \) is discharged (i.e. \( u_{GS,int} \) decreases) and according to (14), the MOSFET channel current \( i_{G,0} \) decreases again, as can be seen in the figure. Although the channel current decreases, the series inductances \( L_S, L_D, \) and \( L_D \) try to keep the constant current and hence, a part of the drain current \( i_D \) commutates to the output capacitance \( C_{GS} \), resulting in a rapid increase of the drain-source voltage \( u_{DS} \) and an inductive overshoot. At the same time, the drain current effectively decreases, and the complete process until this point takes place without any action from the gate driver and is therefore referenced as “self turn-off” of the MOSFET. However, at this point, the decreasing drain current leads to a positive gate current due to the negative induced voltage across \( L_S \), such that the MOSFET partly turns on again. Now, the induced voltage is applied to \( R_G = 20 \Omega \), which is twice the value of \( R_{off} \) and therefore, the increase of the drain current is only small and the oscillation is damped.

As can be seen in Fig. 11(b), due to the self turn-off mechanism and the short reaction time, the OCP is able to clear the FOF within 200 ns, whereby a peak drain current of 320 A is reached. Furthermore, it can be noted that the chip-internal gate-source voltage \( u_{GSS} \) barely exceeds 20 V and hence stays within the absolute maximum ratings, i.e., the MOSFET chip is not endangered.

C. Experimental Results

1) FOF Experiment

Since the results from the FOF simulation show that the OCP is able to successfully clear an FOF in theory, this situation is also tested in real hardware. Thereby, as shown in
the schematic in Fig. 12, the low-side MOSFET is permanently turned on while the high-side MOSFET is substituted by a gas discharge tube (GDT) of type Bourns SA2-7200-CLT-STD and the DC-link voltage is increased until the GDT ignites. Fig. 12 shows the measured drain-source voltage \( u_{DS} \), the gate-source voltage \( u_{GS} \), and the drain current \( i_D \) during an FOF test with a 7.2 kV GDT, which ignited at 7.6 kV (due to tolerances). As can be seen, the waveforms are similar to the simulation, i.e., also in real hardware a self turn-off occurs. Thereby, the drain current reaches a value of 350 A and the drain-source voltage rises to the DC-link level within 6 ns, i.e., an unprecedented dv/dt of 1.2 MV/µs. After the reaction delay of approximately 22 ns, the gate driver actively brings the gate voltage to \(-5 \) V and the fault is cleared within 150 ns.

Fig. 13 shows the situation for the HSF. The schematic in Fig. 13 shows the situation for the HSF test, where the high-side MOSFET \( S_2 \) is in the on-state when \( S_1 \) turns on. The measured waveforms of the drain current \( i_D \), the gate-source voltage \( u_{GS} \), and the FAULT signal are shown for a HSF at 2 kV and 7 kV, respectively. With the increasing gate-source voltage, also the drain current increases and once it reaches the threshold (25 A in this case), a short delay of the internal FAULT signal, which is connected to the enable signal of the driver IC, changes state. The gate driver IC then switches its output to \(-5 \) V and the gate-source voltage decreases after the IC’s propagation delay has passed. Almost independently of the DC-link voltage level, the current reaches a maximum of 48 A.

2) HSF Experiment

In this paper, a highly compact isolated gate driver for 10 kV SiC MOSFETs with ultrafast overcurrent protection is presented. A main challenge for medium-voltage (MV) gate drivers is the galvanic isolation of the gate driver power supply and the isolated low propagation delay signal transmission. In order to obtain a highly compact gate driver circuit, which could be integrated into future MV SiC modules, an encapsulated isolation transformer employed in a resonant converter topology is designed and constructed. Thereby, in contrast to classical transformers with both windings on the same

the presented OCP would also work for modules featuring a Kelvin source contact.

IV. CONCLUSION

In this paper, a highly compact isolated gate driver for 10 kV SiC MOSFETs with ultrafast overcurrent protection is presented. A main challenge for medium-voltage (MV) gate drivers is the galvanic isolation of the gate driver power supply and the isolated low propagation delay signal transmission. In order to obtain a highly compact gate driver circuit, which could be integrated into future MV SiC modules, an encapsulated isolation transformer employed in a resonant converter topology is designed and constructed. Thereby, in contrast to classical transformers with both windings on the same
magnetic core, the primary winding and the secondary winding are wound on separate ferrite core halves, which are separated by a small gap that is filled with a silicone insulation material featuring a low dielectric dissipation factor and a high thermal conductivity to ensure a sufficient heat transport from the windings to the surface of the transformer. The dimensions of the realized transformer are 16 mm × 16 mm × 14 mm and the coupling capacitance is only 2.6 pF. The transformer isolation has been successfully tested for 1 hour with a 20 kV DC voltage and for one hour with a 7 kV, 125 kHz switching-node voltage, which proves the functionality of the designed MV isolation transformer.

Furthermore, in order to protect the 10 kV SiC devices from overcurrents and a possible destruction by short circuits, an ultrafast overcurrent protection (OCP) circuit is implemented. Thereby, the drain current of the device is measured via a gapped toroidal current transformer. The measured signal is subsequently compared to a predefined threshold by an ultrafast comparator whose output signal is latched in case of a fault and fed back to the enable input of the gate driver IC, which then initiates the turn-off of the 10 kV SiC device. The delay between the crossing of the overcurrent threshold and the reaction of the gate voltage is only ≈22 ns. Measurements prove that the realized OCP is also able to successfully clear a flashover fault (FOF) and a hard switching fault (HSF) at a DC-link voltage of 7 kV within less than 200 ns. Furthermore, during the FOF experiment, an unprecedented \(\text{d}v/\text{d}t\) of 1.2 MV/µs has been observed.

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**APPENDIX**

**DESIGN OF THE CURRENT TRANSFORMER**

For the measurement of the drain current of the 10 kV SiC MOSFETs, the current transformer has to be designed for a high bandwidth, such that fast overcurrent transients can be measured accurately. Furthermore, the current transformer should not add a significant signal delay to the protection circuit. Consequently, the leakage inductance and capacitance have to be kept small, which can be achieved by choosing a low number of secondary-side turns equidistantly wound on a toroidal ferrite core. As shown in Fig. 10, the secondary winding is connected to a burden resistor \(R_B = 1 \Omega\) where a current-proportional voltage is measured. If a voltage of 1 V across \(R_B\) is desired for an overcurrent threshold of \(\text{OCT} = 30 \text{ A}\), a turns ratio of \(1 : N_2 = 1 : 30\) results, i.e. the number of secondary turns on the current transformer is \(N_2 = 30\). To operate the ferrite core material in its linear region, the maximum magnetic AC flux density is set to \(B_{\text{max,AC}} = 75 \text{ mT}\) and for an assumed rectangular drain current with 50% duty cycle, a minimum converter switching frequency of \(f_{\text{min}} = 30 \text{ kHz}\), a bottom value of 0 A, and an amplitude of \(i_{\text{d,max}} = 30 \text{ A}\), a core cross section of \(A_c = 7.4 \text{ mm}^2\) is required. Therefore, a R10 × 6 × 4 ferrite core (N30 material) with a magnetic cross section area of 7.83 \(\text{mm}^2\) is selected.

As the drain current of the switches is not a pure AC current but rather a superposition of an AC and a DC current, the current transformer has to be designed appropriately, such that the DC component does not lead to saturation of the magnetic core. Therefore, an air gap is inserted in the ferrite core. For limiting the magnetic DC flux density to \(B_{\text{max,DC}} = 125 \text{ mT}\), the required air gap length is

\[
\delta = \frac{B_{\text{max,DC}} \cdot i_{\text{IDC}}}{\mu_0} = 150 \mu\text{m}
\]

for a maximum DC current component of \(i_{\text{IDC}} = 15 \text{ A}\).

The air gap, however, causes the magnetizing inductance of the current transformer to drop significantly, which increases the AC magnetizing current. For the current transformer at hand, the peak magnetizing current for \(f_{\text{min}} = 30 \text{ kHz}\) and 30 A, 50% duty cycle is 7% of the measured current value, which does not influence the detection of a HSF or an FOF due to the usually large resulting fault currents. For the sake of completeness, it should be noted that the current transformer represents a high-pass system (corner frequency \(f_c = 17 \text{ kHz}\)) and is not able to measure DC currents, since the DC component only occurs as magnetizing current on the primary-side.

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