A New Concept for Minimizing High-Frequency Common-Mode EMI of Three-Phase PWM Rectifier Systems Keeping High Utilization of the Output Voltage

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Abstract. Three-phase PWM rectifier systems in principle show a common-mode voltage with switching frequency between the mains neutral point and the center point of the output voltage. Without any counter-measures this leads to a high common-mode noise emission of the system and possibly to disturbances of the control unit of the converter being fed by the rectifier. In this paper a detailed discussion of the formation of the common-mode voltage for the VIENNA Rectifier I is given and a modified circuit topology which significantly reduces the switching frequency component of the common-mode voltage is given. The proposed circuit modification is applicable also to other three-phase PWM rectifier topologies. The filtering concept is analyzed by digital simulation and guidelines for the dimensioning of the filter components are given. The reduction of the common-mode noise is verified by EMI measurements taken from a 10kW laboratory unit of a VIENNA Rectifier I. Finally, the advantages and drawbacks of the proposed filtering concept compiled in form of an overview.

1 Introduction

Three-phase pulse width modulated (PWM) rectifier systems in principle show a common-mode voltage with switching frequency between the neutral point of the AC mains and the center point of the DC output voltage [1], [2] which leads to a high common-mode EMI (e.g., if the rectifier feeds a distributed load) and possibly to disturbances of the control circuit of a DC/DC converter fed by the output voltage of the PWM rectifier. Until now, only very limited attention has been paid to this problem and/or to possible counter-measures in the literature.

Therefore, in this paper the formation of the common-mode voltage should be discussed in detail for the VIENNA Rectifier I [3] and a simple modification of the power circuit resulting in a substantial reduction of the switching frequency common-mode voltage components should be proposed. The basic operating behavior of the VIENNA Rectifier I is discussed briefly in **section 2**. The split-up of the input voltage of the system into a differential-mode component and into a common-mode component which is not relevant concerning the current formation (no connection between mains star point and center point of the output voltage) is discussed in **section 3**. Both voltages components show a low-frequency and a switching-frequency component. The switching-frequency component of the common-mode voltage which causes the common-mode EMI noise can be significantly lowered if the center point of the DC output voltage of the rectifier is connected to a capacitively formed artificial mains neutral (star) point which will be demonstrated in **section 4** by digital simulation and in **section 5** by measurements taken from a 10kW laboratory prototype of a VIENNA Rectifier I. The low-frequency component of the common-mode voltage showing a fundamental frequency of $3f_N$ (f_N denotes the mains fundamental frequency) which guarantees a high utilization of the DC voltage and/or a high upper limit of the modulation index (cf. *third-harmonic injection* of PWM drives) remains unaffected. The total EMI noise is below the limit given by CISPR 11 (quasi-peak, class A/group 1) if, furthermore, also the heat sink is connected to the output voltage center point. Therefore, concerning the conducted EMI emission the system is applicable for industrial systems without any further filtering components.

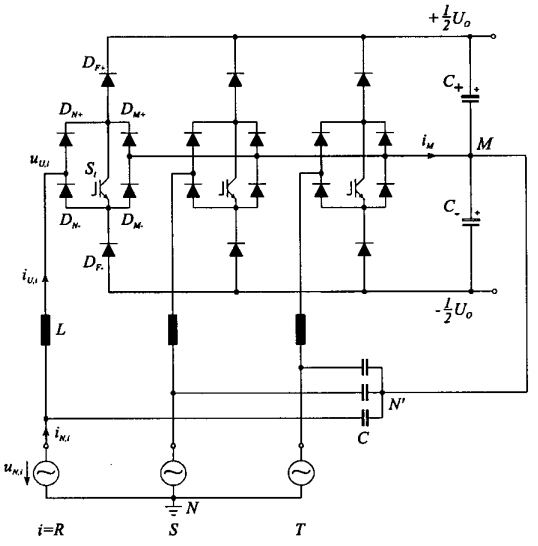

Fig.1: Modified basic structure of the VIENNA Rectifier I according to [7]. The connection of the output voltage center point M with the artificial mains star point N' (formed by capacitors C) results in a significant reduction of the voltage with pulse-frequency occurring between M and the actual mains star point N, which means the common-mode noise emission is reduced considerably (section 4).

2 Vienna Rectifier I

The basic structure of the VIENNA Rectifier I is shown in **Fig.1**. The technical and economic advantages of the system as compared to alternative rectifier concepts were analyzed in detail in [4] and [5]. The main advantages are

- only one turn-off power semiconductor per phase
- simple analogue control circuit
- three-level characteristic of the bridge legs resulting in
- low voltage stress on the power semiconductors
- low amplitudes of switching frequency harmonics of the input phase currents
- two controlled partial output voltages and/or high current handling capability of the output voltage center point in case of an asymmetric distribution of the load to the partial voltages [6]
- high reliability (no possibility of a short-circuit on the output voltage in case of control errors).

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2.1 Basic Operation

Employing pulse width modulation a three-phase voltage system $u_{U,i}$, $i = R, S, T$ is formed on the input side of the rectifier such that the difference to the mains voltages (which are assumed to show a purely sinusoidal shape) results in a voltage across the input inductors which results in a sinusoidal current consumption of the rectifier in phase with the mains voltage.

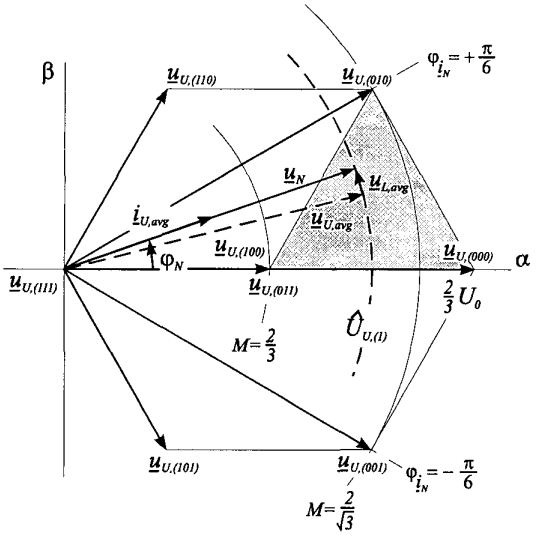


Fig.2: Input voltage space vectors $\underline{u}_{U,j}$ being available for forming of the reference rectifier input voltage $\underline{u}_{U,\mathrm{avg}}$ in the $\frac{\pi}{3}$-wide interval being characterized by $i_{U,R} > 0$, $i_{U,S}, i_{U,T} < 0$. Furthermore shown: Space vector diagram of the fundamentals of the rectifier input quantities; the fundamental $\underline{i}_{U,\mathrm{avg}}$ of the input current space vector is defined by the local average of the fundamental voltage drop $\underline{u}_{L,\mathrm{avg}}$ across the rectifier input inductors. In this paper, all considerations are related to the segment of the space vector plane which is pointed out by the dotted area.

The sign of a phase current defines the polarity of the corresponding phase voltage between input side of a bridge leg (in case of turned off power switch) and output voltage center point

$$u_{U,i} = \begin{cases} \frac{1}{2}U_O \mathrm{sign}(i_{U,i}) & \text{for} \quad s_i = 0 \\ 0 & \text{for} \quad s_i = 1. \end{cases} \tag{1}$$

Therefore, in each $\frac{\pi}{3}$-wide interval with a specific combination of signs of the three phase currents, only 8 different rectifier input voltage space vectors $\underline{u}_{U,j}$ are avaliable for current control (cf. **Fig.2**, there the converter switching state is denoted by the triple $j = (s_R s_S s_T)$ of the switching functions s_i of the phases i=R,S,T; $s_i = 1$ denotes the turn-on state of a power transistor S_i, $s_i = 0$ the turn-off state). For optimum approximation of a reference voltage space vector $\underline{u}_{U,\mathrm{avg}}$ which has to be formed in the average over a pulse half period (a local average value is denoted by the index 'avg') always the three input voltage vectors $\underline{u}_{U,j}$ lying in the immediate vicinity of the reference voltage vector are employed. For location of the tip of the reference voltage vector in the segment of the space vector plane which is pointed out in Fig.2 by the dotted area we, therefore, have as switching sequence

$$\begin{aligned} &|_{t_\mu=0}(100) - (000) - (001) - (011)|_{t_\mu=\frac{1}{2}T_P} - \\ &-(011) - (001) - (000) - (100)|_{t_\mu=T_P} \end{aligned} \tag{2}$$

(t_μ denotes the local time within the pulse period T_P). For the sake of clarity in the following all considerations are based on this switching sequence without impairing the general validity of the discussion.

3 Current-Forming Component and Zero-System of the Rectifier Input Voltage

In the following first the basis structure of the rectifier system [3] without connection of the output voltage center point M to the artifical mains star point N' shall be considered. Concerning the input currents we have in this case

$$i_{U,R} + i_{U,S} + i_{U,T} = 0 \tag{3}$$

which means that a voltage component u_0 (zero-system) being common to all three phase voltages $u_{U,i}$

$$\begin{aligned} u_{U,R} &= u'_{U,R} + u_0 \\ u_{U,S} &= u'_{U,S} + u_0 \\ u_{U,T} &= u'_{U,T} + u_0 \end{aligned} \tag{4}$$

(cf. **Fig. 3**(b)) does not take influence on the formation of the input phase currents $i_{U,i}$

$$L\frac{\mathrm{d}i_{U,i}}{\mathrm{d}t} = u_{N,i} - u'_{U,i} \tag{5}$$

(the voltages $u'_{U,i}$ and u_0 usually are denominated as *differential-mode* and *common-mode* component of the input voltage).

Remark: The transformation of the phase voltage triple $u_{U,i}$ into a voltage space vector

$$\underline{u}_U = \frac{2}{3}(u_{U,R} + \underline{a}u_{U,S} + \underline{a}^2 u_{U,T}) \qquad \underline{a} = \exp j\frac{2\pi}{3} \tag{6}$$

according to

$$\frac{2}{3}(1 + \underline{a} + \underline{a}^2)u_0 = 0 \tag{7}$$

decouples a zero system u_0, i.e., the space vector is only defined by the phase voltage $u'_{U,i}$ without zero-component

$$\underline{u}_{U,j} = \underline{u}'_{U,j} \tag{8}$$

and is, therefore, independent of the choice of the reference potential for measuring the phase voltages $u_{U,i}$. This is one of the major advantages of the space vector calculus for analyzing three-phase systems.

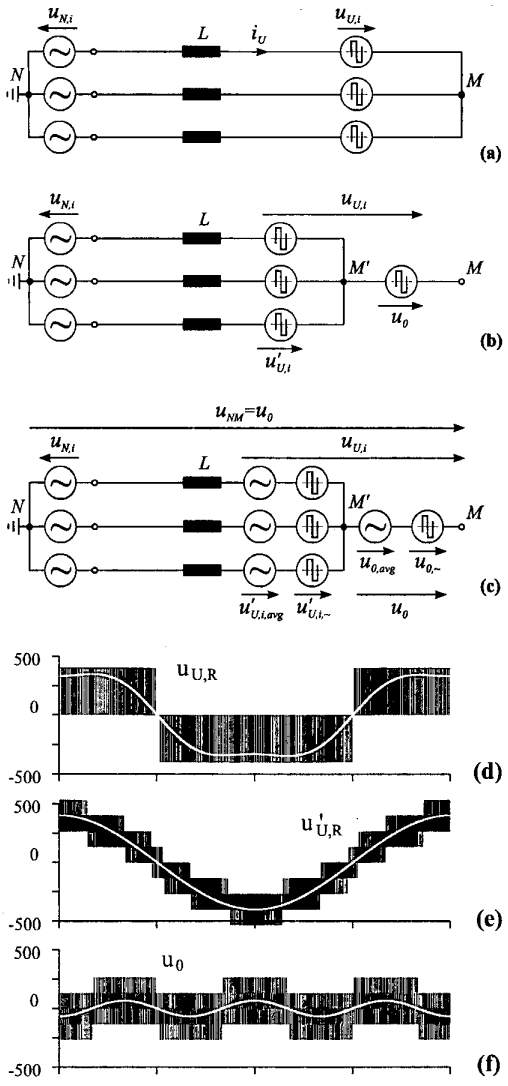
In case of defining M as reference potential of the input phase voltages $u_{U,i}$ within one pulse period (Eq.(2)) the values of $u_{U,i}$, $u'_{U,i}$ and u_0 as given in **Table 1** will occur within a pulse half period.

s_j	$u_{U,R}$	$u_{U,S}$	$u_{U,T}$	$u'_{U,R}$	$u'_{U,S}$	$u'_{U,T}$	u_0
(100)	0	$-\frac{U_0}{2}$	$-\frac{U_0}{2}$	$\frac{U_0}{3}$	$-\frac{U_0}{6}$	$-\frac{U_0}{6}$	$-\frac{U_0}{3}$
(000)	$\frac{U_0}{2}$	$-\frac{U_0}{2}$	$-\frac{U_0}{2}$	$\frac{2U_0}{3}$	$-\frac{U_0}{3}$	$-\frac{U_0}{3}$	$-\frac{U_0}{6}$
(010)	$\frac{U_0}{2}$	0	$-\frac{U_0}{2}$	$\frac{U_0}{2}$	0	$-\frac{U_0}{2}$	0
(011)	$\frac{U_0}{2}$	0	0	$\frac{U_0}{3}$	$-\frac{U_0}{6}$	$\frac{U_0}{6}$	$\frac{U_0}{6}$

Tab.1: Split-up of the rectifier input phase voltages $u_{U,i}$ occurring within a pulse half interval in the shaded area of Fig.2 into a zero-system u_0 and a voltage system $u'_{U,i}$ being free of zero-quantities.

According to Tab.1 u_0 shows discontinuous time-behavior within one pulse period and in general a local average value (referred to a half pulse period $\frac{1}{2}T_P$)

$$u_{0,\mathrm{avg}} = \frac{2}{T_P}\int_{\frac{1}{2}T_P} u_0 \,\mathrm{d}t_\mu \tag{9}$$



i.e., u_0 shows low frequency harmonics

$$u_0 = u_{0,\mathrm{avg}} + u_{0,\sim}\,; \tag{10}$$

$u_{0,\sim}$ denotes the pulse-frequency components of u_0. Tab.1 also clearly shows the redundancy of the switching states (100) and (011) concerning the formation of the input phase voltages $u'_{U,i}$. This redundancy of the two switching states can also be seen in Fig.2 by the identity of the two associated voltage space vectors $u_{U,(100)} = u_{U,(011)}$ which can be used for active control of the symmetry of the partial output voltages as described in [3].

In order to achieve a sinusoidal shape of the local average value $i_{U,i,\mathrm{avg}}$ of a phase current $i_{U,i}$ being in phase with the associated mains phase voltage $u_{N,i}$ (ohmic fundamental mains behavior),

$$\begin{aligned} i_{U,R,\mathrm{avg}} &= \hat{I}_N \cos(\varphi_N) \\ i_{U,S,\mathrm{avg}} &= \hat{I}_N \cos(\varphi_N - \tfrac{2\pi}{3}) \\ i_{U,T,\mathrm{avg}} &= \hat{I}_N \cos(\varphi_N + \tfrac{2\pi}{3}) \end{aligned} \tag{11}$$

at the input side of a bridge leg of the rectifier system a local average voltage (fundamental) of the voltage $u'_{U,i}$ according to

$$u_{U,i,\mathrm{avg}} = u_{N,i} - L\frac{\mathrm{d}i_{U,i,\mathrm{avg}}}{\mathrm{d}t} \tag{12}$$

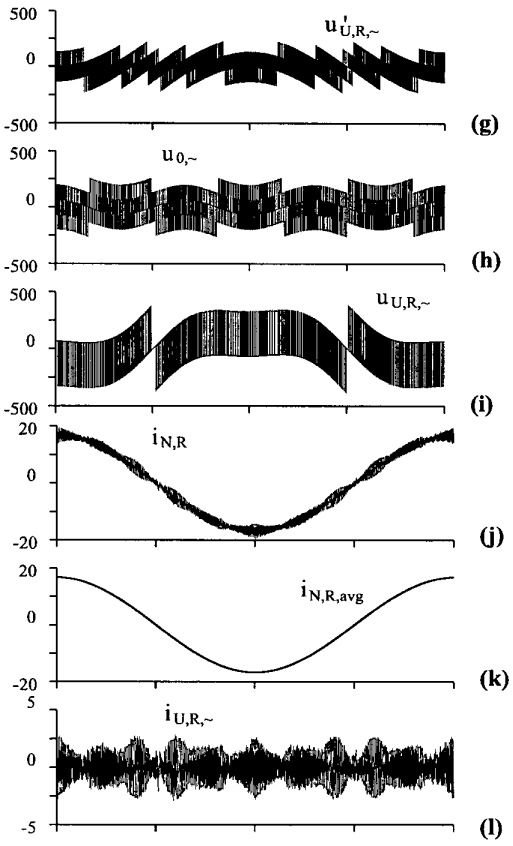


Fig.3: Systematic split-up of the rectifier input phase voltages into a zero-system-free voltage system $u'_{U,i}$ and a zero-system u_0 (cf. **(b)**; the equivalent circuit shown in **(c)** can be derived by further splitting up these voltage components into low-frequency, e.g., mains frequency components (indicated by the index 'avg') and pulse-frequency components (indicated by the index '$\sim$'), $u'_{U,i} = u_{U,i,\mathrm{avg}} + u'_{U,i,\sim}$ and $u_0 = u_{0,\mathrm{avg}} + u_{0,\sim}$. Furthermore shown: simulated time-behavior of the voltage components and of related current components for phase R within one mains period; **(d)**: rectifier input voltage $u_{U,R}$ and low-frequency component $u_{U,R,\mathrm{avg}}$ (referred to M); **(e)**: current-forming component $u'_{U,R}$ of $u_{U,R}$ and low-frequency component $u'_{U,R,\mathrm{avg}}$ (referred to M'); **(f)**: zero-component u_0 of the phase voltage system $u_{U,i}$ and low-frequency component $u_{0,\mathrm{avg}}$; **(g)**: pulse-frequency component $u'_{U,R,\sim}$ of $u'_{U,R}$ defining the ripple $i_{U,R,\sim}$ of the input current $i_{U,R}$; **(h)**: pulse-frequency component $u_{0,\sim}$ of u_0 creating the capacitive earth leakage current; **(i)**: pulse-frequency component $u_{U,R,\sim}$ of $u_{U,R}$ (this voltage component would define the input current ripple in case of a direct connection of M to N (Eq.(26))); **(j)**: time-behavior of the input current $i_{U,R}$; **(k)**: low-frequency component (fundamental) $i_{U,R,\mathrm{avg}}$ of $i_{U,R}$; **(l)**: ripple (pulse-frequency component) $i_{U,R,\sim}$ of $i_{U,R}$; A compilation of the simulation parameters is given in section 4.3.

has to be formed. In case of high pulse frequencies $f_P = \frac{1}{T_P}$ (as compared to the mains frequency f_N) and/or small inductance of the input inductors L the fundamental voltage drop $u_{L,i,\mathrm{avg}} = L\mathrm{d}i_{U,i,\mathrm{avg}}/\mathrm{d}t$ on the rectifier input inductance can be neglected as compared to the mains voltage in good approximation. Therefore, we have in a first approximation independent of the load condition

$$u_{U,i,\mathrm{avg}} \approx u_{N,i} \tag{13}$$

and/or

$$\underline{u}_{U,\mathrm{avg}} = \frac{1}{T_P}\int_{T_P} \underline{u}_{U,j}\mathrm{d}t_\mu \approx \underline{u}_N \tag{14}$$

(cf. Fig.2). As immediately obvious the ripple $i_{U,i,\sim}$ of the phase currents

$$i_{U,i} = i_{U,i,\mathrm{avg}} + i_{U,i,\sim} \tag{15}$$

is defined via the difference

$$u'_{U,i,\sim} = u'_{U,i} - u'_{U,i,\mathrm{avg}} \tag{16}$$

of the pulse frequency discontinuous (actual) rectifier input voltage $u'_{U,i}$ and the continuous (ideally purely sinusoidal) reference voltage $u'_{U,i,\mathrm{avg}}$

$$L\frac{\mathrm{d}i_{U,i,\sim}}{\mathrm{d}t} = -u'_{U,i,\sim}\ . \tag{17}$$

By describing the voltage formation by space vector calculus, $u_{U,i,\sim}$ is the vector difference between the actual voltage space vector $\underline{u}_{U,j}$ and the space vector $\underline{u}'_{U,\mathrm{avg}}$ of the reference rectifier input voltage fundamental.

Because of the redundancy of the switching states (100) and (011) only the sum of the local relative on-times $\delta_{(100)} + \delta_{(011)}$ can be calculated based on Eqs.(2) and (14). The distribution

$$\rho_{--} = \delta_{(100)}/\delta_{(100)} + \delta_{(011)} \tag{18}$$

of this sum of the on-times of the switching states (100) and (011) constitutes a degree of freedom for optimizing the input-side or the output-side system behavior (the distribution ρ_{--} does not only take influence on the input current ripple $i_{U,i,\sim}$ but also on the shape of the center point current i_M and/or the low-frequency harmonics of i_M [8]).

Instead no optimization but only a maximum utilization of the output voltage for forming the rectifier input voltage is aimed for, the distribution of the redundant switching states ρ_{--} has to be defined according to

$$u_{0,\mathrm{avg}} \approx -\frac{1}{6}\hat{U}_U\cos(3\varphi_N) \tag{19}$$

($\hat{U}_U \approx \hat{U}_N$ denotes the amplitude of the fundamental of the phase voltage $u'_{U,i,\mathrm{avg}}$); e.g., we have for the switching sequence of Eq.(2)

$$u_{0,\mathrm{avg}} = \frac{1}{6}U_O(\delta_{(100)} + \delta_{(011)}) = [1 - 3\rho_{--} - \frac{\delta_{(000)}}{(\delta_{(100)} + \delta_{(011)})}] \tag{20}$$

(cf. Eq.(9)). The third harmonic does not directly influence the input current formation (i.e., it only takes influence on the shape of the current ripple $i_{U,i,\sim}$ but not on the current fundamental $i_{U,i,\mathrm{avg}}$) but lowers the low frequency component of the input phase voltage $u_{U,i,\mathrm{avg}} = u'_{U,i,\mathrm{avg}} + u_{0,\mathrm{avg}}$ in the vicinity of the maximum of the fundamental $u'_{U,i,\mathrm{avg}}$ (cf. Fig.3(d)). This results in a modulation range

$$M = \frac{\hat{U}_U}{\frac{1}{2}U_O} = 0\ldots\frac{2}{\sqrt{3}} \tag{21}$$

In contrast, simple sinusoidal modulation is characterized by $u_{0,\mathrm{avg}} = 0$ and/or by $M = 0\ldots1$.

In summary, the rectifier input voltage $u_{U,i}$ of each phase i can be divided into a current-forming voltage-system $u'_{U,i} = u'_{U,i,\mathrm{avg}} + u'_{U,i,\sim}$ and a not (directly) current-forming component u_0. The voltage fundamentals $u'_{U,i,\mathrm{avg}}$ and $u_{N,i}$ define the mains current fundamental $i_{N,i,\mathrm{avg}}$, the voltage $u'_{U,i,\sim}$ with pulse frequency defines the input current ripple $i_{U,i,\sim}$.

The low-frequency component $u_{0,\mathrm{avg}}$ of u_0 can be defined via the distribution ρ_{--} of the redundant switching states between beginning and end of one pulse half period. In the most simple case this distribution can be used to guarantee the maximum width of the modulation range (Eq.(19)). A change of ρ_{--} will influence $u'_{U,i,\sim}$ and, therefore, also the input current ripple $i_{U,i,\sim}$. This clearly shows the possibility of an optimization of the system behavior (e.g., in form of a minimization of the rms-value of the input current ripple [8]). In this case one has to note that the resulting optimized distribution ρ_{--} and/or voltage u_0 possibly does not guarantee $u_{U,i,\mathrm{avg}} \leq \frac{1}{2}U_O$ in the upper modulation region, i.e. a maximum modulation index $M < \frac{2}{\sqrt{3}}$ could result as a consequence of the optimization [8].

Remark: The voltage u_0 clearly describes the mutual influence of the phases and, therefore, helps to understand the behavior of independent tolerance band phase current controllers in three-phase systems. Switching of one phase influences via u_0 also the time-behavior of the currents of the other phases. Furthermore, a maximum current error of two times the width of the tolerance band can occur because, although, e.g., the phase with a current leaving the upper tolerance band is switched, a voltage $u'_{U,i}$ further increasing the absolute value of the current could remain until another phase changes its switching state. On the other hand, u_0 gives the possibility to guide the current of one phase inside the tolerance band by only switching the other phases (clamping of one phase). This guarantees high input current quality with relatively low average switching frequency of the converter.

3.1 Common-Mode Shift of the Rectifier Output Voltage

In the previous section it has been shown that for three-phase PWM rectifier systems advantageously the width of the modulation range can be maximized and/or the system behavior can be optimized by appropriate definition of the low-frequency component $u_{0,\mathrm{avg}}$ of the zero-component u_0 of the rectifier input phase voltages $u_{U,i}$.

However, on the other hand the unavoidable voltage component u_0 physically constitutes a potential shift of the center point M with reference to grounded mains star point N (cf. Figs.3(b) and (f))

$$u_{MN} = u_0 \tag{22}$$

(N shows no potential difference to the star point M' of the voltage system $u'_{U,i}$). Therefore, at each change of the switching state of the rectifier system a steep change of the level of this common-mode voltage will occur and/or because of parasitic earth capacitances of the output capacitors, the output voltage rails and the load relatively high common-mode currents will result. These currents could cause malfunctions of the control circuit of the load (e.g., a DC/DC converter) or neighboring systems and, therefore, must be attenuated accordingly by an EMI filter circuit.

Remark: Three-phase PWM inverter systems for feeding AC-machines show (analogous to u_0) a high-frequency potential shift of the star point of the stator winding system with reference to the center point of the DC link voltage of the feeding inverter. As a result the systems are emitting wide-band common-mode noise. Furthermore, capacitive earth currents could activate fault monitoring systems, and fault currents could destroy the races of the bearings of the machine.

Concerning the filtering of the common-mode effects one has to point out a basic difference between PWM inverter systems and PWM rectifier systems. In case of inverter systems the AC side inductances defining the ripple of the AC currents are the leakage inductances and therefore not explicitly accessible, i.e., no filter capacitors can be connected to the motor-side side of the inductances. For suppression of the potential shift of the stator windings star point, therefore, an explicit (common-mode) filter inductance is required. Concerning a description of different filter concepts, which can be employed in analogous

form also for PWM rectifier systems, we would like to refer to [9] for the sake of brevity.

4 Suppression of the Common-Mode Shift of the Output Voltage

To suppress a potential shift of the center point M at the output side of the rectifier system referring to the mains star point N and/or the occurrence of a common-mode voltage the idea of directly connecting M and N, i.e., of connecting M with the mains neutral is near at hand.

However, the basic problem of a practical realization of this simple concept is the use of three-wire systems without neutral wire for supplying three-phase PWM rectifier systems in order to minimize the realization effort. A further disadvantage is the limitation of the modulation range to $M = 0 \ldots 1$ as a result of a direct connection of M and N. The rectifier input inductors L show very small impedance values according to their small inductance for three-times the mains frequency. Therefore, a direct connection of M and N is equivalent to short-circuiting the voltage $u_{0,\mathrm{avg}}$ (cf. Eq.(19) and **Fig.4**) across the inductors L, which would result in high zero-sequence currents. Therefore, $u_{0,\mathrm{avg}} = 0$ and/or a pure sinusoidal modulation has to be used in this case and/or for application of the rectifier system in the European low voltage mains ($400\mathrm{V_{rms}} \pm 10\%$ line-to-line) a minimum output voltage of $U_O = 750\mathrm{V}$ (according to $M = 0.95$) has to be set. On contrary, in case of no connection between M and N ($M \leq \frac{2}{\sqrt{3}}$) an operation of the system is possible for a minimum output voltage of $U_O = 650\mathrm{V}$ (according to $M = 1.1$). Therefore, as a consequence of the limitation to $M < 1.0$ the voltage stress on the power semiconductors is increased, and because of the higher turn-off voltage of the power semiconductors the rectifier systems shows higher switching losses.

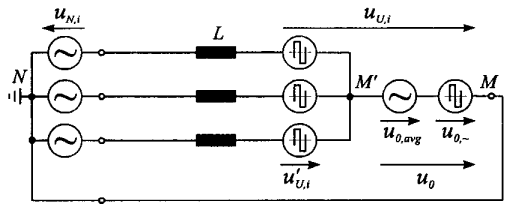


Fig.4: AC-side equivalent circuit of the VIENNA Rectifier I for direct connection between N and M.

Remark: If for the formation of the rectifier input voltage only zero-component-free switching states would be employed (switching states (111), (001), and (010) in the $\frac{\pi}{3}$-wide interval according to Fig.2), e.g., using the switching sequence (111) – (001) – (011), theoretically $u_0 = 0$ could be achieved without physical connection between M and N. (A similar concept for avoiding pulse-frequency changes of u_0 was described in [10] for three-phase two-level PWM *inverter* systems.) However, as a more detailed analysis shows also in this case the degree of modulation is limited to $M = 0 \ldots 1$. Furthermore, the mains current can be guided only in phase with the fundamental of the rectifier input voltage, but not in phase with the mains voltage, and shows a significantly increased ripple as compared to a system without connection between M and N employing the same pulse frequency.

However, the main disadvantage of this concept is the problem that pulse-frequency components of u_0 can be avoided only for ideally synchronized switching of always two bridge legs (e.g., for the switching from state (111) to state (001)). Because of small differences in the delay times of the gate drive circuits and of the switching times of the power semiconductors in a practical realization interim switching states will occur (e.g., the interim switching state (011), being characterized by $u_0 = +\frac{1}{6}U_O$, cf. Tab.1)). Therefore, a reduction of the amplitudes of the harmonics of the common-mode voltage is restricted to relatively low frequencies (in the range of first multiples of the switching frequency). The influence on the high-frequency amplitudes which are defined by the slope of the changes of the parasitically occurring common-mode voltage spikes is neglectable.

4.1 Connection of the Center Point with a Capacitive Artifical Mains Star Point

In order to avoid pulse-frequency ripple currents in the mains in case of a connection between M and N it would be necessary to provide filter capacitors at the rectifier input side between the neutral and the rectifier input terminals. Therefore, it is near at hand to try to reduce the common-mode shift of the output voltage by connecting the center point M to an artificial mains star point N' being formed by these capacitors and to omit the connection of N' to the neutral ([7], cf. Fig.1). A similar concept has been described in [11] and [12] for a PWM inverter system and in [2] for a conventional PWM rectifier system.

The equivalent circuit of the resulting system is shown in **Fig.5**(a). The remaining common-mode voltage $u_{MN} = u_{N'N}$ is ideally the zero-voltage $U_0(j\omega)$ weighted with respect to frequency according to the frequency response of the low-pass filter formed by the rectifier input inductances L and the capacitors C,

$$U_{MN}(j\omega) = \frac{1}{1 - (\frac{\omega}{\omega_0})^2} U_0(j\omega) \qquad \omega_0 = \frac{1}{\sqrt{LC}} \tag{23}$$

If the corner frequency ω_0 is set sufficiently lower than the switching frequency f_P then the pulse-frequency harmonics $U_{0,\sim}(j\omega)$ of $U_0(j\omega)$ that are critical concerning the common-mode noise emission are suppressed in the common-mode voltage $U_{MN}(j\omega)$ (see also Fig.3(f) and **Fig.6**(b)). Only the low-frequency component $U_{0,\mathrm{avg}}(j\omega)$ of $U_0(j\omega)$ remains in a first approximation unchanged as component of the voltage across the capacitors C (cf. Fig.6(a)). This low-frequency component results for $u_{0,\mathrm{avg}}$ according to Eq.(19) in a capacitor current with three-times the mains frequency and an amplitude

$$\hat{I}_{0,\mathrm{avg}} \approx \frac{1}{2}\hat{U}_N \omega_N C \,. \tag{24}$$

(cf. Fig.6(d)) where ω_N denotes the circular frequency of the mains. Under the simplified assumption of an ideal short-circuit of the switching-frequency voltage component $u_{0,\sim}$ of u_0 by the capacitors C, the ripple component $i_{0,\sim}$ of the currents $i_{U,i}$ resulting from $u_{0,\sim}$ can be calculated via

$$L\frac{\mathrm{d}i_{0,\sim}}{\mathrm{d}t} \approx -u_{0,\sim} \tag{25}$$

The total ripple of the current in the rectifier input inductance L, $i_{U,i,\sim} = i'_{U,i,\sim} + i_{0,\sim}$, is therefore defined by

$$-u_{U,i,\sim} = -(u'_{U,i,\sim} + u_{0,\sim}) \,, \tag{26}$$

i.e., by the total switching-frequency component of the rectifier input phase voltage $u_{U,i}$ referred to M (cf. Fig.3(i) and Figs.6(f) and (g)) and not only by $u'_{U,i,\sim}$, as in the case of not connected (free) output voltage center point (cf. Eq.(17)). On the contrary, in case of neglectable inner impedance of the mains the mains current ripple $i_{N,i,\sim}$ is ideally *not* influenced by the capacitors C and the connection between N' and M and/or its time-behavior

$$i_{N,i,\sim} = i'_{U,i,\sim} \tag{27}$$

is still defined by $u'_{U,i,\sim}$ (Fig.3(j) and Fig.6(e)), i.e., remains unchanged with exception of the vicinity of the zero-crossings of the phase currents (cf. Fig.6(a)). Besides the components $i_{0,\text{avg}}$ and $i_{0,\sim}$ the current in the capacitors C shows a further current component which is defined by the mains voltage

$$i_{C,1,i} = -C\frac{\mathrm{d}u_{N,i}}{\mathrm{d}t} \tag{28}$$

Therefore, we have for the total value of the capacitor current

$$i_{C,i} = i_{C,1,i} + i_{0,\text{avg}} + i_{0,\sim}. \tag{29}$$

It is important to point out that according to Eq.(24), contrary to the above described direct connection between N and M, the zero-current $i_{0,\text{avg}}$ resulting from a third harmonic $u_{0,\text{avg}}$ is reduced to small values because of a small inductance value C. Therefore, besides a significant reduction of the amplitudes of the pulse-frequency components of the common-mode voltage it is possible to gain the same modulation range $M = 0 \ldots \frac{2}{\sqrt{3}} \approx 1.15$ as given in case of not connected center point M.

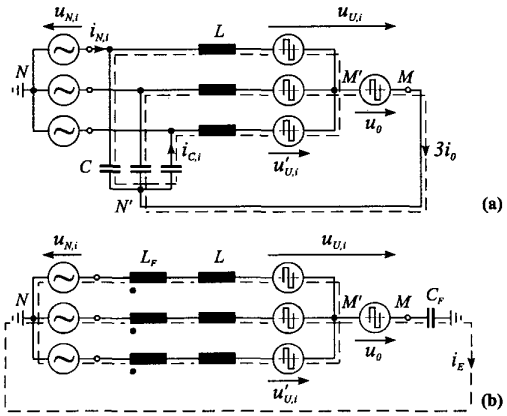


Fig.5: Equivalent circuit of the system according to Fig.1 **(a)** and conventional common-mode filtering **(b)**, which is realized in the most simple way by a capacitor C_F connecting M to ground (earth) and a three-phase common-mode inductor L_F connected in series with the rectifier input inductances L. Paths of capacitive leakage currents as caused by u_0 are shown by broken lines.

As compared to conventional common-mode filtering (Fig.5(b)) a main difference of the above described concept is that the return path of the current i_0 (caused by u_0) is not via earth but via the center point M (cf. Fig.5). Therefore, the capacitance of the filter capacitors C is not limited by standards defining a maximum allowable leakage current. Also, as already mentioned, the ripple component $i_{0,\sim}$ (as caused by $u_{0,\sim}$) of the currents $i_{U,i}$ does not occur in the mains. Therefore, one does not have to employ an explicit common-mode filter inductance. If, considering the turn-off current of the power transistors or the losses of the rectifier input inductances, a limitation of $i_{0,\sim}$ is necessary, the inductance of the inductors L can simply be increased instead of using a common-mode inductance which is difficult to manufacture. This also results in further reduction of the mains current ripple $i_{N,i,\sim} = i'_{U,i,\sim}$. Opposed to this, for common-mode filtering according to Fig.5(b) a common-mode inductance L_F is required in any case because of the rather small capacitance of the capacitor C permitted under consideration of the occurring earth leakage current.

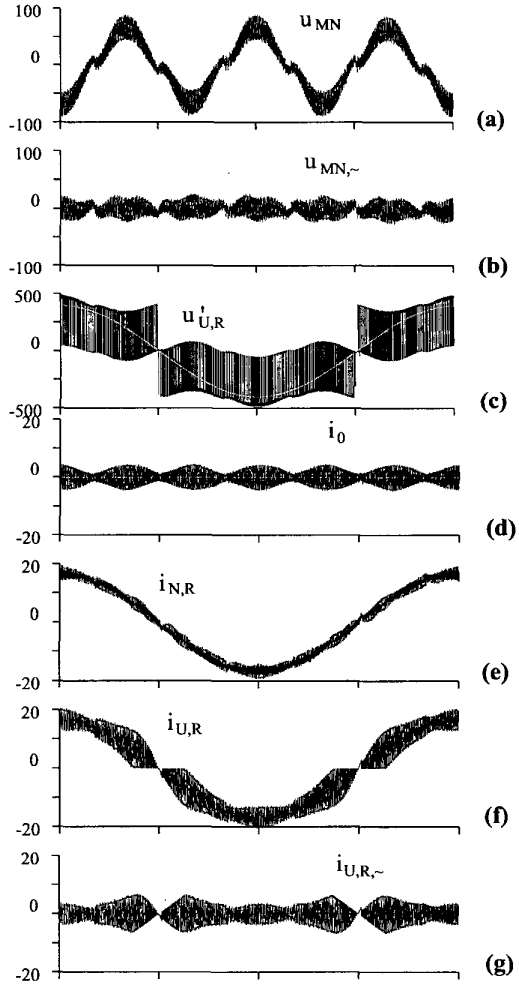


Fig.6: Simulated time-behavior of characteristic voltages and currents within one mains pepiod in case of connecting M and N'. **(a):** remaining common-mode voltage u_{NM}; **(b):** switching-frequency component $u_{MN,\sim}$ of u_{MN}; **(c):** rectifier inputvoltage $u'_{U,R}$ and fundamental $u_{U,R,\text{avg}}$ **(d):**zero-current i_0 and low-frequency component $i_{0,\text{avg}}$ (cf. Eq.(24)); **(e):** mains current $i_{N,R}$; **(f):** rectifier input current $i_{U,R}$; **(g):** ripple $i_{U,R,\sim}$ of the rectifier input current $i_{U,R}$. The simulation parameter are compiled in section 4.3.

4.2 Dimensioning of the Capacitors for Forming the Artificial Mains Star Point

With regard to the stress on the power semiconductors and on the passives components the value of the filter capacitor C has to be chosen in a way that the third harmonic for increasing the degree of modulation referring to sinusoidal modulation (cf. Eq.(19)) results in a zero-current $\hat{I}_{0,\text{avg}}$ that is small as compared to the input current fundamental $\hat{I}_N$ (for rated load)

$$C < \frac{2\hat{I}_{0,\text{avg}}}{\hat{U}_N \omega_N}. \tag{30}$$

Furthermore, it has to be considered that there is a phase shift between the zero-crossing of the voltage $u'_{U,\text{avg}}$ (that has to be formed) and the total input phase current because of the current component $i_{0,\text{avg}}$ (cf. **Fig.7**) that is phase-shifted by 90° to the voltage $u_{0,\text{avg}}$. This results in time-intervals with negative input current $i_{U,i}$ of a bridge leg with the need for positive rectifier input voltage $u_{U,i}$ and/or $u_{U,i,\text{avg}}$ (and vice

versa). The dependency of the voltage formation of the rectifier system from the sign of the input phase current (Eq.(1)) causes distortion of the voltage zero-component u_0 within that time-interval (cf. Fig.6(a)). In order to maintain the maximum degree of modulation $M \approx 1.15$ this distortion has to be limited to small values.

The time-interval of the distortion is given in a first approximation (neglecting the ripple of the input current) by

$$\Delta = \frac{1}{9}\left(\sqrt{\left(\frac{\hat{I}_N}{\hat{I}_{0,\mathrm{avg}}}\right)^2 + 18} - \frac{\hat{I}_N}{\hat{I}_{0,\mathrm{avg}}}\right) . \qquad (31)$$

This time-interval increases with decreasing fundamental amplitude $\hat{I}_U \approx \hat{I}_N$ and increasing capacitance C. The permitted value of the capacitance is found via Eq.(31) and Eq.(24) for a given time-interval $\Delta_{\max}$ under the assumption of minimum input power and/or $\hat{I}_{N,\min}$ by

$$C < \frac{2\hat{I}_{N,\min}}{\omega_N \hat{U}_N\left(\frac{1}{\Delta_{\max}} - \frac{9}{2}\Delta\right)} . \qquad (32)$$

Keeping the above defined limits for C (Eq.(30) and Eq.(32)) results in a sufficient attenuation of the zero-voltage (cf. Eq.(23)).

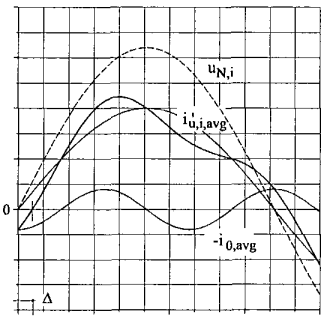


Fig.7: Time-behavior of a mains phase voltage $u_{N,i} \approx u'_{U,i,\mathrm{avg}}$, according input current fundamental $i'_{U,i,\mathrm{avg}}$ and the input current component $-i_{0,\mathrm{avg}}$ (cf. Fig.5(a)) (resulting ideally from $u_{0,\mathrm{avg}}$). Within angular intervals of the width Δ the low-frequency component $i'_{U,i,\mathrm{avg}} - i_{0,\mathrm{avg}}$ of the input current and the voltage $u'_{U,i,\mathrm{avg}} + u_{0,\mathrm{avg}}$ that has to be formed at the input side of a bridge leg show different signs. This results in a distortion of the ideal time-behavior of $u_{0,\mathrm{avg}}$ (cf. Fig.6(a)).

To avoid resonance (for example by load variations) of the circuit formed by the rectifier input inductances L and the capacitors C in the simplest way a series resistor $R_D > 2\sqrt{\frac{L}{C}}$ can be employed. To improve the damping of high frequencies a parallel capacitor C_D is used (cf. **Fig.8**(a)). The cut-off frequency is typically $\frac{1}{R_D C_D} > 3\frac{1}{\sqrt{LC}}$. Alternatively, parallel to C a RLC-series connection can be employed [12]. Using a $R_D C_D$-damping circuit ($C_D \gg C$) in parallel to C is not recommendable in this application due to the resulting significant increase of the capacitive component of the current $i_{U,i}$.

For high frequencies $f > 0.5 \ldots 1.0$MHz the filter characteristics are strongly influenced by parasitic properties of the components (for example, stray capacitances C_S of the rectifier input inductances L and parasitic inductance L_S of the filter capacitors). For $\omega_1 = \frac{1}{\sqrt{LC_S}}$ a parallel resonance occurs in the series path of the filter, and for $\omega_2 \approx \frac{1}{\sqrt{L_S C}}$ a series resonance in the parallel path of the filter (equivalent to a pole of the attenuation $A(j\omega) = U_0(j\omega)/U_{MN}(j\omega)$ of the zero-voltage). For

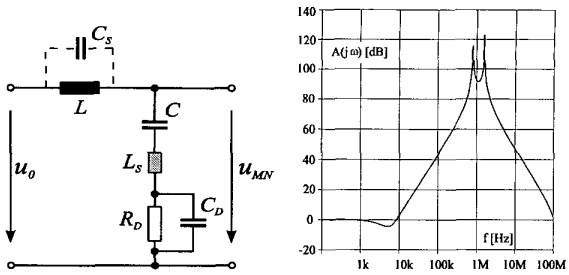


Fig.8: Equivalent circuit **(a)** and frequency response **(b)** of the attenuation $A(j\omega)$ of the common-mode filter under consideration of the damping circuit R_D, C_D, the parasitic capacitor C_S of the rectifier input inductance L , and the equivalent series inductance L_S of the filter capacitor C. Parameters: $L = 700\mu$H, $C = 2\mu$F, $R_D = 30\Omega$, $C_D = 0.2\mu$F, $C_S = 70$pF, $L_S = 15$nH (L_S and C_S have been measured).

frequencies $\omega > \omega_2$ the attenuation decreases for increased frequency, the filter characteristic is defined by L_S andC_S. Then, the filter shows high-pass characteristic and not longer low-pass characteristic. Therefore, for mechanical arrangement of the filter capacitors inside the converter it is important to minimize the length of the connection wires of the filter circuits between phases and center point M (minimization of L_S).

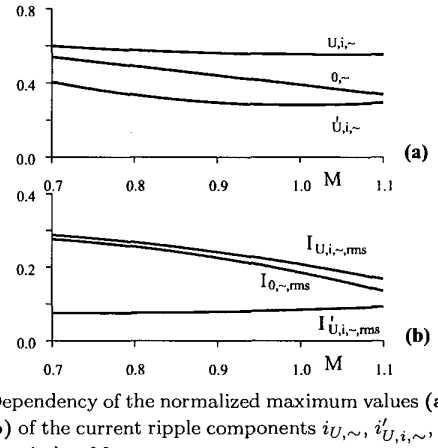


Fig.9: Dependency of the normalized maximum values **(a)** and rms-values **(b)** of the current ripple components $i_{U,\sim}$, $i'_{U,i,\sim}$, $i_{0,\sim}$ on the modulation index M.

4.3 Influence of the Filter Capacitors on the Component Stress

Compared to a system without connected center point M there results an increase of the ripple $i_{U,i,\sim}$ of the input current $i_{U,i}$ for the circuit according to Fig.1. To consider this increase in a simple way for dimensioning, **Fig.9** shows the maximum value and the rms-value (during one mains period) of the total ripple $i_{U,i,\sim}$ and the ripple components $i'_{U,i,\sim} = i_{N,i,\sim}$ and $i_{0,\sim}$ in normalized form in dependency of the modulation index. The normalization factor

$$I_r = \frac{U_O T_P}{8L} \qquad (33)$$

is equal to the maximum value of the current ripple in an inductance L for applying a symmetric rectangular signal (duty cycle 0.5) with the frequency f_P.

For dimensioning the filter capacitor C concerning the current stress one can assume the rms-value $I_{0,\sim,\mathrm{rms}}$ neglecting $i_{0,\mathrm{avg}}$ and $i_{C,1,N}$ in a first approximation.

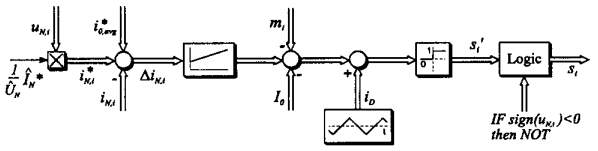


Fig.10: Structure of the current controller. The coding $s_i' \rightarrow s_i$ considers the dependency of the voltage formation of one bridge leg on the sign of the input current. Employing instead of one carrier signal i_D for the phase current control three carrier signals with 120° phase shift between each other, results in a significant reduction of the pulse-frequency component $u_{0,\sim}$ of u_0 and therefore also $i_{0,\sim}$ and/or u_{MN}. But this increases the differential-mode component $u'_{U,i,\sim}$ of the input phase voltages, so that besides the ripple of $i_{U,i}$ also the ripple of the mains current is increased.

The calculation of the characteristic parameters is done by digital simulation using the following parameters being typical for a practical realization:

$$\begin{aligned} P_O &= 10\text{kW} \\ U_O &= 800\text{V} \\ L &= 500\mu\text{H} \\ C &= 2\mu\text{F} \\ U_{N,\text{rms}} &= 200\ldots310\text{V}(M=0.7\ldots1.1) \\ f_P &= 16\text{kHz} \end{aligned}$$

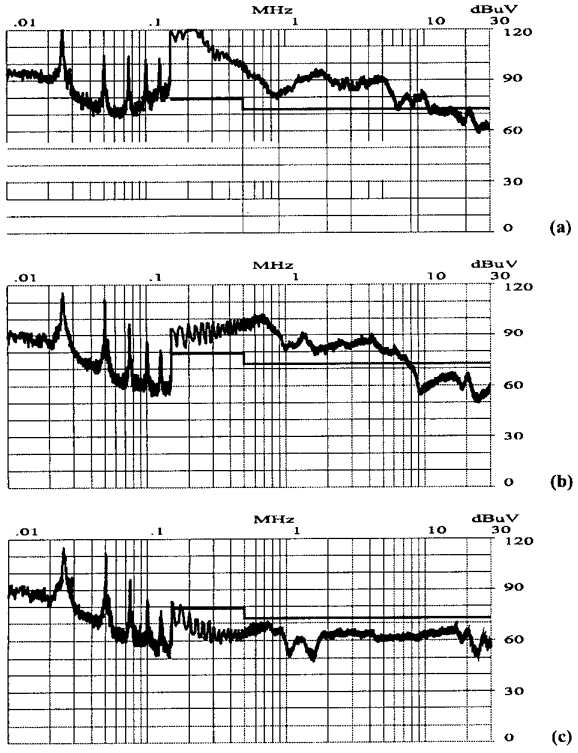


Fig.11: Results of the EMI measurement according to CISPR 11 with and without connection of M to the capacitively formed artificial mains star point N'. **(a):** without connection M to N', heat sink connected to ground (earth); **(b):** M connected to N', heat sink connected to ground; **(c):** center point M and heat sink connected to N'.

The input current control is implemented in form of a ramp-comparison PI-type current controller (**Fig.10**). The pre-control signal m_i of the mains voltage $u_{N,i}$ includes a third harmonic according to Eq.(19) to guarantee a maximum degree of modulation. For sake of simplicity the output voltage is realized as an ideal voltage source. (In a practical realization the control of the balancing of the partial output voltages can be achieved by an offset I_0 to the reference phase currents as described in [3]). The reference value of the current control is formed by adding the fundamental current $i_{N,i,\text{avg}}$ (defining the output power) to the zero-current $i_{0,\text{avg}}$ that is needed to change the voltages of the capacitors C with triple mains frequency (formation of $u_{0,\text{avg}}$).

Remark: The simulation shows that the pre-control signal of $u_{0,\text{avg}}$ (third harmonic of m_i) can be removed without causing serious low-frequency distortion of the mains current for $M > 1$. In that case the formation of the zero-voltage component necessary for increasing the degree of modulation is performed directly by the I-type component of the phase current controller.

As demonstrated by the simulation the current ripple component $i_{0,\sim}$ caused by $u_{0,\sim}$ shows a maximum value always at a maximum of a mains phase voltage (cf. Fig.6(d)). An analytical calculation results in good agreement with the simulation in

$$\hat{I}_{0,\sim} = \frac{2}{3}(1-\frac{2}{3}M)(1+\frac{M}{2})\frac{U_O T_P}{8L} \ . \qquad (34)$$

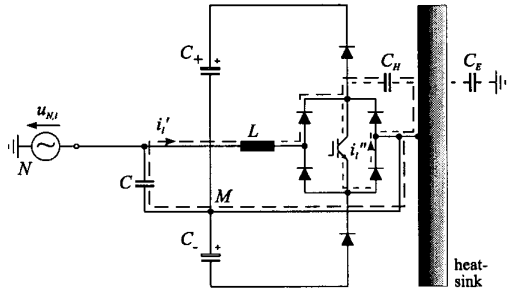


Fig.12: Noise current path for connection of the heat sink to the center point M of the output voltage (i_l' noise current for turn-off of the power transistor S_i, i_l'' current path for turn-on of S_i). The high-frequency noise currents remain within the system and do not flow via C_E into ground.

5 Experimental Results

To verify the theoretical considerations EMI measurements of a product oriented 10kW prototype of a VIENNA Rectifier I has been performed. The nominal values of the system correspond to the parameters of the digital simulation. The system where the measurements are taken from did not have any case or shielding; a resistive loading of the DC voltage has been used.

As compared to a free center point M (cf. **Fig.11**(a)) the connection of M to N' gives a reduction of the noise voltage of about 20dB (quasi-peak measurement, cf. Fig.11 (b)). The lower frequency region of the spectrum clearly shows the appearing harmonics of the switching frequency. For higher frequencies the parasitic characteristics of the filtering components become dominant (cf. Fig.8) which increasingly lowers the improvement.

If, additionally, the heat sink is connected to M the noise currents due to the isolation capacitances of the switching power devices are kept within the system (cf. **Fig.12**) and do not flow into ground which further reduces the EMI noise in the relevant frequency region 150kHz... 30MHz (cf. Fig.11(c)) and CISPR 11 /class A is guaranteed.

6 Conclusions

It is shown by the presented paper that the application of filtering capacitors C connected between the center point M of the DC output voltage and the input (mains) terminals significantly reduces the switching-frequency voltage component of the output voltage with respect to ground (mains neutral point); the common-mode EMI noise being characteristic for three-phase PWM rectifier systems can be substantially improved. If, furthermore, also the heat sink is connected to M the compliance to lower performance EMI regulations, e.g., for industrial applications (CISPR 11, class A) is given. To comply with CISPR 11/class B a small additional EMI filter would be required.

The advantages and drawbacks of the proposed filtering concept can be summarized as follows:

Advantages:

+ the location of the filtering capacitors C does not cause any leakage currents to ground
+ the modulation region (voltage utilization) of the converter is equal to the case of "free" DC output voltage center point ($M = 0 \ldots 1.15$)
+ low realization effort and
+ low additional volume/size (easy implementation into the rectifier unit)
+ application is not limited to the VIENNA Rectifier I concept; conventional PWM rectifier systems usually do not show a current dependency for voltage forming; therefore, the value of C can be increased which further reduces the switching frequency harmonic (νf_P, $\nu = 2, 3, 4 \ldots$) disturbances in the frequency region f_P to 150kHz (cf. Fig.12).

Drawbacks:

- increased rms value of the ripple of the current through the input inductors of the rectifier (but not of the mains current!)
- higher copper losses and higher core losses of the input inductors
- without an explicit common-mode inductor the switching frequency component of the voltage $u_{0,\sim}$ as well as the first appearing switching frequency components νf_P, $\nu = 2, 3, 4 \ldots$ are attenuated insignificantly due to the capacitance value C limited by Eq.(32). For conventional bidirectional PWM converter systems a higher value for C can be chosen (considering the mains reactive power consumption) which allows a further reduction of the EMI
- despite of application of the capacitors C a remaining common-mode noise appears due to the charging currents of the parasitic capacitances between drain and ground at the switching instants of the power transistors; this could possibly require for a common-mode filter located at the AC side of the system as before. Alternatively, for reduction of these noise currents the heat sink can be mounted isolated from ground (earth) and connected to the center point of the DC output voltage (cf. Fig.12(d)).

Further research activities will be concerned on the application of a common-mode inductance in series to the three input inductors of the rectifier. With this, for a given common-mode suppression $A(j\omega)$ the value of the capacitors C can be reduced in order to limit the distortion of the voltage $u_{0,\text{avg}}$ (which defines the voltage utilization) also in case of low output power levels. The damping of the self-resonance of the common-mode filter shall be performed by a fourth winding of the common-mode choke which is terminated by a damping resistor [9].

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