EXPERIMENTAL ANALYSIS OF A 5kW WIDE INPUT VOLTAGE RANGE THREE-PHASE BUCK+BOOST POWER FACTOR CORRECTOR

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Abstract – In this paper the experimental analysis of a three-phase three-switch buck+boost PWM rectifier with unity power factor is discussed. The output voltage and the output current control are realized using a digital signal processor where a modulation scheme is employed which does provide minimum switching losses and minimum input capacitor voltage ripple rms value. The control design which is based on an equivalent DC/DC converter and state-space averaging is discussed briefly. Finally, the efficiency, the power factor, and the total harmonic distortion and the low-frequency harmonics of the mains current are gained in dependency on the output power by measurements on a 5 kW prototype of the system.

1 INTRODUCTION

In [1] a three-phase PWM rectifier being formed by integration of a three-switch buck-derived front-end and a DC/DC boost converter output stage has been proposed (cf. **Fig. 1**) which gives the possibility of controlling the output voltage to e.g. 400 V within a wide input voltage range of (208 ... 480) V_{rms} line-to-line [2].

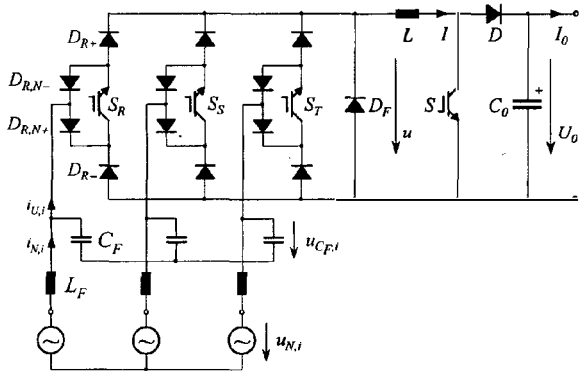

Fig. 1: Structure of the power circuit of the three-phase buck+boost PWM rectifier.

As main advantages of this concept one has to point out

- the sinusoidal shape of the input currents
- the resistive fundamental mains behavior
- the possibility of limiting the input current and/or the current in the buck+boost inductor for mains over-voltages.

Furthermore, in contrast to rectifier systems with boost-type input stage

- no auxiliary start-up circuit is required

and the system shows a

- high efficiency of up to $\eta = 96.6\,\%$, and a
- high power density ($\rho = 965\text{W/dm}^3$ or 15.8W/in^3).

At the Department of Electrical Drives and Machines of the Vienna University of Technology a prototype of the three-phase buck+boost PWM rectifier has been realized using standard power semiconductors (in TO 247 packages) and a digital signal processor for the system control. The specifications of the system are:

$$\begin{aligned} P_0 &= 5\,\text{kW} \\ U_{N,l-l} &= 208\,\text{V} \ldots 480\,\text{V} \\ U_0 &= 400\,\text{V} \\ f_N &= 50\,\text{Hz} \\ f_P &= 23.4\,\text{kHz}. \end{aligned}$$

In this paper the experimental analysis of the three-phase buck+boost PWM rectifier system is discussed in detail. In **section 2** the basic principle of operation is summarized briefly. **Section 3** shows a block diagram of the control structure implemented on a digital signal processor. Furthermore, a brief introduction into the control design with reference to an equivalent DC/DC converter and state-space averaging is given. In **section 4**, the results of the experimental analysis of the system are compiled including the dependency of the mains current total harmonic distortion, of the efficiency, and of the power factor on the output power within the wide input voltage range. Furthermore, the spectrum of the mains phase current is shown for different operating points.

2 BASIC PRINCIPLE OF OPERATION

For achieving a resistive fundamental mains behavior

$$i_{N,i} \sim u_{N,i} \qquad i = R, S, T, \tag{1}$$

and for neglection of the fundamental of the input filter capacitor currents,

$$i_{N,i} \approx i_{U,(1),i}, \tag{2}$$

fundamentals of $i_{U,(1),i}$ of the discontinuous rectifier input phase currents $i_{U,i}$ lying in phase with the corresponding mains phase voltages $u_{N,i} \approx u_{CF,i}$ have to be formed.

Accordingly, the relative on-times δ_{S_i} of the power transistors S_i have to be set proportional to the instantaneous value of the mains phase voltages considering the value of the buck stage output current I which can be assumed as approximately constant and impressed by the buck+boost inductor. With the modulation index M of the buck input stage

$$M = \frac{\hat{I}_N}{I} = \frac{\sqrt{2}\,U}{\sqrt{3}\,U_{N,l-l}} \qquad M \in [0;1] \tag{3}$$

(where $\hat{I}_N$ denotes the amplitude of the mains phase current; U denotes the average value of the output voltage of the buck input stage, and $U_{N,l-l}$ denotes the rms value

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of the line-to-line voltage) one receives for the relative on-times of the power transistors S_i

$$\delta_{S_i} = \sqrt{3}\, M\, \frac{|u_{N,i}|}{\sqrt{2}\, U_{N,l-l}}. \qquad (4)$$

The maximum output voltage U_{max} of the buck input stage is limited according to a selected maximum modulation index M_{max} to

$$U_{max} = \frac{\sqrt{3}}{\sqrt{2}}\, U_{N,l-l}\, M_{max}, \qquad (5)$$

where in the case at hand the stationary maximum modulation index is set to $M_{max} = 0.9$ in order to have a margin to the theoretical limit $M = 1$ (cf. (3)) for system control. If U_{max} is lower than the reference value of the system output voltage U_0, the boost output stage has to be activated, i.e., the on-time and/or duty cycle δ of the boost power transistor has to be set according to

$$\delta = 1 - \frac{U_{max}}{U_0} \qquad \delta \in [0;1]. \qquad (6)$$

In **Fig. 2** the distortion of the mains phase currents and of the buck+boost inductor current is shown for an output voltage reference value being higher than the maximum buck stage output voltage U_{max}, where the boost stage has not been activated, $\delta = 0$.

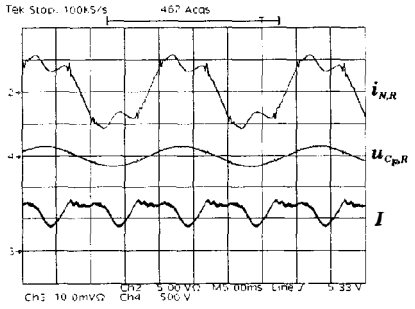


Fig. 2: Time behavior of a mains phase current, of an input filter capacitor voltage, and of the buck+boost inductor current for setting a system output voltage U_0 exceeding U_{max} in case the boost stage power transistor remains in the turn-off state. Current scales: $i_{N,R}$, I: 5 A/div; voltage scale: $u_{C_F,R}$: 500 V/div.

In order to achieve a high system efficiency, and a low mains current ripple a modulation method and/or switching state sequence within a pulse half period of the buck input stage has been identified in [1] and [3] which does provide minimum switching losses and/or does allow to select a high switching frequency.

3 SYSTEM CONTROL

3.1 Control Structure

The block diagram of the two-loop control implemented in the system prototype with an outer output voltage control and an inner buck+boost inductor current control is depicted in **Fig. 3** [1]. The requirement of controlling the buck+boost inductor current I is clearly shown in **Fig 4.** The assumption of a buck+boost inductor current I being constant and impressed by the buck+boost inductor L (cf. section 2) is not true for the low inductance of the inductor employed. A far larger inductance would be required for assuring a constant buck+boost inductor current I which however would result in an unacceptable large inductor volume.

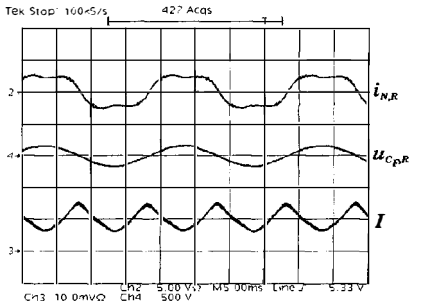


Fig. 4: Operation without buck+boost inductor current control; distorted mains phase current $i_{N,R}$ and buck+boost inductor current I for $U_{N,l-l} = 200\,\mathrm{V}$, $U_0 = 160\,\mathrm{V}$ and $P_0 = 775\,\mathrm{W}$. Current scales: $i_{N,R}$, I: 5 A/div; voltage scale: $u_{C_F,R}$: 500 V/div.

The reference value I_D^* of the local average current in the boost diode is set by the output voltage controller $F(s)$ in dependency on the control error $U_0^* - u_0$ of the output voltage. The controller is defined as of PI-type,

$$F(s) = k_{P,U}\left(1 + \frac{1}{s}\, k_{I,U}\right). \qquad (7)$$

The reference value of the buck+boost inductor current I^* is gained by multiplying the current in the boost diode with the weighting factor $1/(1-\delta)$, where δ denotes the duty cycle of the boost converter (cf. (6)). The buck+boost inductor current controller $G(s)$ sets the reference value U_L^* of the local average voltage across the buck+boost inductor. Adding the local average value of the voltage across the boost transistor

$$U'^* = U_0^*\, \frac{1}{1-\delta}, \qquad (8)$$

as a pre-control signal, one receives the reference value U^* of the local average value of the output voltage of the buck input stage. Due to the pre-control U'^* of the boost transistor voltage the buck+boost inductor current controller $G(s)$ can be of P-type,

$$G(s) = k_{P,I}. \qquad (9)$$

The buck stage output voltage reference value U^* is limited according to (5).

The actual interval of the mains period as required for the calculation of the on-times δ_j of the buck stage switching states j in combination with U^* is determined by comparing the band-pass filtered input filter capacitor voltages $u_{C_F,i}^{BP}$ (mid-frequency of the band-pass filter at $\omega_m = 2\pi 50\mathrm{Hz}$). In the following, the relative on-times[1] δ_j are given for the interval of the mains period where

$$u_{C_F,R} > 0 \quad \text{and} \quad u_{C_F,S} < 0; u_{C_F,T} < 0 \qquad (10)$$

[1]The indices of the relative on-times denote the switching states $j = (s_R\, s_S\, s_T)$ of the power transistors of the buck input stage, where $s_i = 1$ denotes the on-state and $s_i = 0$ denotes the off-state of a phase power transistor S_i.

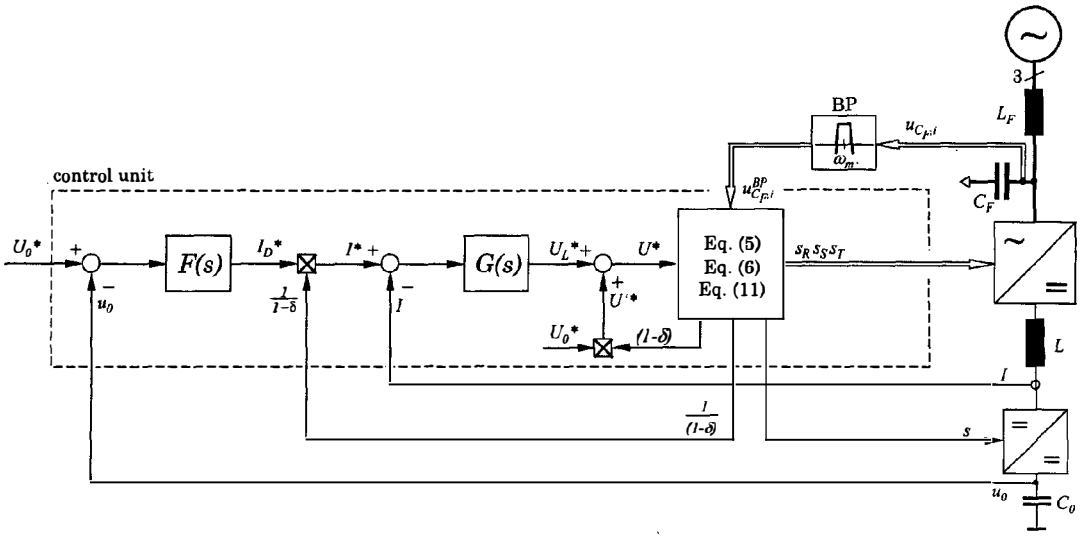


Fig. 3: Block diagram of the two-loop control of the three-phase buck+boost PWM rectifier system (shown only schematically); for the sake of clearness, signal paths being equal for all phases are combined in double lines and filter elements attenuating switching frequency components of measured voltages and currents are not shown.

is valid;

$$\begin{aligned} \delta_{(101)} &= \frac{1}{3}\frac{u^*}{|\underline{u}_{C_F}^{BP}|^2}\left(u_{C_F,R}^{BP} + u_{C_F,S}^{BP} - u_{C_F,T}^{BP}\right) \\ \delta_{(110)} &= \frac{1}{3}\frac{u^*}{|\underline{u}_{C_F}^{BP}|^2}\left(u_{C_F,R}^{BP} - u_{C_F,S}^{BP} + u_{C_F,T}^{BP}\right) \\ \delta_{(100)} &= 1 - \delta_{(101)} - \delta_{(110)}, \end{aligned} \tag{11}$$

There $|\underline{u}_{C_F}^{BP}|$ denotes the absolute value of the space vector of the band-pass filtered input filter capacitor voltages $u_{C_F,i}^{BP}$ which is defined by

$$\begin{aligned} u_{C_F,\alpha}^{BP} &= \frac{2}{3}\left[u_{C_F,R}^{BP} - \frac{1}{2}\left(u_{C_F,S}^{BP} + u_{C_F,T}^{BP}\right)\right], \\ u_{C_F,\beta}^{BP} &= \frac{1}{\sqrt{3}}\left[u_{C_F,S}^{BP} - u_{C_F,T}^{BP}\right], \\ |\underline{u}_{C_F}^{BP}| &= \sqrt{{u_{C_F,\alpha}^{BP}}^2 + {u_{C_F,\beta}^{BP}}^2}. \end{aligned} \tag{12}$$

These equations hold also in case a zero sequence system would be contained in the measured filter capacitor voltages.

3.2 Modelling, Small Signal Analysis and Control Design

For designing the system control in a first step the three-phase buck+boost PWM rectifier system is transformed into an equivalent DC/DC buck+boost PWM rectifier (cf. **Fig. 5**), and the equivalent DC value u_N^{DC} of the input voltage and the equivalent DC input filter inductor L_F^{DC} and equivalent DC filter capacitor C_F^{DC} are calculated,

$$\begin{aligned} u_N^{DC} &= 3\sqrt{3}/(\sqrt{2}\,\pi)\,U_{N,l-l} \\ L_F^{DC} &= 3/2\,L_F \\ C_F^{DC} &= 2/3\,C_F. \end{aligned} \tag{13}$$

Three different operating-modes of the three-phase system (and, correspondingly, also for the equivalent DC/DC system) can be distinguished depending on the on-times of

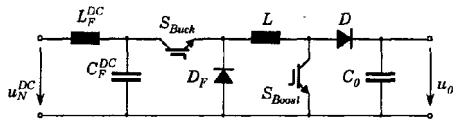


Fig. 5: Equivalent DC/DC converter circuit used for control design.

buck and boost power transistors. In mode $\mathcal{A}$, the modulation index of the buck-input stage is set to M_{max}, and the duty cycle of the boost output stage δ is higher than 10 %. In mode $\mathcal{B}$, $M = M_{max}$ and $\delta < 10\,\%$ is valid. In mode $\mathcal{C}$ the boost stage is deactivated, i.e. $\delta = 0$, and the modulation index of the buck input stage is varied according to the output voltage required. Four different circuit states depending on the switching states of the power transistors S_{Buck} and S_{Boost} can be distinguished (cf. **Tab. 1** and **Fig. 6**).

Topology	S_{Buck}	S_{Boost}	Mode
0	off	off	$\mathcal{B},\mathcal{C}$
1	off	on	$\mathcal{A},\mathcal{B}$
2	on	off	$\mathcal{A},\mathcal{B},\mathcal{C}$
3	on	on	$\mathcal{A}$

Tab. 1: Circuit topologies and corresponding operating modes used as basis for state-space averaging.

Each circuit topology can be described using state-variables, the resulting state-equations are time weighted and/or averaged over a pulse period (state-space averaging, [4], [5]) using the modulation index M and the duty cycle δ. Subsequently, small AC perturbations are introduced, e.g., for the output voltage,

$$u_0 = U_0 + \tilde{u}_0 \tag{14}$$

where U_0 is the steady-state output voltage and $\tilde{u}_0$ denotes

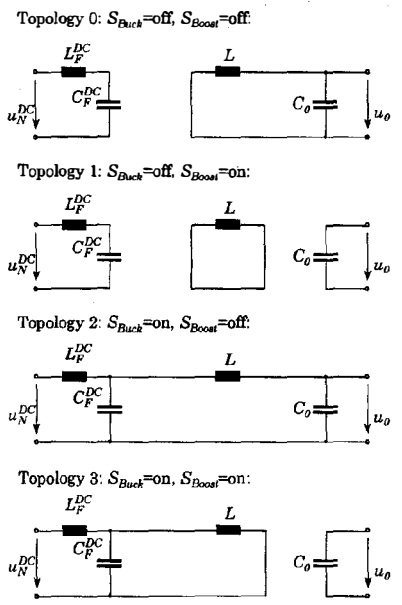


Fig. 6: Topologies for different switching states of the equivalent DC/DC converter.

the small AC perturbation. The perturbation of the input voltage as well as the perturbation of the modulation index M in modes $\mathcal{A}$ and $\mathcal{B}$ are assumed to be equal to zero in order to simplify the analysis. The resulting differential equations for the AC perturbations are transformed into the s-domain using Laplace transformation. Therewith, the desired transfer functions, e.g., $\tilde{u}_0(s)/\tilde{m}(s)$ and $\tilde{u}_0(s)/\tilde{\delta}(s)$, can be calculated.

Combining both the transfer functions and the proposed control scheme (cf. Fig. 3) for the different modes of operation, a basis for determining the control parameters is obtained. There, the effect of the finite sampling time of the DSP (sampling is once per pulse half period, i.e. the sampling frequency is 46.875 kHz) is considered in a first approximation by a first-order delay having a corner frequency of $\omega_c = 2\pi\, 5\,\text{kHz}$.

In **Fig. 7(a)** the root locus diagram of the current control loop is given for the following operating parameters:

$$\begin{array}{ll} P_0 = 5\,\text{kW} & M = 0.9 \\ U_N^{DC} = 444\,\text{V} & U_0 = 400\,\text{V} \\ L_F^{DC} = 225\,\mu\text{H} & C_0 = 750\,\mu\text{F} \\ C_F^{DC} = 2.67\,\mu\text{F} & L = 1\,\text{mH}. \end{array}$$

As the calculation of the root locus of the current control loop shows, the gain $k_{P,I}$ of the current controller has to be set considering

$$k_{P,I} < 40 \quad \text{for} \quad P_0 = 5\,\text{kW} @ U_0 = 400\,\text{V}. \tag{15}$$

The controller gain was varied in the range of $k_{P,I} = 5 \ldots 40$ in dependency on the input voltage in order to avoid oscillations of the input filter. In the course of a further development of the controller, an automatic adaption of the controller parameters and an active damping of the input filter [6] will be implemented. In **Fig. 8** the excitation of the input filter and the corresponding oscillations of the mains current as occurring in case the controller gain is not adapted properly are shown.

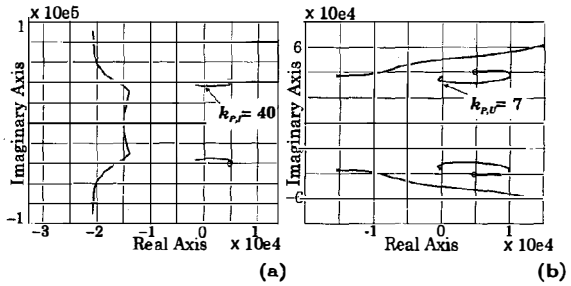


Fig. 7: Root locus diagram **(a)** of the current control loop, and **(b)** of the output voltage control loop, both for rated output power $P_0 = 5\,\text{kW}$.

For the outer output voltage control loop, the integration constant of the PI-type output voltage controller is set to $k_{I,U} = 0.5$, the corresponding root locus diagram is depicted in **Fig. 7(b)**. With this, one receives for the gain of the output voltage controller $k_{P,U} < 7$ for rated output power $P_0 = 5\,\text{kW}$. Details of the design of the system control will be given in a future paper.

3.3 Digital Signal Processor

The control of the 5 kW prototype of the three-phase buck+boost PWM rectifier was realized using a floating point digital signal processor ADSP-21061 SHARC (Analog Devices) [7], [8] in combination with programmable logic devices (PLDs) MAX 7000S [9]. The pulse frequency was defined as $f_P = 23.4\,\text{kHz}$ in order to limit the power semiconductor switching losses to an admissible value (cf. [10]). By employing two interleaved triangular carrier signals for the buck and the boost converter modulation, the ripple of the buck+boost inductor current can be minimized. The switching signals of the boost stage power transistor S then show a displacement of half a pulse period $T_P/2 = 21.3\mu\text{s}$ to the switching signals of the buck stage power transistors S_i, $i = R, S, T$ (cf. **Fig. 9**). The boost converter power transistor is turned on while the buck input stage is in the free-wheeling state, whereby the voltage across the buck+boost inductor and/or the current ripple are minimized.

4 EXPERIMENTAL RESULTS

The operating behavior of the system prototype was investigated for different output power levels P_0 and different line-to-line voltages $U_{N,l-l}$,

$$\begin{array}{rcl} P_0 & = & [0.5; 1; 2; 3; 4; 5]\,\text{kW} \\ U_{N,l-l} & = & [210; 260; 310; 360; 415; 440]\,\text{V}, \end{array} \tag{16}$$

the total harmonic distortion THD of the mains phase currents, the power factor λ at the input of the rectifier system, as well as the efficiency η were determined using a three-phase power analyzer Voltech® PM 300 [11]. The load was represented by an ohmic power resistor, the output voltage was controlled to the rated value of $U_0 = 400\,\text{V}$, the heat sink temperature was held at $\approx 30°\,\text{C}$ by proper forced air cooling. The maximum input voltage was limited to $U_{N,l-l} = 440\,\text{V}$ due to the voltage supply available in the

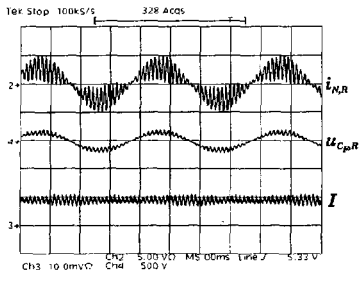


Fig. 8: Excitation of the input filter by the constant input power characteristic of the rectifier system; mains phase current $i_{N,R}$, input filter capacitor voltage $u_{C_F,R}$, and buck+boost inductor current I. Current scales: $i_{N,R}$, I: 5 A/div; voltage scale: $u_{C_F,R}$: 500 V/div.

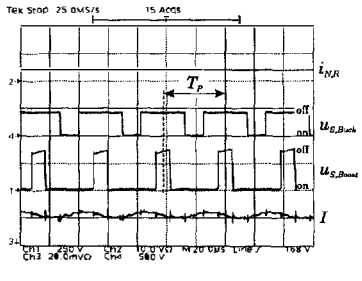


Fig. 9: Switching actions of the buck stage power transistor S_S and of the boost converter power transistor S_{Boost}; mains phase current $i_{N,R}$, voltage $u_{S,Buck}$ across buck stage power transistor S_S, voltage $u_{S,Boost}$ across boost converter power transistor, buck+boost inductor current I.

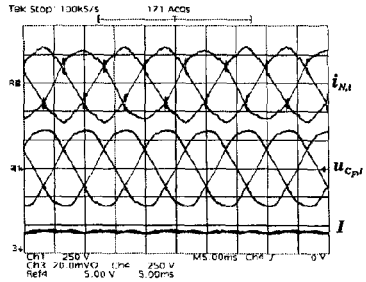
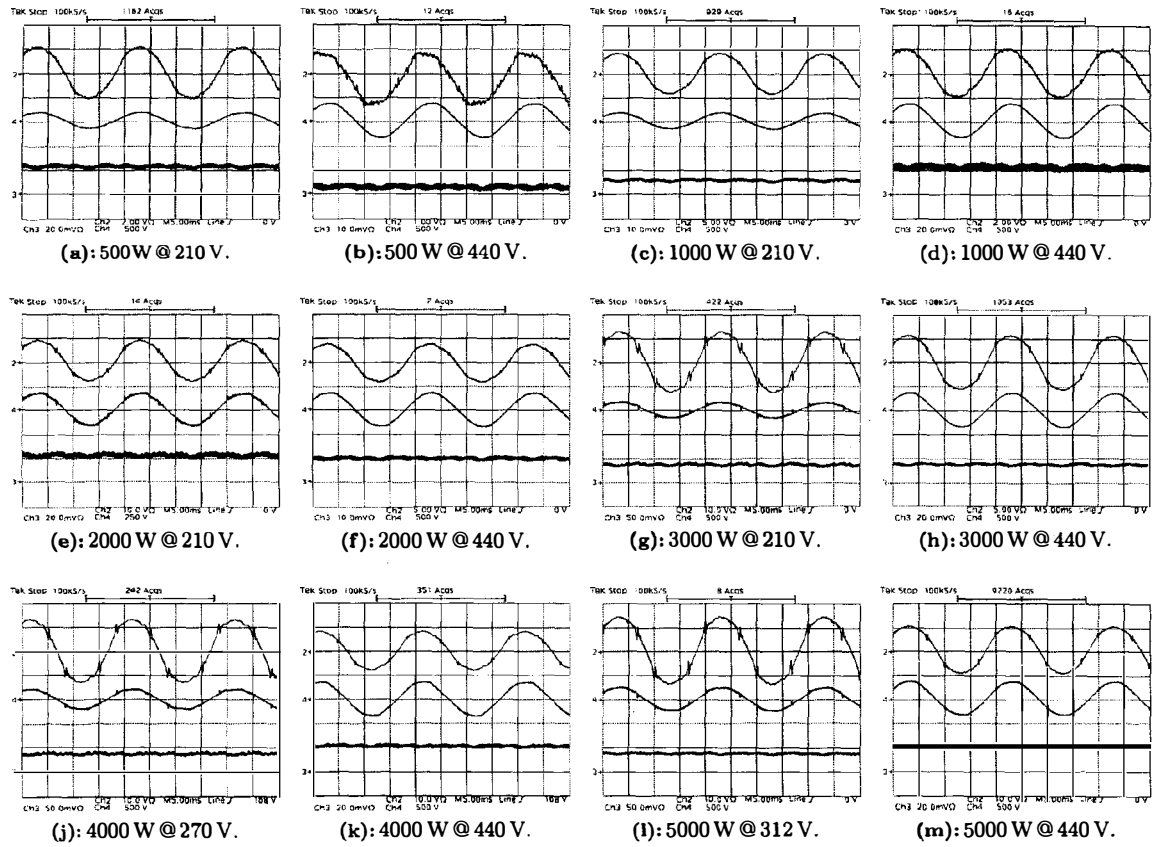


Fig. 10: Time behavior of the mains phase currents $i_{N,i}$, input filter capacitor voltages $u_{C_F,i}$, and buck+boost inductor current I for $U_{N,l-l}$ = 324 V and P_0 = 3 kW. Current scales: $i_{N,R}$: 5 A/div; I: 5 A/div; voltage scale: $u_{C_F,R}$: 250 V/div.



(a): 500 W @ 210 V. **(b):** 500 W @ 440 V. **(c):** 1000 W @ 210 V. **(d):** 1000 W @ 440 V.

(e): 2000 W @ 210 V. **(f):** 2000 W @ 440 V. **(g):** 3000 W @ 210 V. **(h):** 3000 W @ 440 V.

(j): 4000 W @ 270 V. **(k):** 4000 W @ 440 V. **(l):** 5000 W @ 312 V. **(m):** 5000 W @ 440 V.

Fig. 11: Mains phase current $i_{N,R}$ (Ch. 2, trace 1) and corresponding input filter capacitor voltage $u_{C_F,R}$ (Ch. 4, trace 2), and buck+boost inductor current I (Ch. 3, trace 3) for different output power levels P_0 and different line-to-line voltages $U_{N,l-l}$. Mains phase current scales (Ch. 1): (b): 1 A/div; (a), (d): 2 A/div; (c), (f), (h): 5 A/div; (e), (g), (j)–(m): 10 A/div; input filter capacitor voltage scales (Ch. 4): (a)–(d), (f)–(m): 500 V/div; (e): 250 V/div; buck+Boost inductor current scales (Ch. 3): (a), (d): 2 A/div; (b), (c), (f): 5 A/div; (e), (h), (k), (m): 10 A/div; (g), (j), (l): 10 A/div.

laboratory. In order to avoid oscillations of the mains phase current, the gain of the current controller $G(s)$ was adjusted for operating points with low input voltage manually (cf. section 3.2; for the experimental setup there was a high influence on the input filter resonant frequency by the stray inductance of the autotransformer varying with the transformer output voltage). The results of the measurements are approximated by trend lines (cf. Figs. 12, 14, 15).

In **Fig. 10** the time behavior of the mains phase currents $i_{N,i}$, $i = R, S, T$, of the input filter capacitor voltages $u_{C_F,i}$ and of the buck+boost inductor current I is given for a line-to-line voltage of $U_{N,l-l}$ = 324 V and an output

power of $P_0 = 3\,\mathrm{kW}$. In **Fig. 11** the behavior of the mains phase current $i_{N,R}$, of the corresponding input filter capacitor voltage $u_{C_F,R}$, and of the buck+boost inductor current I is depicted for different output power levels and for operation at the upper and at the lower input voltage level (cf. (16)). For large values of the mains phase currents, one can notice the excitation of the input filter at the changes of the operating intervals of the mains period as defined by the changes of the combination of signs (cf. (10) of the input filter capacitor voltages (e.g., cf. Fig. 11(g), (j), (l)).

4.1 Power Factor

The power factor λ of the buck+boost PWM rectifier,

$$\lambda = \frac{P}{S} = \frac{\frac{1}{T_N}\sum_i \int_0^{T_N} u_{N,i}\, i_{N,i}\, dt}{\sqrt{\frac{1}{T_N}\int_0^{T_N} u_{N,i}^2\, \mathrm{d}t}\sqrt{\frac{1}{T_N}\int_0^{T_N} i_{N,i}^2\, \mathrm{d}t}}, \qquad (17)$$

is shown in **Fig. 12** in dependency on the line-to-line voltage for different output power levels. At low output power and close to the maximum input voltage, the power factor shows lower values than at higher output power and low input voltage. This is due to the lower mains phase current $i_{N,i}$ and the higher percentage of the input filter capacitor current. In **Fig. 13** the behavior of the mains phase current is shown for disabled rectifier, where mains current and input filter capacitor current are identical. Especially for a low output power of $P_0 = 500\,\mathrm{W}$ this influence can be recognized clearly in Fig. 12(b).

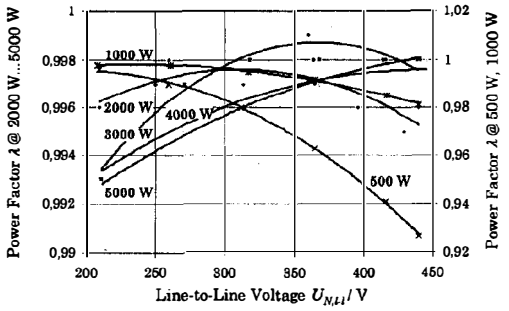


Fig. 12: Power factor λ in dependency on the line-to-line voltage $U_{N,l-l}$ for different output power levels P_0.

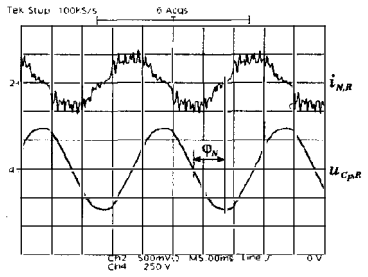


Fig. 13: Behavior of mains phase current $i_{N,R}$ and of the corresponding input filter capacitor voltage $u_{C_F,R}$ in case the rectifier is disabled.

4.2 Efficiency

The system efficiency

$$\eta = \frac{P_0}{P} = \frac{U_0\, I_0}{\frac{1}{T_N}\sum_i \int_0^{T_N} u_{N,i}\, i_{N,i}\, dt}. \qquad (18)$$

is shown in **Fig. 14**. For the input voltages close to the upper limit, the efficiency is in the range of approx. 95 % to 96.6 %, for the maximum input voltage of $U_{N,l-l} = 480\,\mathrm{V}$ (which could not be achieved in the laboratory) an increase of 1 % could be expected. The efficiency for constant output power is highly dependent on the input voltage, i.e. on the input current. For decreasing input voltage the mains phase current does increase for constant output power, which results in higher switching and conduction losses of the power semiconductors and/or in higher losses in the passive power components.

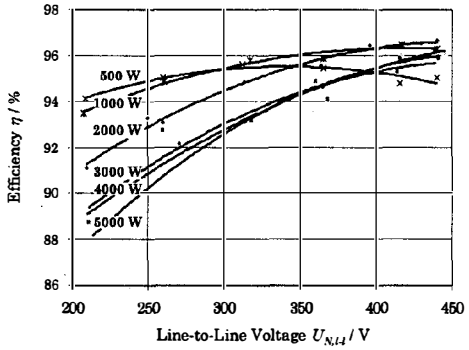


Fig. 14: Efficiency η in dependency on the line-to-line voltage $U_{N,l-l}$ for different output power levels P_0.

4.3 Total Harmonic Distortion

In **Fig. 15**, the average value THD of the total harmonic distortions THD_i of mains phase currents is given in dependency on output power and input voltage. There, as given in [11] the total harmonic distortion of the mains phase currents is calculated by the power analyzer with reference to

$$THD_i = \frac{\sqrt{I_{N,i}^2 - I_{N,(1),i}^2}}{I_{N,(1),i}} \cdot 100\% \qquad \forall THD_i > 6\%$$
$$THD_i = \frac{\sqrt{\sum_{n\neq 1} I_{N,(n),i}}}{I_{N,(1),i}} \cdot 100\% \qquad \forall THD_i < 6\% \qquad (19)$$

For low input voltage, the THD shows higher values than for high higher input voltage, except at low output power levels, where the THD is influenced by the input filter. The low values at low input voltage are due to the parasitic second harmonic of the buck+boost inductor current I, which does result in a low frequency distortion of the mains phase currents (cf. section 4.4).

4.4 Spectrum of the Mains Phase Currents

The spectrum of the mains currents was determined for two different output power levels ($P_0 = 2$ kW and $P_0 = 5$ kW)

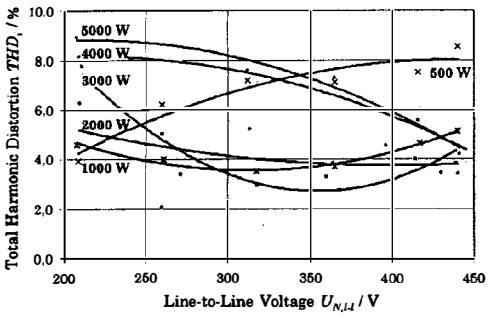


Fig. 15: Total harmonic distortion THD of the mains current in dependency on the line-to-line voltage $U_{N,l-l}$ for different levels of the output power P_0.

and different values of the input voltage[2], cf. **Fig. 17**. The spectra show 3^{rd}, 5^{th} and 7^{th} harmonics, which are not attenuated by the switching frequency input filter. The origin of the low frequency harmonics is explained in the following.

Third Harmonic

Since there is no connection of the system to the mains neutral, a zero sequence system formed by 3^{rd} harmonic currents of equal phase cannot exist. Accordingly, the analysis of the amplitudes $\hat{I}_{N,(3),i}$, $i = R, S, T$, of the 3^{rd} harmonics and of their phase-displacement $\varphi_{(3),i}$ to the related fundamentals $I_{N,(1),i}$ shows, that the 3^{rd} harmonics are not of zero-sequence type but constitute a three-phase system having three times the mains frequency, $3\,f_N = 150\,\text{Hz}$. For $P = 2\,\text{kW}$ and $U_{N,l-l} = 440\,\text{V}$ one receives for the 3^{rd} harmonics:

$$\begin{aligned} \varphi_{(3),R} &= -33^\circ \text{ el.} & I_{N,(3),R}/I_{N,(1),R} &= 0.037 \\ \varphi_{(3),S} &= -228^\circ \text{ el.} & I_{N,(3),S}/I_{N,(1),S} &= 0.013 \\ \varphi_{(3),T} &= -202^\circ \text{ el.} & I_{N,(3),T}/I_{N,(1),T} &= 0.026. \end{aligned} \quad (20)$$

The investigation furthermore identifies a dependency of the 3^{rd} harmonic current system on the gain $k_{P,I}$ of the buck+boost inductor current controller $G(s)$. For small values of $k_{P,I}$ as set for the operation at high output power and/or low mains voltage the 3^{rd} harmonics show a substantially larger value than for the operating point 2 kW @ 440 V, with higher $k_{P,I}$. The higher value of $k_{P,I}$ does provide a reduction of the amplitude of the 3^{rd} harmonics of 35 %.

The 3^{rd} harmonics do occur for the following reason: According to (4) the buck+boost inductor current is distributed sinusoidally to the mains phases in dependency on the modulation index M. E.g., if phase R is considered one receives for the mains phase current

$$i_{N,R} = I\,M\,\cos(\omega\,t) = \hat{I}_N\,\cos(\omega\,t) \quad (21)$$

incorporating (3). Therefore, the behavior of each phase of the buck input stage in the average over a pulse period is equivalent to multiplying the constant buck+boost inductor current with a sinusoidal (modulation) signal with mains frequency (cf. **Fig. 16**). If now the buck+boost

[2]One has to mention, that the voltage supply was represented by an auto-transformer and not by a purely sinusoidal three-phase AC voltage source; therefore, the mains current distortion is partly due to the mains voltage distortion.

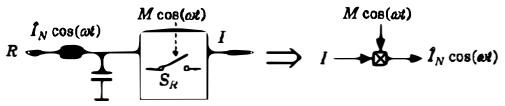


Fig. 16: Equivalence of a bridge leg of the buck input stage in the average over a pulse period to a multiplier.

inductor current is distorted, i.e. if I does contain any harmonics, e.g., a 2^{nd} harmonic of amplitude $\hat{I}_{(2)}$,

$$I_{dist.} = I + \hat{I}_{(2)}\,\sin(2\omega\,t) \quad (22)$$

one receives for the mains phase current in phase R[3]

$$\begin{aligned} i_{N,R} &= I_{dist.}\,M\,\cos(\omega\,t) = \\ &= \left[I + \hat{I}_{(2)}\,\sin(2\omega\,t)\right]\,M\,\cos(\omega\,t) = \\ &= \hat{I}_{N,(1)}\,\cos(\omega\,t) + \frac{\hat{I}_{N,(2)}}{2}\,[\cos(\omega\,t) - \cos(3\omega\,t)] \end{aligned} \quad (23)$$

where $\hat{I}_{N,(1)}$ denotes the amplitude of the mains current fundamental, and $\hat{I}_{N,(2)}$ denotes the amplitude of the 2^{nd} mains current harmonic. Accordingly, a 2^{nd} harmonic of the buck+boost inductor current is responsible for a 3^{rd} harmonic of the mains phase current [12], [13].
In the following, the amplitude of the voltage being necessary to cause a 2^{nd} harmonic $\hat{I}_{(2)} \approx 2\,\text{A}$ (cf. Fig. 11(m)) shall be calculated in order to point out the sensitivity of the system to non-idealities in case the buck+boost inductor current controller shows low gain. One receives for the absolute value $Z_{L,(2)}$ of the impedance of the buck+boost inductor[4] L for the 2^{nd} harmonic

$$Z_{L,(2)} = 2\omega L = 4\,\pi\,50\,\text{Hz} \cdot 1750\,\mu\text{H} \approx 1\,\Omega. \quad (24)$$

This results in an amplitude of the 2^{nd} harmonic of the output voltage u of the buck stage required for generating $\hat{I}_{(2)} \approx 2\,\text{A}$ of

$$\hat{U}_{(2)} = Z_{L,(2)} \cdot \hat{I}_{(2)} = 1\,\Omega \cdot 2\,\text{A} = 2\,\text{V} \quad (25)$$

what is in the range of the forward voltage drops of the power semiconductors (!). Also, e.g., a slight unbalance of the mains voltages which is not perfectly eliminated in the course of the calculation of the duty cycles of the buck stage power transistors (e.g. due to imperfections of the capacitor voltage measurement) or does only apparently occur due to tolerances of the input filter capacitors would be large enough to cause a 2^{nd} harmonic amplitude as occurring in the case at hand. The effect of such non-ideal behavior on the operating behavior of the three-phase/switch buck+boost PWM rectifier will be calculated analytically in a future paper.

Fifth and Seventh Harmonics

As **Fig. 17** shows, both the 5^{th} and the 7^{th} harmonic of the mains phase currents, which are not attenuated by the input filter, show a large amplitude. This is due to the 5^{th} and the 7^{th} harmonics contained in the feeding AC mains voltage as resulting from heavy loading with single-phase

[3]With $\sin(\alpha)\sin(\beta) = \frac{1}{2}\,[\cos(\alpha-\beta) - \cos(\alpha+\beta)]$.

[4]$L = 1750\,\mu\text{H}$ @ 15 A.

diode rectifiers with capacitive smoothing. The buck input stage shows a purely ohmic behavior, i.e., the shape of the mains phase currents is proportional to the shape of the mains phase voltages. Therefore, the 5^{th} and the 7^{th} harmonics of the mains phase voltages also do occur in the mains phase currents.

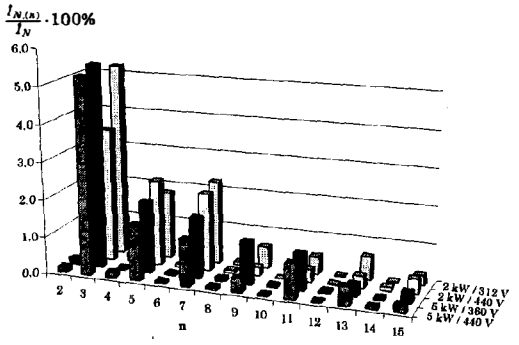


Fig. 17: Normalized spectra of the mains phase current, fundamental component $\hat{I}_N$ suppressed. n denotes the ordinal number of the harmonics with reference to the mains frequency $f_N = 50$ Hz.

5 CONCLUSIONS

In this paper, a new wide input voltage range three-phase buck+boost PWM rectifier (VIENNA Rectifier IV) is analyzed experimentally. The system provides a controlled DC output voltage $U_0 = 400\,\mathrm{V}$, a high power factor and a high efficiency (up to $\lambda = 0.998$ and $\eta = 0.966$ for high output power and high input voltage). The control of the converter is realized using a digital signal processor and two programmable logic devices. An approach for the control design based on an equivalent DC/DC converter and state-space averaging is proposed, and the control stability is investigated.

A basic problem of the system is the excitation of the input filter of the buck-derived input stage which results in oscillations of the mains currents and correspondingly of the buck+boost inductor current. In the case at hand the excitation was avoided by adaption of the gain of the buck+boost inductor current controller in dependency on the output power. The drawback of the adaption of the controller gain is the resulting distortion of the buck+boost inductor current and/or of the mains current for low controller gain. Another possibility is the implementation of an active damping of the input filter (in combination with a passive and/or resistive damping in order to ensure damping also at no-load conditions). There, the filter should be split-up into two stages. The passive damping then could be implemented only for the filter input stage [14] what would limit the reduction of the filter attenuation by the damping resistor. Furthermore, the two-stage filter attenuation characteristic would be less sensitive to variations of the inner mains impedance and the filter volume would be lower as compared to a single-stage approach for a given attenuation at the switching frequency. The investigation of an adaptive control in combination with an active and passive damping of the input filter is currently under way and will be published at a future conference.

References

[1] **Baumann, M., Drofenik, U., and Kolar, J. W.:** *New Wide Input Voltage Range Three-Phase Unity Power Factor Rectifier Formed by Integration of a Three-Switch Buck-Derived Front-End and a DC/DC Boost Converter Output Stage.* Proceedings of the 22^{nd} IEEE International Telecommunications Energy Conference, Phoenix, Arizona, U.S.A., Sept. 14 - 18, pp. 461–470 (2000).

[2] **Kolar, J. W.:** *Netzrückwirkungsarmes Dreiphasen-Stromzwischenkreis-Pulsgleichrichtersystem mit weitem Stellbereich der Ausgangsspannung.* Austrian Patent Application A9/2000, filed: Jan. 5, 2000.

[3] **Baumann, M., and Kolar, J. W.:** *Comparative Evaluation of Modulation Methods for a Three-Phase/Switch Buck Power Factor Corrector Concerning the Input Capacitor Voltage Ripple.* Proceedings of the 32^{nd} IEEE Power Electronics Specialists Conference, Vancouver, Canada, June 17 - 21, pp. 1327–1332 (2001).

[4] **Middlebrook, R. D., and Cuk, S.:** *A General Unified Approach to Modeling Switching Converter Power Stages.* Proceedings of the IEEE Power Electronics Specialists Conference, Cleveland, Ohio, U.S.A., June 8 - 10, pp. 18–34 (1976).

[5] **Mohan, N., Undeland, T. M., and Robbins, W. P.:** *Power Electronics - Converters, Applications, and Design.* John Wiley & Sons, Inc. (1989).

[6] **Marques, G. D.:** *A Current-Type PWM Rectifier Control System with Active Damping Based in the Space Vector Technique.* Proceedings of the IEEE International Symposium on Industrial Electronics, Guimarães, Portugal, pp. 318–322 (1997).

[7] **Morauf, G.:** *Signalprozessorregelung eines neuen Dreiphasen-Pulsgleichrichtersystems mit weitem Eingangsspannungsbereich (VIENNA Rectifier IV).* Diploma Thesis (in German), Vienna University of Technology, Dept. of Electrical Drives and Machines, Vienna, Austria, Jan. 2001.

[8] **Analog Devices:** *ADSP-2106x SHARC DSP Family; ADSP-21061/ADSP 21061L.* Data Sheet, Rev. B, U.S.A. (2000).

[9] **Altera:** *MAX 7000S Programmable Logic Device Family.* Data Sheet, Version 6.01, U.S.A., December 1999.

[10] **Baumann, M., and Kolar, J. W.:** *Experimental Evaluation of a Three-Phase Three-Switch Buck-Type Unity Power Factor Corrector.* Proceedings of the European Power Quality Conference, Nuremberg, Germany, June 19 - 21, pp. 69–75 (2001).

[11] **Voltech:** *PM 300 Power Analyzer User Manual.* Voltech Instruments Ltd, Version 04, Oxon, England (1996).

[12] **Halkosaari, T., Kuusela, K., and Tuusa, H.:** *Effect of Non-Idealities on the Performance of the 3-Phase Current Source PWM Converter.* Proceedings of the 32^{nd} IEEE Power Electronics Specialists Conference, Vancouver, Canada, June 17 - 21, pp. 654–659 (2001).

[13] **Kolar, J. W., and Sun, J.:** *Three-Phase Power Factor Correction Technology.* Tutorial Workbook of the 32^{nd} IEEE Power Electronics Specialists Conference, Seminars 1 & 4, Vancouver, Canada, June 17 - 21 (2001).

[14] **Erickson, R. W.:** *Optimal Single Resistor Damping of Input Filters.* Proceedings of the 14^{th} Applied Power Electronics Conference, Dallas, Texas, U.S.A., March 14 - 18, pp. 1073–1079 (1999).