A New Concept for Reconstruction of the Input Phase Currents of a Three-Phase/Switch/Level PWM (VIENNA) Rectifier Based on Neutral Point Current Measurement

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Abstract. A novel concept utilizing the neutral point current information which is gained by an AC current sense transformer or a shunt for observer-based continuous reconstruction of the input phase currents of a three-phase/switch/level boost-type PWM (VIENNA) rectifier system is proposed. The basic principle of operation and the dimensioning of the observer circuit which in modified form also could feature an output voltage earth fault detection are discussed in detail. Furthermore, results of a practical application of the system in connection with a highly dynamic ramp comparison mains current control of a 10kW laboratory model of the VIENNA rectifier are given.

1 Introduction

The DC-link current of three-phase voltage-source PWM rectifier systems is formed by sections of the input phase currents which are impressed by inductors connected in series on the AC side dependent on the switching state of the power transistors (Fig.9 in [1]). Therefore, it is obvious to reconstruct the input phase currents (which are required for the current control of the rectifier system) based on a measurement of the DC link current. Thereby, as compared to a direct measurement of two input phase currents (the third phase current can be calculated since the sum of all three mains phase currents is forced to zero for missing connection of the rectifier output voltage center point and the mains star point) the measurement effort is reduced and problems concerning different current transducer gains or DC offsets of the measured phase currents are eliminated.

In the literature this concept so far has been discussed only for three-phase two-level PWM inverter systems. E.g., in [2]-[7] two phase currents are determined within each pulse half period by sampling of the DC-link current. There, the PWM signals have to be adjusted for operating conditions where the time for which one or both phase currents appear in the DC link may fall below a minimum value beyond which reliable sampling is not possible as, e.g., in the case of low modulation index or overmodulation. Alternatively, for ensuring a reliable current information under all operating conditions one also could employ a state observer and/or machine model [8],[9]. There, the estimated phase current samples are corrected in a closed loop manner in case samples of the currents can be directly measured in the DC link otherwise the observer continues to provide phase current information in open loop.

In this paper a new concept for an observer-based reconstruction of the mains phase currents of a three-phase three-level PWM rectifier (VIENNA rectifier) is proposed. There, in contrast to sampled data based concepts as discussed in the literature so far a continuous mains phase current information is derived for a ramp comparison control of the input phase currents which is realized in analogue technique because of the high switching frequency \( f_s = 30...50\text{kHz} \). In section 2 the basic function of the VIENNA rectifier and the formation of the neutral point current are discussed. In section 3 the reconstruction of the input phase currents based on neutral point current measurement (as gained by an AC current sense transformer) and information about the rectifier switching state (cf. Fig.1 and/or [11]) is treated in detail. Furthermore, in section 4 the practical realization of the current observer system is discussed. Finally, in section 5 guidelines for dimensioning the observer components are given and experimental results as gained from an application of the system in a 10kW laboratory model of the VIENNA rectifier are shown.

Fig. 1: Structure of the power circuit of the VIENNA rectifier (three-phase/switch/level PWM rectifier system) [10] and of the proposed circuit for the reconstruction of the mains phase currents based on measurement of the center point current \( i_w \) [11].
2 Basic Function of the VIENNA Rectifier

2.1 Control of the Rectifier Input Voltage

In the turn-off state of a power transistor $S_i$ of a phase $i = R, S, T$ which is impressed by the respective input side inductor $L$ is flowing via the diodes $D_{R,i}, D_{S,i}$ into the positive (upper) DC link rail for $i_{u,i} > 0$; for $i_{u,i} < 0$ the current flow is via $D_{P,i}$ and $D_{N,i}$ out of the negative (lower) DC link rail. Accordingly, on the input side of the rectifier bridge leg a voltage $u_{u,i} = +\frac{1}{2} U_0$ or $u_{u,i} = -\frac{1}{2} U_0$ will appear with reference to the output voltage center point $M$. In contrast, for $S_i$ in the turn-on state a bidirectional connection of the input side of a phase leg and $M$ is given and the current flow is via $D_{N,i}, S_i, D_{M,i}$ or $D_{N,i}, S_i, D_{M,i}$ i.e. we have for the rectifier input voltage $u_{u,i} = 0$ independent of the direction of the phase current flow (cf. Fig.2). Accordingly, besides the binary switching function $s_i$ ($s_i = 1$ denotes the turn-on state and $s_i = 0$ the turn-off state of a power transistor $S_i$) also the sign $\text{sign}(i_{u,i})$ of a phase current $i_{u,i}$ takes influence on the resulting rectifier input voltage

$$u_{u,i} = \begin{cases} \frac{1}{2} \text{sign}(i_{u,i}) & \text{if } s_i = 0 \\ 0 & \text{if } s_i = 1 \end{cases}$$

Fig.2: Conduction states of a bridge leg for positive and negative input current (current path for power transistor $S$ in the turn-off state shown by a dashed line).

By considering the phase symmetry of the converter structure for the assumption of a purely sinusoidal mains voltage system a detailed analysis of the rectifier system can be constrained to a $90^\circ$-wide interval, e.g., to $\varphi_i \in (\varphi_i, \varphi_i + 90^\circ)$ of the mains period $\frac{2\pi}{T_0}$ where $i_{u,R} > 0$, $i_{u,S} < 0$, $i_{u,T} < 0$ is valid. As discussed in [12] in this case the $2^2 = 8$ possible combinations $j = (x, y, z)$ of phase switching functions result in the rectifier input voltage space vectors shown in Fig.3.

In order to achieve a purely sinusoidal input current one would have to form a rectifier input voltage space vector

$$u_L^* = \begin{cases} u_L \exp(j\varphi_i) & \text{if } s_i = 0 \\ -j\omega_0 L_i i_{u,i} & \text{if } s_i = 1 \end{cases}$$

where $u_L = U_0$ is the mains voltage, $\varphi_i = \omega_0 t_i$ of constant magnitude and constant angular speed $\omega_0$ denotes the space vector and/or phasor of the input current fundamental, $u_{L,i}$ designates the space vector and/or phasor of the rectifier input voltage fundamental. Since, however, only 8 discrete voltage space vectors $u_L^*$ are available (cf. Fig.3) the actual voltage formation is in a discontinuous manner, i.e. the space vector $u_L^*$ is formed in the average over a pulse half period $\frac{1}{2} T_p$ by a sequence of rectifier switching states $j$ and/or voltage space vectors $u_L^*$. There, the continuous rotation of the space vector $u_L^*$ is approximated by shifting the reference voltage vector in phase for a respective following pulse half period $u_L^{*+} = u_L^{*+}(t_i + \frac{1}{2} T_p)$, $u_L^{*+} = u_L^{*+}(t_i + \frac{1}{2} T_p)$ (the discrete time $t_i$ defines the position of a pulse half period within the mains period $T_0$).

As Fig.3 shows, there are 7 input voltage space vectors available for the approximation of $u_L^*$. With regard to a best possible approximation one applies only those rectifier input voltage space vectors $u_L^*$ lying in the immediate vicinity of the vector tip $u_L^*$ or those switching states $j$ which are assigned to the corner points of that triangular region of the space vector plane into which the tip of the vector $u_L^*$ points [14].

2.2 Formation of the Center Point Current

As Fig.2 clearly shows, by turning on the power transistor of a phase ($S_{i \rightarrow T}$, $i = R, S, T$) the corresponding phase current $i_{u,i}$ is fed into the neutral point $M$. For the total center point current being formed there by all phases we therefore have [12]...
modified ramp comparison current controller (cf. Fig.4: Block diagram of a conventional ramp comparison input cmnt lines for all phases. In the case at hand converter switching state multipliers for determining the phase current reference values, no mains ia'i. The switching decisions formation on the sign of the phase currents (cf. Eq.(1)). Furthemore shown: voltage pre-control). There, the control of the amplitude of the input current fundamental is performed via the amplitude $I_D$ of the carrier signal $i_D$.

$$i_m = s_x i_{u,i} + s_y i_{u,j} + s_t i_{u,j}.$$  

(4)

Accordingly, the switching states of the rectifier system lead to center point currents $i_m$ as compiled in Tab.1.

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Tab.1: Center point current $i_m$ in dependency on the rectifier switching state $(s_x, s_y, s_t)$.

3 Reconstruction of the Mains Phase Currents based on Center Point Current Measurement

According to Tab.2 the center point current $i_m$ within each pulse half period is formed by sections of in any case two input phase currents $i_{u,i}$. In order to minimize the measuring effort it therefore is near at hand to employ only a single current sensor in the connection to the output voltage center point (instead of a direct measurement of at least two input phase currents) and to reconstruct the phase current shapes under consideration of the the actual converter switching state $(s_x, s_y, s_t)$.

![Block diagram of a conventional ramp comparison input current control](image-url)

Fig.4: Blocking diagram of an inversion ramp comparison input current control (cf. (a)). The amplitude $I_0$ of the phase current reference values $i_{u,i}$ is set by an outer output voltage controller (not shown). For the sake of clarity signal paths being equivalent for all phases are combined into double lines for all phases. In the case at hand $R(s)$ is realized by a P-type controller. The switching decisions $s_j$ of the phase comparators have to be inverted for sign($u_{i,j}$) $= -1$ (13) due to the dependency of the rectifier input voltage formation on the sign of the phase currents (cf. Eq.(1)). Furthermore shown: modified ramp comparison current controller (cf. (b)) being characterized by low realization effort (no need to sense the mains voltage, no analog multipliers for determining the phase current reference values, no mains voltage pre-control). There, the control of the amplitude of the input current fundamental is performed via the amplitude $I_D$ of the carrier signal $I_D$. 

\[
I_m = s_x i_{u,i} + s_y i_{u,j} + s_t i_{u,j}.
\]

(4)

Accordingly, the switching states of the rectifier system lead to center point currents $i_m$ as compiled in Tab.1.

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Tab.2: Switching state sequences and corresponding formation of $i_m$ by sections of input phase currents $i_{u,i}$ for $\phi_k \in \{\varphi_k^S, \varphi_k^D\}$. The consideration is based on the assumption of a high modulation index, i.e. $\varphi_k^S > \frac{1}{2} \varphi_k^D$ as typically given for the PWM rectifier systems with high output voltage utilization.

Therefore, in analogy to [8] and [9] the time-continuous phase current information which is required for a ramp comparison input current control can be derived by a state observer modeling the rectifier system AC side and the estimation error can be corrected based on measuring values of the center point current $i_m$ (basic principle of the Luenberger observer). The estimated value $\hat{i}_{u,i}$ of a phase current $i_{u,i}$ is calculated by integration of the voltage drop $u_{i,i}$ across the respective input inductor $L_i$. In time intervals where the center point current $i_m$ is formed by the input current $i_{u,i}$ of a phase $i$ (cf. Tab.1), a correction control $H(s)$ is activated in this phase ($\delta_i \to 1$). As a result the estimated phase current $\hat{i}_{u,i}$ is corrected to the actual phase current shape $i_{u,i}$. (An estimation error $\hat{i}_{u,i} - i_{u,i}$ could result, e.g., due to inaccurate parameters of the system model or an inaccurate measurement of the voltage drop across the input inductors.) Therefore, according to Tab.1 one has to perform an inversion of the estimated center point current $i_m$ for the switching states $j = (011)$, (101) and (110) (cf. Tab.3) before comparing it with the estimated phase current $i_{u,i}$.

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Tab.3: Gating signals $\hat{s}_x$, $\hat{s}_y$, $\hat{s}_t$ of the switches $S_x$, $S_y$, $S_t$ closing the feedback loops provided for the correction of the estimation $i_{u,i} - i_{u,i}$ of the phase models in dependency of the rectifier switching state $j = (s_x, s_y, s_t)$. The auxiliary signal $\delta$ is employed for controlling the inversion of $i_m$ which has to be performed for $j = (011), (101), (110)$. The switching states (000) and (111) result in $i_m = 0$, accordingly, no correction of the observer outputs is possible ($\delta = 0$) and the value of $\delta$ is of no meaning.

Remark: The inductor voltages $u_{i,i}$ can be measured directly by differential amplifiers or by auxiliary secondary windings on the input inductors. Alternatively, the voltages also could be derived with low effort from the mains phase voltages $u_{i,i}$ (as available from the calculation of the phase current reference values, cf. Fig.4), the converter switching state $j = (s_x, s_y, s_t)$ and the output voltage $U_O$ (which in any case has to be measured in connection with the output voltage control or could be assumed here to be identical with the output voltage reference value for high quality output voltage control) based on

$$u_{i,i} = u_{i,i} - (u_{i,j} - u_{i,i})$$

and/or

$$u_O = \frac{1}{2} (u_{i,i} + u_{i,j} + u_{i,j})$$

(5)
(the common-mode voltage component \( u_0 \) of the rectifier input voltages has no influence on the current formation because of the missing connection between the mains star point \( N \) and the rectifier output voltage center point \( M \)). However, due to the dependency of the input voltage formation on the sign of the corresponding input current (cf. Eq. (1)) the quality of the input current reconstruction based on Eq.(6) could be impaired in the vicinity of the phase current zero crossings.

Due to the missing connection between mains star point \( N \) and the center point \( M \) of the rectifier output voltage the sum of the input phase currents is forced to zero, i.e.

\[
i_{U^R} + i_{U^S} + i_{U^T} = 0,
\]

which means that only 2 of the 3 rectifier input inductors represent independent energy storage devices. The current in the third input inductor is defined unequivocally if the currents of the other two phases are known and, therefore, does not represent a state variable. Therefore, the system model basically could be limited to two phases. The advantage of providing a model for each phase (cf. Fig.1) is the resulting phase symmetry of the observer which gives the opportunity of a direct correction of a phase model output for each switching state resulting in a center point current. However, there a system of second order is represented by a model of third order. Therefore, in order to ensure Eq. (7) also for the estimated phase currents \( i_{U^i} \) an additional controller \( K(s) \) has to be provided which corrects a deviation \( i_0 \) of the sum of the estimated phase current values from zero. Since during each pulse half period in any case the estimated current values of two phases are corrected by the respective controllers \( H(s) \) due to \( K(s) \) also the estimation of the third phase current is with low error.

### 4 Practical Realization of the Observer

As shown in Fig.1 the measurement of the voltage \( u_{U^i} \) across an input inductor is realized advantageously by an auxiliary secondary winding \( N_{Zu} \). For high resistance termination of the auxiliary winding there an output signal \( u_{U_{Zu}} \) results which directly is proportional to the rate of change \( di_{U^i}/dt \) of the respective input phase current. The reconstruction of the phase current therefore can be achieved with low effort by integration of \( u_{U_{Zu}} \) (cf. Fig.5, integrators \( Q_1, Q_2, Q_3 \)). There, in contrast to measuring the total voltage occurring across the inductors

\[
u_{U^i} = \frac{dL_i i_{U^i}}{dt}
\]

(e.g., by using a differential amplifier) the parasitic ohmic component \( i_{U^i} R_L \) must not be taken into account by the circuit model. As further advantage this form of voltage measurement provides galvanic isolation from the power circuit.

**Remark:** As shown in section 5 for rectifier systems in the power range of 5kW...20kW the input inductors typically show a lower limit of the inductive behavior (i.e., change from inductive to resistive behavior) at frequencies \( f_L = \frac{1}{2\pi R_L L} = 10 \ldots 15 \text{Hz} \) which is quite close to the mains frequency \( f_N \). (\( f_L \) could be considered in the reconstruction of the current by a resistor connected in parallel to the capacitor \( C_L \) of the integrator).

**Fig.5:** Practical realization of the phase current observer in analogue technique. For realization in SMD technique the circuit covers a printed circuit board area of \( 40 \text{mm} \times 40 \text{mm} \).
4.1 Circuit Structure

The analogue circuit shown in Fig.5 is a direct translation of the block diagram of the input current observer depicted in Fig.1 into hardware, a detailed description therefore should be omitted for the sake of brevity.

However, it is important to note that the turn-on of the analog switches $S_i$ is delayed by RC-elements $R_p$, $C_p$ ($t_d$ in Fig.7) with reference to the signals $s_i$, which are derived by a 256-bit TTL-PROM $Q_6$ (e.g., AMD, AM27S19ACP) according to Tab.3 from the switching functions $s_i$. This realizes a blanking of the measured center point current $i_{ocn}$ for the correction control loops $H(s)$ in the time period required for the transition of $i_{ocn}$ to the actual signal level after a change of the rectifier switching state has occurred. The width of this transition period is defined by the time delay of the gate drive circuits of the power transistors and by the bandwidth and/or rise time of the amplifiers $Q_2$ and $Q_6$.

Contrary, the control of the inversion $Q_7$ of $i_{ocn}$ is without delay directly by $S$. Accordingly, the total blanking interval $t_d$ is available for the settling of the output of $Q_2$ which due to the large step change in the input signal is with limited dynamic as defined by the slew-rate of the operational amplifier employed.

5 Experimental Analysis

The theoretical considerations are verified in the following by a practical application of the observer for the determination of the instantaneous phase current values for a ramp comparison input current control of a prototype of the VIENNA Rectifier I.

Operating parameters of the VIENNA Rectifier I:

- Mains voltage: $U_o = 400 \, V_{max}$ (line-to-line)
- Rated power: $P_o = 10 \, kW$
- Output voltage: $U_o = 670 \, V$
- Switching frequency: $f_r = 25 \, kHz$

The input inductors of the system are realized with toroidal iron powder cores MICROMETALS T184-40 having $N_1 = 72$ turns of litz wire 20x 0.355CuL. The ohmic resistance of the winding amounts to $R = 60 \, m\Omega$.

Accordingly, the dimensioning of the integrators $R_i$ and $C_i$ is set to be a factor of $10$ below the current zero crossings cannot be considered in a simple form for the integration of the inductor voltages

$$u_{L,i} = \frac{N_i}{N_1} \left( \frac{L_i(\dot{u}_{L,i})}{dt} + \frac{dL_i(\dot{u}_{L,i})}{dt} \right).$$

Accordingly, the dimensioning of the integrators $Q_2$, $Q_6$ and $Q_9$ is based on an average inductance value.

Aiming for a low realization effort the correction controllers $H(s)$ and $K(s)$, $Q_5$, $Q_6$, $Q_9$ and $Q_{10}$ are realized by simple proportional amplifiers. The amplification is selected such that the constant time of the first-order system behavior resulting for closed control loop in connection with the respective integrator is in the range of $t_\gamma = 0.25...0.5 \, T_p$. Because the feedback loop is closed always only in sections of the pulse periods then the actual time constant will be $t_\gamma = 2...5 \, T_p$. Accordingly, the reconstructed phase currents $i_{ocn}$ will show a correct fundamental amplitude independent of inaccuracies of the system model. The remaining deviation of the time behavior of the ripple components of the currents $i_{ocn}$ from the actual shape of the input current ripple is of no significance for a ramp comparison control of the input phase currents.

Independent of the non-linear behavior of the input inductors $\Sigma_i$ has to be fulfilled by the reconstructed phase current values. If with respect to the continuous action of $K(s)$ the gain of $Q_6$ is set to a factor of 10 below the gain of $H(s)$ and/or of the amplifiers $Q_5$, $Q_6$ and $Q_9$ both correction feedback loops show approximately equal dynamic and a high quality of the phase current reconstruction is achieved despite the interruption of the action of $H(s)$ in $N_v$-wide intervals of a mains period (cf. Figs.9 and 11(a)).

It is important to note that the correction of the integrator outputs is not connected to an operation of the rectifier power circuit, but in a continuous manner also in intervals with zero output power and/or in case of intermittent operation (as occurring for low output power levels). In this case the switching functions resulting from the intersection of the pre-control...
functions \( m_1 \) and the carrier signal \( i_0 \) are not applied to the gate drive circuits of the power transistors \( S_i \) but are applied to the input of \( Q_1 \). In connection with \( i_{M,m} = 0 \), as given for missing center point current (no load condition) therefore also \( i_{LT} = 0 \) is guaranteed by the correction controllers \( H(s) \) and \( K(s) \), and/or an influence of the offset quantities of the operational amplifiers \( Q_i, Q_2, Q_3 \) on the current reconstruction is suppressed.

5.3 Measuring Results

Figure 6 verifies the theoretical considerations given in section 2.2; for \((t_m, s_0, s_y) = (110)\) the center point current \( i_M \) and the phase current \( -i_T \) show identical time behavior.

![Figure 6: Center point current \( i_M \), input phase current \( -i_{LT} \) and phase switching functions \( s_t \); scales: \( 5A/\text{div}, 10V/\text{div}, 10\mu s/\text{div} \).]

As Fig.7 shows the change of \( i_M \) is delayed with reference to the rising edge of \( s_T \) due to the time delay of the gate drive circuit and the switching time of the power transistor \( S_T \). The rate of rise of \( i_{M,m} \) is relatively low due to the limited bandwidth of the amplifiers \( Q_3 \) and \( Q_6 \) as caused by the high gain of \( a = 10 \). The transition period is suppressed for the observer correction by activating the correction control loop with a time delay \( (R_D, C_D \text{ in Fig.5}) \); contrary, the interruption of the correction at the falling edge of \( s_T \) is without delay.

A change of the switching state of the rectifier results in a step change of the line-to-line input voltages and of the common-mode component \( u_0 \) of the rectifier input phase voltages (and/or of the output voltage center point with reference to earth). This stimulates a resonant circuit formed by parasitic capacitances \( C_E = 500pF \ldots 1nF \) of the load circuit and of the power semiconductors and by the input inductors \( L \) and/or results in a synchronous oscillation of the voltages across the input inductors \( L \) as depicted in Fig.8 for Phase \( T \). The corresponding common-mode currents remain limited to relatively low values due to the high characteristic impedance of the resonant circuit and therefore cannot be identified in the shape of the phase currents.

According to Fig.9 within a mains period the correction of a phase current observer is interrupted only in intervals of a width of \( \pi/6 \) (for high modulation index) lying symmetrical to the maxima of the corresponding phase current. Within these intervals the correction of the phase current observer is in an indirect manner via \( Q_3 \) and/or \( K(s) \) and the phase current observers of the other two phases operating with activated correction control (cf. Fig.10(b)). This ensures a high quality of the current reconstruction throughout the whole mains period.

We would like to point out that the very good coincidence of the actual and of the reconstructed current shape is maintained also in the vicinity of the phase current zero crossings (cf. Eq.(1)) which could be considered being critical due to the dependency of the formation of the rectifier input phase voltage \( u_{LT} \) on the sign of the respective phase current (cf. Eq.(1)).
Fig. 10: Output signal $U_{H,T}$ of the P-type controller $Q_0 \ (H(s)$ in Fig.1) correcting the output of integrator $Q_1$ and output signal $U_K$ of the P-type controller $Q_2 \ (K(s)$ in Fig.1) ensuring $\Sigma_i = 0$. Furthermore shown are the time behavior of the actual and the reconstructed input current of phase $T$ within a section of the mains period (a) for active (direct) observer output correction via $H(s)$, i.e. closed loop operation of the phase current observer $Q_2$ \ (2A/div, 10μA/div), (b) for only indirect correction of the integration of $u_{L,T}$ via $K(s)$ and/or $\dot{x}_T$ remaining at 0 (2A/div, 10μA/div), and (c) in the vicinity of the zero crossing of $i_{L,T}$ (1A/div, 50μA/div). The scaling of $u_{H,T}$ (1V/div) and $u_K$ (10V/div) considers the different gains of the controllers $H(s)$ and $K(s)$; therefore, equal magnitudes of the signals shown result in an equal influence on the output of the integrator $Q_2$.

Fig. 11: Sensitivity of the phase current reconstruction concerning inaccuracies of the inductance value on which the integration of the voltages $u_{L,Tb}$ is based. (a): zero sequence current correction activated, (b): no zero sequence current correction, i.e. $K(s) = 0$.

$H(s)$. Accordingly, also the output of the observer of the third phase shows a low estimation error due to the indirect correction via the zero sequence current controller $K(s)$. In case the zero sequence component correction is disabled, i.e. $K(s) = 0$, the reconstruction of a phase current is in sections where the correction via $H(s)$ is interrupted (cf., e.g., sections with $\dot{x}_T = 0$ in Fig.9) independent of the other phases. This results in a relatively high deviation of the reconstructed phase current $i_{L,dc=\infty}$ from the actual current shape $i_{L,T}$ in case the inductance considered by the system model (integrator) is different from the actual inductance value.

6 Conclusions

In this paper a simple concept for observer-based reconstruction of the continuous shape of the input phase currents of a VIENNA Rectifier is proposed. For current measurement there only a single AC current sensor in the connection to the output voltage center point is employed and the realization costs (on a single component price basis) for deriving the phase current information are reduced by about a factor of 4 as compared to employing compensated Hall-effect current transducers in two input lines. Additionally, problems resulting from an offset of the measured current signals or a different gain or drift of two current transducers are avoided inherently. Furthermore the concept is insensitive to a non-linear behavior of the input inductors and therefore can be used advantageous for realizing a highly dynamic ramp comparison phase current control also for application of input inductors with iron powder cores.

In case the reference potential (ground) of the signal electronics is connected to the center point $M$ of the rectifier output voltage the AC current sensor can be replaced by a shunt what results in an additional reduction of the realization costs. According to the lower rms value of $i_{L,T}$ as compared to
the rms value of the phase current (typ. $I_{rms} = 0.25...0.5 \times I_{rms}$) there also the losses occurring for equal magnitude of the sensor output signal are reduced. However, there is a potential risk of a disturbance of the signal and control electronics by capacitive leakage currents to earth occurring due to the common mode voltage of $M$ with switching frequency (cf. Fig.5(b) in [18]).

Aiming for a further reduction of the realization effort of the control of the VIENNA Rectifier I the continuation of the research will be on a simplified concept of the ramp comparison current control (cf. Fig.4(b), [19]) which can be realized without analog multipliers for phase current reference value generation and does not require input voltage information. The approach is known from single-phase power factor correction [20] and has been treated in different form for three-phase rectifier systems in [21].

Furthermore, the application of a modified version of the center point current measurement [22] featuring a detection of an earth-fault of the rectifier output voltage (similar to the concept for earth fault detection known for two-level inverter systems in connection with DC link current based phase current reconstruction [5], [23]) shall be investigated.

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References


