ZVS of Power MOSFETs Revisited

M. Kasper,
R. Burkart,
G. Deboy,
J. W. Kolar

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Abstract—Aiming for converters with high efficiency and high power density demands converter topologies with zero-voltage switching (ZVS) capabilities. This letter shows that in order to determine whether ZVS is provided at a given operating point, the stored charge within the MOSFETs has to be considered and the condition $L^2 f_t^2 \geq 2Q_{\text{oss}} V_{\text{DC}}$ has to be fulfilled. In the case of incomplete soft switching, nonzero losses occur which are analytically derived and experimentally verified in this letter. Furthermore, the issue of nonideal soft-switching behavior of Si superjunction MOSFETs is addressed.

Index Terms—Power MOSFET, zero-voltage switching (ZVS).

I. INTRODUCTION

W ith the emergence of wide bandgap semiconductors such as SiC JFETs and MOSFETs and GaN HEMTs, power electronic converters have seen a significant performance increase due to the improved figure-of-merit (FOM = $1/\sqrt{R_{\text{DS,on}}C_{\text{oss}}}$ [1]) of these devices compared to traditional Si semiconductors. The improved switching performance allows us to operate systems at higher switching frequencies and, thus, to reduce the size of passive components. At high frequencies, however, the switching losses become a limiting factor again even for wide bandgap semiconductors. Thus, topologies providing soft switching are preferred such as, e.g., phase-shift full-bridge (PSFB), dual active bridge (DAB) or cascaded buck-boost converters [2] for dc–dc conversion, and triangular current mode (TCM) boost converter [3] for power factor corrected (PFC) ac–dc conversion, as shown in Fig. 1. For a design and optimization of a converter system with zero-voltage switching (ZVS), it is crucial to identify the conditions under which soft switching can be achieved. A basic requirement for ZVS is a semiconductor half-bridge with an inductive element connected to the midpoint, which is also common to the topologies of Fig. 1. In order to calculate the required energy stored in the inductive component at the beginning of a switching transition for achieving soft switching, a practical approach such as presented in [4] can be used.

Fig. 1. Popular ZVS converter topologies: (a) PSFB converter, (b) DAB converter, (c) cascaded buck–boost converter with constant switching frequency ZVS modulation [2], and (d) TCM PFC rectifier. The basic structure of all soft-switching topologies consisting of a MOSFET bridge leg and an output inductance $L$ is highlighted.

This letter, however, introduces an analytical approach to specify the conditions for ZVS, which only relies on data sheet values of the semiconductors. At first, the nonlinear behavior of the parasitic MOSFET capacitances is described in Section II. Section III analyzes the conditions to achieve ideal soft switching. In Section IV, analytical formulas are presented that allow to calculate the losses associated with incomplete soft switching, i.e., turn-on of switches at nonzero voltage. The derived equations are validated with measurements on different hardware setups with different types of semiconductors in Section V. Finally, Section VI summarizes the key results of this letter.

II. NONLINEAR PARASITIC MOSFET CAPACITANCES

It is widely known that the parasitic output capacitance $C_{\text{oss}}$ of MOSFETs exhibits a nonlinear dependence on the applied drain–source voltage $V_{\text{DS}}$, which is shown in Fig. 2(a) for a low-voltage Si MOSFET (BS046N100NS3/Infineon). Due to this nonlinearity, the charge stored in parasitic capacitances is also a function of the applied voltage, as shown in Fig. 2(b) for the charge $Q_{\text{oss}}$ stored in $C_{\text{oss}}$. In order to facilitate the modeling of
MOSFETs, a linear charge-equivalent capacitance $C_{Q, eq}$ can be introduced which exhibits the same amount of stored charge as the nonlinear capacitance at a given drain–source voltage $V_{DS}$ [5], i.e.,

$$C_{Q, eq}(V_{DS}) = \frac{Q_{oss}(V_{DS})}{V_{DS}} = \int_{0}^{V_{DS}} C_{oss}(v) \, dv.$$

In a similar way, the energy $E_{oss}$ stored in the nonlinear capacitance $C_{oss}$ can be determined. In Fig. 2(b), the blue shaded area enclosed between the graph of the charge $Q_{oss}$ and the $y$-axis equals the energy which is stored in $C_{oss}$ at a given voltage $V_{DS}$. Thus, a linear energy-equivalent capacitance $C_{E, eq}$ that stores the same amount of energy as $C_{oss}$ at a selected voltage $V_{DS}$ needs to have the same enclosed area, i.e.,

$$C_{E, eq}(V_{DS}) = \frac{2 \cdot E_{oss}(V_{DS})}{V_{DS}^{2}} = \frac{2 \cdot \int_{0}^{V_{DS}} v \cdot C_{oss}(v) \, dv}{V_{DS}^{2}}.$$

As a result, the energy-equivalent capacitance $C_{E, eq}$ and the charge-equivalent capacitance $C_{Q, eq}$ can be calculated for every drain–source voltage $V_{DS}$ [cf., Fig. 2(c)]. It can be seen that the values of these capacitances differ by a factor of up to $C_{Q, eq}(V_{DS, \text{max}})/C_{E, eq}(V_{DS, \text{max}}) = 1.5$. For other MOSFET devices, such as superjunction MOSFETs, the equivalent capacitances may even differ up to a factor of 4 to 5. This difference implies the necessity to clarify which equivalent capacitance has to be used in the case of modeling the soft-switching behavior of MOSFETs.

III. CONDITIONS FOR IDEAL SOFT-SWITCHING

In order to avoid the losses caused by hard-switching transitions of MOSFETs, ZVS is commonly applied. This requires the presence of an impressed current of an inductive component which charges/discharges the output capacitances of the MOSFETs within a bridge leg during the interlocking time of the associated gate signals, as visualized in Fig. 3 for a transition where switch $S_2$ turns off and resonant transition starts with additional current path through the dc source (For simplicity reasons, the parasitic output capacitances are assumed to be linear); (c) end of transition when the drain–source voltage of $S_2$ has reached the source voltage, i.e., $v_2 = V_{DC}$, and switch $S_1$ turns on at zero voltage. As a result of the transition, the charge $Q_{oss}$ was moved from switch $S_1$ to the dc source and the energy of the inductor $L_{oss}$ is zero whereas the total energy stored in the MOSFET bridge leg remains unchanged. Thus, the condition for complete soft switching equals $\frac{1}{2} L_{T} I_{T}^{2} \geq Q_{oss}(V_{DC}) \cdot V_{DC}$.
dependence of \( V_{DC} \). This is also typically the case in half-bridge configurations with bidirectional power flow capability.

At the beginning of the transition (\( t < t_1 \)), the current \( i_L \) of the inductor is free-wheeling through \( S_2 \) and the output capacitance \( C_{oss,1} \) of switch \( S_1 \) is charged to the source voltage \( V_{DC} \). Assuming a linear inductance, the energy within the system for \( t < t_1 \) is, therefore, equal to

\[
E_{initial} = E_{oss}(V_{DC}) + \frac{1}{2} L I_1^2.
\]  

During the switching transition (\( t_1 < t < t_2 \)), the inductor and the capacitances of the switches form a resonant circuit. The current \( i_L \) is split up between both capacitances and charges \( C_{oss,2} \) and discharges \( C_{oss,1} \). In the case of a complete ZVS transition at the boundary to loosing ZVS, the charging/discharging process is finished at the same time (\( t_2 \)) when the inductor current reaches \( i_L = 0 \) A which is also when switch \( S_1 \) is turned on. Thus, the energy in the system after the ZVS transition equals

\[
E_{final} = E_{oss}(V_{DC})
\]  

and the energy received by the source during the transition equals

\[
E_{delivered} = -Q_{oss}(V_{DC}) \cdot V_{DC}
\]  

since the charge of switch \( S_1 \) was moved by \( i_S \) to the source with voltage \( V_{DC} \). As a result, the energy balance of (3) reveals that the requirement for a complete zero-voltage transition is given by

\[
\frac{1}{2} L I_1^2 \geq Q_{oss}(V_{DC}) \cdot V_{DC}.
\]  

This requires the evaluation of the charge-equivalent (and not the energy-equivalent [6]–[9]) capacitance at the voltage \( V_{DC} \)

\[
\frac{1}{2} L I_1^2 \geq C_{par}(V_{DC}) \cdot V_{DC}.
\]  

Please note that additional parasitic capacitances of the switch node (e.g., PCB capacitances and the parasitic capacitance of the inductor) also influence the required energy of the inductor for soft switching. The parasitic capacitances are assumed to be linear with respect to their capacitance value in dependence of the applied voltage, which allows us to lump them into a total parasitic capacitance \( C_{par} \). Accordingly, considering Fig. 3 the energy term \( \frac{1}{2} C_{par} V_{DC}^2 \) has to be added to the right-hand sides of (7) and (8).

**ZVS losses due to nonidealties:** Even if the aforementioned condition for ZVS is fulfilled, switching losses might still be measured due to following two effects:

1. At large inductor currents, turn-off losses can occur if the gate drive circuitry is too slow to turn-off the semiconductor before the drain–source voltage rises. The resulting overlapping of drain–source current and drain–source voltage leads to losses within the semiconductor.
2. The charging/discharging process of the output capacitances is not free of losses [10]. For SiC MOSFETs, GaN HEMTs, and low-voltage Si MOSFETs, losses of up to 10% of the energy stored in the output capacitance could occur, as indicated by measurements of the authors. For super-junction Si MOSFETs, however, the loss mechanism is a combination of a resistive and a diode-like component and might dissipate more than 50% of the stored energy. More details about the \( C_{oss} \) related losses can be found in [10] and [11]. As a result, a sufficiently larger energy has to be stored in \( L \) to achieve ZVS and/or even with ZVS significant switching losses can occur.

**IV. INCOMPLETE SOFT-SWITCHING**

Even if all nonidealities of real MOSFET circuits (cf., Section III) are disregarded, the soft-switching transition can result in losses if the condition for ZVS, (7), is not fulfilled and/or incomplete soft-switching [incomplete ZVS (iZVS)] occurs. This means that there is still a voltage \( \Delta V \) present across the switch \( S_1 \) that turns on after the resonant transition. In order to calculate the remaining voltage \( \Delta V \), the energy expression \( E_{final} \) has to be revised to

\[
E_{final} = E_{oss}(V_{DC} - \Delta V) + E_{oss}(\Delta V)
\]  

and the energy delivered by the source has to be changed to

\[
E_{delivered} = -(Q_{oss}(V_{DC}) - Q_{oss}(\Delta V)) \cdot V_{DC}.
\]  

The value of \( \Delta V \) can then be found by solving the energy balance of (3) (again for \( E_{dissipated} = 0 \)). Please note that additional parasitic capacitances and resistive losses are not included in this equation.

In the iZVS transition, switch \( S_1 \) turns on while \( C_{oss,1} \) is still charged to \( \Delta V \), which dissipates a certain amount of energy that can be derived by solving the energy balance of

\[
E_{diss, iZVS} = E_{initial, iZVS} - E_{final, iZVS} + E_{delivered, iZVS}.
\]

Before \( S_1 \) turns on, the energy within the system is equal to

\[
E_{initial, iZVS} = E_{oss}(V_{DC} - \Delta V) + E_{oss}(\Delta V).
\]

After \( S_1 \) has turned on, \( C_{oss,2} \) of switch \( S_2 \) is charged to \( V_{DC} \), therefore

\[
E_{final, iZVS} = E_{oss}(V_{DC}).
\]

In order to charge the output capacitance of \( S_2 \) to \( V_{DC} \), the remaining charge

\[
\Delta Q_{S2} = Q_{oss}(V_{DC}) - Q_{oss}(V_{DC} - \Delta V)
\]

has to be taken from the source; accordingly the source delivers the energy

\[
E_{delivered, iZVS} = \Delta Q_{S2} \cdot V_{DC}.
\]
As a result, the dissipated energy of the iZVS transition can be derived and interpreted as

\[
E_{\text{diss, iZVS}} = E_{\text{oss}}(\Delta V) + \Delta Q_{S_1} \cdot V_{\text{DC}} - (E_{\text{oss}}(V_{\text{DC}}) - E_{\text{oss}}(V_{\text{DC}} - \Delta V)) \cdot \text{Share of energy of } Q_{S_1} \text{ which is stored in } S_2.
\]

For the case of a complete soft-switching transition (i.e., \(\Delta V \rightarrow 0\)) the above equation yields \(E_{\text{diss, iZVS}} \rightarrow 0\). For the second limit case of \(\Delta V \rightarrow V_{\text{DC}}\), which denotes hard switching, the energy \(E_{\text{diss, iZVS}} \rightarrow Q_{\text{oss}}(V_{\text{DC}}) \cdot V_{\text{DC}} = C_{Q, \text{eq}} \cdot V_{\text{DC}}^2\) can be used to estimate the losses which occur due to the parasitic output capacitance in the event of hard switching [5]. Please note again that in the case of incomplete soft-switching and also in the case of (full) hard switching, the charge-equivalent and not the energy-equivalent capacitance (as frequently used in literature) is relevant and, therefore, the actual switching losses are greater than switching losses estimated using the energy-equivalent capacitance. Furthermore, nonidealities resulting in additional losses are not included in the equations.

V. EXPERIMENTAL VALIDATION

The theoretical derivations of the previous sections have been experimentally validated and the results are shown in the following.

A. Incomplete Soft-Switching Transition

The incomplete soft-switching process was tested with a bridge leg containing two low-voltage MOSFETs (BS046N100NS3/Infineon) connected to a voltage source with \(V_{\text{DC}} = 60\, \text{V}\) and an inductor with \(L = 4.6\, \mu\text{H}\). The voltage \(\Delta V\), which remains at the switch node after an incomplete soft-switching process, was calculated according to (4) and (9) and is shown in Fig. 4(a) for different values of the initial inductor current \(I_1\) and compared to measurement results. The difference between the measurements and calculations can be attributed to ohmic losses in the conduction path (i.e., coil winding, MOSFETs, PCB) and to additional layout-dependent capacitances which require additional energy to be charged/discharged. In addition, the calculated value of the energy \(E_{\text{diss, iZVS}}\) which is dissipated at this iZVS transition is also shown as a function of the initial inductor current. The transient waveforms of the inductor current and the bridge-leg voltage are depicted for an initial inductor current of \(I_1 = 1.2\, \text{A}\) in Fig. 4(b).

B. Loss Measurements

In order to verify the derived formulas of Section IV of the switching losses occurring in case of incomplete
soft-switching, a measurement setup for precise switching loss measurements [cf., Fig. 5(a)] was used with SiC MOSFETs (C2M0080120D/Cree) which have an almost ideal soft-switching behavior; accordingly the losses of the charging and discharging process of $C_{\text{oss}}$ can be neglected (as discussed in Section III). In this setup, the current and voltage waveforms across the top switch $S_1$ are measured by means of a high-bandwidth oscilloscope and a current shunt which allows us to determine the energy released or stored by this switch during the incomplete soft-switching process and, thus, to verify (16). The experimental setup contains specific layout-dependent parasitic capacitances (e.g., probes, PCB) that are included in the calculations, which yields

$$E_{\text{diss, iZVS, calc}} = E_{\text{diss, iZVS}} + \frac{1}{2} C_{\text{par}} \Delta V^2. \quad (17)$$

The measurements were conducted for different levels of dc-link voltage $V_{\text{DC}}$ and different levels of remaining midpoint voltage $\Delta V$. The results are visualized in Fig. 5(b) and a detailed overview of the measurement results is provided in Table I. The theory is confirmed by the measurements with a high accuracy.

### VI. Conclusion

In order to determine whether soft switching can be achieved in a circuit with a MOSFET bridge leg and an inductor carrying the initial current $i_L = I_1$, the stored charge $Q_{\text{oss}}$ of the MOSFETs has to be considered and the condition

$$\frac{1}{2} L I_1^2 \geq Q_{\text{oss}}(V_{\text{DC}}) \cdot V_{\text{DC}} \quad (18)$$

has to be fulfilled. For the case that the condition for complete soft switching is not fulfilled, the additional losses of the incomplete soft-switching process can be calculated based on the formulas derived in this letter. The formulas also allow to calculate the losses which occur due to the parasitic output capacitances in the event of (full) hard switching. The derived equations have been validated with high accuracy on dedicated measurement setups with low-voltage silicon MOSFETs and high-voltage SiC MOSFETs.

### Table I

**Detailed Comparison of Selected iZVS Loss Measurement Results with Calculated Values**

<table>
<thead>
<tr>
<th>$V_{\text{DC}}$</th>
<th>$\Delta V$</th>
<th>$E_{\text{diss, iZVS, mea}}$</th>
<th>$E_{\text{diss, iZVS, calc}}$</th>
<th>Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>200 V</td>
<td>200 V</td>
<td>8.26 µJ</td>
<td>8.39 µJ</td>
<td>1.5%</td>
</tr>
<tr>
<td>200 V</td>
<td>100 V</td>
<td>1.26 µJ</td>
<td>1.35 µJ</td>
<td>7.0%</td>
</tr>
<tr>
<td>200 V</td>
<td>50 V</td>
<td>0.273 µJ</td>
<td>0.318 µJ</td>
<td>13.9%</td>
</tr>
<tr>
<td>400 V</td>
<td>300 V</td>
<td>11.6 µJ</td>
<td>11.4 µJ</td>
<td>-1.8%</td>
</tr>
<tr>
<td>400 V</td>
<td>100 V</td>
<td>1.11 µJ</td>
<td>1.11 µJ</td>
<td>0.5%</td>
</tr>
<tr>
<td>600 V</td>
<td>400 V</td>
<td>18.1 µJ</td>
<td>18.1 µJ</td>
<td>0.4%</td>
</tr>
<tr>
<td>600 V</td>
<td>200 V</td>
<td>4.13 µJ</td>
<td>4.3 µJ</td>
<td>3.9%</td>
</tr>
</tbody>
</table>

### References


