Identifying and Addressing Important Developments of Power Electronics Core Technologies

Future of Power Electronics

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FEPPCON 2019
Tromsö / Norway / June 26-28/2019

Topology
Components
Control
Design
Manufacturing
Outline

► Performance Trends
► X-Concepts / "Moon-Shot" Technologies
► Power Electronics 4.0
Required Performance Improvements

Environmental Impact... [kg_{Fe} /kW]
[kg_{Cu} /kW]
[kg_{Al} /kW]
[cm^{2}_{Si} /kW]

Future  Cost / Cost / Cost & Robustness & Availability & Recyclability

- Power Density [kW/dm^{3}]
- Power per Unit Weight [kW/kg]
- Relative Costs [kW/$]
- Relative Losses [%]
- Failure Rate [h^{-1}]
**S-Curve of Power Electronics**

- **Power Electronics 1.0 → Power Electronics 4.0**
- **Identify “X-Concepts” / “Moon-Shot” Technologies**
- **10x Improvement NOT Only 10% !**

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<table>
<thead>
<tr>
<th>Performance</th>
<th>Effort / Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Emergent</td>
<td>Established</td>
</tr>
<tr>
<td>Existing Technology</td>
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</tbody>
</table>

- **SCRs / Diodes**
- **Solid-State Devices**
- **Modulation Concepts**
- **Control Concepts**

- **Power MOSFETs & IGBTs**
- **Microelectronics**
- **Circuit Topologies**
- **Digital Power Modeling & Simulation**
- **Super-Junct. Techn. / WBG**

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**1958** to **2025**
The term "electronic power converter" needs some definition. The object may be to convert power from direct current to alternating current for d-c power transmission, or to convert power from one frequency into another, or to serve as a commutator for operating an a-c motor at variable speed, or for transforming high voltage direct current into low-voltage direct current. Other objectives may be mentioned. It is thus evidently not the objective but the means which characterizes the electronic power converter. Other names have been used tentatively but have not been accepted. The emphasis is on electronic means and the term is limited to conversion of power as distinguished from electric energy for purposes of communication. Thus the name is a definition.
AC-DC CONVERTER HAVING AN IMPROVED POWER FACTOR

Inventor: Daniel M. Mitchell, Cedar Rapids, Iowa

Assignee: Rockwell International Corporation, El Segundo, Calif.

Appl. No.: 414,757

Filed: Sep. 3, 1982

ABSTRACT
An AC to DC converter utilizes a first power converter for converting an AC signal to a DC signal under the control of a control signal. The control signal is generated by a control circuit that includes a first analog generator that provides a first signal that is analogous to the voltage of the AC signal that is to be converted. A second analog generator generates a second signal that is analogous to the current of the AC signal that is to be converted and a third analog generator generates a third signal that is analogous to the voltage of the DC output signal. The third signal and the first signal are multiplied together to obtain a fourth signal. The control signal is generated from the fourth signal and the second signal and is used to control the power converter such that the waveform of the current of the AC signal is limited to a sinusoidal waveform of the same frequency and phase as the AC signal.

8 Claims, 2 Drawing Figures
ZVS/TCM Operation of Bridge-Legs

- Avoids Utilization of Slow Internal Diodes of Si MOSFETs
- Enables High Sw. Frequency → Low Filter Inductor Volume

● Generation of Continuous / Sinusoidal Motor Voltage w/o CM-Component

Source: Joensson

Source: NFO Sinus

PCIM’88 (POWER CONVERSION) CONERENCE
DECEMBER 9-10, 1988
TOKYO, JAPAN

Source:
— Basic Topologies Known > 30...40 Years
— Min. Complexity Circuits Used in Industry
— Optimization of Modulation / Control Completed
— Several Solutions of Equal Performance

... “Refinements” & Hybrid SCCs
& Comparative Evaluation (!)
Passive Components

Magnetics as Example

Source: www.electronics-tutorials.ws
**Operation Frequency Limit (1)**

- **Serious Limitation of Operating Frequency by HF Losses**
  - Core Losses (incr. @ High Frequ. & High Operating Temp.)
  - Temp. Dependent Lifetime of the Core
  - Skin-Effect Losses
  - Proximity Effect Losses

\[
p_{VE} = \frac{\Delta P_{VE}}{\Delta E} = k \cdot f^\alpha \cdot \hat{B}^\beta = \text{const.}
\]

- Adm. Flux Density for given Loss Density
- Skin-Factor \(F_s\) for Litz Wires with \(N\) Strands

Source: Prof. Albach, 2011
Operation Frequency Limit (2)

- **Higher Frequency** Results in Smaller Size only Up to Certain Limit (for MnZn Core-Based Designs)
- **Optimal Converter Operating Frequencies** < 1MHz
- **Difficult to Manufacture**

Source: Philips

- Automated Manufacturing → Magnetic Integration / PCB-Windings / Planar Shapes
X-Technology #1 Wide Bandgap Power Semiconductors
Low $R_{DS(on)}$ High-Voltage Devices (1)

- High Critical E-Field of SiC $\rightarrow$ Thinner Drift Layer
- High Maximum Junction Temperature $T_{j,max}$

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>GaAs</th>
<th>4H/6H-SiC</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_g$ (eV)</td>
<td>1.12</td>
<td>1.4</td>
<td>3.0-3.2</td>
<td>3.4</td>
</tr>
<tr>
<td>$E_c$ (MV/cm)</td>
<td>0.25</td>
<td>0.3</td>
<td>2.2-2.5</td>
<td>3</td>
</tr>
<tr>
<td>$\mu_n$ (cm$^2$/Vs)</td>
<td>1350</td>
<td>8500</td>
<td>1000-1000</td>
<td>1000</td>
</tr>
<tr>
<td>$\varepsilon_r$</td>
<td>11.9</td>
<td>13</td>
<td>10</td>
<td>9.5</td>
</tr>
<tr>
<td>$V_{sat}$ (cm/s)</td>
<td>$1\times10^7$</td>
<td>$1\times10^7$</td>
<td>$2\times10^7$</td>
<td>$3\times10^7$</td>
</tr>
<tr>
<td>$\lambda$ (W/cmK)</td>
<td>1.5</td>
<td>0.5</td>
<td>3-5</td>
<td>1.3</td>
</tr>
</tbody>
</table>

For 1kV: $R_{on}^* = \frac{4V_B^2}{\varepsilon \mu_n E_C^3}$

$R_{on,SiC}^* \approx \frac{1}{300} R_{on,Si}^*$

- Massive Reduction of Relative On-Resistance $\rightarrow$ High Blocking Voltage Unipolar Devices
Low $R_{DS(\text{on})}$ High-Voltage Devices (2)

- Low Circuit Complexity
- High Power Conversion Efficiency
- SiC / GaN (Monolithic AC-Switch) / Diamond

*High Heat Conductivity & Excellent Switching Performance*
Low Switching Losses

- Si-IGBT \(\rightarrow\) Up to 6.5\(\text{kV}\) / Rel. Low Switching Speed
- SiC-MOSFETs \(\rightarrow\) Up to 15\(\text{kV}\) (1\(^{\text{st}}\) Samples) / Factor 10...100 Higher Sw. Speed

**Si-IGBT / Hybrid-Pack 2**

![Graph showing turn-off characteristics](image)

- Turn-off @ \(T_j = 25^\circ\text{C}\)
- \(U_{\text{in}} \cdot I_{\text{in}}\)
- \(25\text{nH}\)
- \(7\text{A/\text{ns}}\)
- \(6\text{V/\text{ns}}\)

\(E_{\text{off}} = 45900\ \mu\text{J}\)

\(\rightarrow\) 8 \(\text{kV/\mu}\text{s}\) at 400\(\text{V}\)

**SiC-MOSFET / (scaled for low inductance)**

![Graph showing turn-off characteristics](image)

- Turn-off @ \(T_j = 25^\circ\text{C}\)
- \(U_{\text{in}} \cdot I_{\text{in}}\)
- \(16\text{par. Chips}\)
- \(6\text{nH}\)
- \(50\text{A/\text{ns}}\)
- \(33\text{V/\text{ns}}\)

\(E_{\text{off}} = 4672\ \mu\text{J}\)

\(\rightarrow\) 44 \(\text{kV/\mu}\text{s}\) at 400 \(\text{V}\)

- Extremely High \(\text{di/\text{dt}}\) & \(\text{dv/\text{dt}}\) \(\rightarrow\) Challenges in Packaging / EMI
Challenges

IDEA: F.C. Lee
Circuit Parasitics (1)

- Extremely High $\frac{di}{dt}$
- Commutation Loop Inductance $L_s$
- Allowed $L_s$ Directly Related to Switching Time $t_s$  

$$L \frac{di}{dt} = u$$

$$L_s \leq \alpha \frac{U_i}{I_L} = \alpha t_s \frac{U_i}{I_L}$$

- Advanced Packaging & Parallel Interleaving for Partitioning of Large Currents
Circuit Parasitics (2)

- Extremely High $dv/dt$
- Switch Node Capacitance
- Allowed $C_p$ Directly Related to Switching Time $t_s$  

\[
C \frac{du}{dt} = i
\]

\[
C_p \leq \frac{\alpha I_i}{U_i} = \alpha t_s \left(\frac{U_i}{I_i}\right)^{-1}
\]

- Advanced Packaging & Series Interleaving for Partitioning of Large Voltages
**EMI Emissions**

- Higher \( dv/dt \) \( \rightarrow \) Factor 10
- Higher Switching Frequencies \( \rightarrow \) Factor 10
- EMI Envelope Shifted to Higher Frequencies

\[ f_s = 10kHz \quad \& \quad 5\, kV/us \text{ for (Si IGBT)} \]
\[ f_s = 100kHz \quad \& \quad 50\, kV/us \text{ for (SiC MOSFET)} \]

\[ V_{DC} = 800V \]
DC/DC @ \( D = 50\% \)

- Higher Influence of Filter Component Parasitics and Couplings \( \rightarrow \) Advanced Design
X-Technology #2
Interleaving & Modularity
**Parallel Interleaving (1)**

- Loss-Neutral Multiplication of Switching Frequency
- Reduced Ripple @ Same (!) Switching Losses

\[ f_{S,\text{eff}} = N \cdot f_s \]

\[ \Delta I_{\text{max},N} = \frac{1}{N^2} \Delta I_{\text{max},N=1} \]

\[ \Delta U_{\text{max},N} = \frac{1}{N^3} \Delta U_{\text{max},N=1} \]

- Scalability / Manufacturability / Standardization / Impedance Matching / Redundancy
**Parallel Interleaving (2)**

- Loss-Neutral Multiplication of Switching Frequency
- Reduced Ripple @ Same (!) Switching Losses

\[ f_{S,\text{eff}} = N \cdot f_S \]
\[ \Delta I_{\text{max},N} = \frac{1}{N^2} \Delta I_{\text{max},N=1} \]
\[ \Delta U_{\text{max},N} = \frac{1}{N^3} \Delta U_{\text{max},N=1} \]

- **Scalability / Manufacturability / Standardization / Impedance Matching / Redundancy**
Series Interleaving (1)

- Reduced Ripple @ Same (!) Switching Losses
- Lower On-Resistance @ Given Blocking Voltage → 1+1=2 NOT $2^2 = 4$ (!)
- Extends LV Technology to HV

\[
\Delta I_{\text{max},N} = \frac{1}{N^2} \Delta I_{\text{max},N=1}
\]

\[
\frac{\Delta U_{\text{C,max},N}}{U} = \frac{\pi^2}{32} \left( \frac{f_O}{f_S} \right)^2 \frac{1}{N^3}
\]

- Scalability / Manufacturability / Standardization / Impedance Matching / Redundancy
**Series Interleaving (2)**

- Dramatically Reduced Switching Losses (or Harmonics) for Equal $\Delta i/I$ and $dv/dt$

\[
P_{S,N} \approx P_{S,N=1}\left(\frac{1}{2N^2} \cdots \frac{1}{N^3}\right)
\]

- High Efficiency @ High Effective Switching Frequency → High Power Density
Series Interleaving – Example #1

- Realization of a 99%++ Efficient 10kW 3-Φ 400V_{rms,li} Inverter System
- 7-Level Hybrid Active NPC Topology / LV Si-Technology

![Diagram of inverter system with 7 levels and voltage waveform](image)

99.35% 2.6kW/kg 56 W/in^3
**Series Interleaving – Example #2**

- **Example of Google Little Box Challenge**
- **Target:** 2kW 1-Φ Solar Inverter with Worldwide Highest Power Density
- **Comparative Analysis of Approaches of the Finalists**

- **Source:** R. Pilawa-Podgurski

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**Efficiency (%)**

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<tr>
<th>Power Density (W/in²)</th>
<th>90</th>
<th>91</th>
<th>92</th>
<th>93</th>
<th>94</th>
<th>95</th>
<th>96</th>
<th>97</th>
<th>98</th>
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<td>100</td>
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</tbody>
</table>

- $f_S = 140\text{kHz}$
- $f_{S,\text{eff}} = 6 \times 120\text{kHz} = 720\text{kHz}$

- **3D-Packaging / Integration Highly Crucial for Utilizing Multi-Level Advantages (!)**


**Series Interleaving – Example #2**

- *Example of Google Little Box Challenge*
- *Target: 2kW 1-Φ Solar Inverter with Worldwide Highest Power Density*
- *Comparative Analysis of Approaches of the Finalists*

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**ETH zürich**

**Little-Box 2.0**

- **240 W/in³**
- **97.4%**

**Series Interleaving**

- **215 W/in³**
- **97.6%**

*3D-Packaging / Integration Highly Crucial for Utilizing Multi-Level Advantages (!)*

Source: R. Pilawa-Podgurski
Observation

* Conventional Packaging * → Very Limited Room for Performance Improvement (!)
X-Technology #3

3D-Packaging Automated Manufacturing
3D-Packaging / Heterogeneous Integration

- **System in Package (SiP) Approach**
- **Minim. of Parasitic Inductances / EMI Shielding / Integr. Thermal Management**
- **Very High Power Density (No Bond Wires / Solder / Thermal Paste)**
- **Automated Manufacturing**

*Future Application Up to 100kW (!)*
*New Design Tools & Measurement Systems (!)*
**Monolithic 3D-Integration**

- **GaN 3x3 Matrix Converter Chipset with Drive-By-Microwave (DBM) Technology**
  - 9 Dual-Gate GaN AC-Switches
  - DBM Gate Drive Transmitter Chip & Isolating Couplers
  - Ultra Compact → 25 x 18 mm² (600V, 10A – 5kW Motor)

5.0GHz Isolated (5kVDC) Dividing Coupler

Source: Panasonic ISSCC 2014
X-Technology #4

Automated Design
Digital Twin / Industry 4.0
**Digital Integrated Circuits**

- Exponentially Improving uC / Storage Technology (!)
  - Extreme Levels of Density / Processing Speed
  - Software Defined Functions / Flexibility
  - Cont. Relative Cost Reduction

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**Moore's Law**

- Gulfown Core 6
- Ivy Bridge
- Sandy Bridge
- AMD K10
- Core i7
- AMD K8
- Core2 Quad
- AMD Athlon
- Core2 Duo
- Pentium 4
- Core Duo
- Pentium III
- Pentium M
- Pentium II
- Pentium Pro
- Pentium
- i486
- i860
- MC68020
- 80386
- 80286
- MC68000
- 8086
- 8080
- 8008
- 4004

**Source:** Ostendorf & König / DeGruyter

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- Fully Digital Control of Complex Systems
- Massive Computational Power → Fully Automated Design & Manufacturing / Industrial IoT (IIoT)
Automated Design
Automated Design (1)

Performance Space
- Efficiency
- Power Density
- Costs
- Reliability
- etc.

Design Space

System
- Phase-Shift DC/DC Conv.
- Resonant DC/DC Conv.
- DC Link AC/AC Conv.
- Matrix AC/AC Conv.
- etc.

Components
- Power Semiconductor
- Interconnections
- Inductors, Transf.
- Capacitors
- Control Circuit
- etc.

Materials
- Semiconductor Mat.
- Conductor Mat.
- Magnetic Mat.
- Dielectric Mat.
- etc.

- Evaluation Formulas
- Lifetime Models
- Cost Models
- etc.

- Specifications
- Operation Limits
- Converter Topology
- Modulation Scheme
- Control Concept
- Operation Mode
- Operating Freq.
- etc.

- Doping Profiles
- Geometric Properties
- Winding Arrangements
- Magnetic Core Geometries
- etc.

Mathematical Description of the Mapping  "Technologies" \(\rightarrow\)  "System Performance"
Automated Design (2)

- Based on Mathematical Model of the Technology Mapping
- Multi-Objective Optimization → Best Utilization of the “Design Space”
- Identifies Absolute Performance Limits → Pareto Front / Surface

- Clarifies Sensitivity $\Delta \rho / \Delta k$ to Improvements of Technologies
- Trade-Off Analysis
Automated Design Roadmap

- **End-to-End Horizon of Modeling & Simulation**
- **Design for Cost / Volume / Efficiency Target / Manufacturing / Testing / Reliability / Recycling**

**Autonomous Design → Design 4.0**
- Independent Generation of Full Designs for Final Expert Judgement

**Augmented Design**
- **Suggestion of Design Details Based on Previous Designs**

**State-of-the-Art**
- **User Defined Models and Simulation / Fragmented**

**Assisted Design**
- **Support of the User with Abstracted Database of Former Designs**

- **AI-Based Summaries → No Other Way to Survive in a World of Exp. Increasing # of Publications (!)**
Digital Twin / Industry 4.0
**IIoT in Power Electronics**

- **Digital Twin** → Physics-Based Digital Mirror Image
- **Digital Thread** → “Weaving” Real/Physical & Virtual World Together

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**Physical Asset**

- Operational History
- Maintenance History
- Real Time Operational Data
- FMEA
- CAD Model
- FEA Model

**Digital Twin**

- Physics Based Models
  + Statistical Models
  + Machine Learning

- Fleet Aggregate Data

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- **Model of System’s Past/Current/Future State** → **Design Corrections / Prev. Maintenance etc.**
Scaling Law of Digitalization

- **Metcalfe's Law**

  Moving from Hub-Based Concept to Community Concept Increases Value Exponentially ($\sim n(n-1)$ or $\sim n \log(n)$)

- **Automated Design / Digital Control / Digital Twin / Industry 4.0**
Conclusions
Topologies → Technologies

- Only Incremental Improvements from Topologies / Control Methods etc.
- Consider Converters like “ICs”

Shift to New Paradigm!

- New Textbooks
- New Design Tools
- New Manufacturing Processes
- New Measurement / Testing Devices

- University Research → Technology Partnership OR “Fab-Less” Power Electronics
**S-Curve of Power Electronics**

- **Power Electronics 1.0 → Power Electronics 4.0**
- Identify “X-Concepts” / “Moon-Shot” Technologies
- **10x Improvement NOT Only 10% !**

- **#1** WBG Semiconductors
- **#2** Multi-Cell/Level Concepts
- **#3** 3D-Packaging/Integration
- **#4** Automated Design

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**Performance**

- **Effort / Time**

**S-Curve Phases**

1. **Emerging**
2. **Established**
3. **Mature**

**Technology Phases**

1. **Existing Technology**
2. **Replacement (Disruptive) Technology**

**Key Technologies**

- **Power Electronics**
- **Digital Power Modeling & Simulation**
- **Super-Junct. Techn. / WBG**
- **Power MOSFETs & IGBTs**
- **Microelectronics**
- **Circuit Topologies**
- **Modulation Concepts**
- **Control Concepts**

**Timeline**

- **1958**
- **2015**
- **2025**

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**ETH Zürich**

**Power Electronic Systems Laboratory**
**Future Standardization / Integration**

- **Complicated** → **Basic/Standardized**
- **Discrete** → **Integrated**
- **Single-Obj.** → **Multi-Objective**

- **Main Driver** → **Cost Minimization by Automated High-Volume Manufacturing**
- **Main Enabler** → **Computer-Based Design Providing Insight & Digital Control for Flexibility**
Thank you!