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All-SiC 9.5 kW/dm3 On-Board Power Electronics for 50 kW/85 kHz Automotive IPT System

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***Abstract*— Inductive power transfer (IPT) is widely discussed for the automated *opportunity charging* of plug-in hybrid and electric public transport buses without moving mechanical components and reduced maintenance requirements. In this paper, the design of an on-board active rectifier and dc–dc converter for interfacing the receiver coil of a 50 kW/85 kHz IPT system is designed. Both conversion stages employ 1.2 kV SiC MOSFET devices for their low switching losses. For the dc–dc conversion, a modular, nonisolated buck+boost-type topology with coupled magnetic devices is used for increasing the power density. For the presented hardware prototype, a power density of 9.5 kW/dm^3 (or 156 W/in^3) is achieved, while the ac–dc efficiency from the IPT receiver coil to the vehicle battery is 98.6%. Comprehensive experimental results are presented throughout this paper to support the theoretical analysis.**

***Index Terms*— Electric vehicles, inductive power transmission, magnetic devices, power conversion, silicon carbide.**

I. Introduction

BATTERY electric and plug-in hybrid public transport buses are more and more preferred over conventional diesel-powered vehicles or trolleybuses in urban environments for the reduced noise and exhaust emissions, and the less visible infrastructure [1]–[5]. Electric vehicles (EVs) additionally benefit from lower operating cost and reduced fuel price volatility. However, plug-in plug-in EVs require longer dwell times for the recharging, and the battery presents a major share of the initial cost. Besides, the battery weight increases the vehicle energy consumption and its volume reduces the passenger-carrying capability of public transport vehicles [5].

Therefore, equipment manufacturers have recently presented novel fast-charging concepts with reduced battery capacity and shorter dwell time [5]–[11]. *Opportunity charging* stations distributed at bus stops along the route enable frequent recharging intervals and thus reduce the necessary energy storage capacity. In [5]–[8], mechanical connectors are used to establish a galvanic connection between the charging station and the on-board power electronics. However, as the charging station is fully exposed to the environment, it suffers from corrosion of unprotected metal contacts, and from wear and fatigue of the moving mechanical components.

As an alternative without a galvanic connection, contactless EV chargers using inductive power transfer (IPT) were proposed for public transport buses in [9]–[11]. Using a high-frequency ac current in a transmission coil embedded in the road surface, the battery charging energy is transferred across the air gap between the vehicle and the charging platform to a receiver coil mounted to the EV chassis. As shown in [11], at moderate charging power levels of up to 50 kW, IPT systems can be designed without mechanical positioning systems. Therefore, lower maintenance cost is the main advantage of this technology besides the higher flexibility that results from the elimination of the charging cable.

As a result of the large air gap of the contactless power transfer system, which is defined by the EV ground clearance of typically 100–200 mm, comparably large transmission coils are required in order to achieve a sufficiently high magnetic coupling and a high efficiency of the power transfer. Consequently, the power density of the receiver coil is low compared with the state-of-the-art conductive chargers [12]. While this might be an acceptable compromise given the discussed advantages of the contactless EV charger, the remaining on-board power electronics must have a high compactness due to the limited construction volume on the vehicle.

A miniaturization of the power electronic equipment is typically achieved by increasing the converter switching frequency, an approach that is limited by the switching losses and the degradation of the power semiconductor performance at high junction temperatures. Soft-switching topologies and modulation schemes [13]–[15] largely avoid switching losses and thus push the switching frequency barrier upward. In addition, novel silicon carbide (SiC) or gallium nitride (GaN) wide bandgap (WBG) power devices with reduced switching losses and higher temperature capability can expand today's limits [16]–[21]. In this paper, the excellent switching performance of the state-of-the-art SiC power MOSFET devices is utilized for the design of a highly compact and efficient on-board power converter for the 50 kW contactless EV charger of [12] and [22]–[24].

Power converters for IPT systems typically employ a full-bridge inverter to supply a high-frequency ac voltage to the transmitter coil, which is connected to a capacitor to form a resonant circuit [25]. For the resonant frequency, the upcoming charging standard J2954 by the Society of Automotive Engineers (SAE) proposes 85 kHz as a common operating frequency to ensure interoperability between

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charging equipment of different manufacturers [26]. For a hard-switched pulsewidth modulation, high switching losses occur in the converter as a result of the high switching frequency, even if WBG power semiconductors are employed. Therefore, most IPT power converters only supply a fundamental-frequency rectangular voltage waveform to the coils. Selecting the switching frequency slightly above the resonant frequency allows achieving zero voltage switching (ZVS) of the devices in the inverter, which drastically reduces switching losses. Due to the bandpass characteristics of the resonant circuit, approximately sinusoidal currents result in the transmitter and receiver IPT coils despite the high harmonic content of the applied voltage waveform. A second resonant circuit, tuned to the same frequency, is formed by the receiver coil and a second resonant capacitor. A passive or active rectifier is connected to the receiver-side resonant circuit to produce a dc output voltage. Throughout this paper, a series–series compensation of the IPT coils is considered for the good controllability and the high partial load efficiency.

For the regulation of the power flow, two degrees-of-freedom are available. First, the switching frequency of the converter can be controlled in the ZVS region above the resonance. In the case of a series compensated transmitter, this increases the inductive impedance of the resonant circuit and introduces a series voltage drop that reduces the transferred power. However, the efficiency at light load conditions drops significantly as a result of the inductive component of the transmitter current.

Second, the harmonic amplitude of the switched voltage can be varied to control the power flow. On one hand, this can be achieved by controlling the duty cycles of the fundamental-frequency rectangular voltage waveform applied to the IPT coils [27]. However, the switching losses in the inverter significantly affect the charging efficiency, given the targeted transmission frequency of 85 kHz. On the other hand, the voltage of the dc-link can be used for controlling the fundamental amplitude of the inverter output voltage while maintaining a constant switching frequency and 50% duty cycle [28]–[30]. The IPT resonant system can be maintained at its natural efficiency optimum if the dc-link voltage at the receiver is regulated in addition. At the transmitter side, either a dedicated dc–dc conversion stage must be cascaded with the grid interface, or a buck-type or buck+boost-type mains rectifier is required for the regulation of the transmitter-side dc-link voltage [31]. For controlling the receiver-side dc-link voltage, a dc–dc converter is needed between the active rectifier and the high-voltage battery of the EV [see Fig. 1(a)]. As an additional advantage, the dc–dc conversion stage allows decoupling the receiver-side dc-link voltage from the battery voltage. It is possible to design the IPT system with a dc-link voltage, which is higher than the battery voltage. This enables a further increase of the transmission efficiency and a reduction of the magnetic stray fields, as a result of the lower coil currents. The additional conversion stage increases the complexity of the on-board power converter; however, the large gain in efficiency and the added control functionality justify the approach [30].

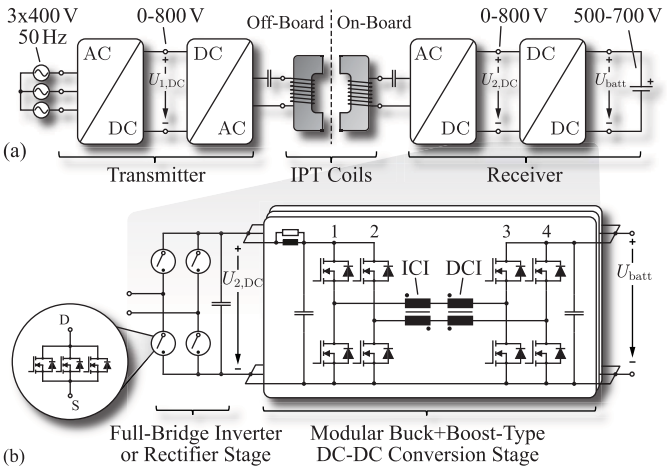

Fig. 1. (a) IPT power conversion chain from the European three-phase mains to the EV high-voltage battery. (b) Topology of the on-board power electronics: full-bridge synchronous rectifier comprising three parallel-connected SiC MOSFET devices per switch, and three parallel-interleaved buck+boost-type dc–dc converter modules with coupled magnetic components.

This paper discusses the design of an integrated on-board rectifier and dc–dc converter with the topology of Fig. 1(b). The presented power converter is part of the IPT system designed in [22]. The details of the multi-objective design of the IPT coils are published in separate papers [23], [24], including a comprehensive experimental investigation of the realized 50 kW IPT hardware prototype. Herein, the details of the IPT coil design are omitted in favor of a comprehensive analysis of the power electronics.

The selected converter topology consists of a full-bridge active rectifier stage that interfaces the receiver-side resonant circuit, and of a buck+boost-type dc–dc conversion stage. Section II describes the design of the full-bridge stage. Parallel-connected discrete SiC MOSFET devices in TO-247 housings are used instead of power modules for their lower parasitics and the improved power density of the full-bridge. Measurements of the individual drain currents are carried out to validate the employed gate driver concept and the design of the printed circuit board (PCB).

For the dc–dc conversion stage, a hard-switched bidirectional non-isolated buck+boost topology with coupled magnetic components is selected. The final converter comprises three identical, parallel-interleaved 20 kW dc–dc converter modules. In Section III, the principal converter operation is analyzed and the necessary design equations for the coupled magnetic devices are derived. A hardware prototype with a switching frequency of 50 kHz and a power density of 12.7 kW/dm^3 (or 208 W/in^3) is designed and experimentally investigated in Section IV. Measurements demonstrate that the efficiency of the dc–dc converter module is 98.8% at 20 kW and 600 to 800 V boost operation. The final converter assembly of the on-board rectifier and dc–dc converter for the 50 kW IPT system reaches a power density of 9.5 kW/dm^3 (or 156 W/in^3) and an ac–dc efficiency from the IPT receiver coil to the vehicle battery of 98.6%, a result of using coupled magnetic components and the high switching frequency that

is achieved with SiC devices. The section is concluded by a discussion of the dc–dc efficiency measurements obtained from the 50 kW/85 kHz IPT prototype.

Finally, in Section V, the main conclusions are summarized and the options for a further miniaturization of IPT power converters are discussed.

II. Full-Bridge Active Rectifier

For interfacing the receiver coil of the 50 kW/85 kHz IPT system of [22] and [23], a synchronous rectifier is designed with novel 1.2 kV/25 mΩ SiC MOSFET devices, operated at a nominal dc-link voltage of 800 V. For increasing the SiC chip area of the active rectifier while avoiding the higher parasitics and low compactness of today's SiC half-bridge modules, multiple discrete devices are used in parallel. This section describes the theoretical and practical considerations for achieving balanced drain currents in all paralleled devices, as well as the generation of the synchronous gate signals for the active rectifier.

A. Design of the Power Circuit

At the time of writing, most commercially available SiC half-bridge modules are realized in conventional IGBT housings for compatibility with existing industry products. Therefore, these devices have comparably high package inductances [17], [18]. Under ZVS conditions, particularly, the source inductance is critical, because the inductive voltage drop caused by the rising or falling drain current in the source inductance reduces the voltage that is effectively applied to the gate. In addition, the gate inductance limits the slope of the gate current. Both effects together determine how fast the gate can be charged or discharged. For a high inductive output current of the half-bridge, high ZVS losses occur if the gate driver is too slow to turn OFF the MOSFET channel before the drain-to-source voltage starts rising. Furthermore, a compact realization of the full-bridge stage is complicated by the comparably large volume of the available half-bridge modules. Therefore, three discrete devices of type C2M0025120D (1.2 kV/25 mΩ) in TO-247 housings are used for each switch of the full-bridge, which allows handling input currents up to 120 A rms, as is required for the operation of the contactless EV charger at the maximum IPT coil misalignment [23].

For a symmetrical utilization of all three paralleled devices and an approximately equal distribution of the conduction losses, the internal device characteristics (ON-state resistance and threshold voltage), as well as the parasitic elements of the external power circuit layout are of crucial importance [32]–[34]. The considered layout of the power circuit is shown in Fig. 2(a). The symmetrical layout ensures similar gate and commutation inductances for all paralleled devices. The approximative Finite Element Method (FEM) simulation model shown in Fig. 2(b) is analyzed to validate the proposed layout of the power PCB. The calculated current distribution at 85 kHz for a total current of 100 A is shown in Fig. 2(b) for the case where the low-side (LS) devices LS1–LS3 of half-bridge A and the high-side (HS) devices HS1–HS3 of half-bridge B are turned ON.

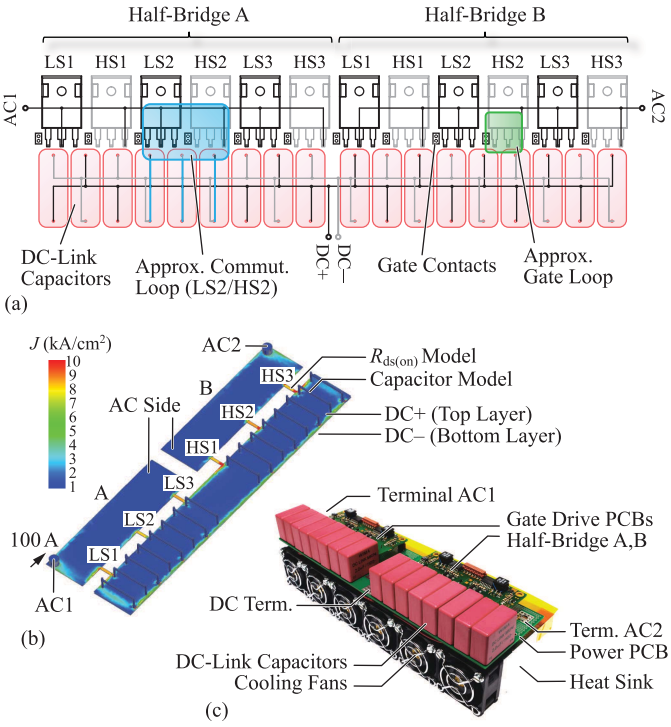

Fig. 2. (a) Power board layout with minimum commutation and gate loop for the paralleled devices. (b) FEM-calculated current distribution in the power board of the full-bridge at 85 kHz. (c) Photograph of the final assembly of the full-bridge active rectifier. The form factor is optimized for the combination with the dc–dc converter stage.

A sequence of three simulations is executed, where in each step, one of the three paralleled MOSFETs in the LS switch and all three HS devices are conducting. The process is repeated for the HS switches. The FEM results show that the power path inductances differ by approximately 2.1%. As a result of the small inductance differences, the FEM-calculated device currents differ by less than 5%.

For driving the three paralleled devices, a common driver circuit is implemented on a dedicated PCB [see Fig. 2(c)]. A driver of type 1ED020I12 is used as the signal isolator for its high common mode (CM) immunity. The driver is connected to two paralleled push–pull stages, each consisting of a pair of bipolar transistors. The positive and negative gate voltages +22/−5 V are generated by an isolated supply circuit. Individual gate resistors are used for each of the three paralleled MOSFET devices. Separate resistors are employed for the turn-ON (10 Ω) and the turn-OFF transitions (5 Ω), separated by SiC Schottky diodes. For the PCB layout, special care was taken for a symmetric layout with minimum gate inductance added by the PCB traces. Due to the limiting effect of the gate inductance on the slope of the gate current, this is critical to ensure simultaneous turn-ON and turn-OFF transitions of all three devices.

B. Verification of Drain Current Balancing

In order to verify the layout of the power and gate driving circuits of the prototype shown in Fig. 2(c), pulse measurements are conducted with an inductive load of 28 μH at 800 V

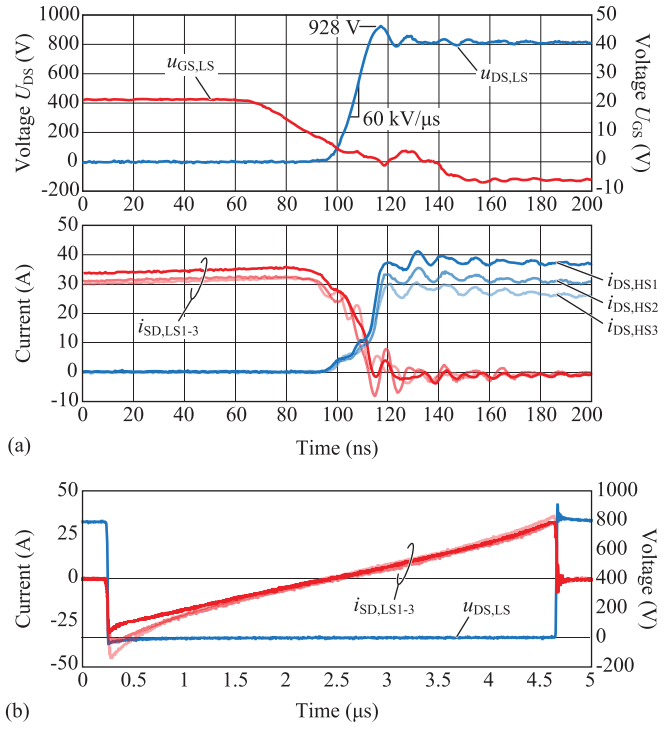

Fig. 3. (a) LS gate–source and drain–source voltages and individual drain currents in the paralleled SiC MOSFETs during a switching transition of half-bridge A. (b) Individual LS device currents and drain-to-source voltage during continuous conduction with an inductive load of 28 µH.

dc-link voltage. The measured LS device voltages $u_{GS,LS}$ and $u_{DS,LS}$, as well as the individual drain currents during a switching transition of inverter half-bridge A are shown in Fig. 3(a). The measurement shows a similar behavior of all LS currents during the transition phase. The HS currents show differences immediately after the transition. According to [34], this can be caused by differences in inductance or ON-state resistance along the current paths through the paralleled devices. However, the transient imbalance of the drain currents during the switching transition is acceptable, because the full-bridge is always operated with ZVS. For hard-switched operation, the somewhat asymmetric current distribution during the transition could lead to unbalanced switching losses. The complete conduction interval of the LS switch is shown in Fig. 3(b). During the ON-state, the current sharing between the paralleled devices is sufficiently symmetric. Finally, the small overshoot of the drain–source voltage u_{DS} despite the 60 kV/µs voltage slope confirms that due to the symmetrical arrangement of the devices, a small commutation loop inductance is achieved.

C. Generation of Synchronous Gate Signals

The main disadvantage of using SiC MOSFETs for the active rectifier is the high forward voltage drop of the SiC body diode. Therefore, a synchronous turn-ON of the MOSFET channel is necessary to reduce the conduction losses. The synchronous gate signals are derived from a measurement of the ac current in the receiver coil with a current transformer.

The high input current of up to 120 A demands a high transformation ratio for the current transformer, which can

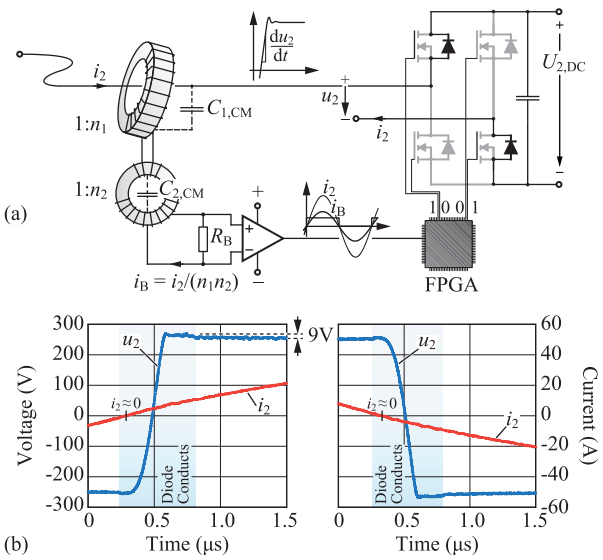

Fig. 4. (a) Two-stage ac current measurement with cascaded transformers to reduce the CM stress, and circuit diagram for the generation of the synchronous gate signals. (b) Waveforms of the rectifier input voltage u_2 and the receiver coil current i_2 during positive and negative switching transitions.

be obtained with a high secondary turns number. However, this limits the bandwidth of the measurement and exposes the signal electronics to a high CM stress. As a result of the high CM capacitance $C_{1,CM}$ between the transformer winding and the primary conductor and the steep voltage slopes du_2/dt at the switch node of the SiC MOSFET full-bridge, a high CM rejection ratio is required for the measurement circuitry.

A smaller turns number is possible for the current transformer if it is cascaded with a second transformer as shown in Fig. 4(a). In this arrangement, the current in the burden resistor i_B is scaled by the product of the transformation ratios of both transformers and fewer turns are possible ($n_1 = 80$ and $n_2 = 5$). Consequently, the capacitances $C_{1,CM} = 2.7$ pF and $C_{2,CM} = 3$ pF of the two transformers are small due to the lower turns numbers, and they are connected in series, which further reduces the total CM capacitance. Therefore, the CM stress for the measurement circuitry is significantly reduced compared with using only a single current transformer. The measurement signal at the burden is connected to a comparator circuit for the detection of the current zero crossings. The comparator output is fed to a field programmable gate array (FPGA), where the synchronous gate signals are generated.

Fig. 4(b) shows the measured receiver coil current i_2 and the rectifier input voltage u_2 during switching transitions of the rectifier. The smooth slopes of the voltage waveforms and the fact that the current crosses zero before the voltage transition confirms ZVS of the rectifier stage. For this measurement, the receiver-side dc-link voltage $U_{2,dc}$ is adjusted to 250 V in order to capture the effect of the synchronous MOSFET turn-ON. The two diode forward voltages of approximately 9 V (4.5 V per device) are visible shortly before and after the voltage transition. The elimination of the diode forward voltage by the synchronous rectification leads to a significant reduction of the conduction losses of the converter, given the low ON-state resistance of the three paralleled devices.

III. DC–DC Converter With Coupled Inductors

Given the typical voltage levels of high power and energy density traction batteries of 500–700 V [35], [36], and the selected control scheme for the IPT system, for which the dc-link voltage needs to be varied between 0 and 800 V, a buck+boost topology is selected for the dc–dc conversion stage. Coupled inductors are used for a high power density of the magnetic components. The detailed operation of the converter is discussed in the first part of this section. Thereafter, the design equations for the coupled magnetic components are derived, and it is shown that the required total magnetics area product is smaller than for conventional parallel-interleaved inductors.

A. Modular Converter Topology

The dc–dc conversion stage is implemented as three parallel-interleaved converter modules of identical topology. Each dc–dc module is designed for an output power of 20 kW. This results in a total power capability of 60 kW for the presented IPT on-board power converter, giving a sufficient margin for the experimental investigation of suboptimal operating points with high losses, e. g., due to IPT coil misalignment.

The division of the dc–dc conversion stage into three 20 kW modules reduces the current loading of each module to a level where the use of PCB technology instead of copper bus bars and discrete power semiconductors instead of power modules are possible. Both aspects are favorable for a highly compact realization. In addition, the internal splitting into two parallel phases with 180° phase shift and coupled inductors enables a volume reduction due to the smaller magnetic devices [37], [38] and the lower output current ripple, which allows using a smaller dc-link capacitance in the modules.

B. Inverse-Coupled and Direct-Coupled Inductors

Before the discussion of the converter operation, the necessary conventions for the inverse-coupled inductor (ICI) and the direct-coupled inductor (DCI) are introduced.

As shown in Fig. 1(b), the ICI and the DCI are connected in series between the half-bridges 1/2 and 3/4 of the dc–dc converter. Therefore, they share the same winding currents i_{L1} and i_{L2}, which each contribute half of the dc current that is responsible for the power flow through the converter. The winding sense and the magnetic circuits are shown in Fig. 5(a) and (b). The windings senses of the two devices are selected, such that the dc flux components cancel out in the core of the ICI, while in the core of the DCI the dc flux components add up. Therefore, the core of the DCI is realized with an air gap δ to lower the inductance in order to avoid saturation. Theoretically, the ICI core does not require an air gap, if the winding currents are sufficiently well balanced during operation. In practice, a small air gap is useful to increase the tolerance toward small dc current imbalances.

The turns numbers of the two windings on the ICI core are equal. Therefore, the same self-inductance L_{ICI} is observed for both windings of the ICI. Also, the two windings on the DCI core have the same turns numbers and, therefore, also the self-inductance L_{DCI} is the same for both windings of the DCI.

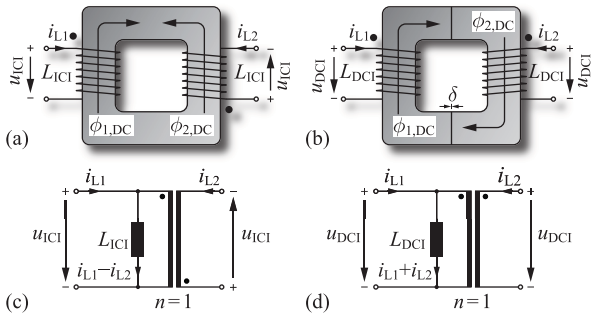

Fig. 5. (a) and (b) definition of the winding sense and (c) and (d) transformer equivalent circuit diagrams for the ICI and DCI.

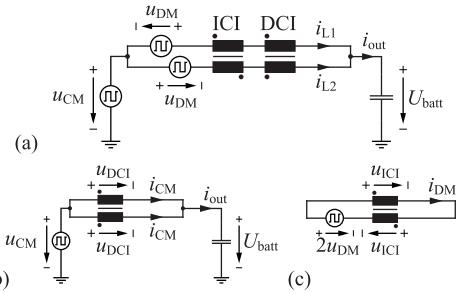

Fig. 6. (a) Buck mode equivalent circuit diagram with replacement of the switch node voltages u_{11} and u_{21} by rectangular CM and DM voltage sources. Splitting of the circuit into (b) CM and (c) DM equivalent circuits [39].

If an ideal coupling of the two windings is assumed, the transformer equivalent circuits shown in Fig. 5(c) and (d) result. From the equivalent circuit diagram of the ICI, the slope of the differential mode (DM) current i_{DM} follows as:

$$\frac{\mathrm{d}i_{\mathrm{DM}}}{\mathrm{d}t} = \frac{\mathrm{d}}{\mathrm{d}t}\frac{i_{\mathrm{L1}} - i_{\mathrm{L2}}}{2} = \frac{u_{\mathrm{ICI}}}{2L_{\mathrm{ICI}}}. \tag{1}$$

Therefore, the effective inductance for the DM current ripple $\Delta i_{\mathrm{DM,pp}}$ is $2L_{\mathrm{ICI}}$. Equally, from the DCI transformer equivalent circuit diagram of Fig. 5(d), the slope of the CM current i_{CM} is calculated as

$$\frac{\mathrm{d}i_{\mathrm{CM}}}{\mathrm{d}t} = \frac{\mathrm{d}}{\mathrm{d}t}\frac{i_{\mathrm{L1}} + i_{\mathrm{L2}}}{2} = \frac{u_{\mathrm{DCI}}}{2L_{\mathrm{DCI}}} \tag{2}$$

and hence, the CM current ripple $\Delta i_{\mathrm{CM,pp}}$ results from the effective inductance $2L_{\mathrm{DCI}}$ of the DCI.

These relations indicate the main advantage of the coupled magnetic components instead of uncoupled inductors for the parallel-interleaved converter. The DM and CM current ripples can be independently adjusted by the design of the inductances L_{ICI} and L_{DCI}. This additional degree-of-freedom in the design is responsible for the smaller required area product of this design option. However, for the derivation of these relations, first, the operation of the dc–dc converter needs to be introduced.

C. Steady-State Converter Operation

For buck operation, the two input-side bridge legs 1/2 are operated with a constant phase shift of 180° and equal duty cycles, while the bridge legs 3/4 at the output side are

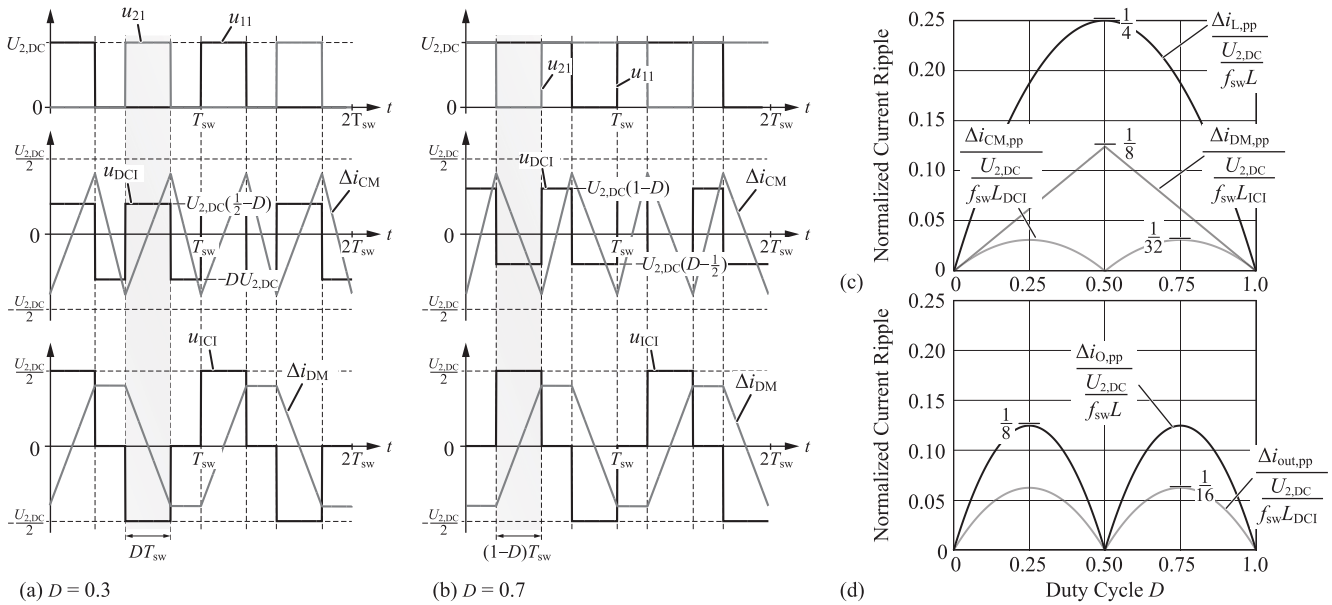

Fig. 7. Calculated waveforms for the dc–dc converter with ICI and DCI for duty cycle (a) $D = 0.3$ and (b) $D = 0.7$. The shaded intervals are used for the calculation of the CM and DM ripple currents Δi_{CM} and Δi_{DM}. (c) Normalized CM and DM current ripples and (d) output current ripple in comparison to the current ripple of two parallel-interleaved uncoupled inductors with inductance L.

constantly connected to the output voltage U_{batt} [see Fig. 1(b)]. For boost operation, the scheme is inverted. Bidirectional power transfer and minimum conduction losses are achieved if the body diodes are only used during the interlock delay time and the gates of the MOSFETs are operated as in a synchronous buck or boost converter.

Following [39], in Fig. 6(a), an equivalent circuit diagram for the buck mode of the converter is shown, where the switch node voltages of the bridge legs 1/2, denoted by u_{11} and u_{21}, are replaced by rectangular voltage sources. The switch node voltages can be divided into a CM and a DM component

$$u_{\mathrm{CM}} = \frac{u_{11} + u_{21}}{2}$$
$$u_{\mathrm{DM}} = \frac{u_{11} - u_{21}}{2}. \tag{3}$$

Considering the opposite winding senses of the ICI and the DCI, independent CM and DM equivalent circuit diagrams can be derived, as in Fig. 6(b) and (c). Solving Kirchhoff's equations for the simplified equivalent circuits shows

$$u_{\mathrm{DCI}} = u_{\mathrm{CM}} - U_{\mathrm{batt}}$$
$$u_{\mathrm{ICI}} = u_{\mathrm{DM}}. \tag{4}$$

Schematic waveforms of the switch node voltages and the calculated DCI and ICI voltages for operation in synchronous buck mode with duty cycle $D = 0.3$ and $D = 0.7$ are shown in Fig. 7(a) and (b). It shall be noted that the lowest harmonic component in the CM current ripple waveform is at twice the switching frequency of the converter, while the first harmonic component of the DM current ripple is already at the switching frequency. This important difference is considered during the selection of suitable core materials for the two magnetic devices, as discussed in the following.

Considering the shaded time intervals in Fig. 7(a) and (b), the peak-to-peak values of the CM and DM current ripples are calculated as

$$\Delta i_{\mathrm{CM,pp}} = \frac{U_{2,\mathrm{dc}}\left(\frac{1}{2} - D_{\mathrm{eff}}\right)}{2L_{\mathrm{DCI}}} \cdot \frac{D_{\mathrm{eff}}}{f_{\mathrm{sw}}}$$
$$\Delta i_{\mathrm{DM,pp}} = \frac{\frac{1}{2}U_{2,\mathrm{dc}}}{2L_{\mathrm{ICI}}} \cdot \frac{D_{\mathrm{eff}}}{f_{\mathrm{sw}}} \tag{5}$$

using the calculated DCI and ICI winding voltage amplitudes that are indicated in Fig. 7. The introduction of the effective duty cycle

$$D_{\mathrm{eff}} = \begin{cases} D, & \text{for } 0 \le D \le 0.5 \\ 1 - D, & \text{for } 0.5 < D \le 1 \end{cases} \tag{6}$$

serves the purpose of representing the results for $D \le 0.5$ and $D > 0.5$ in a single equation.

The peak-to-peak CM and DM current ripples are shown in Fig. 7(c) as the functions of the duty cycle. For comparison, also the peak-to-peak current ripple $\Delta i_{\mathrm{L,pp}}$ in the windings of two parallel-interleaved uncoupled inductors with inductance L is shown [39]. All current ripple values are normalized to the dc-link voltage $U_{2,\mathrm{dc}}$, the switching frequency f_{sw}, and the respective inductance. The maximum CM and DM current ripples are obtained at $D = 0.25$ or $D = 0.75$, and at $D = 0.5$, respectively, as

$$\Delta i_{\mathrm{CM,pp,max}} = \frac{1}{32}\frac{U_{2,\mathrm{dc}}}{f_{\mathrm{sw}}L_{\mathrm{DCI}}}$$
$$\Delta i_{\mathrm{DM,pp,max}} = \frac{1}{8}\frac{U_{2,\mathrm{dc}}}{f_{\mathrm{sw}}L_{\mathrm{ICI}}}. \tag{7}$$

The winding current ripples Δi_{L1}, Δi_{L2} are calculated from the CM and DM current ripples as

$$\Delta i_{L1,pp} = \Delta i_{CM,pp} + \Delta i_{DM,pp}$$
$$\Delta i_{L2,pp} = \Delta i_{CM,pp} - \Delta i_{DM,pp} \quad (8)$$

and the ripple of the converter output current $\Delta i_{out,pp}$ follows from the sum of the winding currents as:

$$\Delta i_{out,pp} = 2\Delta i_{CM,pp} \quad (9)$$

which is shown in normalized form in Fig. 7(d) as a function of the duty cycle. The normalized output current $\Delta i_{O,pp}$ of a converter with two uncoupled inductors is shown as a comparison [39]. The maximum output current ripple appears in both cases at $D = 0.25$ or at $D = 0.75$. For the converter with coupled inductors, the maximum is calculated as

$$\Delta i_{out,pp,max} = \frac{1}{16}\frac{U_{2,dc}}{f_{sw}L_{DCI}} \quad (10)$$

whereas for the converter with uncoupled inductors of inductance L, the maximum is [39]

$$\Delta i_{O,pp,max} = \frac{1}{8}\frac{U_{2,dc}}{f_{sw}L}. \quad (11)$$

This comparison shows that for the same switching frequency and inductance $L = L_{DCI}$, and assuming an ICI that limits the DM current ripple, the output current ripple is reduced by a factor of two by the direct coupling of the parallel-interleaved inductors. As shown in the following, in more detail, the current ripple reduction occurs, because the stored magnetic energy in the DCI is increased by a factor of two compared with two parallel-interleaved inductors of the same inductance as a result of the coupling of the DCI windings. In addition, (9) shows that the ripple of the output current depends only on the CM current ripple, i.e., on the inductance L_{DCI}, and not on the inductance of the ICI. However, according to (8), the winding current ripples depend on both inductance values. Therefore, the inductance L_{DCI} can be used to fulfill an output current ripple criterion, while the additional degree-of-freedom L_{ICI} is used for the attenuation of undesired DM currents between the interleaved bridges. Thereby, the winding rms currents, the resistive losses in the coils, as well as conduction and switching losses in the power semiconductors are minimized. This ability is a fundamental advantage of the solution with coupled inductors.

In order to confirm the theoretical analysis, the voltage and current waveforms measured at the coupled inductors of the realized hardware prototype are shown in Fig. 8 for an input voltage of 600 V and a duty cycle of $D = 0.25$. The voltage across the ICI and the DCI is measured with two high-voltage differential probes. The winding current ripples are measured with two current probes set to ac coupling. The measured winding current waveforms of Fig. 8(a) are mathematically separated into the CM and DM ripple current components shown in Fig. 8(b) and (c). As expected, the DCI voltage u_{DCI} defines the CM ripple current Δi_{CM} and the ICI voltage u_{ICI} is responsible for the DM ripple current Δi_{DM}.

The peak-to-peak CM and DM current ripples calculated with the inductance values $L_{DCI} = 300$ µH, and $L_{ICI} = 1.5$ mH of the prototype are $\Delta i_{CM,pp} = 1.25$ A and $\Delta i_{DM,pp} = 0.5$ A. The measured waveforms confirm the accuracy of the presented circuit analysis.

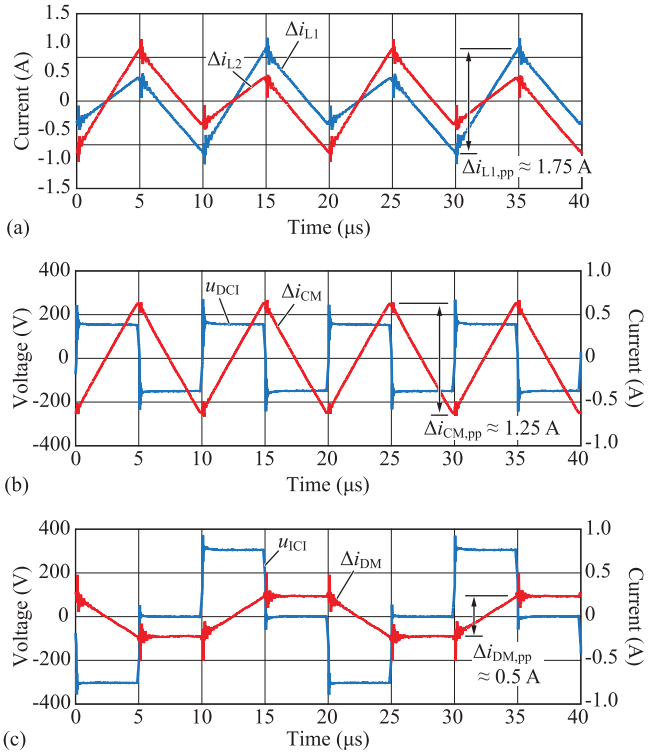

Fig. 8. (a) Measured winding ripple currents of a prototype dc–dc converter module ($U_{2,dc} = 600$ V and $D = 0.25$). (b) CM current ripple Δi_{CM} and DCI voltage u_{DCI}. (c) DM current ripple Δi_{DM} and ICI voltage u_{ICI}.

D. Calculation of Area Product and Stored Energy

If the current density in the inductor windings is limited to the maximum rms current density J_{max}, the required DCI or ICI winding window is

$$A_{cu} = \frac{N\,(I_{L1} + I_{L2})}{k_{cu}J_{max}} = \frac{2NI_{L1}}{k_{cu}J_{max}} \quad (12)$$

where N stands for the turns number and k_{cu} is the copper filling factor of the winding window. The given simplification is possible, because the rms values of the winding currents I_{L1} and I_{L2} are equal.

The rms values of the winding currents of the coupled inductors depend on the ratio of L_{ICI} to L_{DCI} [22]. For a design $L_{ICI} = L_{DCI}$, the winding current ripple has a single maximum at $D = 0.5$, which is exactly 50% of the winding current ripple of uncoupled inductors with the same inductance $L = L_{DCI}$. This selection for the inductance L_{ICI} leads to the same winding and output current ripples than for uncoupled inductors at one half of the switching frequency. For this reason, this design is considered in the analysis of the area product. Using this assumption, the maximum rms currents can be extracted for $D = 0.5$, where the CM ripple vanishes. The result is

$$I_{L1} = I_{L2} = \sqrt{\left(\frac{I_{dc}}{2}\right)^2 + \left(\frac{\Delta i_{DM,pp,max}}{2\sqrt{3}}\right)^2} \quad (13)$$

where I_{dc} is the total dc output current of the converter. The remaining calculations are not affected by the selection of the L_{ICI} to L_{DCI} ratio.

The peak value of the flux linkage in the DCI is given by

$$\hat{\psi}_{DCI} = 2L_{DCI}\left(\frac{I_{dc}}{2} + \frac{\Delta i_{CM,pp,max}}{2}\right) \tag{14}$$

and the flux linkage of the ICI is calculated as

$$\hat{\psi}_{ICI} = 2L_{ICI}\left(\frac{I_{dc,offset}}{2} + \frac{\Delta i_{DM,pp,max}}{2}\right) \tag{15}$$

if also a dc offset $I_{dc,offset}$ is considered. The dc offset could result, for instance, from a sensor offset in the current measurement, from the analog-to-digital conversion and discretization for the digital control, from transient or steady-state control errors, or if unbalanced voltage time areas are applied to the circuit by the two interleaved half-bridges. As an approximation, the offset is considered to be proportional to the load current of the converter and $I_{dc,offset} = 5\% I_{dc}$ is assumed for the presented discussion.

The minimum core cross section A_{core} needed to limit the flux density in the DCI to the maximum value B_{max} is given by

$$A_{core} = \frac{\hat{\psi}_{DCI}}{2NB_{max}}. \tag{16}$$

The multiplication of (16) with (12) leads to the DCI area product $A_{cu}A_{core}$. The ICI area product results when replacing the flux linkage $\hat{\psi}_{DCI}$ by $\hat{\psi}_{DCI}$ in (16).

The peak value of the total current is given by the sum $i_{L1} + i_{L2} = 2i_{CM}$ for the DCI and by the difference $i_{L1} - i_{L2} = 2i_{DM}$ for the ICI. Hence, the peak value of the stored magnetic energy in the DCI is given by

$$E_{DCI} = \frac{1}{2}\hat{\psi}_{DCI} \cdot 2\hat{I}_{CM} \tag{17}$$

which results in the simplified expression

$$E_{DCI} = 2L_{DCI}\left(\frac{I_{dc}}{2} + \frac{\Delta i_{CM,pp,max}}{2}\right)^2. \tag{18}$$

For the ICI, the peak stored magnetic energy analogously results as

$$E_{ICI} = 2L_{ICI}\left(\frac{I_{dc,offset}}{2} + \frac{\Delta i_{DM,pp,max}}{2}\right)^2. \tag{19}$$

This result can be intuitively understood from a simplified consideration. The magnetic energy in the DCI is given by

$$E_{DCI} = \frac{1}{2}L_{DCI}i_{L1}^2 + \frac{1}{2}L_{DCI}i_{L2}^2 + M_{DCI}i_{L1}i_{L2} \tag{20}$$

where M_{DCI} is the mutual inductance of the DCI. If the DCI windings are ideally coupled, the mutual inductance is equal to the DCI self-inductance $M_{DCI} = L_{DCI}$ as used throughout in the above-mentioned derivation. Since only the CM current causes a magnetic flux in the core, the winding currents can be replaced by $i_{L1} = i_{L2} = i_{CM}$. Therefore, the peak value of the magnetic energy is

$$E_{DCI} = 2L_{DCI}\hat{I}_{CM}^2 \tag{21}$$

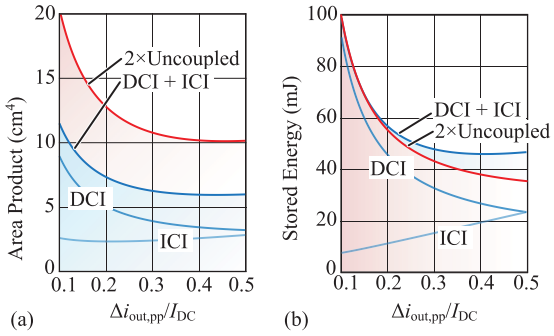

Fig. 9. (a) Calculated area products and (b) peak stored magnetic energy for two uncoupled inductors and for coupled magnetic components as a function of the relative output current ripple.

which is equivalent to (18). This result shows that the coupling increases the stored magnetic energy by a factor of two compared with uncoupled inductors of the same inductance.

A comparison of the area products and the stored magnetic energy for the ICI and the DCI to the values for two uncoupled inductors is shown in Fig. 9 as a function of the relative peak-to-peak current ripple $\Delta i_{out,pp}/I_{dc}$ at the converter output. For the calculation, the values $J_{max} = 2$ A/mm^2, $k_{cu} = 0.5$, $B_{max} = 1$ T, $f_{sw} = 50$ kHz, $U_{2,dc} = 800$ V, and $I_{dc} = 16.7$ A are used in reference to the presented prototype.

At a low relative output current ripple, the DCI inductance has to be large for the required attenuation of the CM current ripple. Due to the linking of the two inductance values by the assumption $L_{ICI} = L_{DCI}$ taken above for the calculation of the rms currents, the ICI inductance is also higher at a low relative output current ripple. Therefore, the contributions of the decreasing CM and DM current ripples to the flux linkages become smaller and smaller compared with that of the dc components. Hence, the area product is dominated by the stored dc magnetic energy.

Because the considered dc offset $I_{dc,offset}$ is much smaller than the dc output current I_{dc}, the stored energy and the area product of the ICI are significantly smaller than that of the DCI. As the relative output current ripple is increased, the inductances become smaller. Therefore, the area products of the ICI and the DCI initially decrease. As confirmed by Fig. 9(b), the magnetic energy stored in the DCI becomes lower as the inductance reduces. However, also for higher relative output current ripples, the CM and DM ripple currents increase. The stored magnetic energy in the ICI is dominated by the DM ripple component, because the dc offset $I_{dc,offset}$ is small. Therefore, the stored magnetic energy in the ICI rises proportionally to the relative output current ripple.

At a certain point, the ac current components caused by the DM and CM current ripples become comparable to the dc components caused by the output current I_{dc} and the dc offset $I_{dc,offset}$. They start dominating the peak values of the flux linkages and the winding rms current. Therefore, the area product decreases at a reducing rate for the DCI. For the ICI, the area product even has a minimum at $\Delta i_{out,pp}/I_{dc} \approx 0.2$, as seen in Fig. 9(a), after which it starts increasing again. At high relative output current ripples, the area products of the ICI become comparable to that of the DCI.

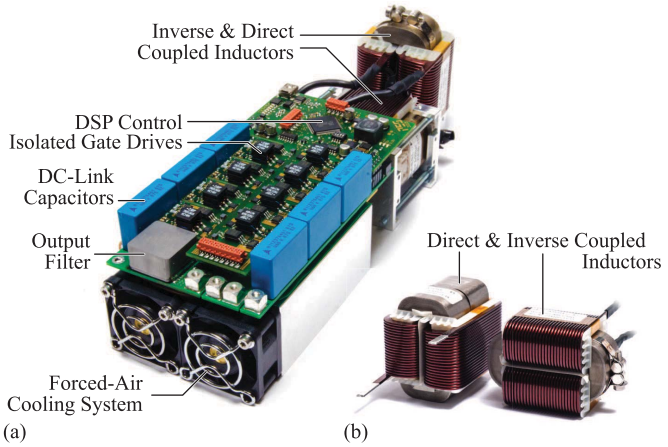

Fig. 10. (a) Photograph of the final assembly and (b) DCI and ICI of the 20 kW/50 kHz buck+boost-type nonisolated dc–dc converter module with a power density of 12.7 kW/dm^3 (or 208 W/in^3) at 98.80% nominal efficiency and 99.17% maximum efficiency.

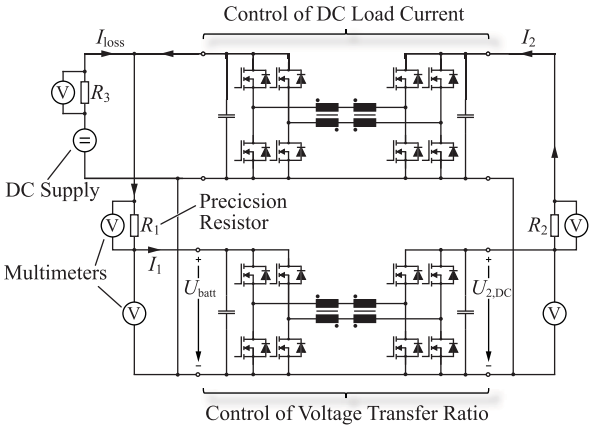

Fig. 11. Back-to-back setup of two identical dc–dc converter modules for direct power loss and efficiency measurements. One module operates at a fixed duty cycle, while the second module controls the circulating dc load current.

All in all, the combined area product of the ICI and the DCI together is more than 40% smaller than the area product for two uncoupled inductors. The total stored magnetic energy at a given relative output current ripple is similar for the coupled magnetic devices and for uncoupled inductors. Hence, as a result of the magnetic coupling, the energy storage capability is increased by approximately a factor of two for a given area product.

IV. Experimental Results

In this section, the prototype design and the experimental results are presented. First, the efficiency of a single 20 kW converter module of the dc–dc stage is measured in a back-to-back setup. Then, the full converter assembly for the IPT on-board power electronics is shown and the dc–dc efficiency is measured. Additional measurements related to the IPT system can be found in [22] and [23].

A. Realized DC–DC Converter Module

In a first step, a hardware prototype of the proposed dc–dc converter with coupled magnetic devices is realized. The DCI has to store a net magnetic energy that is proportional to the output power. The first harmonic component of the DCI flux is at twice the switching frequency, which means a comparably low ac excitation if the system is designed for a moderate output current ripple of 10%–20%. Therefore, an amorphous iron core with air gap is used for this device, because of the high saturation flux density of this material. The ICI flux does not contain a dc component, but is excited at the fundamental switching frequency of the switch node voltage and its odd harmonics. The device can, therefore, be realized with a smaller core cross section for the same ripple current, but needs to be designed with a magnetic material with lower ac losses. Therefore, for this device, a nanocrystalline core material is used. A small air gap is used to avoid saturation up to $I_{\mathrm{dc,offset}} \leq 1.5$ A.

Tape wound C-cores and a helical winding construction are used for both magnetic devices. The helical winding leads to a high copper filling factor $k_{\mathrm{cu}} \approx 0.54$, which reduces the required winding window and the magnetics area product.

The necessary core size, the turns numbers, and the converter switching frequency are determined from the area products as described earlier and then iteratively improved based on FEM-calculated core and winding loss data. The power losses of the hard-switched power semiconductors are calculated from the switching loss data of the used devices (C2M0080120D, 1.2 kV/80 mΩ) measured in [40]. For the final design, the inductances $L_{\mathrm{DCI}} = 300$ μH and $L_{\mathrm{ICI}} = 1.5$ mH and the switching frequency $f_{\mathrm{sw}} = 50$ kHz are selected.

A forced-air cooling system is dimensioned, considering 45 °C ambient temperature with the models in [41]. In the final converter arrangement, the coupled magnetic components are arranged in the air stream at the outlet of the aluminum heat sink, such that they are actively cooled. A photograph of the converter assembly, including the coupled magnetic devices and the forced-air cooling system, is shown in Fig. 10(a). An enlarged image of the coupled inductors is shown in Fig. 10(b). For the realized dc–dc converter, a power density of 12.7 kW/dm^3 (or 208 W/in^3) is achieved. The efficiency measurement is discussed in the following.

B. Efficiency of the DC–DC Converter Module

For measuring the dc–dc converter efficiency, two of the realized prototypes are connected in a back-to-back configuration, as shown in Fig. 11. In the shown cascaded configuration, one dc–dc converter module is operated in boost mode, while the second module operates in buck mode. The output voltage is controlled to the maximum receiver-side dc-link voltage of the IPT system $U_{2,\mathrm{dc}} = 800$ V by operating the first dc–dc converter module with a fixed duty cycle. The circulating dc load current is set by the proportional–integral (PI) CM current controller of the second module, which actuates on the CM voltage that is applied to the coupled inductors.

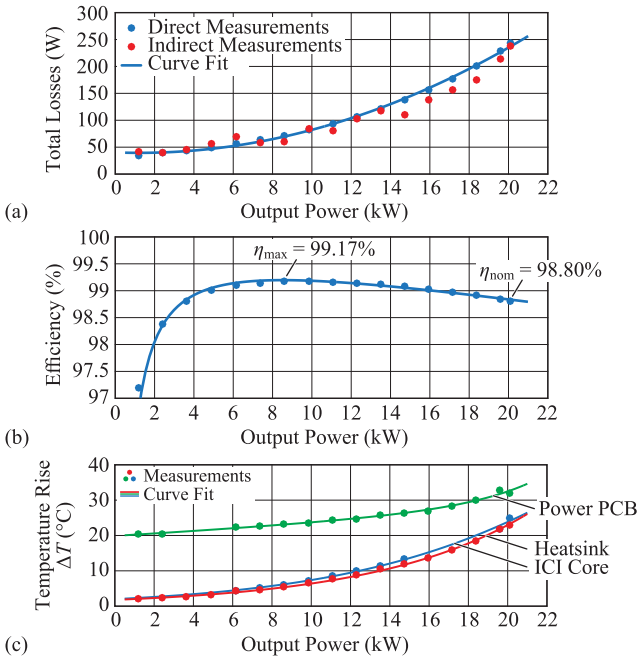

Fig. 12. (a) Direct and indirect measurements of the total losses of a single dc–dc converter module, curve fit for the directly measured power losses, and (b) efficiency of the dc–dc module at 600 to 800 V boost operation. (c) Component temperature rise $\Delta T = T - T_{amb}$ at ambient temperature $T_{amb} \approx 25$ °C.

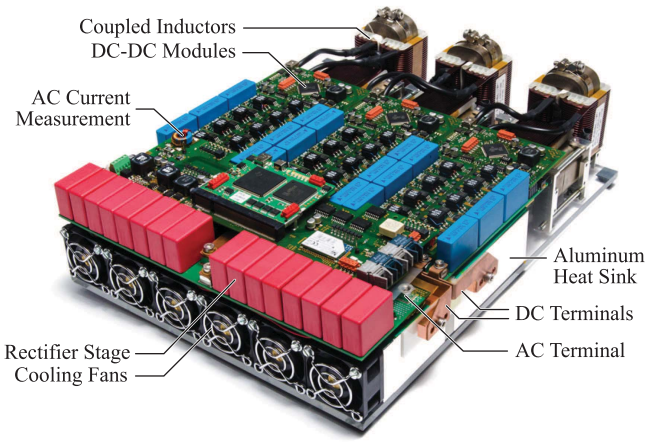

Fig. 13. Photograph of the fully assembled 60 kW all-SiC IPT on-board power electronic converter with 98.62% efficiency and a volumetric power density of 9.5 kW/dm^3 (or 156 W/in^3) and a gravimetric power density of 6.8 kW/kg (or 3.1 kW/lb).

In order to avoid saturation of the ICI, the winding currents of each module are actively balanced by controlling the DM current to zero with a separate PI controller, which actuates on the DM voltage applied to the coupled inductors [22].

The input- and output-side dc links of both converter modules are connected via the precision shunt resistors $R_1 = R_2 = 10\,\text{m}\Omega$ for measuring the input and output currents I_1 and I_2 of the converters. For supplying the power losses to the back-to-back circuit, an external dc power supply is connected via another precision shunt resistor $R_3 = 10\,\text{m}\Omega$ for measuring the supply current I_{loss}. The supply voltage is set to the nominal battery voltage $U_{batt} = 600$ V. Multimeters of type Agilent 34410A are used for all voltage measurements. During the power loss measurements, the component temperatures at different spots of the converter are measured using thermocouples. All power loss measurements are taken after the measured temperatures have settled to their steady-state values.

The total power losses of both converters together can be determined directly from the current I_{loss} measured at the dc supply. Alternatively, an indirect loss measurement can be obtained by using the measurements of I_1 and I_2 and taking the difference of the input and output power of one of the converters. The power losses of a single converter measured with both methods are shown in Fig. 12(a) as a function of the output power. The larger variance of the indirect measurements confirms that the direct loss measurement method is much better conditioned for measuring the power losses of converters with very high efficiency [42]. The direct efficiency measurement results for a single dc–dc converter module are shown in Fig. 12(b). The peak efficiency of $\eta_{max} = 99.17\%$ is reached at 8.6 kW (=43%) output power. The efficiency at the nominal power output of 20 kW is 98.80%.

The measured component temperatures are shown in Fig. 12(c) as temperature differences $\Delta T = T - T_{amb}$ with respect to the measured, approximately constant ambient temperature $T_{amb} \approx 25$ °C. The most critical part is the power PCB, because it experiences current densities of up to 15A/mm^2 in the 100 µm copper traces and is only cooled by natural convection. The highest core temperature is measured for the ICI as 32.7 °C above ambient, because its positioning in the converter arrangement limits the air flow from the cooling system. From the measured heat sink temperature, the junction temperature of the power semiconductors is estimated with a thermal model consisting of the thermal resistances from the junction to the case of the device, of the insulation layer between case and heat sink, and the calculated power losses of the devices. For the worst case operating conditions, the calculated junction temperature is 85.8 °C above ambient temperature. Given the targeted 45 °C ambient temperature, these measurements indicate a good utilization of the SiC devices and the magnetic components.

C. Efficiency of the 50 kW IPT System

The final assembly of the IPT on-board power converter, comprising three parallel-interleaved 20 kW dc–dc modules, is shown in Fig. 13. An individual digital signal processor (DSP) of type TMS320F28069 is used in each dc–dc converter module for the cascaded feedback control of the dc–dc converter output voltage and the inductor currents. Another DSP of type TMS320F28335 in combination with an FPGA of type LFXP2-5E is used as the main controller that manages the interaction of the three dc–dc modules and the generation of the gate signals for the ZVS full-bridge. For the communication between the DSPs of the dc–dc converter modules and the main controller, the controller area network interface of the DSPs is used. For the communication between

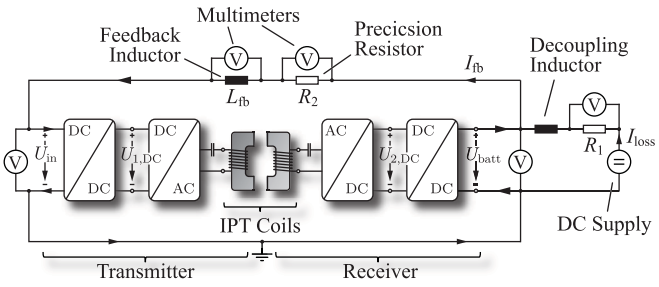

Fig. 14. Measurement setup with identical power converters on both sides of the air gap and energy feedback via L_{fb} for circulating 50 kW in the IPT prototype system (figure reproduced from [23]).

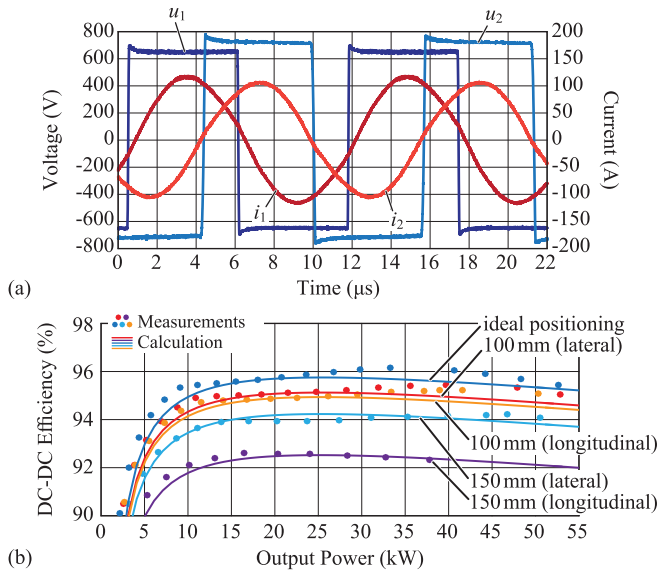

Fig. 15. (a) Principal waveforms in the IPT measurement setup of Fig. 1 measured at 50 kW output power and $U_{batt} = 600$ V output voltage: transmitter-side full-bridge inverter output voltage u_1 and coil current i_1 and receiver-side active rectifier input voltage u_2 and coil current i_2. (b) Calculated and measured dc–dc efficiency for an air gap of 160 mm and variable horizontal coil misalignment (figure reproduced from [23]).

the power converter used at the transmitter side and the converter at the receiver side of the IPT system, a wireless communication module of type RN-171-DS is integrated on the main control board. Owing to the interleaving, the high switching frequency, and the coupling of the magnetics, a volumetric power density of 9.5 kW/dm^3 (or 156 W/in^3) and a gravimetric power density of 6.8 kW/kg (or 3.1 kW/lb) are achieved for the final converter assembly. The calculated ac–dc efficiency of the full converter is 98.6%.

For measuring the performance of the IPT system with up to 50 kW in the laboratory, a test setup with energy feedback is implemented, as shown in Fig. 14. The presented on-board converter is produced in duplicate and also employed at the transmitter side. Therefore, the full-bridge of the active rectifier is operated as inverter for the supply of the transmitter coil with a 85 kHz rectangular voltage waveform u_1, as shown in Fig. 15(a). An energy feedback inductor with $L_{fb} = 3.4$ mH is connected between the dc links of the two power converters. The transferred power and the power losses are determined by measuring I_{fb} and I_{loss} using Agilent 34410A multimeters and the precision shunt resistors $R_1 = 10$ mΩ and $R_2 = 1$ mΩ. For subtracting the dc losses of the air core inductor L_{fb} from the total loss measurements, also the voltage drop along the feedback path is measured.

For the series–series resonant compensation of the IPT coils, polypropylene film capacitors are employed on both sides of the air gap. The power transfer is controlled by regulating the dc-link voltages $U_{1,dc}$ and $U_{2,dc}$ with the dc–dc conversion stages, as discussed in [29] and [30]. The voltages U_{batt} and U_{in} are set to approximately 600 V with the external dc supply, which represents the EV high-voltage battery.

The measured dc–dc efficiency from U_{in} to U_{batt} is shown in Fig. 15(b) for four different IPT coil positions. For an ideal coil positioning and an air gap of 160 mm, the efficiency at 50 kW is 95.8%. For a coil misalignment of 150 mm in the longitudinal direction (worst case), the efficiency drops by 3.8% points to approximately 92% due to the significantly increased transmitter current.

The measured efficiency includes the IPT resonant system and two power electronics stages. In the actual charging system, the transmitter-side converter additionally comprises a three-phase mains interface [see Fig. 1(a)], possibly with buck+boost capability to avoid a cascaded dc–dc conversion stage at the transmitter. Adding the mains interface is expected to lower the total charging efficiency by approximately 1%–2% points, depending on the employed power electronics solution.

V. Conclusion

In this paper, the design of the on-board power electronics, comprising an active rectifier and a cascaded dc–dc converter, for interfacing the receiver coil of a 50 kW IPT system was presented. Owing to the use of coupled magnetic devices and the outstanding switching performance of the employed SiC power semiconductors, a power density of 9.5 kW/dm^3 (or 156 W/in^3) was achieved at an ac–dc efficiency of 98.6%. The dc–dc efficiency of the investigated IPT system is 95.8% at 160 mm air gap with $410 \times 760 \times 60$ mm^3 coils, including all power electronics stages.

Apart from the power converter, the large IPT receiver coil and the high-frequency electromagnetic stray fields are the main factors that limit the efficiency and power density of a contactless EV charger. However, it was shown in previous work that increasing the transmission frequency can improve both aspects simultaneously. Since the efficiency of the power transfer is determined by the product of the magnetic coupling and the quality factors of the IPT coils, the same efficiency is possible with smaller IPT coils if a higher transmission frequency is used. Moreover, the voltage induced in the secondary is proportional to the product of the magnetic flux density at the receiver and the transmission frequency. Hence, at higher frequencies, a lower flux density leads to the same power transfer, making it easier to comply with the relevant field exposure standards.

Therefore, high-frequency converter designs, such as the one presented in this paper, are particularly interesting for IPT. The presented power converter was designed for the 85 kHz transmission frequency as proposed by the upcoming SAE standard J2954. However, given the low ZVS losses

of the employed SiC MOSFET devices and the excellent switching performance of the presented active rectifier with parallel-connected devices, also higher switching frequencies are possible. Therefore, the presented converter design is a promising candidate for future research and development projects that aim at increasing the system power density by high-frequency power transmission.

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