New Optimum Modulation of Three-Phase ZVS Triangular Current Mode GaN Inverter Ensuring Limited Switching Frequency Variation

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Abstract

In three-phase pulse width modulation inverters with an LC output filter, switching losses can be reduced by increasing the current ripple in the inductor until a current zero crossing occurs between the two switching instances of a bridge leg. A disadvantage of this triangular current mode (TCM) operation is the varying switching frequency. This paper presents new modulation methods where the current ripple amplitude is adjusted and a common-mode voltage is introduced in order to limit the switching frequency variation. Moreover, the possibility of increasing the efficiency and minimizing the filter volume are investigated. Numerical optimization results are presented for a 2.5 kW inverter with 400 V DC link voltage as a case study.

1 Introduction

In two-level three-phase pulse width modulation inverters with LC output filters, the switching actions of a bridge leg within one switching period can benefit from a resonant transition if the current ripple in the inductor is increased until a current zero crossing occurs between the two switching instances [1]. This mode of operation is called triangular current mode (TCM), and enables zero-voltage switching (ZVS), which results in lower switching losses [2].

On the other hand, the switching frequency of TCM operation is not fixed as in standard space vector modulation (SVM), and may vary significantly depending on the operating point of the inverter. The large switching frequency variation makes the design of an EMI filter, which might be arranged between inverter and load (e.g. a motor) much more challenging than having a constant switching frequency. Furthermore, delays in measurements and signal processing impose a maximum switching frequency limit that cannot be exceeded in practical applications, which also makes the varying switching frequency an undesirable feature.

One way to decrease the ratio between maximum and minimum switching frequencies is to use two or more interleaved bridge legs per phase with individual filter inductors, and to operate more bridge legs with increasing output currents [3]. However, this approach comes with significant additional hardware effort, partly hindering the filter volume reduction possibility that is enabled by the low-loss (ZVS) application of higher switching frequencies.

This paper discusses an alternative modulation method for three-phase TCM inverters, in which the possibility of utilizing a common-mode (CM) voltage is discussed along with the option of increasing the inductor current ripple amplitude in excess of the minimum ripple required for ZVS, with the goal of limiting the switching frequency variation, the losses, and the filter volume.

In the following section 2, the basic principle of operation of TCM inverters is explained. In section 3, the new modulation techniques are presented and their performances are assessed based on a case study. Finally, a conclusion and an outlook are given in section 4.

2 Two-Level Three-Phase TCM Inverters

2.1 Principle of Operation

Figure 1 shows a two-level three-phase TCM inverter, and Figure 2 (a) depicts the corresponding six different operating phases that occur within a switching period [4]. During interval 1, the upper switch $S_+$ is conducting and thus, the current $i_L$ increases linearly, given the assumption that the output voltage ripple is negligible. After having turned off $S_+$, the parasitic output capacitance $C_{+P}$ of $S_+$ is charged and $C_{-P}$ of $S_-$ is discharged in interval 2 during a resonant transition. Interval 3 starts when $C_{+P}$ is fully discharged and diode $D_-$ starts conducting. Now, switch $S_-$ can be turned on at ZVS. When the current $i_L$ reaches zero, interval 4 begins and it ends by turning $S_-$ off at a desired current level $i_{L,S-off}$. During interval 5, another resonant charging and discharging of the parasitic capacitances

...
The inductor current waveform can be approximated in a first step with sufficient accuracy using a linear model as in Figure 2 (b), since the duration of the resonant transitions is negligible for practical switching frequencies.

The reverse current $i_0$ should be large enough such that the energy stored in the inductor suffices to fully discharge and charge the parasitic capacitances of the switches, hence to ensure ZVS. The minimum required $i_0$ is dependent on the output voltage $u_C$. Therefore, it varies within an output (fundamental) period even for constant load [4]. A larger $i_0$ leads to an increase of the conduction losses in the transistors ($f$) that determines the output voltage ripple (b). Consequently, the switching losses in the switches of one bridge leg can be approximated as

\[
P_{\text{cond}} = \frac{1}{f_1} \int_{0}^{1/f_1} R_{\text{DS,on}} \left( i_L^2 + \frac{1}{12} (2i_L^2 + 2i_0)^2 \right) dt,
\]

where $R_{\text{DS,on}}$ is the on-state resistance of one switch and $f_1$ is the fundamental output frequency. Similarly, the switching losses in a bridge leg can be approximated as

\[
P_{\text{sw}} = \frac{1}{f_1} \int_{0}^{1/f_1} f_1 E_{\text{sw}}(i_{\text{sw}}) \, dt,
\]

where $E_{\text{sw}}$ is the switching energy as a function of the switched current $i_{\text{sw}}$. The inductor current ripple amplitude $\Delta i_L = |i_L^*| + i_0$ leads to a peak-to-peak output voltage ripple

\[
\Delta u_C = \frac{\Delta E_{\text{conv}}}{c_L} = \frac{|i_L^*|^2 i_0}{4 c_L f_1}. \tag{5}
\]

### 2.2 Case Study

Today, variable speed drives make up a significant share of the market for low-voltage inverters. Power ratings around 2.5 kW and output frequencies up to 400 Hz are typical for a wide range of applications such as pumps, gantry robots, packaging, conveyor technology and handling belts in various industries [5]-[8]. Therefore, similar specifications are assumed for a case study in this work, as shown in Table 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC link voltage $U_{DC}$</td>
<td>400 V</td>
</tr>
<tr>
<td>Machine phase voltage (RMS) $u_M$</td>
<td>110 V</td>
</tr>
<tr>
<td>Machine current (RMS) $i_R$</td>
<td>8.5 A</td>
</tr>
<tr>
<td>Machine fundamental frequency $f_1$</td>
<td>400 Hz</td>
</tr>
<tr>
<td>Power factor $\cos(\phi)$</td>
<td>0.92</td>
</tr>
</tbody>
</table>

Table 1. Parameters selected for the case study.

GaN power transistors with a rated blocking voltage of 600 V and $R_{\text{DS,on}} \approx 100$ mΩ (at 100 °C junction temperature) are considered as switches. Soft switching losses are measured using a bridge leg hardware prototype. Details about the switching loss measurement setup and the used gate drive are given in [9]. In this work, the switching energy is approximated as

\[
E_{\text{sw}}(i_{\text{sw}}) = E_0 + E_1 i_{\text{sw}} + E_2 i_{\text{sw}}^2 + E_3 i_{\text{sw}}^3, \tag{6}
\]

where $i_{\text{sw}}$ is the switched current, yielding
where $E_0 = 1.17 \mu J$, $E_1 = 0.1 \mu J/A$, $E_2 = 0.002 \mu J/A^2$ and $E_3 = 0.0027 \mu J/A^3$.

As can be seen in Equation 1, the filter inductance $L_f$ directly affects the maximum occurring switching frequency. Therefore, the minimum value of $L_f$ is constrained by the maximum switching frequency defined by the delays of the signal processing hardware (FPGA) and the measurement circuitry. Thus, the maximum switching frequency is set to $1 \text{ MHz}$. This results in a minimum filter inductance of $9.5 \mu H$, for the operating conditions of Table 1. Since the filter inductors are contributing significantly to the overall inverter volume, it would be a good design choice to use the minimum allowed inductance value. Once the $L_f$ value is set, the minimum filter capacitance value $C_f$ can be determined easily regarding the maximum allowed output voltage ripple $\Delta u_C$ at the worst case. When a maximum voltage ripple of $\Delta u = \Delta u_C / \mu \text{ MR} = 5\%$ is set where $\mu \text{ MR}$ is the peak fundamental machine phase voltage, a minimum filter capacitance of $C_f = 4.7 \mu F$ is necessary.

Figure 3 illustrates the relationship between $m_0$ and the switching frequencies in the three phases, without taking into account the influence of the common mode component of $i_L$.

A circuit simulation using GeckoCIRCUITS software [10] is used in order to numerically verify the analysis presented above. Ideal switches with antiparallel ideal diodes and no parasitic capacitances are used and switched using a hysteresis band control of the inductor current resulting in the TCM current waveform. A fixed time step of $5 \text{ ns}$ is used for solving the circuit model. The resulting switching frequencies, machine phase voltages and the inductor current in phase R are shown in Figure 4.

Table 2 compares the transistor losses calculated analytically, and the transistor losses calculated based on the current waveforms generated by the numerical circuit simulation, and verifies the analytical models.

<table>
<thead>
<tr>
<th></th>
<th>Analytical (Eq. 3, Eq. 7)</th>
<th>Numerical (GeckoCIRCUITS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{\text{cond}}$</td>
<td>35.82 W</td>
<td>36.11 W</td>
</tr>
<tr>
<td>$P_{\text{sw}}$</td>
<td>22.12 W</td>
<td>22.15 W</td>
</tr>
</tbody>
</table>

Table 2. Calculated transistor losses for the case study.

3 Optimum Modulation

3.1 Degrees of Freedom

In order to limit the switching frequency variation, the switching losses and the filter volume, the common-mode voltage $u_0$ (cf. Figure 1) can be utilized as well as a reverse current value $i_0$ that exceeds the value that is needed for ZVS, i.e. $i_0 \geq i_{\text{min}}$ [11]. Considering these two degrees of freedom, Equation 1 for the switching frequency transforms into

$$f_{sX}(\theta) = \frac{m_X - (m_{\text{MAX}} + m_0(\theta))^2}{2\cdot(|i_{LX}(\theta)| + i_{0X}(\theta))} \cdot u_{DC},$$

where $m_{\text{MAX}} = u_{MAX}/u_{DC}$, $m_0 = u_0/u_{DC}$, $i_0 \geq i_{\text{min}}$ is the reverse inductor current and $\theta$ is the electrical angle within the fundamental period. $D_X = m_{\text{MAX}} + m_0 + \frac{1}{2}$ is the duty cycle in phase $X$. Thus, $|m_{\text{MAX}} + m_0| \leq \frac{1}{2}$ has to be satisfied for all three phases.

Figure 5 illustrates the relationship between $m_0$ and the switching frequencies in the three phases, without taking into account the influence of the common mode component of $i_L$. 
caused by \( i_0 \) on the switching frequency. The reverse current is set to its minimum value \( i_{min} \) for all three phases. The boundaries of \( m_0 \) for ensuring \( 0 < D < 1 \) are denoted by the dashed black lines.

Figure 5. Inductor reference currents \( i_L^* \) for \( m_0 = 0 \) and \( i_0 = i_{min} \) (a) and the influence of \( m_0 \) on \( f_s \) at the angle \(-145^\circ\) (b) and \( 132^\circ\) (c). Blue, green and red denote phases R, S and T, respectively. The dashed grey lines in (a) indicate the inductor current situation for (b) and (c). The dashed black lines in (b) and (c) denote the boundaries for \( m_0 \) due to the duty cycle limitation \( 0 < D < 1 \).

3.2 Numerical Optimization

Numerical optimizations are used for finding the optimum \( i_0 \) and \( m_0 \) values that minimize the switching frequency variation, the losses and the filter volume. In order to do so, the waveforms \( i_d(\theta) \) and \( m_0(\theta) \) are parameterized as shown in Figure 6. Parameters \( p_1...p_6 \) define \( i_{d0} \) for \(-180^\circ < \theta < 0\), which is repeated for the other half of the fundamental period. \( i_{d0} \) and \( i_{d0} \) have the same waveform but are \(120^\circ\) phase-shifted. Parameters \( p_7...p_{10} \) are describing \( m_0 \), which is defined as the sum of a sinusoidal and a triangular function with three times the fundamental frequency and with parameterized amplitudes and phases. Particle swarm optimization is chosen as numerical minimization algorithm. A maximum peak-to-peak output voltage ripple of \( \Delta u_{max} = 5\% \), a maximum switching frequency of \( f_{s,\text{max}} = 1 \text{ MHz} \), and a limit on the duty cycle of \( 0.03 < D < 0.97 \) are applied as constraints. Moreover, \( p_6 \geq i_{min} = 5 \text{ A} \) is enforced to guarantee ZVS, and \( p_2 \) is limited to \( p_2 \leq 25 \text{ A} \).

Figure 7 shows the optimization results when a set of optimum values of \( i_0 \) and \( m_0 \) is searched with the goal of minimizing the equally weighted sum of the total transistor losses \( (P_{\text{cond}} + P_{\text{sw}}) \) and the ratio of maximum and minimum switching frequency within a fundamental period. As can be seen, both a nonzero common-mode voltage and \( i_0 \geq i_{min} \) are utilized. As a result, the ratio of the maximum and minimum switching frequency decreases from 7.95 to 2.12. However, the significant increase in \( i_0 \) leads to an 8% increase of the conduction losses (from 35.8 W to 38.77 W). Similarly, the switching losses increase by 12%, increasing the overall transistor losses from 58 W to 63.8 W.

Figure 7. The switching frequency before (solid) and after (dashed) applying the optimized \( m_0 \) and \( i_0 \) values (a). Boundaries (dashed) and optimum waveform (solid) of the common-mode modulation index \( m_0 \) (b). Reverse current profiles (c). Resulting envelope (dashed) and short-term average (solid) of the inductor current in phase R (d). Blue, green and red denote phases R, S and T, respectively. The steps of \( i_{LR} \) arise due to the common-mode current \( i_{CM} = C_d \frac{du_0}{dt} = C_d \frac{u_{DC}}{2} \frac{d}{dt} \frac{m_0}{2} \).

Limiting the switching frequency variation makes the design of a second-stage filter easier, which could be necessary for a grid-tied application of an inverter with strict EMC requirements. Moreover, based on the optimization results shown in Figure 7, the filter inductance \( L_f \) can now be made smaller than 9.5 \( \mu \text{H} \) to minimize the filter volume without violating the 1 MHz switching frequency limit. On the other hand, when the inverter in TCM operation is used for driving an electric machine, the 5% output voltage ripple limit may be sufficient in terms of output voltage distortion. In this case, \( i_0 \) and \( m_0 \) can be optimized for increasing the inverter efficiency.

ZVS allows for higher switching frequencies which is beneficial for miniaturization. However, as an intrinsic property of the TCM operation, the flux in the filter inductors \( L_f \) varies largely within each switching cycle which increases the core losses and complicates the inductor design.
Figure 8 shows the results of an optimization run where the goal has been set to minimize the inductor core losses, which are approximated as

\[
P_{\text{core}} \propto f_i \int_{0}^{1/f_i} f_i^2 (i_{L,UB} - i_{L,LB})^3 \, dt.
\]

(9)

It can be seen that an increase in \(i_0\) is avoided for obviating additional losses, and a different waveform of common mode voltage is applied, which in turn effects the switching frequency (slightly) and the inductor current waveform. As a result, a 14% decrease in core losses are achieved compared to \(u_0 = 0\) and \(i_0 = i_{\text{min}}\).

As explained above, \(L_f = 9.5 \mu\text{H}\) and \(C_f = 4.7 \mu\text{F}\) are the minimum filter component values to ensure \(f_s < 1\text{ MHz}\) and \(\Delta u < 5\%\) for \(i_0 = i_{\text{min}}\) and \(m_0 = 0\). On the other hand, previous examples demonstrate that \(i_0\) and \(m_0\) can be used to affect the circuit behaviour significantly. Therefore, in the next example, the filter components \(L_f\) and \(C_f\) are also optimized along with \(i_0\) and \(m_0\), with the goal of minimizing the sum of equally weighted total transistor losses and the inductor volume, which is approximated to scale as

\[
V_L \propto L_f i_{L,UB} \cdot i_{L,RMS},
\]

(10)

where \(i_{L,RMS}\) denotes the root mean square value of the inductor current. The resulting \(L_f\) is not much different to 9.5 \(\mu\text{H}\), but \(C_f\) has increased to 13 \(\mu\text{F}\). As can be seen in Figure 9, the switching frequency is almost unchanged, and \(i_0\) is not modified; however, a common-mode voltage is used in order to shape the inductor current, and its upper and lower boundaries using the superposition of the common mode current through the inductors. The resulting total transistor losses are nearly identical, but a 10.5% decrease is achieved for the inductor volume.

3.3 Intersection Algorithm

The intersection algorithm bases on the contemplation of figures like depicted in Figure 5(b-c). It goes through the following steps to determine \(m_0\) for a given electrical angle:

1. Determine the switching frequencies of the three phases for \(m_0 = 0\) and \(i_0 = i_{\text{min}}\) and identify the phase with the lowest switching frequency, without loss of generality, e.g. phase T.
2. Calculate for which \(m_0\) phase T has the same switching frequency as phase R or S, i.e. look for the intersections in the \(m_0-f_s\) plots, cf. Figure 5.
3. Take the \(m_0\) with the smallest absolute value and calculate the switching frequency of phase T for this \(m_0\), subsequently called \(f_{s,\text{intersect}}\).

After having determined the \(m_0\) and \(f_{s,\text{intersect}}\) values for the whole fundamental period, identify the maximal \(f_{s,\text{intersect}}\) and utilize \(i_0\) to limit the maximum switching frequency in all phases over the whole period to this value.

The intersection algorithm yields very similar \(m_0\) references as the numerical optimization (compare Figure 7 and Figure 10). According to the circuit simulation, the peak-to-peak output voltage ripple decreased from 5\% to less than 3\%, the transistor
losses increased by 28% and the ratio between maximum and minimum switching frequency decreased from 7.95 to 1.84.

Figure 10. Analytically calculated switching frequency before (solid) and after (dashed) applying the intersection algorithm (a). Boundaries (dashed) and the optimum waveform (solid) of the common-mode modulation index \( m_0 \) (b). Reverse current profiles (c) and the resulting envelope of the inductor current (dashed) and its local average (solid) of phase R (d). Blue, green and red denote phases R, S and T, respectively. The steps of \( i_{LR} \) arise due to the common-mode current \( i_{CM} = C_f \cdot \Delta u_0 / \Delta t = C_f \cdot u_{DC} \cdot \Delta m_0 / \Delta t \).

4 Conclusion and Outlook

Triangular-current mode (TCM) operation may result in higher efficiencies and higher power densities of inverter systems with output filter due to the higher switching frequencies enabled by zero-voltage switching. On the other hand, this mode of operation is characterized by a largely varying switching frequency which is undesired in several applications.

This paper presents new modulation methods for three-phase TCM inverters where the current ripple amplitude and the common-mode voltage are adjusted in order to limit switching frequency variation as well as to increase the efficiency and to minimize the filter volume. Considering 2.5 kW variable speed drive inverter specifications, numerical optimizations are performed with different goals and a reduction of the switching frequency variation by a factor of 4 is demonstrated. Alternatively, the inductor core losses could be decreased by 14% or the filter inductor volume by 10.5%.

A possible challenge in the implementation of the presented methods is the storage and application of the optimum common-mode voltage and reverse current profiles calculated offline. Therefore, an online optimization method, such as perturb and observe, will be considered in the future, and the findings will be verified by measurements.

References