A Novel Three-Phase Utility Interface Minimizing Line Current Harmonics of High-Power Telecommunications Rectifier Modules

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Abstract

Based on the combination of a three-phase diode bridge and DC/DC boost converter a new three-phase three-switch three-level PWM rectifier system is developed. It can be characterized by sinusoidal mains current consumption, controlled output voltage and low blocking voltage stress on the power transistors. The application could be, e.g., for feeding the DC link of a telecommunications power supply module. The stationary operational behavior, the control of the mains currents and of the output voltage are analyzed. Finally, the stresses on the system components are determined by digital simulation and compared to the stresses in a conventional PWM rectifier system.

1 Introduction

Conventional power supplies of the interchanges of telecommunication systems are being replaced more and more by modular rectifier systems due to the advantages of the latter concerning operational behavior, systems technology and costs. There, the rectifier modules (having a three-phase supply for a higher number of subscribers) are realized as voltage DC link converters in general. In the simplest case, the mains AC voltage is converted into a DC link voltage by a three-phase diode bridge with capacitive smoothing. This DC link voltage then is transformed into the output DC voltage by a high-frequency DC-DC converter connected in series.

The realization of the input stage of a power supply module as uncontrolled three-phase bridge (in many cases directly connected to the mains) is motivated by the requirement of a high power density, high efficiency, high reliability (robustness) and low cost. However, this concept shows the disadvantage of high effects on the mains due to high amplitudes of low-frequency mains current harmonics which lead to a distortion of the mains voltage. Therefore the danger of an influence on or disturbance of other loads is present. This is true especially for high installed power and high inner mains impedance. In connection with the limitation of harmonics stress on the public low-voltage mains caused by power electronic converters - as requested by guidelines [1], recommendations and future standards (IEEE Std. 519-1992, IEC-555-2 and IEC-555-4 [2]) - the development of AC-DC converters having low influence on the mains is of special importance. This is especially important for guaranteeing universal applicability of telecommunication rectifier modules.

The scope of this paper is the development and analysis of a new, three-phase, high-frequency unidirectional PWM AC/DC converter for feeding the DC link of a 12-kW-telecommunication power supply module. For the determination of the circuit concept the following basic requirements are given:

- approximately sinusoidal current consumption
- resistive mains behavior
- controlled output voltage
- low blocking voltage stress on the power transistors
- high power density
- high efficiency
- low complexity of the power and control circuits
- high reliability.

In the following (**section 2**) the topology of a new three-phase three-switch three-level boost converter is derived based on the basic structure of the power circuit of a three-phase AC/DC converter with controlled output voltage. This basic structure mentioned is based on the series connection of a three-phase diode bridge and a DC/DC boost converter. In **section 3** the stationary operational behavior, as well as the hysteresis control (in order to have low development and production costs) of the mains current and the output voltage control are discussed. The realization of these considerations is discussed in **section 4** by using digital simulation. Finally, in **section 5** the voltage and current stresses on the active and passive components are given for

- output power 12.6 kW
- output voltage 700 V
- mains line-to-line voltage 400 V

Also, a comparison is made to the component stresses of a conventional six-switch two-level voltage DC link PWM rectifier system.

2 Derivation of the Circuit Structure

For the realization of a three-phase, unidirectional AC/DC converter with controllable output voltage a series connection of an uncontrolled diode bridge and a DC/DC boost converter can be used in the simplest case (cf. **Fig.1(a)**, [4]). However, in the mains current spectrum of this system low frequency harmonics of high amplitude are present because due to the operating principle of a three-phase diode bridge always only two phases conduct current (with the exception of the commutation intervals). Therefore, the phase current shape shows $\frac{\pi}{3}$-wide intervals with zero current.

A reduction of the effects on the mains of this system can be obtained by placing the inductor L on the AC side and by operating the converter in the discontinuous conduction mode (DCM) [6]. Analogous to the DCM of single-phase AC/DC boost converters [7] in this case a voltage proportional guidance of the peak values of the discontinuous input currents (for time constant duty cycle of the power transistor T) is given directly by the mains phase voltages. As a closer analysis of the system behavior shows, the harmonic content of the mains currents remaining after filtering of the discontinuous input quantities is essentially determined by the output voltage level [8]. A largely sinusoidal mains current shape is linked to an output voltage being large with respect to the amplitude of the line-to-line mains voltage. For operating the system with the European low voltage mains (nominal line-to-line voltage: 380 V) we therefore have to split up the DC-side converter part (due to the blocking voltage stress on the DC side power semiconductors for an output voltage > 1 kV) into two simultaneously pulsed partial systems (cf. Fig.1(**b**)) having each to sustain half of the DC link voltage.

The application of the circuit described so far is limited especially by the discontinuous input current shape leading to high current stress on the power semiconductor devices and by the filtering effort required for limiting the conducted EMI (electromagnetic influence) [10]. These aspects exist additionally to the high blocking voltage stress on the power semiconductor devices of a converter fed from the high DC link voltage. Therefore, for the requirement of high output power one has to ask the question for alternate concepts of three-phase, unidirectional PWM boost rectifiers with continuous input current showing (ideally) purely sinusoidal shape and being independent of the output voltage level (being larger than the maximum value of the line-to-line mains voltage).

The current consumption of the system shown in Fig.1(b) is defined in general by the difference between mains voltage and rectifier input voltage lying across the inductances connected in series at the input. A continuous, sinusoidal mains current shape (with the exception of the harmonics with

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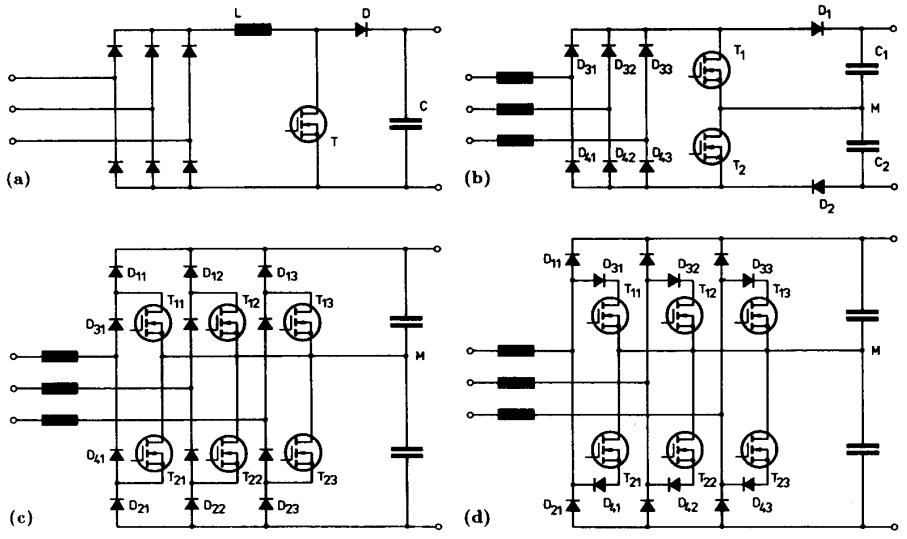

Fig.1: Development of the basic circuit structures of three-phase three-level PWM rectifiers (cf. **(c)** and **(d)**) based on a combination of a three-phase diode bridge and a DC/DC boost converter **(a)**.

pulse frequency and their multiples) therefore is obtained only by rectifier input voltages having sinusoidal shape in the average over a pulse period. Therefore, this requires a seperate controllability of the voltage synthesis of each phase or the application of transistors T_{1j} and T_{2j} and of ouptput diodes D_{1j} and D_{2j}, $j = 1, 2, 3$, in each bridge leg, respectively (cf. Fig.1(c)). Due to the inclusion of the center point of the output voltage into the system function, all power semiconductors of the resulting circuit (called *forced commutated three-phase boost type rectifier* in [11]) only have to sustain half of the output voltage. However, the advantage of the low blocking voltage stress is followed by the disadvantage of relatively high conduction losses because the entire current flow connected with supplying the output power goes through the diode legs due to the rectifier function of the converter.

A reduction of the conduction losses can be obtained by shifting the diodes D_{3j} and D_{4j} into the circuit legs controlling the conduction state of the converter (cf. Fig.1(**d**)). Due to the control legs of each phase lying in antiparallel a bidirectional, bipolar turn-off power switch is realized by this which can be replaced by a combination of a single-phase diode bridge D_i and a power transistor T_i, i =R,S,T, (cf. **Fig.2**). Compared to a realization according to Fig.1(c) this results (besides reducing the conduction losses) in reduced circuit complexity and control effort and in a higher utilization of the switching capacity of the power transistors. Therefore, in the case at hand we want to limit a closer analysis to the circuit shown in Fig.2, being called *three-phase three-switch three-level (three-phase/switch/level) PWM rectifier* in the following.

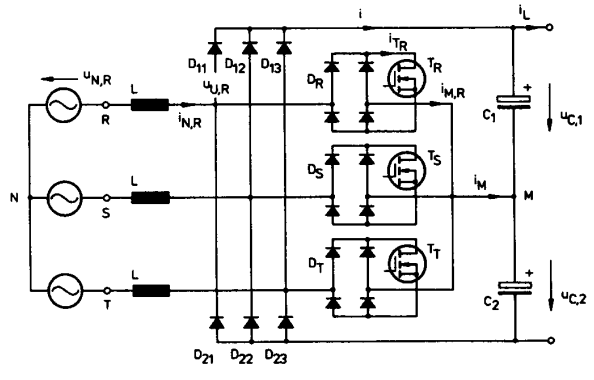

Fig.2: Basic structure of a three-phase/switch/level unity power factor PWM rectifier resulting by further development of of Fig.1(d); the feeding mains is replaced by a voltage sources $u_{N,i}$, $i = R, S, T$.

One has to mention that regarding the circuits shown in Fig.1(c) and Fig.1(d) a close topological relationship exists to the basic types of three-phase three-level PWM *inverters* introduced in [12] and [13]. Furthermore, one has to point out a modified circuit realization proposed in [14] according to Fig.1(c), a PWM inverter circuit being identical with Fig.2 regarding the control leg realization (as analyzed in [15]) and a converter structure which can be derived by further development of the circuit according to Fig.2 as described in [16] using low switching frequency, i.e. three times the mains frequency. Single-phase realizations of the circuits given in Figs.1(b)–(d) are analyzed in [17].

For the sake of completeness we finally want to point the attention to papers describing circuit concepts of three-switch *two-level* PWM rectifiers, e.g., [18], [19] (cf. pp. 87–89), [20], [21] and [22].

3 Principle of Operation

3.1 Basic Function

For describing the basic function of the rectifier system shown in Fig.2 the analysis is limited to the fundamentals of the system quantities on the AC side.

Based on a single-phase equivalent circuit (cf. **Fig.3**) there follows (using complex AC current calculus) for the phasor of the rectifier input voltage fundamental

$$\underline{U}_{U,(1)} = \underline{U}_N - j\omega_N L \underline{I}_{N,(1)} \,. \tag{1}$$

The current consumption (and, therefore, the basis for the power consumption)

$$\underline{I}_{N,(1)} = \hat{I}_{N,(1)} \exp j(\varphi_N - \varphi) \tag{2}$$

($\varphi_N = \omega_N t$) of the system is defined by the voltage lying across the inductances L connected in series on the AC side. There, this voltage is the difference between the (sinusoidal) mains voltage

$$\underline{U}_N = \hat{U}_N \exp j\varphi_N \tag{3}$$

and the rectifier input voltage fundamental $\underline{U}_{U,(1)}$ which can be controlled regarding amplitude and phase via appropriate pulsation of the power transistors T_i, i = R,S,T (cf. sections 3.2 and 3.4).

The power delivered to the DC side follows (if the system losses are neglected), based on the power balance, as

$$P_O = U_O I_O = \frac{3}{2} \hat{U}_N \hat{I}_{N,(1)} \cos\varphi \,. \tag{4}$$

3.2 Rectifier Input Voltage

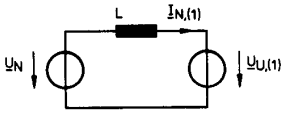

Fig.3: Single-phase equivalent circuit related to the fundamental for the AC-side system section of a three-phase/switch/level PWM rectifier.

Forming of a rectifier input phase voltage $u_{U,i}$ is influenced according to

$$u_{U,i} = \begin{cases} \text{sign}\{i_{N,i}\}\frac{U_O}{2} & \text{if } s_i = 0 \\ 0 & \text{if } s_i = 1 \end{cases} \tag{5}$$

also by the sign (direction) of the associated mains phase current $i_{N,i}$ besides by the switching state of the power transistor T_i defined by a binary switching function s_i. (As reference point of the voltage $u_{U,i}$ the center point M of the DC link voltage is chosen.) Each brigde leg shows a three-level characteristic, i.e. three possible voltage values $+\frac{U_O}{2}$, 0 and $-\frac{U_O}{2}$. Accordingly, the system is called three-level PWM rectifier.

3.3 Stationary Operating Region

Due to the influence on the voltage generation caused by the sign of the phase currents (cf. Eq.(5)), the stationary maximum amplitude of the rectifier input voltage fundamental $\hat{U}_{U,(1),\max}$ (how it can be obtained without overmodulation) is defined also by the phase difference between $\underline{U}_{U,(1)}$ and the mains current $\underline{I}_{N,(1)}$. This definition by the phase difference has to be seen besides the control limit $\hat{U}_{U,(1),\max} \leq \frac{1}{\sqrt{3}}U_O$ which is given basically for bridge circuits. The definition of $\underline{U}_{U,(1)}$ is equivalent to defining the operating region of the converter (cf. Eq.(1)).

For the case of a resistive mains fundamental behavior ($\varphi = 0$, cf. Eq.(2)) being important for practical applications the operating region of the PWM rectifier system is determined by

$$u_K \leq \begin{cases} \frac{1}{\sqrt{3}}(M-1) & \text{if } M \leq 2 \\ \frac{1}{\sqrt{3}} & \text{if } M > 2 \end{cases} \tag{6}$$

where

$$u_K = \frac{1}{\hat{U}_N}\hat{I}_{N,(1)}\omega_N L \tag{7}$$

characterizes the load condition of the converter and where

$$M = \frac{U_O}{\sqrt{3}\hat{U}_N} \tag{8}$$

defines the system voltage transformation. Because for high pulse frequency of the system there is always $u_K \ll 1$ (typically $u_K \approx 0.01 \ldots 0.02$), only the limitation for $M \leq 2$ is of importance in Eq.(6). For the minimum value of the output voltage there follows accordingly

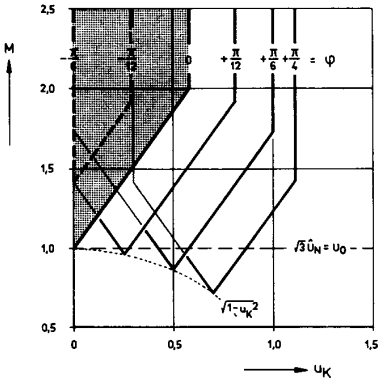

Fig.4: Dependency of the operating region of a three-phase/switch/level PWM rectifier system on the phase angle φ of the mains current (representation limited to angles within the interval $\varphi \in [-\frac{\pi}{6}, +\frac{\pi}{4}]$ for the sake of clearness). The limits of the operating regions are show by solid lines for $\varphi > 0$, for $\varphi < 0$ dashed lines are used. The operation region for resistive mains fundamental behavior ($\varphi = 0$) is marked by the dotted area.

$$U_O \geq \sqrt{3}\hat{U}_N + 3\hat{I}_{N,(1),\max}\omega_N L \; . \tag{9}$$

Remark: For deriving Eq.(6) a description of the system operation based on complex three-phase phasors (complex space vectors) is advantageous due to special clearness and a simpler calculation [23] as compared to a calculation with phase quantities. The analysis (not shown in detail here for the sake of brevity) also shows a basic restriction

$$-\frac{\pi}{6} \leq \varphi \leq \frac{\pi}{2} \tag{10}$$

of the operation of the rectifier system with inductive ($\varphi > 0$) or capacitive phase angle of the mains current. According to **Fig.4** $\varphi = -\frac{\pi}{6}$ is only obtained there for $u_K \to 0$ or for $\hat{I}_{N,(1)} \to 0$ and, therefore, it constitutes only a theoretical limiting case. The real power transferred to the output circuit

$$P_O = \frac{3}{2}\frac{\hat{U}_N^2}{\omega_N L}u_K \cos\varphi \tag{11}$$

becomes zero at both limits of the operating region. Feeding back of energy from the output circuit into the mains ($\varphi \in (\frac{\pi}{2}, \pi]$ or $\varphi \in (-\pi, -\frac{\pi}{2})$) therefore is not possible as can be seen also immediately from the circuit structure (cf. Fig.2).

System operation with a capacitive phase angle in general is linked to a higher amplitude of the rectifier input voltage as compared to inductive mains behavior. This can be explained based on a phasor diagram. This also means, that a higher value of the DC link voltage and/or a higher voltage transformation ratio M is involved (cf. **Fig.4**).

Due to the dependency of the system control region on the phase difference of the fundamental of the rectifier input voltage and of the mains current, the minimum value $M_{\min}$ to be maintained for $u_K \to 0$ for capacitive *and* inductive mains current phase angle φ lies above the value $M_{\min} = 1$ which is given for resistive mains behavior. For inductive mains behavior the output voltage U_O can theoretically be lowered in a section of the operating region below the voltage value $U_O = \sqrt{3}\hat{U}_N$ (and/or $M = 1$) resulting in the case of no-load and uncontrolled rectification ($s_i = 0$). $\varphi \geq \frac{\pi}{6}$ requires a minimum load $u_K > 0$ of the system and is, therefore, of little practical importance.

3.4 Mains Current Control

The control of the power transistors and/or of the rectifier input voltage synthesis can be performed in the simplest case by a a hysteresis control of the phase currents by independent phase current controllers.

The amplitude of the phase current reference values

$$i_{N,i}^{*\prime} = \hat{I}_N^* \frac{u_{N,i}}{\hat{U}_N} \tag{12}$$

(which are derived directly from the phase voltages for resistive mains behavior) is given there by an output voltage controller $F(s)$ which is superimposed on the current control loop (cf. **Fig.5**).

The dependency of the sign of a rectifier input phase voltage $u_{U,i}$ (formed for $s_i = 0$) on the sign of the associated phase current $i_{N,i}$ (cf. Eq.(5)) has to be considered by generating the control signals s_i of the power transistors by an inversion

$$s_i = \begin{cases} s_i' & \text{if } i_{N,i}^* \geq 0 \\ \text{NOT}\, s_i' & \text{if } i_{N,i}^* < 0 \end{cases} \tag{13}$$

(as controlled by the sign of the mains current reference value $\text{sign}(i_{N,i}^*)$, cf. Fig.5) of the switching decision

$$s_i' = \begin{cases} 0 & \text{if } i_{N,i} > i_{N,i}^* + h \\ 1 & \text{if } i_{N,i} < i_{N,i}^* - h \end{cases} \tag{14}$$

of the associated hysteresis controller.

As already explained in section 3.1, the mains current consumption of the PWM rectifier system is defined by the voltage lying across the series inductances L

$$L\frac{\mathrm{d}i_{N,i}}{\mathrm{d}t} = u_{N,i} - (u_{U,i} - u_N) \qquad i = \mathrm{R,S,T} \; . \tag{15}$$

Via the voltage of the floating mains star point

$$u_N = \frac{1}{3}\sum_{i=\mathrm{R,S,T}} u_{U,i} \tag{16}$$

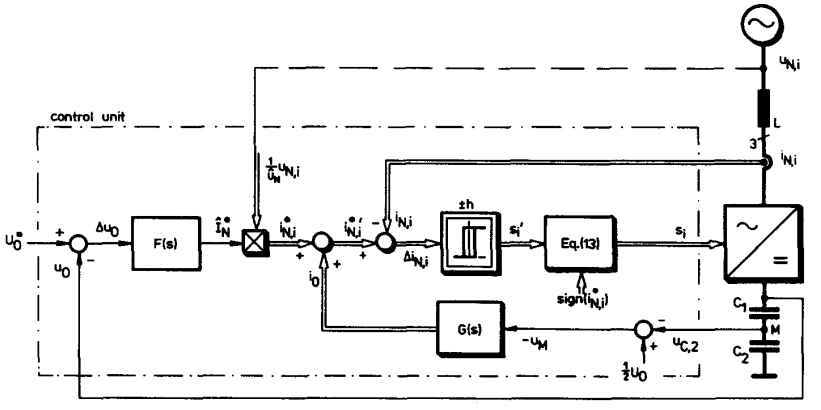

Fig.5: Multi-loop control of a three-phase/switch/level PWM rectifier system. Outer control loops: $F(s)$: control of the output voltage u_O; $G(s)$: balancing of the output partial voltages $u_{C,1}$ und $u_{C,2}$. Inner control loop: hysteresis control of the phase currents $i_{N,i}$, $i = R, S, T$. The switching decisions of the hysteresis controllers are inverted according to Eq.(13) for $\text{sign}(i^*_{N,i}) = -1$; for the sake of clearness signal paths equivalent for all phases are combined into double lines.

which is influenced by the switching state of all phases a coupling of the phase current changes is given. If independent phase current controllers are used, this coupling leads to the occurrence of limit cycles [24] and, therefore, to a non-optimal utilization of the converter pulse frequency. Furthermore, the control error is not restricted to the deadband width h; the maximum value of the phase current ripple is defined by twice the value of the deadband width.

An avoidance of this disadvantages mentioned so can be achieved by coordinating the switching actions of the phase current controllers [25], [26], [24]. This shall not be explained here in detail for the sake of brevity.

3.5 Balancing of the Output Partial Voltages

Besides control of the output voltage and of the mains phase currents a symmetrical split

$$u_{C,1} = u_{C,2} = \frac{U_O}{2} \tag{17}$$

of the output voltage has to be guaranteed by the control system of the converter. An unsymmetry of the output capacitor voltages $u_{C,1}$ and $u_{C,2}$ (caused by loading the capacitive center point M by a DC current or low frequency AC current) may be characterized by the voltage

$$u_M = \frac{1}{2}(u_{C,2} - u_{C,1}) \tag{18}$$

referred to the ficticious (ideal) center point of the output voltage. This unsymmetry will cause an increased voltage stress on the output capacitors, an increased blocking voltage stress on the power semiconductor devices situated in the control legs and to an uneven current stress on the components over the fundamental period. An ideally symmetric split of the output voltage is given for $u_M = 0$ (as can be seen from Eq.(18)). The current

$$i_M = \sum_{i=\text{R,S,T}} s_i \, i_{N,i} \tag{19}$$

loading the capacitive center point is formed by segments of the phase currents in dependency on the switching states s_i of the power transistors T_i. For the voltage shift of the center point there follows with $C_1 = C_2 = C$ (cf. Fig.2):

$$\frac{\mathrm{d}u_M}{\mathrm{d}t} = \frac{1}{2C} i_M \; . \tag{20}$$

For a clear description of the behavior in the following a purely sinusoidal and symmetrical shape of the mains phase currents

$$\begin{aligned} i_{N,R} &= \hat{I}^*_N \cos(\varphi_N) \\ i_{N,S} &= \hat{I}^*_N \cos(\varphi_N - \frac{2\pi}{3}) \\ i_{N,T} &= \hat{I}^*_N \cos(\varphi_N + \frac{2\pi}{3}) \; , \end{aligned} \tag{21}$$

and/or $i_{N,i} = i^*_{N,i}$ is assumed. Also, the analysis of the (stationary) operation is limited to an interval of the mains period $\varphi_N \in [-\frac{\pi}{6}, +\frac{\pi}{6}]$. Due to the phase-symmetrical circuit structure this includes the basic relationships within the entire mains period.

The center point currents i_M (cf. Gl.(19)) resulting for the possible combinations of the phase switching functions s_i (the different switching states of the converter) are given in **Tab.1**.

s_R	s_S	s_T	i_M	$(\frac{\mathrm{d}u_M}{\mathrm{d}t})_{\text{avg}}$
0	0	0	0	0
0	0	1	i_T	−
0	1	0	i_S	−
0	1	1	$-i_R$	−−
1	0	0	$+i_R$	++
1	0	1	$-i_S$	+
1	1	0	$-i_T$	+
1	1	1	0	0

Tab.1: Center point current i_M and variation of the center point potential u_M in dependency on the converter switching state for $\varphi_N \in [-\frac{\pi}{6}, +\frac{\pi}{6}]$ or $i_{N,R} > 0$, $i_{N,S} < 0$, $i_{N,T} < 0$ ($i_{N,R} \geq |i_{N,S}|, |i_{N,T}|$), respectively (cf. Eq.(21)). $(\frac{\mathrm{d}u_M}{\mathrm{d}t})_{\text{avg}}$ weights the potential shift (caused by a switching state) based on a relative on-time being equal for each switching state (s_R, s_S, s_T) and being constant over φ_N; assumptions: purely sinusoidal mains current shape and high, time constant pulse frequency.

As described already in section 3.4, a mutual influence of the phase current controllers is given due to the floating mains star point for independent hysteresis control of the phase currents; this leads to an arbitrary sequence and to a very variable duration of the single converter switching states (s_R, s_S, s_T). It is clear from the weighting of the switching states regarding the influence of the center point potential (cf. Tab.1) that one cannot expect a time constant average value of the center point voltage U_M (gained by averaging u_M over the mains period). This is also true because, as a closer analysis shows, for hysteresis control of the phase currents a positive feedback effect occurs: an unsymmetry of the output voltage leads to the occurrence of a current mean value (related to the fundamental period)

$$I_M = R_M^{-1} U_M \tag{22}$$

(being in a first approximation proportional to the unsymmetry) increasing the unsymmetry. Therefore, a symmetrical split of the output voltage can only be obtained by controlling the voltage u_M via influencing the frequency and duration of the single switching states. Because the converter switching state is derived directly from the difference of reference and actual values of the phase currents the possibiltiy of control interaction is basically limited to a modification of the current reference value synthesis. The only degree of freedom existing here is by addition of a zero component

$$\begin{aligned} i^*_{N,R} &= i^*_{N,R}{}' + i_0 \\ i^*_{N,S} &= i^*_{N,S}{}' + i_0 \\ i^*_{N,T} &= i^*_{N,T}{}' + i_0 \end{aligned} \tag{23}$$

(of an offset i_0 equal for all phases) due to the amplitude $\hat{I}^*_N$ being fixed by the power to be delivered and by the sinusoidal shape required for low influence on the mains. The zero component i_0 cannot be set by the phase current controllers due to the floating mains star point $(i_{N,R} + i_{N,S} + i_{N,T} \equiv$

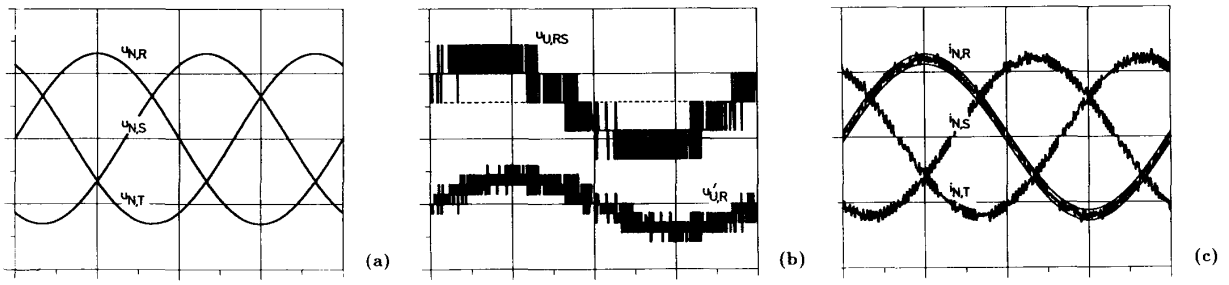

Fig.6: Digital simulation of a three-phase/ switch/level unity power factor PWM rectifier. Representation for one mains period; hysteresis control of the phase currents. **(a):** mains phase voltages $u_{N,(RST)}$ (related to the mains star point N, cf. Fig.2), 250 V/div; **(b):** line-to-line rectifier voltage $u_{U,RS} = u_{U,R} - u_{U,S}$ and phase voltage $u'_{U,R} = u_{U,R} - u_N$ determining the phase current $i_{N,R}$ in connection with $u_{N,R}$ (cf. Eq.(15)), 800 V/div; **(c):** mains phase currents $i_{N,i}$, for phase R the switching thresholds $i^*_{N,R} + h$ and $i^*_{N,R} - h$ of the hysteresis control are shown, 25 A/div. Parameters: $P_O = 14.7\,\mathrm{kW}$, $U_N = 230\,\mathrm{V}$, $U_O = 700\,\mathrm{V}$, $L = 2.5\,\mathrm{mH}$, $h = 2.0\,\mathrm{A}$.

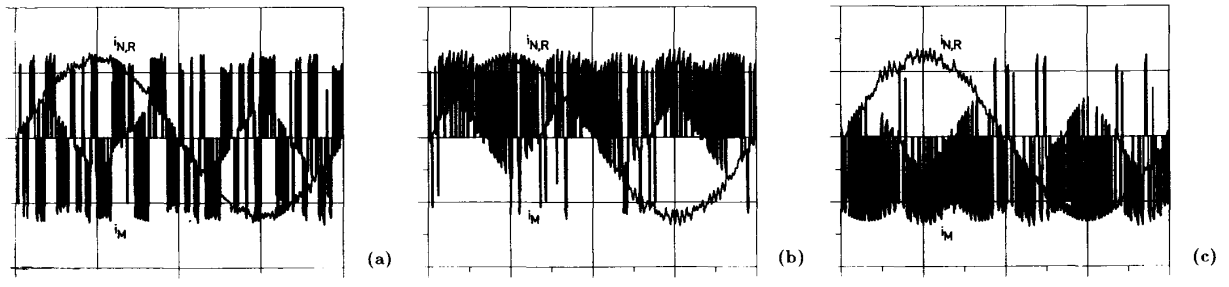

Fig.7: Digital simulation of the function of balancing the output partial voltages $u_{C,1}$ and $u_{C,2}$ by addition of an offset i_0 to the reference values of the phase current hysteresis control (cf. Fig.5). Representation of the mains phase current $i_{N,R}$ and of the current i_M loading the center point (cf. Fig.2 and Eq.(19)); 25 A/div; **(a):** $i_0 = 0$ (no influence of the current control), $I_M = -0.53\,\mathrm{A}$ (I_M denotes the mean value of the center point current i_M within one mains period); **(b):** $i_0 = I_0 = +0.5\,\mathrm{A}$, $I_M = 10.4\,A$ ($k_M = 20.8$, cf Eq.(24)) and **(c):** $i_0 = I_0 = -0.5\,\mathrm{A}$, $I_M = -11.1\,\mathrm{A}$ ($k_M = 22.2$). Parameters equal as for Fig.6.

0) and therefore does not lead to a direct influence on the mains current shape. However, it influences the frequency and duration of the switching states used for control of the mains current and, therefore, also of the value of the center point current i_M.

According to Eq.(13) and Eq.(14) a time-constant positive value $i_0 = I_0 > 0$ in the angle interval $\varphi_U \in [-\frac{\pi}{6}, +\frac{\pi}{6}]$ considered leads to favoring of the switching states $s_R = 1, s_S = 0$ and $s_T = 0$ leading to a time average $I_M > 0$ (cf. Tab. 1). For $I_0 < 0$ there follows in an analogous manner $I_M < 0$. As shown in Fig.3, with this the quantitiy i_0 can be used directly for balancing of the output partial voltages.

4 Digital Simulation

The results of a digital simulation of the stationary operating behavior of the system are shown in Figs.6 and 7.

As **Fig.6** shows, the three-level characteristic of the bridge legs of the converter results in a very good approximation of the effective rectifier input voltage $u_{U,i}' = u_{U,i} - u_N$ (cf. Eq.(15)) to the ideal sinusoidal form. Therefore, also for relatively low average switching frequency or low rated power of the inductances L a low rms value of the current ripple is obtained.

By the signal shapes shown in **Fig.7** the considerations concerning the control of the output center point voltage u_M via a shift by i_0 of the phase current reference values are proven. For a clear representation of the relationships very large values I_0 are chosen (which are not characteristic for the - in reality - only low influence of the control). In general, the amount of the resulting center point current mean value I_M is determined essentially by the ratio of the amplitude of the mains currents $\hat{I}_N$ and the hysteresis width $2h$. Due to the then high gain

$$k_M = \frac{I_M}{I_0} \tag{24}$$

of the system to be controlled the balancing of the output partial voltages is made possible by addition of an offset i_0 being small as compared to h.

As an FFT (Fast Fourier Transform, which is not discussed here for the sake of brevity) of various mains fundamental periods of the rectifier input current shape shows and and as is immediately clear from a relation of the quantities

$$i_0 \approx 0.01 \ldots 0.05\,h \tag{25}$$

($h \approx 0.05 \ldots 0.1\,\hat{I}_{N,(1),\mathrm{max}}$) being typical for a practical system realization, the amplitudes and the spectrum distribution of the current harmonics are only little influenced there. There do not occur low-frequency distortions of the mains current. The amplitudes of the even-order harmonics (which are caused by the unsymmetry due to the shift i_0 of the phase current reference values) remain limited to the values of neighbouring odd harmonics.

5 System Evaluation

For an evaluation of the proposed system the characteristic current and voltage stresses on the devices are compared (cf. Tab.2) to those of a conventional two-level voltage DC link PWM rectifier system shown in **Fig.8** (cf. e.g., section 17-7 in [27] or [28]). Because this converter circuit is also incorporated into a comparison of concepts of converters with low effects on the mains in [29] and [30], there is also given a relation to other rectifier circuits.

There has to be pointed out, however, that the circuit shown in Fig.8 allows (contrary to the circuit described in the paper) also an energy feedback from the output circuit into the mains. One also can say that it does not have a basic limitation of the phase angle region of the mains current. Furthermore, one has to mention that the control limit is not influenced by the phase difference of the fundamentals of the rectifier input voltage and of the mains current (cf. section 3.3). The system operating region for resistive mains load is defined by

$$u_K \leq \sqrt{M^2 - 1}\ . \tag{26}$$

For given input power (and equal rating of the series inductors L) this results in a minimum value of the DC link voltage which is lower as compared to Eq.(9). Therefore, the comparison of the component stresses as given in the following has to be seen as making reference to a (general) evaluation basis and not as a direct comparison of the circuit concepts.

The characteristic component stresses are determined by digital simulation based on nominal values:

$$\begin{aligned} P_O &= 12.6\,\mathrm{kW} \\ U_N &= 400\,\mathrm{V}/230\,\mathrm{V} \\ f_N &= 50\,\mathrm{Hz} \\ U_O &= 700\,\mathrm{V} \end{aligned} \tag{27}$$

as given for the development of a 200 A/60 V-telecommunications power supply module intended to be used with the European low voltage system. There, the control of the mains current is realized by hysteresis control as described in section 3.4. The phase current reference values are given proportional to the mains phase voltages (cf. Eq.(12)). The efficiency of the DC/DC output stage of the module (whose concept is laid out as an AC/DC-DC/DC converter) is estimated by $\eta_{\mathrm{DC/DC}} = 0.95$. For the circuit parameters we choose:

$$\begin{aligned} L &= 0.3\,\mathrm{mH} \\ h &= 1.5\,\mathrm{A}\ . \end{aligned} \tag{28}$$

As one can see from the comparison of the component stresses of the converter systems (cf. **Tab.2**), a significantly lower average switching frequency of the power transistors occurs for the three-phase/switch/level PWM rectifier for equal hysteresis width and for approximately equal harmonic rms value $\Delta I_{N,\mathrm{rms}}$ ($\Delta i_{N,i} = i^*_{N,i} - i_{N,i}$) of the mains current. This is obtained by the better approximation of an ideally sinusoidal shape of the rectifier input voltages due to the three-level characteristic . Therefore, equal average switching frequency can reduce the value of L (as compared to a realization by a two-level PWM rectifier). Furthermore, this results in a higher power density of the converter.

A further advantage of the three-level rectifier system consists in the cutting of the blocking voltage stress $U_{T,\mathrm{max},i}$ (without considering switching overvoltages) of the power transistors into one half. This allows the application of MOSFETs with lower blocking voltage. Due to the lower on-resistance $R_{DS,\mathrm{on}}$ for lower blocking voltage also lower transistor conduction losses are obtained (besides lower turn-off losses due to the lower blocking voltage). This gives higher efficiency of the energy conversion.

Characteristic Value	Proposed System	Conventional System
$I_{N,(1),\mathrm{rms}}$ [A]	19.0	19.0
$I_{N,\mathrm{max},i}$ [A]	29.9	29.9
$\Delta I_{N,\mathrm{rms}}$ [A]	0.62	0.65
$I_{T,\mathrm{avg}}$ [A]	4.4	1.2
$I_{T,\mathrm{rms}}$ [A]	8.6	4.5
$U_{T,\mathrm{max},i}$ [V]	350	700
$I_{D,\mathrm{avg}}$ [A]	6.0	7.2
$I_{D,\mathrm{rms}}$ [A]	11.5	12.4
$U_{D,\mathrm{max},i}$ [V]	700	700
$I_{C,\mathrm{rms}}$ [A]	9.3	9.5
$f_{P,\mathrm{avg}}$ [kHz]	33.3	57.3

Tab.2: Comparison of the quantities characterizing the component stress of a three-phase/switch/level PWM rectifier system and of a conventional three-phase six-switch two-level PWM rectifier system (cf. Fig.8). Operating parameters: $P_O = 12.6\,\mathrm{kW}$, $U_O = 700\,\mathrm{V}$, $U_{N,\mathrm{rms}} = 230\,\mathrm{V}$, $L = 0.3\,\mathrm{mH}$. $h = 1.5\,\mathrm{A}$ ($= 0.05\hat{I}_{N,(1)}$).

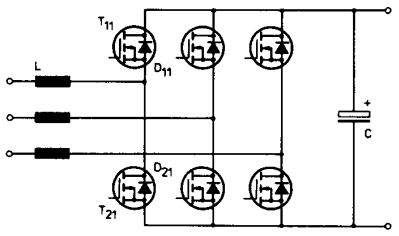

Fig.8: Structure of the power circuit of a conventional three-phase six-switch *two-level* PWM rectifier system.

Also, a comparison of the total volt-ampere-rating $\sum U_{T,\mathrm{max},i}\, I_{T,\mathrm{max},i}$, i = R,S,T ($I_{T,\mathrm{max},i} = \hat{I}_{N,\mathrm{max},i}$), of the transistors of the conventional system shows an advantage of the three-level converter; the two-level rectifier system requires a *four times* higher total volt-ampere-rating of the power transistors.

If the two turn-off power semiconductors which are located in each of the three bridge legs of the conventional rectifier system are paralled (e.g., T_{11} and T_{21}, cf. Fig.8) in each phase and used for realization of the corresponding turn-off power switch of the three-level rectifier, we have an approximately equal average current stress $I_{T,\mathrm{avg}}$ and $I_{T,\mathrm{rms}}$ for the single transistors in both cases. Also, regarding the rms values $I_{N,\mathrm{rms}}$ of the mains currents, the stresses on the diodes carrying the power flow and the stresses on the capacitors, there are only minor differences between both systems.

6 Conclusions

Based on the basic structure of a three-phase AC/DC boost converter in this paper the topology of a three-phase/switch/level PWM rectifier is developed. Also, a method for controlling the output voltage and the mains current and for balancing of the partial output voltages is given.

In the following the advantages and disadvantages being relevant for a qualitative evaluation of the converter concept (as can be used, e.g., for a concept study) are summarized briefly:

Advantages:

- simple structure of power and control circuit, only one power transistor per phase (low control/driving effort); possibility of realization of the control circuit by analog techniques – high dynamics, avoidance of the development effort associated with the application of microprocessor control
- low harmonics rms value of the mains current due to inclusion of the center point of the output voltage into the synthesis of the rectifier input phase voltages (three-level characteristic); for hysteresis control of the input currents: distribution of the power harmonics over a wide frequency range due to time-varying switching frequency [31] – as compared to constant switching frequency lower filtering effort for compliance to the regulations concerning conducted EMI [32] is required
- low blocking voltage stress on the power transistors (possibility of application of low-voltage MOSFETs even for high DC link voltage – low transistor conduction losses; low switching losses)
- low nominal power of the inductances connected in series on the mains side (high dynamics of the DC link voltage control and/or reduction of the DC link capacitance required for buffering of load steps) – high power density and/or power/weight ratio of the converter
- possibility of operating the system with inductive mains phase current angle allows partial compensation of the capacitive reactive power caused by an EMI filter; furthermore, this gives a degree of freedom for an optimization of the mains filter (cf. Fig.7 and Fig.8 in [33])
- as compared to bridge circuits: significantly higher utilization of the switching capacity of the power transistors (conduction of each transistor during positive and negative half period of the related phase current); higher reliability of operation – in the case of a control malfunction of the power transistors no short circuit of the output voltage occurs.

Disadvantages:

- Limitation of the system operating region concerning the phase angle of the mains current and voltage transformation ratio M (cf. section 3.3), especially limitation to unidirectional energy conversion
- minimum output voltage and blocking voltage stress on the diodes $D_{1,j}$ and $D_{2,j}$, $j = 1, 2, 3$, lying above the peak value of the line-to-line mains voltage (the blocking behavior of the diodes has an essential influence on the resulting switching losses [34])
- the single-phase diode bridges D_i, i = R,S,T (cf. Fig.2), situated in the center point legs, cannot be realized as mains rectifier modules (due to the high current rate of rise when the phase transitors T_i are turned on); for avoiding high turn-on losses diodes with short forward recovery time have to be applied. A commutation of the diodes with switching frequency can be avoided by integration of the diode bridges D_i (and of the power transistors T_i) into the associated legs of the three-phase diode bridge at the input side (cf. **Fig.9**). However, this is followed by an increase of the conduction losses. *Remark:* If the bridge legs of the circuit according to Fig.9 are connected in delta, we receive a *two-level* PWM rectifier as introduced in [18].
- for hysteresis control of the input currents by independent phase controllers: current control error possible in the order of magnitude of twice the hysteresis width; occurrance of limit cycles [24] – non optimal utilization of the converter pulse frequency.

In order to minimize the effort regarding the circuit technology and/or of development, system and fabrication costs in the present case a simple control method (which can be realized by analog means) has been selected on purpose. Naturally, this does not lead to a minimization of the harmonics rms value of the mains current or of the switching frequency. The possibility of a relevant optimization (described in the literature for three-level PWM *inverters* [35], [36], [37]) is only given when the converter control unit is realized by digital means, e.g., when a signal processor system is used. This is the topic of further research at present.

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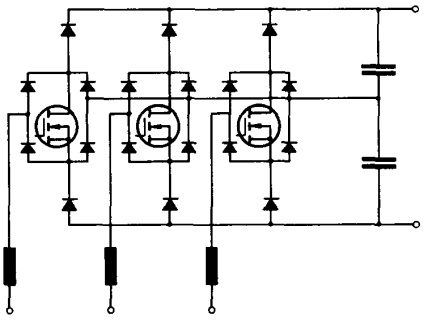

Fig.9 Structure of the power circuit of a three-phase/switch/level PWM rectifier when the control elements T_i and D_i, i =R,S,T, are integrated into the associated legs of the three-phase diode bridge on the input side (cf. Fig.2).

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