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Proceedings of the 39th Applied Power Electronics Conference and Exposition (APEC 2024), Long Beach, CA, USA February 25-29, 2024

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Comparative Evaluation of Voltage- and Current-Impressed Inductive Power Transfer to Multiple Stainless-Steel-Enclosed Moving Receivers

Junzhong Xu*, Spasoje Mirić[†], Markus Blickenstorfer[‡], Marco Hitz[‡], Johann W. Kolar*, and Jonas Huber*

*Power Electronic Systems Laboratory, ETH Zurich, Switzerland, xu@lem.ee.ethz.ch

[†]Drive and Energy Systems Laboratory (i-DES), University of Innsbruck, Austria

[‡]NTI AG, Switzerland

Abstract-Linear actuators in high-purity environments require full stainless-steel (SS) encapsulation and, advantageously, contactless, i.e., inductive power transfer (IPT) to several moving sliders which carry the actuator motor drives and applicationspecific tools. To avoid high eddy current losses in the SS enclosures by avoiding perpendicular magnetic field components, each IPT receiver features a closed toroidal magnetic core (with the secondary-side winding) that is arranged coaxially around the common primary-side winding which extends along the full stroke of the linear actuator. The primary winding is supplied with a full-bridge inverter through a compensation network that either compensates the primary windings' series inductance (voltageimpressed operation, V-I) or ensures a constant, load-independent amplitude of the primary current (current-impressed operation, C-I). Both operating modes support operation with multiple receivers but differ in terms of realization effort and efficiency characteristics in dependence of the load situation and/or the number of connected receivers. Therefore, after introducing the operating principles, this paper proposes a procedure to identify optimum V-I and C-I designs for given specifications, which then facilitates a comparative evaluation. All in all, an optimized C-I system achieves better efficiencies in the range of 98% at high load and with the maximum supported number of receivers actually used, but this comes at the price of a larger and more expensive compensation network. The modeling procedure is finally verified by equipping an industrial SS-enclosed linear actuator demonstrator with IPT to two moving receivers, each providing an output power of 100 W at an output voltage of 72 V.

Index Terms—Linear actuator, Stainless-Steel Enclosure, Inductive Power Transfer (IPT), Voltage-Impressed IPT, Current-Impressed IPT, Multi-Receiver IPT.

I. INTRODUCTION

Linear actuators enclosed in stainless-steel (SS) housings are widely used in industries that demand high-purity environments [1]–[3], i.e., strict hygiene standards. Conventional approaches employ cables and cable carriers to deliver power to the moving sliders/tool carriages. However, such cabling assemblies cannot be enclosed in SS and are thus difficult to clean. Further, wear and tear generates tiny particles that pose a contamination risk for high-purity applications. Therefore, implementing a contactless, i.e., inductive power transfer (IPT) emerges as a viable alternative which not only obviates cables but also minimizes the contamination risk [4]–[6]. However, all IPT



Fig. 1. (a) Stainless-steel-(SS)-enclosed multi-receiver IPT system with coaxially arranged toroidal magnetic cores carrying the secondary windings of the individual receivers (SS enclosures of receivers not shown). (b) Power circuit of the IPT system, which, depending on the compensation network, operates the primary winding either with impressed voltage (V-I) or impressed current (C-I).

components must be encapsulated in SS to comply with the requirements of high-purity environments.

IPT systems with stationary primary-side and secondary-side windings, which transmit power through metal enclosures have been reported in the literature and typically operate at low frequencies below 1 kHz [7]–[9]. For example, adopting the

typical geometric configuration of the IPT coil and magnetic cores that results in a magnetic field perpendicular to the SS enclosures, the authors have demonstrated IPT of 70 W through two 0.5 mm SS sheets at an operating frequency of 2.25 kHz [5]; the perpendicular magnetic field, however, causes substantial eddy-current losses in the SS sheets, which limits the efficiency to about 71%.

Considering that in a *linear* actuator, the movement of the receivers (mounted on the sliders/tool carriages) is confined to a single dimension, a coaxial arrangement employing closed magnetic cores as shown in Fig. 1a can advantageously be employed, i.e., similar to concepts known from non-SS-enclosed systems since the 1990s [10], [11]. This configuration largely mitigates the formation of eddy currents in the (coaxial) SS enclosures due to the absence of perpendicular field components, facilitating high power transfer efficiency and operating frequencies above the audible range. The high magnetic coupling achieved by this coaxial arrangement and the closed magnetic cores enable operating the IPT system like a series-resonant dc-dc converter, using a series capacitor to compensate the series inductance at the desired operating frequency; i.e., the IPT system behaves like a dc transformer (DCX) [12]-[14] that achieves a constant and (almost) loadindependent voltage transfer ratio and/or output voltage in openloop operation. Specifically, the authors have demonstrated such an IPT system capable of transferring 100W through two 0.5 mm SS enclosures at a frequency of 20 kHz, achieving a peak efficiency of 97% for a track length (i.e., length of the primary winding corresponding to the stroke of the linear actuator) of about 1 m [6]. Note that for DCX operation, the current flowing in the primary winding automatically adapts to the power consumed by the receiver whereas the voltage across the primary winding is of constant amplitude, i.e., the system operates in a voltage-impressed (V-I) mode.

In industry, linear-motion applications typically operate more than a single mover per linear actuator to handle different tasks. Hence, the IPT system must be able to supply multiple receivers. However, if more than one receiver is present, and because all receivers are coupled to the same primary winding (see Fig. 1), a magnetic series connection of the secondary windings results, i.e., the primary voltage is shared among all secondary-side windings. Thus, for DCX operation, the output voltages would depend on the number of receivers. In order to retain the advantageous V-I DCX operation while maintaining constant output voltages for all receivers, only a single receiver must be linked to the shared primary winding at any given time. This can be achieved using time-division multiplexing (TDM) to ensure mutually exclusive linking of the receivers to the primary winding [6], [15], [16], which is further explained in Section II-A below.

An alternative solution operates the primary winding with a current of constant (load-independent) amplitude, i.e., in a current-impressed (C-I) mode, typically using an LCL compensation network to transform a square voltage generated by the primary-side inverter stage into a constant-amplitude ac current [17]–[21]. Whereas C-I IPT systems typically

TABLE I Main specifications of the considered SS-enclosed V-I or C-I IPT systems with multiple receivers.

Symbol	Parameter	Value
U_{dc} $P_{o,r}$ $P_{o,max}$ $U_{o,r}$ l_{ss} $d_{o,ss}$ d_{ss} N	Rated voltage of dc supply Rated power per receiver Maximum power per receiver Rated output voltage Track (stroke) length Outer diameter of SS pipe Distance between SS pipes Maximum number of receivers	72 V 100 W 120 W 72 V 82 cm 10 mm 10 cm
- · mdx		0

are characterized by a loose magnetic coupling and thus a compensation network is commonly integrated on the secondary side, i.e., at the ac input of the receivers, too, to enhance the power transfer capacity and achieve constant output voltage [22], the SS-enclosed application requires closed magnetic cores (to prevent stray fields from causing eddy current losses), which results in a high magnetic coupling. As shown in [4], to prevent saturation of the magnetic cores, it is advantageous to omit any secondary-side compensation network; a receiver can then regulate its output voltage (independently) by using its transistors to adjust the duty cycle of its input voltage u_s (see **Fig. 1b**); this will be further discussed in **Section II-B**.

Both, V-I and C-I IPT thus represent viable options for supplying power to multiple SS-enclosed moving receivers. However, a comprehensive comparison of the respective design guidelines/constraints, the efficiency characteristics, and the achievable performances in general is missing in the literature. Thus, this paper provides a theoretical and experimental comparative evaluation of both concepts considering an SSenclosed linear actuator system with V-I or C-I IPT to up to three receivers; Table. I lists the main specifications. In the following, first Section II explains the operating principles of the V-I and C-I IPT; Section III introduces an optimization framework to identify the power conversion efficiency limits of V-I and C-I designs; and finally, Section IV provides an experimental verification using an industrial SS-enclosed linear actuator hardware demonstrator system with two IPT receivers. Section V concludes the paper.

II. OPERATING PRINCIPLES AND MODELING

Fig. 1a shows the physical arrangement of the IPT system and **Fig. 1b** depicts the corresponding power circuit. The primaryside full-bridge inverter is supplied with a constant dc input voltage U_{dc} and operated with a fixed 50% duty cycle, thereby generating a rectangular voltage $u_{in} = U_{dc} \cdot \text{sign}(\sin(2\pi f_{sw}))$ where f_{sw} denotes the switching frequency.

The primary winding extends over the full length of the linear actuator's stroke and thus contributes a significant series inductance L_s and a series resistance R_s ; the corresponding contributions of the secondary-side windings are (almost) negligible and lumped into L_s and R_s . A compensation network (see **Fig. 1b**) specifically designed for V-I or C-I operation integrates/compensates the (lumped) series inductance L_s , and ensures either a constant amplitude of the voltage u_t appearing across the (lumped) series resistance R_s and the coupled



Fig. 2. Conceptual key waveforms for (a) V-I and (b) C-I operation with three receivers and unity turns ratio (i.e., $N_1 = N_2$). $S_{\{a,b\},k}$ indicate the gate signals of the transistors $T_{\{a,b\},k}$; note the power sharing over several switching cycles in case of V-I operation (i.e., power is always only delivered to one receiver in any given switching cycle) in contrast to the simultaneous power sharing of the C-I system within each switching cycle.

receivers (for V-I operation), or a constant amplitude of the current i_t flowing in the primary winding (for C-I operation). Note that due to the resonant compensation, essentially only a fundamental-frequency (at f_{sw}) current flow is possible.

The IPT system features N_r receivers, each with rated output power $P_{o,r}$ and nominal output voltage $U_{o,r}$, as detailed in **Table I**. To handle short-term overloads, each receiver must be capable of providing up to $P_{o,max} > P_{o,r}$ to its load, which has implications in particular on the design of the C-I IPT system. Each receiver features a semi-active rectifier (SAR). As long as the two transistors i.e., T_a and T_b , are turned off, the receiver is magnetically linked to the primary-side winding and delivers power to the load. If the two transistors are turned on, short-circuiting the secondary-side winding, the receiver is not linked to the primary-side, no power transfer to its output takes place, and it is magnetically "invisible" to the other parts of the system.

A. Voltage-Impressed (V-I) Operation with Multiple Receivers

For V-I operation, the compensation network reduces to a capacitor C_t in series with the primary winding, as shown in **Fig. 1b**. The capacitance value is selected such that the capacitive impedance compensates the impedance of the series inductance L_s at the operating frequency f_{sw} , i.e., $C_t = (4\pi^2 f_{sw}^2 L_s)^{-1}$, such that the DCX operating mode results. If a single receiver is supplied, its output voltage U_o roughly equals the dc input voltage U_{dc} (for unity turns ratio, which is

assumed in the following for simplicity) without the need for closed-loop control [12]–[14].

However, if $N_r > 1$ receivers are coupled to the same primary winding, their output voltages would reduce to (roughly) U_{dc}/N_r and thus depend on the number of receivers [6], [23]. This means that only one of the N_r receivers should be linked to the primary winding (and thus receive power) at any given time, such that DCX operation ensures $U_o \approx U_{dc}$. As discussed above, a receiver can *disconnect* from the primary winding by turning on its transistors, which short-circuits its secondaryside winding and renders the receiver invisible/transparent for the other parts of the system. In order to provide power to all receivers, the *connected* state must thus be handed over from one receiver to the next in a cyclic and mutually exclusive way, resulting in TDM operation, which we briefly summarize in the following based on [23], where a more detailed explanation is provided.

Handovers of the connected state from one receiver to the next are permissible only after complete switching periods. Thus, the TDM period T_{tdm} lasts for several switching periods: $T_{tdm} = N_{tdm}T_s$ with $N_{tdm} \ge N_r$, i.e., during a TDM period, each receiver is connected for at least one switching period. To minimize conduction losses, the amplitude of the primary-winding current should not change at the handovers [23], i.e., the local average value of the (rectified) primary-winding current, $I_{t,avg}$, should be constant. Then, $I_{t,avg}U_o$ is the *instantaneous* power available to a connected receiver. Since a receiver is not always connected but only during a certain share of T_{tdm} , the average output power $P_{0,k}$ of a receiver becomes

$$P_{\mathrm{o},k} = \frac{t_{\mathrm{conn},k}}{T_{\mathrm{tdm}}} I_{\mathrm{t,avg}} U_{\mathrm{o}} = D_k I_{\mathrm{t,avg}} U_{\mathrm{o}}, \qquad k = 1, 2, \cdots N_{\mathrm{r}}, \quad (1)$$

where $t_{\text{conn},k}$ is the time the receiver stays in the connected state and D_k is the TDM duty cycle for receiver k, which corresponds to the receiver's fraction of the total power consumed by all receivers:

$$D_k = \frac{P_{o,k}}{\sum_{k=1}^{N_r} P_{o,k}}$$
 with $\sum D_k = 1$, (2)

Fig. 2a shows conceptual waveforms for V-I operation with three receivers and ideal TDM with a fixed $T_{tdm} = 20 \cdot T_s$. Throughout a TDM period, each receiver is in the connected state only during a fraction that corresponds to its share of the total load supplied by all receivers, which ensures equal average output voltages, i.e., $U_{o,1} = U_{o,2} = U_{o,3} \approx U_{dc}$. Clearly, as a receiver's dc output capacitor is charged during the connected state and discharged (by the load) in the disconnected state, the output voltage exhibits a fluctuation with a period of T_{tdm} . Both, the TDM period and the output capacitance C_o determine the magnitude of that fluctuation as

$$\Delta u_{\rm o,pp} = (1 - D_k) \cdot T_{\rm tdm} \cdot \frac{P_{\rm o,k}}{C_{\rm o}U_{\rm o}}.$$
(3)

Selecting a longer T_{tdm} enhances the resolution of D_k , yet it requires a larger C_0 to limit the peak-to-peak output voltage ripple to a certain fraction $\delta u_{0,pp}$ of the dc value. Thus, for a given T_{tdm} , the worst case (all N_r receivers operate with maximum load) defines the minimum required capacitance as

$$C_{\rm o} \ge \frac{P_{\rm o,max}}{\delta u_{\rm o,pp} U_{\rm o}^2} \cdot \left(1 - \frac{1}{N_{\rm r}}\right) \cdot T_{\rm tdm},\tag{4}$$

whereby a minimum offset value required for buffering the high-frequency ripple also in case of $N_r = 1$ is neglected.

Note that ideal TDM operation in conventional form inherently requires centralized coordination, as implied by (2). Therefore, a communication channel to the receivers is required, which can be seen as a drawback compared to the C-I operation discussed below. However, the automatic TDM (A-TDM) method proposed in [23], which achieves communication via power quantities that each receiver can independently measure, facilitates TDM-based V-I operation of an IPT system with multiple receivers but without dedicated communication channels.

B. Current-Impressed (C-I) Operation with Multiple Receivers

For C-I operation, a T-compensation network (see **Fig. 1b**) is typically employed on the primary side, consisting of L_f , C_f , and L_t or C_t (depending on the sign of $L_f - L_s$), which essentially converts the constant-amplitude square-wave voltage generated by the inverter to a constant-amplitude ac current in the primary winding. Following [4], the inductor L_f is defined by the desired (impressed/constant-amplitude) current in the primary winding as $L_f = U_{in,1}/(2\pi f_{sw}I_t)$, where $U_{in,1}$ and I_t are the RMS values of the fundamental components of the square-wave voltage generated by the primary-side inverter and

the impressed current (note that the resonant compensation essentially suppresses any higher-order current harmonics). The design value for the impressed primary winding current follows from the maximum power demand $P_{o,max}$ of a single receiver as

$$I_{\rm t} \approx \frac{N_2}{N_1} \cdot \frac{\pi}{2\sqrt{2}} \frac{P_{\rm o,max}}{U_{\rm o}},\tag{5}$$

which is accurate for the case of high magnetic coupling (high values of the magnetizing inductance $L_{\rm m}$) considered here, and assumes operation as a full-wave (diode) rectifier. Then, the other elements of the compensation networks follow as $C_{\rm f} = (4\pi^2 f_{\rm sw}^2 L_{\rm f})^{-1}$, and $L_{\rm t} = L_{\rm f} - L_{\rm s}$ (if $L_{\rm f} \ge L_{\rm s}$) or $C_{\rm t} = (4\pi^2 f_{\rm sw}^2 (L_{\rm s} - L_{\rm f}))^{-1}$ (if $L_{\rm f} < L_{\rm s}$) [4].

As mentioned in the introduction, in typical C-I IPT systems, there is also a compensation network on the secondary side that ensures constant output voltage of the receivers. However, as shown in [4], in case of high magnetic coupling (which is typically not present in IPT systems with relatively large air gaps in the magnetic circuit, but is needed here to prevent stray fields from causing eddy current losses in the SS enclosures), *not* employing a secondary-side compensation network reduces the flux density in the magnetic core and prevents saturation issues, e.g., during short-term overload situations. Without a secondary-side compensation network, however, the impressed constant-amplitude current would result in a load-dependence of the receiver's output voltage if a diode rectifier (full-wave rectification) would be used, i.e.,

$$P_{\mathrm{o},k} = \frac{U_{\mathrm{o},k}^2}{R_{\mathrm{L},k}} \stackrel{!}{=} I_{\mathrm{s}}^2 R_{\mathrm{ac},k} \Longrightarrow U_{\mathrm{o},k} = \frac{2\sqrt{2}}{\pi} I_{\mathrm{s}} R_{\mathrm{L},k}, \qquad (6)$$

where $I_{\rm s} = N_1/N_2I_{\rm t}$ denotes the RMS value of the impressed current on the secondary side and $R_{{\rm ac},k} = 8/\pi^2 R_{{\rm L},k}$ is the equivalent ac resistance of the full-wave rectifier with a dc-side load resistance of $R_{{\rm L},k}$.

Therefore, to maintain a constant output voltage $U_{0,k}$ for arbitrary load power $P_{0,k}$, the equivalent ac resistance the receiver represents must be adjusted. This can be achieved by using the receiver's transistors to bypass the constant-amplitude ac current from the output during a fraction of the switching period and thereby reducing the average value of the bridge output current i_0 , i.e., by introducing a duty cycle $D_{r,k}$ (see **Fig. 2b**):

$$R_{\mathrm{ac},k}(D_{\mathrm{r},k}) = \frac{8}{\pi^2} \sin^2\left(\frac{\pi}{2}D_{\mathrm{r},k}\right) R_{\mathrm{L},k} = \frac{8}{\pi^2} \sin^2\left(\frac{\pi}{2}D_{\mathrm{r},k}\right) \frac{U_{\mathrm{o}}^2}{P_{\mathrm{o},k}}.$$
(7)

Solving for the duty cycle and expressing in terms of the maximum output power $P_{o,max}$ obtainable for full-wave rectification (i.e., $D_{r,k} = 1$), the duty cycle ensuring constant output voltage for arbitrary load $P_{o,k} \le P_{o,max}$ becomes

$$D_{\rm r,k} = \frac{2}{\pi} \sin^{-1} \left(\frac{P_{\rm o,k}}{P_{\rm o,max}} \right).$$
 (8)

Fig. 2b shows conceptual waveforms for C-I operation with three receivers. The transistors on the secondary side operate



Fig. 3. Conceptual representation of V-I and C-I IPT systems from **Fig. 1b**, where the receivers are represented by their equivalent ac resistances and the primary-side inverter and the compensation network (including the series inductance L_s) are modeled with a voltage source (V-I) or a current source (C-I). (a) V-I IPT with one receiver; (b) C-I IPT with one receiver; (c) V-I IPT with N_r receivers (note the effective parallel connection of the equivalent ac resistances resulting from TDM operation); (d) C-I IPT with N_r receivers (note the series connection of the equivalent ac resistances).

at $2f_{sw}$; note how the (rectified) winding current only flows to the load if the corresponding transistors are off. In this way, the receivers independently regulate their output voltage by employing different duty cycles $D_{r,k}$ to adjust the equivalent ac resistance $R_{ac,k}$ they represent according to their load.

C. Comparison of Maximum Theoretical Efficiencies

Given that in the considered linear actuator applications the primary winding is typically long and hence dominates the series resistance R_s , which contributes significantly to the overall losses¹, it is interesting to briefly consider how the V-I and the C-I concept scale regarding this often dominant loss component, which limits the attainable efficiencies. Thus, **Fig. 3** shows simplified representations of V-I and C-I IPT systems, where the receivers are represented by their equivalent ac resistances, and where the primary-side inverter and the compensation network are either modeled as a constantamplitude ac voltage source, u_t , or a constant-amplitude ac current source, i_t .

First, considering V-I operation with multiple receivers (see **Fig. 3c**), TDM ensures a cyclic and mutually exclusive connection of the individual loads (e.g., in **Fig. 3c**, only receiver $k = N_r$ is linked). Neglecting the voltage drop across R_s and using (1) and (2), we find $I_t \approx \sum_{k=1}^{N_r} P_{o,k}/U_t$, which clearly indicates that the primary current follows from a (virtual) parallel connection of the individual receivers' equivalent ac resistances, and, in particular, adapts to the (total) load. The losses in the primary winding are thus $R_s I_t^2$ and impose an upper bound on the attainable efficiency as

$$\lceil \eta_{\text{V-I}} \rceil = \frac{1}{1 + R_{\text{s}} \cdot \left(\sum_{k=1}^{N_{\text{r}}} \frac{1}{R_{\text{ac},k}} \right)}.$$
(9)

¹Note that also the on-state resistances of the transistors and other series resistances in the current path essentially contribute to R_s .

For C-I operation (see **Fig. 3d**) with multiple receivers, the impressed primary-winding current I_t flows through the series connection of the receivers' equivalent ac resistances. Again neglecting the voltage drop across R_s , the input voltage U_t thus increases with the number of receivers, i.e., $U_t \approx \sum_{k=1}^{N_t} I_t R_{ac,k}$ (note that this implies increasing voltage stress for the primary winding isolation for a higher receiver count, which must be designed accordingly). Thus, the losses in the primary winding are load-independent like I_t , and the expression for the upper bound of the efficiency becomes

$$\left[\eta_{\text{C-I}}\right] = \frac{1}{1 + R_{\text{s}} / \left(\sum_{k=1}^{N_{\text{r}}} R_{\text{ac},k}\right)}.$$
 (10)

For a given load P_0 and output voltage U_0 , the equivalent ac resistances for V-I and C-I operation are

$$R_{\rm ac, V-I} = \frac{8}{\pi^2} \frac{U_{\rm o}^2}{P_{\rm o}}$$
 and $R_{\rm ac, C-I} = \frac{8}{\pi^2} \frac{U_{\rm o}^2}{P_{\rm o}} \left(\frac{P_{\rm o}}{P_{\rm o,max}}\right)^2$, (11)

as discussed above. Assuming then that all receivers are loaded equally, i.e., $P_{o,k} = P_o$, equating (9) and (10) results in

$$\lceil \eta_{\text{V-I}} \rceil \ge \lceil \eta_{\text{C-I}} \rceil \quad \Leftrightarrow \quad P_{\text{o}} \le P_{\text{o},\text{max}} / N_{\text{r}}. \tag{12}$$

There is, thus, a crossover of the upper bounds of the efficiencies, which should be expected given that $\lceil \eta_{V-I} \rceil$ is defined by losses with a quadratic dependence on the load and thus shows a decrease at higher loads, whereas $\lceil \eta_{C-I} \rceil$ follows from load-independent (constant) losses, i.e., increases for higher load. Specifically, (12) indicates that the V-I concept's efficiency has a higher upper bound compared to the C-I system if the *total* load of the V-I system, i.e., $\sum_{k=1}^{N_r} P_{o,k}$ which simplifies to $N_r P_o$ if all receivers are loaded equally, is lower than the maximum allowed load $P_{o,max}$ of a *single* receiver in the C-I system. Of course, there are other loss components like switching losses or magnetic core losses, which influence the system design trade-offs. This motivates the comprehensive optimization procedure described in **Section III**.

III. Optimization and Comparative Evaluation of V-I and C-I Multi-Receiver IPT Systems

Considering the specifications of an industrial demonstrator system for multi-receiver IPT in SS-enclosed linear actuator applications provided in **Tab. I**, the optimization procedure from **Fig. 4** is used to design V-I and C-I IPT systems and to estimate and compare the achievable efficiencies (including not only the series resistance as previously done, but also further loss components detailed below).

A. Optimization Procedure

Due to geometrical constraints and the need to limit the weight carried on the movers, only a single closed toroidal core (VAC Vitroperm 500F, W516) is considered as indicated in **Fig. 4**; the high permeability ($\mu_r \approx 70\,000$) is particularly applicable for SS-enclosed applications as it reduces stray fields, ensuring low eddy current losses in the SS enclosures. The (minimum) dimensions are defined by the diameter of the SS



Fig. 4. Flowchart of the implemented optimization procedure for V-I and C-I IPT systems with multiple receivers.

 TABLE II

 Key parameters of optimum V-I and C-I designs.

Parameter	V-I	C-I
Number of turns $N_1 : N_2$ Switching frequency f_{sw}	9 : 9, 27 kHz	8 : 8 33 kHz
Series inductance L_s Series resistance R_s	92 μH 0.30 Ω	73 μH 0.27 Ω
Compensation inductance $L_{\rm f}$ Compensation capacitance $C_{\rm f}$ Compensation capacitance $C_{\rm t}$ Compensation inductance $L_{\rm t}$	- 38 nF -	164 µH 141 nF – 91 µH

pipe enclosing the primary winding, and to limit the moving mass, larger cores and/or stacking of more than one core is not considered. Similarly, the power semiconductors used in the primary-side inverter and the secondary-side receivers are selected based on compatibility considerations with an existing product portfolio.

Under these constraints, the optimization identifies the optimal switching frequency f_{sw} and the number of turns N_1 of the primary winding and N_2 of the secondary winding, such that the maximum efficiency at nominal load (3 receivers with

100 W each) results; to do so, these degrees of freedom are varied as indicated in Fig. 4. For each combination of these degrees of freedom, the lumped parameters of the magnetic circuit (L_s , L_m , and R_s) are calculated as described in [6]. Then, the compensation network elements for V-I or C-I operation are designed as described above in Section II. The inductive components of the C-I compensation network are designed using the method from [24], whereby the most efficient design whose volume does not exceed the approximate boxed volume of the primary-side inverter (80 cm³) is selected among all possible realizations. The losses of the magnetic circuit (primary-side and secondary-side windings, magnetic cores) and also in the SS enclosures are obtained using the analytical approach detailed in [6], where the available copper crosssection area A_w , which influences the winding resistance R_s , depends on both, f_{sw} (because of the skin depth) and N_1 . The power semiconductors' conduction and switching losses are estimated based on datasheet values. Finally, designs that are not feasible are discarded, e.g., in case of overtemperature of the SS pipe ($T_{ss} > 60 \,^{\circ}$ C) modeled as in [6], excessive flux density > 0.8 T in the magnetic core at the nominal operating point (and/or > 1.2 T at the short-term maximum power operating point in case of C-I designs), and, also in case of C-I designs, if the compensation capacitor voltage $U_{\rm c}$ exceeds 650 V. Among all valid designs, the V-I design and the C-I design with the respective maximum efficiency under nominal load conditions are finally selected, and Table II summarizes their key parameters.

B. Optimization Results

The efficiency curves of these optimized V-I and the C-I designs, which feature the highest efficiency at nominal output power with $3 \cdot 100$ W loads, are shown in **Fig. 5a**. As expected from the discussion of the upper efficiency bounds from **Section II-C**, the C-I design achieves higher efficiency under nominal load conditions, and the shapes of the efficiency curves are clearly dominated by quadratic loss components in the V-I system but by constant (load-independent) loss components in the C-I system. Thus, there is a crossover of the efficiency curves at around 30 W (per module), i.e., slightly below $P_{o,max}/3 = 40$ W, which would be expected if only resistive conduction losses were present.

The efficiency of the V-I and the C-I designs are also evaluated considering applications with only 2 or only 1 (instead of 3) receivers. Note the opposite trends: the efficiency for a lower number of receivers increases for V-I operation (because the primary-winding current automatically adapts to the load) and decreases for C-I operation (because the primarywinding current remains constant even though the total output power reduces). Therefore, the crossover point shifts to higher per-receiver load levels if less than the maximum number of supported receivers is used. This is also visible in the loss breakdowns shown in **Fig. 5b**: whereas under nominal conditions $(3 \cdot 100 \text{ W load})$ the winding losses of the V-I system are much higher than those of the C-I system, they reduce



Fig. 5. (a) Efficiency characteristics of the optimum (with maximum efficiency under nominal conditions $(3 \cdot 100 \text{ W})$) V-I and C-I designs for operation with 3, 2, or 1 equally loaded receivers. (b) Loss breakdown for the nominal operating point and a part-load case; note how the winding losses of the V-I system depend on the load whereas those of the C-I system remain constant. (c) Comparison of the two designs regarding relative losses with different numbers or receivers (operating at rated load each), overall volume of the primary-side inverter and compensation network, and minimum required output capacitance.

significantly if the load is reduced to $2 \cdot 50$ W only, whereas the winding losses of the C-I system remain unchanged.

Finally, the radar plot in **Fig. 5c** compares optimum V-I and C-I designs regarding relative losses with $N_r = 1, 2, 3$ receivers (each loaded with 100 W), the overall volume of the primary-side power electronics (the inverter contributes 77 cm³ to both systems, but the C-I compensation network requires an additional 178 cm³ for its two inductors), and the minimum output capacitance of the receivers for equal voltage ripples of $u_{o,pp} = 10 \%$ (for the V-I system, TDM operation with $T_{tdm} = 10 \cdot T_s$ is assumed, resulting in $C_o = 115 \mu$ F, whereas $C_o = 6 \mu$ F suffices given the continuous high-frequency supply of the C-I system). In general, the application might



Fig. 6. (a) Industrial SS-enclosed linear actuator prototype with two receivers (movers) and equipped with the discussed IPT system. The full-bridge inverter and the compensation capacitor for V-I operation are mounted. (b) Close-up of the 100 W semi-active-rectifier-(SAR)-based receiver module. (c) Full-bridge inverter and compensation network for C-I operation on the primary side.

TABLE III Key parameters of the experimental setup used to verify V-I and C-I operation.

Parameter	V-I	C-I
Number of turns $N_1 : N_2$	16:16 (existing demonstr.)	
Switching frequency f_{sw}	20 kHz	
Series inductance L_s	300 μH	
Series resistance R_s	1.6 Ω	
Compensation inductance $L_{\rm f}$ Compensation capacitance $C_{\rm f}$ Compensation capacitance $C_{\rm t}$ Compensation inductance $L_{\rm t}$	- 200 nF -	270 μH 230 nF 2.2 μF

require higher capacitance values, e.g., to handle load transients, however.

All in all, an optimized C-I system achieves better efficiencies at high load and with the maximum supported numbers of receivers actually used by the application, but this comes at the price of a larger and more expensive compensation network.

IV. EXPERIMENTAL VERIFICATION

In order to experimentally verify the presented analysis, the industrial SS-enclosed linear actuator demonstrator system shown in **Fig. 6** is equipped with V-I or C-I IPT for supplying power to two moving receivers. As the system has originally been designed as a test platform for through-SS IPT using the V-I approach but only a single 100 W receiver [6], the number of primary and secondary turns ($N_1 = N_2 = 16$) of the industrial demonstrator are fixed and thus a relatively high overall series resistance of about 1.6 Ω results.² Consequently, the optimization procedure introduced in **Section III** has been

²Doubling the number of turns from 8 (see **Table II**) to 16 implies, first, a doubling of the length, but, second, also a halving of the cross section area per turn (details see [6]), i.e., a fourfold increase of the winding resistance. In addition, there is also a significant contribution from the PCB-based realization of the end windings.



Fig. 7. Measured key waveforms for V-I operation with two receivers loaded with $P_{o,r} = 100$ W each (resistive load). When TDM operation connects receiver 1 (S₁ is low; the transistors are turned off) to the link, power transfer from the primary to the receiver recharges the corresponding output capacitor, while at the same time, receiver 2 is disconnected and its output capacitor discharges supplying the load.

re-run with fixed N_1 and N_2 and considering $N_r = 2$ (i.e., two receivers), identifying $f_{sw} = 20 \text{ kHz}$ as the optimum switching frequency for V-I operation and $f_{sw} = 16 \text{ kHz}$ for C-I operation. However, as the frequency-dependent loss contributions are very low, and to facilitate a direct comparison, $f_{sw} = 20 \text{ kHz}$ has been selected for both, V-I and C-I operation. Tab. III summarizes the resulting compensation network parameters, and Figs. 6bc show detailed views of the realized receiver and inverter PCB assemblies. The receivers are equipped with an output capacitor $C_0 = 260 \,\mu\text{F}$, providing a stable 72 V output voltage to two actuator motor drive inverters that control the linear movement along the x-axis and z-axis, respectively. Furthermore, a 24 V output for supplying the control electronics of these industrial actuator motor drives is provided. Each receiver features an STM32G431 ARM microcontroller (MCU), whose built-in ADCs are used to measure the ac input current i_s , the ac input voltage u_s , and the output dc voltage u_0 : For C-I operation, the ac input current $i_{\rm s}$ is used to synchronize the switching signal by means of a rapid zero-crossing detection circuit. However, because for V-I operation the ac current can reach very low values (at low load), potentially causing synchronization issues, the zero crossings of the ac input voltage u_s are detected, too, and serve as an alternative for synchronizing a local carrier signal to the primary-side voltage/current. The MCU, sensing and gate drive circuitry account for a power consumption of about 1.5 W per receiver.

A. Continuous Operation and Load Steps

Fig. 7 shows measured waveforms for V-I operation with both receivers providing nominal power $P_{o,r} = 100$ W to (for simplicity) resistive loads. As expected from (2), TDM results in a TDM duty cycle of D = 0.5. Note further that each handover triggers a transient response of the primary-winding current, which is a consequence of the difference between the output voltages of the disconnecting and the connecting receiver (see [14], [23]). Similarly, **Fig. 8** shows the measured waveforms for C-I operation, again with both receivers equally



Fig. 8. Measured key waveforms for C-I operation with two receivers loaded with $P_{0,r} = 100$ W each (resistive load). Note that the receivers operate with a duty cycle below unity according to (8), because $P_{0,r} < P_{0,max}$.

loaded with the nominal $P_{o,r} = 100 \text{ W}$ (resistive load). The closed-loop control of the output voltage adjusts the duty cycle accordingly, and in particular to a value below 1 as expected from (8) because $P_{o,r} < P_{o,max}$.

Fig. 9 show the transient behavior of the V-I and the C-I system during a load step of receiver 1 (from essentially 0 W to 100 W) while receiver 2 keeps operating with nominal load of 100 W. For the V-I system, TDM operation adapts the TDM duty cycles (of both) receivers after the load step. For the C-I system the duty cycle of receiver 1 increases according to the increasing power consumption after the load step. Importantly, in both cases the output voltages of both receivers remain essentially stable during the load steps. Finally, note how the primary current adapts to the increased load in case of the V-I system, but remains unaffected for the C-I system, which corresponds to the discussion of **Section II-C**.

B. Efficiency Measurements

Fig. 10 shows the measured and calculated (using the approach from Section III) efficiency characteristics for V-I and C-I operation. The measured efficiencies are in good agreement with the calculated values. In particular, the two efficiency curves intersect at approximately $P_{o,max}/2 = 60 \text{ W}$, which is in good agreement with the theoretical discussion from **Section II-C** because here, due to the relatively high series resistance R_s , the ohmic conduction losses dominate the overall losses. C-I operation shows a higher efficiency than V-I operation at nominal load but lower efficiency at part load operating points. However, if averaged over the entire power range (assuming that each power level is used equally over time), the average efficiencies of the two operating modes are comparable, i.e., 88.6% for the C-I system and 87.0% for the V-I system. In general, the measured efficiency values are lower than those obtained for optimized systems (see Section III), which can be attributed to the higher number of turns of the available industrial demonstrator system's primary winding, and hence higher winding losses.

V. CONCLUSION

This paper conducts a comparative evaluation of voltageimpressed (V-I) and current-impressed (C-I) inductive power



Fig. 9. Measured transient behavior for (a) V-I and (b) C-I. In both cases, receiver 1 is subject to a load step from essentially 0 W to $P_{o,r} = 100$ W while receiver 2 continuously operates with $P_{o,r} = 100$ W. Note how the primary-winding current of the V-I system automatically adapts to the higher load. Note further that the C-I system's output voltage ripple is much lower because, for practical reasons, the same output capacitor is used for both operating modes.



Fig. 10. Measured (Yokogawa WT1804E) and calculated efficiencies for V-I and C-I operation of the demonstrator system with two equally loaded receivers. Note the crossover point at approximately $P_{o,max}/2 = 60$ W; the theoretical discussion from **Section II-C** matches well, because here, the primary-winding's series resistance dominates the system losses due to the relatively high number of turns.

transfer (IPT) to several stainless-steel-enclosed movers of a linear actuator. For V-I operation, the voltage drop across the stray inductance is compensated with a series capacitor, whereas for C-I operation, the compensation network ensures a constant-amplitude (load-independent) current in the primary winding. The C-I system's primary-side compensation network thus requires one or two inductive components, which implies larger size and higher costs.

If only a single receiver should be supplied, V-I operation is clearly preferable because the primary-winding current automatically adapts to the load, and the output voltage is essentially load-independent without closed-loop control. In contrast, the (load-independent) primary-winding current of a C-I system is defined by the maximum power a single receiver can draw. This is an advantage if multiple receivers are supplied, because the primary-winding losses (which can be dominant given that the winding length is defined by the linear actuator's stroke) remain constant whereas the output power increases with the number of receivers. Thus, if the maximum number of supported receivers is present, and these receivers operate near their rated power, C-I operation is more favorable. On the other hand, if the loads are characterized by short power peaks and longer phases of relatively low power consumption (a typical situation for linear actuator applications, where the power demand peaks during acceleration of the mover only), V-I operation with adaptive primary-winding current may be advantageous. Note further that the C-I system must be designed for a given maximum load per receiver, which cannot be exceeded even if the number of receivers is so low that the primary-side inverter's power capability is not fully utilized. For a V-I system, such a limitation does not exist, i.e., the load distribution among the receivers can be arbitrary as long as the total power does not exceed the primary-side inverter's capability.

Whereas C-I operation does not require any communication channels, i.e., each receiver can regulate its output voltage independently, the time-division multiplexing (TDM) link access method used for V-I operation typically requires a communication channel to the receivers (communication-free A-TDM has been proposed [23], but comes with a certain implementation complexity). However, in linear actuator applications a communication channel to the movers is typically available, e.g., to control the actuator motor drives and the tools that are carried on the movers.

Finally, the feasibility of both, V-I and C-I operation has been demonstrated using an SS-enclosed linear actuator demonstrator with two receivers providing 100 W at 72 V each. The described trade-offs ultimately facilitate an application-specific selection of the most suitable method.

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