99.3% Efficient Three-Phase Buck-Type All-SiC SWISS Rectifier for DC Distribution Systems

L. Schrittwieser,
M. Leibl,
M. Haider,
F. Thöny,
J. W. Kolar,
T. B. Soeiro

This material is published in order to provide access to research results of the Power Electronic Systems Laboratory / D-ITET / ETH Zurich. Internal or personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution must be obtained from the copyright holder. By choosing to view this document, you agree to all provisions of the copyright laws protecting it.
99.3% Efficient Three-Phase Buck-Type All-SiC SWISS Rectifier for DC Distribution Systems

L. Schrittwieser*, M. Leibl*, M. Haider*, F. Thöny*, J. W. Kolar* and T. B. Soeiro†

Power Electronic Systems Laboratory, ETH Zurich, Switzerland, Email: schrittwieser@lem.ee.ethz.ch
†ABB Switzerland Ltd., Corporate Research, 5405 Baden-Dättwil, Switzerland

Abstract—DC power distribution systems for data centers, industrial applications and residential areas are expected to provide higher efficiency, reliability and lower cost compared to ac systems. Accordingly they have been an important research topic in recent years. In these applications an efficient power factor correction rectifier, supplying a dc distribution bus from the conventional three-phase ac mains is typically required. This paper analyzes the three-phase buck-type unity power factor SWISS Rectifier showing that its input current THD can be improved significantly by interleaving. The dc output filter is implemented using a current compensated Integrated Common Mode Coupled Inductor which ensures equal current sharing between interleaved half bridges and provides common mode inductance. Based on the analysis an high efficient 8 kW, 4 kW dm−3 (64 Wm−3) lab-scale prototype converter is designed using SiC MOSFETS. Measurements taken on a hardware prototype confirm a full power efficiency of 99.16% and a peak efficiency of 99.26%.

I. INTRODUCTION

Over the last decades the power demand of intrinsic dc loads, such as information and communication technology equipment, data centers, electric vehicle battery charging, LED lighting, etc. increased substantially. Furthermore renewable energy sources such as PV modules, fuel cells and battery storage are also based on dc. Therefore, dc distribution systems are expected to give advantages in terms of efficiency, reliability and/or cost as the total number of conversion stages can be reduced. Consequently, dc power supply and distribution systems for information and communication technology equipment, electric vehicle traction battery fast charging and dc microgrids have been a major topic in research and industry in recent years and corresponding standards have been created [1–9].

In these applications, loads, with typically tens of kilowatts or more, are supplied from a dc bus with ≈ 400 V which is powered from the conventional 400 V or 480 V rms three-phase ac mains. Due to the high power levels sinusoidal ac input currents, in-phase with the mains voltage are required. As the dc bus voltage is lower than the amplitude of the full-wave rectified three-phase line-to-line voltage, two-stage systems are normally used which consist of a boost-type power factor correction (PFC) rectifier front end providing ≈ 800 V dc and a subsequent step-down dc-dc converter. Buck-type PFC rectifiers, which allow a direct conversion from the three-phase ac mains to a dc bus with lower voltage, are an advantageous alternative offering potentially lower losses, volume and cost [11].

The schematic of the three-phase buck-type SWISS Rectifier introduced in [10] is shown in Fig. 1(a). It consists of an ac-side EMI input filter, an Input Voltage Selector (IVS) and two series-connected buck-type dc-dc converters $S_{xp}$, $D_{yp}$ and $S_{xn}$, $D_{yn}$. Note that all diodes and switches in the IVS are commutated at mains frequency only, therefore basically no switching losses occur in the IVS. Hence, diodes with a low forward voltage drop, or MOSFET-based synchronous rectifiers can be used in the IVS. The IVS output voltages $u_{x}$, $u_{y}$, $u_{z}$ are piece-wise sinusoidal as the input phase with highest potential is connected to node x, the one with lowest potential to z and the remaining phase to node y.

In this paper the conventional (single buck converter output stage), cf. Fig. 1(a), and interleaved SWISS Rectifier, cf. Fig. 1(b), are compared regarding their ac input and dc
output properties in Section II. The implemented prototype converter is presented in Section III, including measurement results.

II. SWISS RECTIFIER

A. Non-Interleaved SWISS Rectifier

In Fig. 1(a) the SWISS Rectifier with two coupled dc output inductors $L_{cm}$ (common mode) and $L_{dm}$ (differential mode) is shown. As the dc load is connected between output nodes p and n of the converter and has no connection to the star point N of the ac mains $i_p = i_n$ can usually be assumed and the differential mode inductor alone would be sufficient. However, this is not the case if the load is, for example, a widespread dc distribution bus, potentially including physically large backup batteries, which can have a significant capacitance $C_{cm}$ to ground. This creates a conduction path for high frequency common mode (cm) currents $i_{cm}$ from the output nodes p and n to the grounded star point N as shown in Fig. 1, which is also the case if dedicated cm capacitors are added to the converter as part of a cm filter, which is typically required to comply with EMI regulations.

Simulation results for a conventional non-interleaved 8 kW SWISS Rectifier specified in Table I are shown in Fig. 2(a). It can be seen that the ac input currents $i_a$, $i_b$, $i_c$ show a significant switching frequency ripple and distortions with an amplitude of $\approx 6\,\text{A}$ at every $60^\circ$ mains voltage sector boundary. Detailed simulation results for the vicinity of the first sector boundary at $\omega t \approx 60^\circ$ are shown in Fig. 3(a). These distortions are due to the switching frequency voltage ripple on the filter capacitors $C_{x,y,z}$ as described in [12]. As $u_x$, $u_y$ and $u_z$ are piece-wise sinusoidal due to the IVS operation, $C_{x,y,z}$ create reactive power at the ac input which typically has to be limited to a few percent of the converter’s rated output power, which limits the capacitance value of $C_{x,y,z}$. As the SWISS Rectifier is a buck-type topology the input currents $i'_a$, $i'_b$ and $i'_c$ of the dc-dc converter are discontinuous which, in connection with the limited capacitance of $C_{x,y,z}$ results in a high switching frequency ripple of $u_x$, $u_y$ and $u_z$, cf. Fig. 3(a).

B. SWISS Rectifier with Interleaved Output Stages

To reduce the input current and voltage ripples either the ac input filter capacitance and inductance can be increased or a higher switching frequency can be used. Both options increase volume, losses and cost of the converter system. In order to overcome these disadvantages two interleaved dc-dc converters can be used as output stage to reduce the input and output current ripples [13]. The schematic of the resulting system, denominated as interleaved SWISS Rectifier in the following, is shown in Fig. 1(b) where two individual bridge legs $S_{xp1}$ / $D_{xp1}$ and $S_{xp2}$ / $D_{xp2}$ are used for the p side dc-dc converter stage and $S_{np1}$ / $D_{np1}$, $S_{np2}$ / $D_{np2}$ are used for the n side. By using the same duty cycle but 180° phase shifted carriers for the pulse width modulation of $S_{xp1}$ and $S_{xp2}$ the high frequency components of the resulting input current $i'_c$ have twice the frequency and half the amplitude compared to the non-interleaved case as shown in the detailed simulation results in Fig. 3(b).

Simulation results of the interleaved SWISS Rectifier are shown in Fig. 2(b), where it can be seen that the differential mode (dm) and cm current ripples are reduced significantly compared to Fig. 2(a). Detailed simulation results for the first mains voltage intersection are shown in Fig. 3(b). Due to the reduced ripple of the buck converter input currents $i'_a$, $i'_b$ and $i'_c$, the peak-peak ripple on the filter capacitor voltages $u_x$, $u_y$ and $u_z$ reduces from 105 V without interleaving to 24 V with interleaving. Also the ripple and the distortions of the input currents $i_a$, $i_b$ and $i_c$ occurring at every $60^\circ$ mains voltage sector boundary are reduced from $\approx 6\,\text{A}$ to $< 1\,\text{A}$.
Intercell Transformers (ICTs) [14–16], were the interleaved SWISS Rectifier would require two ICTs, one for the p and n sides respectively. The ICTs are typically implemented with a so-called air-gap, leading to a larger inductance value, similar to a single winding inductor where the currents are split into inner differential mode (idm) and outer differential mode (odm) and two inner differential modes (idm) as shown in Fig. 4(b). A similar equivalent circuit of the conventional SWISS Rectifier is shown in Fig. 4(a) for comparison. These equivalent voltages can be derived as

$$u_{cm} = \frac{u_{p1} + u_{p2} + u_{n1} + u_{n2}}{4},$$

$$u_{odm} = \frac{u_{p1} + u_{p2}}{2} \cdot \frac{u_{n1} + u_{n2}}{2},$$

$$u_{idm,p} = u_{p1} - u_{p2},$$

$$u_{idm,n} = u_{n1} - u_{n2}.$$

Neglecting any stray fields in the ICMC the fluxes $\Phi_{p1}$, $\Phi_{p2}$, $\Phi_{n1}$, $\Phi_{n2}$ generated by the four windings have to sum up to zero due to the ICMC’s core, cf. Eq. (5):

$$\Phi_{p1} + \Phi_{p2} + \Phi_{n1} + \Phi_{n2} = 0.$$

This implies that the voltages applied to the four windings sum to zero as well due to inverse winding direction of the p and n side ICMC windings. Using Kirchhoff’s voltage law on the circuit shown in Fig. 4(b) three additional equations can be found, which yields four equations that define the ICMC’s voltages

$$ u_{w,p1} + u_{w,p2} + u_{w,n1} + u_{w,n2} = 0,$$

$$ u_{w,p1} - u_{w,p2} = u_{idm,p},$$

$$ -u_{w,n1} + u_{w,n2} = u_{idm,n},$$

$$ u_{w,p1} + u_{w,p2} - u_{w,n1} - u_{w,n2} = 4u_{cm,hf}. $$

C. Integrated Common Mode Coupled Inductor - ICMC

In order to analyze the properties of the ICMC the SWISS Rectifier’s input filter, IVS and dc-dc converters are replaced by equivalent voltage sources which define the potentials of the four windings. Typically this is implemented with so called Intercell Transformers (ICTs) [14–16], were the interleaved SWISS Rectifier would require two ICTs, one for the p and one for the n side bridges. However, the two ICTs and the cm inductor $L_{cm}$ can be integrated into a single four winding magnetic device in the following denominated as Integrated Common Mode Coupled Inductor (ICMC) as shown in Fig. 1(b) and Fig. 4(b).
of an interleaved SWISS Rectifier using an ICMCI. Due to the interleaving the outer differential mode (odm) voltage and current waveforms is shown in Fig. 5(a). Compared to a non-interleaved SWISS Rectifier, the outer dm voltage for nominal operation are shown in Fig. 5(b). Simulation results of the corresponding quantities of an interleaved SWISS Rectifier using an ICMCI. Due to the interleaving the outer differential mode (odm) voltage \( u_{odm} \) peak-to-peak value reduces, which leads to a reduction of the ripple in the corresponding current \( i_{odm} \).

It can be seen that the ICMCI’s winding voltages are defined only by the switching frequency cm voltage and the inner dm voltages, while the outer dm voltage is applied only to the differential mode inductor \( L_{dm} \) and the dc output \( u_{p,n} \).

Simulation results of the ICMCI’s winding voltages and the outer dm voltage for nominal operation are shown in Fig. 5(b). Compared to a non-interleaved SWISS Rectifier, as shown in Fig. 5(a), the (outer) dm voltage applied to \( L_{dm} \) is reduced which leads to a significant reduction of the peak-to-peak ripple in \( u_{odm} \) compared to \( i_{dm} \). The same holds for the cm current \( i_{cm} \).

A drawing of the resulting switching frequency voltage and current waveforms is shown in Fig. 6 for \( 0^\circ \leq \omega t \leq 30^\circ \). It can be seen that the ICMCI’s winding voltages \( u_{w,1} \), \( u_{w,2} \) and \( u_{w,n1} \) and \( u_{w,n2} \) are periodic with the switching frequency, while the voltage \( u_{odm, hf} \) applied to \( L_{dm} \) shows twice that frequency due to harmonic cancellation.

### III. Rectifier Prototype

For power supply systems which are operated 24/7, as in data centers, a high efficiency is desirable to minimize the cost of conversion losses and cooling and hence the operating costs of the system [17]. Furthermore a high efficiency over a wide range of output currents is desirable in applications where redundant supplies are used resulting in a nominal operation at half of the rated power or less. Therefore, a system which achieves an efficiency of \( > 99 \% \) for \( P > P_{rated}/3 \) for the operating condition listed in Table I was designed.

Silicon carbide (SiC) MOSFETs are selected due to their low conduction and switching losses and high blocking voltage rating (1.2kV) compared to Si IGBTs and Si MOSFETs [18, 19]. Nanocrystalline core material (FINEMET) is used for dm inductor \( L_{dm} \) due to its high saturation flux density (\( \approx 1.2 \text{T} \)) and lower losses compared to amorphous alloys. For the current compensated ICMCI core 3C94 ferrite material is used due to its lower core losses. A symmetrical, cube-type core as shown in Fig. 7 is used for the ICMCI. This shape is achieved by using four conventional C cores,
each carrying one winding as shown in Fig. 7(b). The semiconductors and magnetic components selected for the prototype are listed in Table II.

The calculated losses of the selected components for nominal operation are shown in Fig. 8(a) with the corresponding volumes given in (b). About 60% of the total losses result from semiconductors, 13% from the main magnetic components and 27% from the EMI filter, control, gate drivers, auxiliary supply etc. A picture of the implemented hardware prototype, achieving a power density of 4.0 kW dm\(^{-3}\) (66 W in\(^{-3}\)) is shown in Fig. 9.

Measurement results of the rectifier’s mains voltages and currents at nominal operation are shown in Fig. 10. The resulting input currents \(i_{a,b,c}\) are nearly sinusoidal and free of distortions at the sector boundaries as expected from the presented simulation results. Note that the rectifier’s control circuit is configured for ohmic mains behavior as described in [20]. An input current THD of 2.45% results for a mains voltage THD of 2.29%.

The calculated efficiency of the rectifier for \(U_{pn} = 400\) V as function of dc load current \(I_1\) is shown in Fig. 11, together with measurement results taken using a Yokogawa WT3000 power analyzer. It can be seen that the measurement results of the prototype converter match the calculated efficiency.
over a wide range of output currents. A peak efficiency of $\eta = 99.26\%$ (error range: $98.80\% - 99.74\%$) was measured for $I_L = 12.5\,A$ and $\eta = 99.16\%$ (error range: $98.84\% - 99.49\%$) at rated load $I_L = 20\,A$.

IV. CONCLUSION
This paper describes a three-phase buck-type unity power factor SWISS Rectifier with interleaved dc-dc converter output stages. The system allows a single-stage conversion from the three-phase mains to a lower dc voltage. Using interleaved dc-dc converter stages reduces the input current and voltage ripples which improves the ac input current THD and reduces the dc output current ripple. Furthermore, the required dc output inductors can be combined into a current compensated Integrated Common Mode Coupled Inductor (ICMCI) and a differential mode inductor. Based on this approach a high efficiency interleaved SWISS Rectifier for dc distribution and power supply systems is designed, achieving a power density of $4\,kW\,dm^{-3}$. Measurements taken on a prototype verify an efficiency of $99.16\% \pm (0.32\%)$ at nominal operation with $8\,kW$ dc output power and a peak efficiency of $99.26\% \pm (0.48\%)$. Note that for a similar $5\,kW$ three-phase buck-type rectifier, based on Si MOSFETS and SiC diodes, an efficiency of $98.8\%$ and a power density of $2.2\,kW\,dm^{-3}$ were reported in [11]. However, further research is required to assess potential benefits regarding efficiency and/or power density which could result from novel wide band-gap semiconductor devices such as monolithic bidirectional switches which could be used in the IVS [21].

ACKNOWLEDGMENT
The authors would like to thank ABB Switzerland Ltd. for the funding and for their support of this research project.

REFERENCES


[9] ETSI, “Environmental Engineering (EE); Power Supply Interface at the Input to Telecommunications and Datacom (ICT) Equipment; Part 3: Operated by Rectified Current Source, Alternating Current Source or Direct Current Source up to 400 V; Sub-part 1: Direct Current Source up to 400V;” EN 300 132-3-1, Feb 2012.


