Comparative Evaluation of T-Type Topologies Comprising Standard and Reverse-Blocking IGBTs

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Comparative Evaluation of T-Type Topologies Comprising Standard and Reverse-Blocking IGBTs

Hirofumi Uemura, Florian Krismer, and Johann W. Kolar

Power Electronic Systems Laboratory
Swiss Institute of Technology, Physikstrasse 3
8092 Zurich, Switzerland
Email: uemura@lem.ee.ethz.ch, www.pes.ee.ethz.ch

Abstract—For a Three-Level Three-phase T-type (3LTTC) rectifier and inverter of a high efficiency Uninterruptible Power Supply (UPS) with an output power of 20 kVA, most suitable semiconductor components are selected. For this purpose, this paper details conduction and switching loss models of T-type rectifiers and inverters, compares the total semiconductor losses achieved for RB-IGBTs and for different types of conventional IGBTs, and evaluates the improvements achieved if the Si rectifier diodes are replaced by SiC Schottky Barrier Diodes (SiC SBDs). The switching loss model is parameterized with measured switching losses. According to the results of this comparison, the rectifier preferably employs RB-IGBTs to realize the bi-directional switch and SiC SBDs for the rectifier diodes; switching frequencies up to 5 kHz are feasible for total semiconductor losses of the rectifier of 250 W. For the inverter, a realization of the bi-directional switch using an anti-series connection of conventional IGBT/SiC SBD modules is found to be most suitable and facilitates a switching frequency of 19.7 kHz for maximum allowed losses of 250 W.

I. INTRODUCTION

Uninterruptible Power Supply (UPS) systems ensure uninterruptible operation of highly available equipment, for example IT equipment of a data center, from a mains failure. For critical loads which need low input voltage distortion, a back-to-back configuration, as shown in Fig. 1, is often employed, since this configuration effectively suppresses mains voltage distortions; such UPS systems are called online or double conversion systems [1].

The investigated UPS system is an online UPS according to Fig. 1 with a rated power of 20 kVA. The rms input and output line-to-neutral voltages of the considered system are 230 V, the input and output frequencies are 50 Hz, and the dc bus voltage is kept constant at $V_{dc} = 720$ V. Rectifier and inverter stages of this UPS are designed for high efficiency, since, during normal mode of operation, both stages may be continuously operated up to nominal power.

Typical three-phase rectifier and inverter topologies include conventional two-level topologies and three-level neutral point clamped (NPC) topologies [2]. Three-phase two-level converters feature a low number of diodes (rectifier) or IGBTs (inverter) with maximum blocking voltages of 1200 V in the considered system and generate low conduction losses [3]. Two-level converters, however, require a comparably large EMI filter due to the high generation of harmonic content [4]. Three-level NPC inverters and rectifiers cause less harmonic content and, thus, allow for a reduced EMI filtering effort. These converters, however, require more diodes and/or switches (maximum break-down voltages are 600 V in the given system) and generate higher conduction losses than two-level converters, since each phase current is fed through two semiconductor devices, e.g., two IGBTs, with the sum of the voltage drops across two 600 V IGBTs being greater than the voltage drop across a single 1200 V IGBT [3]. T-type NPC converters, in comparison, allow for three-level operation at reduced conduction losses, since only a single diode or IGBT (again rated for 1200 V) conducts the phase current to the positive or negative bus bar of the dc link [3]. Therefore, the T-type NPC inverter and rectifier topologies are very attractive regarding the investigated UPS system in order to achieve low conduction losses and reduced EMI filtering effort.

![Three-phase three-level UPS](image)

Fig. 1. (a) Proposed configuration of the three-phase three-level UPS system showing EMI filter, mains side rectifier, load side inverter, and dc-dc converters including backup batteries. (b) Schematic drawing of the power circuits of the mains side rectifier and the load side inverter; both, rectifier and inverter, employ 3LTTC topologies.

The T-type NPC converters require one bi-directional switch per phase, cf. Fig. 1(b). Bi-directional switches are typically realized with a common-emitter series connection of two IGBT/Free Wheeling Diode (FWD) modules as shown in Fig. 2(a) [3], [5]. As a consequence, two series connected semiconductor components, a diode and an IGBT, conduct the current through the bi-directional switch. In this context, reverse blocking IGBTs (RB-IGBTs) can be advantageously used to reduce the conduction losses of T-type rectifiers and inverters [6]–[8].

This paper details a comparison of the semiconductor losses of rectifier and inverter of the three-phase three-level UPS converter depicted in Fig. 1 for different realizations of the bi-directional switches, which includes realizations with RB-IGBTs and different types of conventional IGBT/FWD modules. The paper further investigates the improvements achieved with 1200 V SiC Schottky Barrier Diodes (SBDs) (instead of 1200 V Si rectifier diodes and FWDs) and 600 V SiC SBDs (instead of 600 V Si FWDs used in the bi-directional switches). Section II describes two realizations of the bi-directional switches, which are considered for loss comparison. Section III details the analytical semiconductor loss calculation models, i.e., conduction and switching loss models, for T-type rectifiers and inverters. Section IV presents measured switching losses, which are used to parameterize the switching loss model.
of Section III. Section IV further compares the losses and the total system efficiencies achieved with different realizations of the bi-directional switches, with and without SiC SBD, and for different switching frequencies.

II. BI-DIRECTIONAL POWER SWITCH

A. Switch realizations

Fig. 2 shows two realizations of bi-directional switches with conventional IGBTs and FWDs or with RB-IGBTs. Further realizations of bi-directional switches, e.g. the realizations given in [2], [5], are expected to have higher or similar conduction losses than the realization of Fig. 2(a), and are, therefore, not considered in this comparison.

B. Internal structure of the RB-IGBT

The internal structures of a conventional IGBT and a RB-IGBT and the respective depletion layers under reverse voltage conditions are shown in Fig. 3. When a reverse voltage is applied to a conventional IGBT, the depletion layer extends from the backside anode (collector) towards the surface cathode (emitter). The depletion layer also extends to the doped side wall and causes high local electric fields, that are proportional to the reverse voltage. The semiconductor dicing process, however, unavoidably generates numerous crystal defects and mechanical imperfections at the doped side walls. The high local electric fields generate free carriers at these crystal defects causing the so-called leakage current fountain, which may irreversibly damage the IGBT [8].

The first concept of a RB-IGBT and the realization of its internal structure has been introduced in 2001 [6], [7]. Deep diffusion of a p+-side wall protection at the doped side wall surface [cf. Fig. 3(b)] prevents the depletion layer from extending to the doped surface area of the IGBT under reverse voltage conditions. As a result, a huge reduction of the reverse leakage current under reverse voltage conditions is achieved.

Since the RB-IGBT and the conventional IGBT are only different with respect to the edge structures, same conduction and switching losses can be expected for both types of IGBTs if operated in forward direction. The RB-IGBT, however, shows a reverse recovery behavior similar to a rectifier diode if operated with reverse voltage, which causes the switching losses to increase and needs to be considered in the loss model detailed in the next section.

III. ANALYTICAL LOSS CALCULATION MODEL OF T-TYPE CONVERTERS

A. Voltage and current waveforms at ac input/output side

Fig. 4(b) illustrates general input/output voltage and current waveforms of a single phase-leg of the 3LTTC converter at ac input/output side (e.g. mains input side or load output side), shown in Fig. 4(a). It is formed with two IGBTs (T1 and T2), two FWDs (D1 and D2) and two bi-directional switches (T3 and T4). In this paper, the multi-carrier pulse width modulation (PWM) scheme detailed in [9], [10] is considered. In Fig. 4(b), Vac and Iac are instantaneous input/output voltage and current of single phase-leg at ac side, respectively. \( \nu_c \) is the temporal average voltage of \( V_{ac} \) which is same with fundamental input voltage at mains side or output voltage at load side. \( \psi = \omega t \) denotes the phase of the fundamental voltage, \( \Phi_d \) is the phase displacement between the fundamental components of current and voltage, \( \dot{V} \) is the peak fundamental phase voltage, and \( \ddot{I} \) is the peak fundamental phase current. Thus, \( \Phi_d = 0^\circ \) denotes inverter mode of operation with unity power factor and \( \Phi_d = 180^\circ \) denotes rectifier mode of operation with unity power factor. Voltage and current amplitudes, \( \dot{V} \) and \( \ddot{I} \), are derived from the modulation index \( M \) and the input/output apparent power \( S_{ac} \) as shown below.

\[
\dot{V} = M \frac{V_{dc}}{2} \\
\ddot{I} = \frac{2}{3} \frac{S_{ac}}{\dot{V}}
\]

B. Conduction loss model

Fig. 5(a) shows a general on-state characteristic of an IGBT or a diode. Linearization of the characteristic, obtained at a given junction temperature \( T_j \), yields the loss model parameters \( V_i(T_j) \) and \( R_{on}(T_j) \). The corresponding losses are calculated with the rms and the average currents through the device according to:

\[
P_c = R_{on}(T_j) I_{rms}^2 (M, \dot{I}, \Phi_d) + V_i(T_j) I_{avg} (M, \ddot{I}, \Phi_d).
\]

\( R_{on}(T_j) \) and \( V_i(T_j) \) denote temperature dependent on-state resistance and forward voltage drop values of the considered semiconductor, respectively. The temperature dependency is considered according to [11]:

\[
R_{on}(T_j) = R_{on}(T_{j0}) \left( \frac{T_j}{T_{j0}} \right)^{k_{R_{on}}},
\]

\[
V_i(T_j) = V_i(T_{j0}) \left( \frac{T_j}{T_{j0}} \right)^{k_{V_i}},
\]
The analytical expressions of average and rms currents through all devices are derived according to [9]. The currents through the IGBTs with a suggested break-down voltage of 1200 V, i.e. the two IGBTs $T_1$ and $T_2$ in Fig. 4, are:

$$I_{\text{avg.}, T_{12}} = \frac{1}{4\pi} \int_0^\infty M [\sin (\Phi f) - \sin (\Phi_1)]$$

$$I_{\text{rms.}, T_{12}} = \frac{1}{2\pi} \int_0^\infty M \sin (\Phi f)$$

The currents through $D_1$ and $D_2$ (or the FWD of $T_1$ and $T_2$) are:

$$I_{\text{avg.}, D_{12}} = \frac{1}{4\pi} \int_0^\infty M [\sin (\Phi f) - \sin (\Phi_1)]$$

$$I_{\text{rms.}, D_{12}} = \frac{1}{2\pi} \int_0^\infty M \sin (\Phi f)$$

And the currents in each IGBT of the bi-directional switch (and in the IGBTs’ FWD, if applicable), i.e. $T_3$ and $T_4$, are:

$$I_{\text{avg.}, T_{12}} = \frac{1}{2\pi} \int_0^\infty M [\sin (\Phi f) - \sin (\Phi_1)]$$

$$I_{\text{rms.}, T_{12}} = \frac{1}{2\pi} \int_0^\infty M \sin (\Phi f)$$

The equations are valid for both inverter and rectifier mode of operations $(0^\circ \leq \Phi f \leq 180^\circ)$.

C. Switching loss model

The switching states of a single leg of the 3LTC, except for transient states during dead time intervals, are listed in Tab. I. The current commutation paths related to the switching states and the input/output current conditions are shown in Fig. 6. Tab. II summarizes the expressions for the switching loss energies that result for different state transitions.

Fig. 7 serves as a basis for explaining the switching operations present in the given 3LTC converter. It depicts the considered waveform of $v_{ac}(t)$ and two switching operations for inverter mode of operation in Fig. 7(a), at $t = t_b$ ($S_{0011} \rightarrow S_{0011}$) and $t = t_i$ ($S_{1001} \rightarrow S_{1001}$): positive and approximately constant input/output current is assumed. The states involved in both depicted switching operations are, thus, $S_{1001}$ and $S_{0011}$ and, according to Tab I,

$$E_{\text{on}, T_{12}} = \int_{t_b}^{t_i} i_{\text{sw, T}_{12}}(t) \cdot v_{ac, T_{12}}(t) \, dt$$

$$E_{\text{off}, T_{12}} = \int_{t_i}^{t_f} i_{\text{sw, T}_{12}}(t) \cdot v_{ac, T_{12}}(t) \, dt$$

The turn-on losses of $T_4$, Fig. 7(c), are negligible.

Fig. 7(d) and (e) show emitter to collector voltages (blue) and collector currents (red) of $T_1$ and $T_2$ at $t = t_i$. The switch $T_1$ turns on at $t = t_b$, which causes the collector current of $T_3$ to fall. $T_1$’s collector current is zero at $t = t_b$, and, subsequently, gets negative due to reverse recovery effects. At $t = t_b$ the collector current reaches the maximum reverse recovery current $i_{rr}$, Fig. 7(e), thus, shows the reverse recovery behavior of $T_4$, i.e. the RB-IGBT FGW855N60RB. The reverse recovery charge obtained from this figure, $Q_{rr} + Q_{rt} \approx 6.5 \mu C$, causes reverse recovery losses of $T_4$ during $t_{rr} < t < t_{rr}$. Moreover, the reverse recovery behavior of $T_4$ causes a high temporary collector current in $T_1$, which increases the turn-on losses of $T_1$, as can be seen in Fig. 7(d). The turn-on losses $E_{\text{on}, T_{12}}$ and the reverse recovery losses $E_{\text{off}, T_{34}}$ are evaluated with:

$$E_{\text{on}, T_{12}} = \int_{t_b}^{t_f} i_{\text{sw, T}_{12}}(t) \cdot v_{ac, T_{12}}(t) \, dt$$

$$E_{\text{off}, T_{34}} = \int_{t_i}^{t_f} i_{\text{sw, T}_{34}}(t) \cdot v_{ac, T_{34}}(t) \, dt$$
The turn-on losses of the FWDs are neglected in this paper. $I_{sw,\text{avg}}$ denotes the averaged switching current over single fundamental period, $D_{sw}$ is the normalized period the device acts as a switch, and $f_{sw}$ is the switching frequency. Analytical expressions for the average switching current are given in [12] and summarized below:

\begin{align}
I_{sw,\text{avg},T12} &= I_{ac} \left[ 1 + \cos \left( \frac{\Phi_d}{2} \right) \right], \\
D_{sw,T12} &= \frac{\Phi_d}{2\pi}, \\
I_{sw,\text{avg},D12} &= I_{ac} \left[ \sin \left( \frac{\Phi_d}{\pi} \right) \right]^{2}, \\
D_{sw,D12} &= \frac{\Phi_d}{2\pi},
\end{align}

$I_{sw,\text{avg},T34}$ is the average switching current of $T_3$ and $T_4$ when the devices are operated as IGCTs (e.g. switching in rectifier mode of operation) and $I_{sw,\text{avg},D34}$ is the average switching current of $T_3$ and $T_4$ when the devices are operated as FWDs (e.g. switching in inverter mode of operation). The same notation is used for $D_{sw,T34}$ and $D_{sw,D34}$. These equations are valid for both inverter and rectifier mode of operations ($0^\circ \leq \Phi_d \leq 180^\circ$). The six coefficients needed to calculate the switching losses, $E_{off,1}$, $E_{off,\text{const}}$, $E_{on,1}$, $E_{on,\text{const}}$, $E_{rr,1}$, and $E_{rr,\text{const}}$, are extracted as shown in Fig. 5(b) and (c) from device’s data sheet or measurement results. The impact of the dc bus voltage, $V_{dc}$, and the junction temperature, $T_j$, is considered according to [11]:

\begin{align}
E_{off,1} &= E_{off,1,V_0,T_0,T_0} \left( \frac{V_{dc}}{V_{dc,0}} \right) \left( \frac{T_j}{T_{j0}} \right)^{\delta_{Eoff}}, \\
E_{off,\text{const}} &= E_{off,\text{const},V_0,T_0,T_0} \left( \frac{V_{dc}}{V_{dc,0}} \right) \left( \frac{T_j}{T_{j0}} \right)^{\delta_{Eoff}}, \\
E_{on,1} &= E_{on,1,V_0,T_0,T_0} \left( \frac{V_{dc}}{V_{dc,0}} \right) \left( \frac{T_j}{T_{j0}} \right)^{\delta_{Eon}}, \\
E_{on,\text{const}} &= E_{on,\text{const},V_0,T_0,T_0} \left( \frac{V_{dc}}{V_{dc,0}} \right) \left( \frac{T_j}{T_{j0}} \right)^{\delta_{Eon}}, \\
E_{rr,1} &= E_{rr,1,V_0,T_0,T_0} \left( \frac{V_{dc}}{V_{dc,0}} \right) \left( \frac{T_j}{T_{j0}} \right)^{\delta_{Err}}, \\
E_{rr,\text{const}} &= E_{rr,\text{const},V_0,T_0,T_0} \left( \frac{V_{dc}}{V_{dc,0}} \right) \left( \frac{T_j}{T_{j0}} \right)^{\delta_{Err}}.
\end{align}

Here, $V_{dc,0} = 720$ V is the voltage and $T_{j0} = (273.15 + 150)$ K is the junction temperature at which the measurements have been conducted.

D. Estimating the increase of the turn-on loss energy due to the reverse recovery charge of FWDs

Most of the results presented in Section IV are solely based on experimental results, only the losses of the two converter

\begin{table}[h]
\centering
\caption{Switching states}
\begin{tabular}{c|c|c|c|c}
\hline
$S_{on1}$ & $S_{on1}$ & $S_{on1}$ & $S_{on1}$ \\
\hline\hline
$T_1$: & on & off & off \& on \\
$T_2$: & off & on & on \& on \\
$T_3$: & off & off & on \\
$T_4$: & on & on & on \\
\hline
\end{tabular}
\end{table}
conventional IGBTs and anti-parallel SiC SBDs. The bi-directional switch (configurations B3 and C3 in Section IV) are estimated.

According to Section III-C the amount of reverse recovery charge, \( Q_{rr} = Q_{acs} + Q_{t} \), of the FWD (or RB-IGBT) has a strong impact on the resulting turn-on losses. Thus, the turn-on switching losses available in data sheets are not readily applicable for the presented comparison, since the T-type inverter employs different types of power semiconductor switches, i.e., T1 and T2 are conventional IGBT/FWD modules with \( V_{(BR)CES} = 1200 \) V and T3 and T4 are RB-IGBTs with \( V_{(BR)CES} = 600 \) V.

The expected turn-on losses can be estimated based on [13] using the transient voltage and current waveforms during turn-on depicted in Fig. 7(d) and (e). According to [13] the turn-on losses of the IGBT, \( E_{on,T} \), can be separated into two parts. The first part denotes the turn-on losses without reverse recovery:

\[
E_{on,T,0} = E_{on,T} - \Delta E_{on,T},
\]

and the second part denotes additional losses due to reverse recovery:

\[
\Delta E_{on,T} \equiv (t_s \cdot i_{acs} + Q_{t}) \frac{V_{dc}}{2},
\]

\( t_s \) is the delay time due to reverse recovery,

\[
t_s = t_{b3} - t_{b2}.
\]

\( E_{on,T,0} \) is calculated based on measurement results, then the turn-on losses with SiC SBDs instead of Si FWDs (configurations B3 and C3 in Section IV) are estimated with (32) as below:

\[
\tilde{E}_{on,T} = E_{on,T,0} + \Delta \tilde{E}_{on,T},
\]

and the second part estimates additional losses due to the total capacitive charge \( Q_{t} \) from SiC SBDs,

\[
\Delta \tilde{E}_{on,T} = \left( \tilde{t}_s \cdot i_{acs} + Q_{t} \right) \frac{V_{dc}}{2},
\]

\( \tilde{t}_s \) is the estimated delay time due to \( Q_{t} \),

\[
\tilde{t}_s = \sqrt{\frac{2Q_{t}}{i_{c,s}(t_{b2})}},
\]

\( i_{c,s}(t_{b2}) \) is a derivative value of collector current at \( t = t_{b2} \) and measurement results are used for this value. \( Q_{t} = 16 \mu C \) at reverse voltage \( V_r = 360 \) V is obtained from the data sheet of C3D2060D.

E. Thermal model

The temperature of each semiconductor’s junction is calculated based on the conduction and switching losses, \( P_c \) and \( P_{sw} \), of the considered switch and with a simplified linear thermal model, which considers the thermal resistance from junction to case, \( R_{th,j-e} \):

\[
T_j = R_{th,j-e} \cdot (P_c + P_{sw}) + T_{case}.
\]

Conduction losses and switching losses show a non-linear temperature dependency. Hence, an iterative procedure is implemented to solve for junction temperature, conduction losses, and switching losses.

### Table II. Switching loss energies

<table>
<thead>
<tr>
<th>Input/output current condition</th>
<th>Switching transitions</th>
<th>( E_{on,T,0} \rightarrow S_{011} )</th>
<th>( S_{1011} \rightarrow S_{011} )</th>
<th>( S_{011} \rightarrow S_{1011} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( i_{acs} &gt; 0 )</td>
<td>( E_{on,T,0} \cdot T_{j} + E_{on,T,12} \cdot T_{j} + E_{on,T,24} \cdot T_{j} )</td>
<td>( E_{off,T,0} \cdot T_{j} + E_{off,T,12} \cdot T_{j} + E_{off,T,24} \cdot T_{j} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( i_{acs} &lt; 0 )</td>
<td>( E_{on,T,0} \cdot T_{j} + E_{on,T,12} \cdot T_{j} + E_{on,T,24} \cdot T_{j} )</td>
<td>( E_{off,T,0} \cdot T_{j} + E_{off,T,12} \cdot T_{j} + E_{off,T,24} \cdot T_{j} )</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table IV. Extracted conduction loss model parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>( f / V \cdot A )</th>
<th>( V_{f} / V )</th>
<th>( R_{on,T} / 10 )</th>
<th>( V_{(BR)CES} / V )</th>
<th>( k_{mc} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>IGBT1(T)</td>
<td>175</td>
<td>1.04</td>
<td>0.016</td>
<td>-0.0563</td>
<td>1.22</td>
</tr>
<tr>
<td>IGBT1(D)</td>
<td>175</td>
<td>0.86</td>
<td>0.016</td>
<td>-1.1163</td>
<td>0.288</td>
</tr>
<tr>
<td>IGBT2</td>
<td>150</td>
<td>0.75</td>
<td>0.037</td>
<td>-0.6346</td>
<td>1.824</td>
</tr>
<tr>
<td>IGBT3</td>
<td>150</td>
<td>0.76</td>
<td>0.018</td>
<td>-0.3604</td>
<td>1.155</td>
</tr>
<tr>
<td>IGBT4(D)</td>
<td>150</td>
<td>1.01</td>
<td>0.018</td>
<td>-1.5906</td>
<td>0.819</td>
</tr>
<tr>
<td>SBD</td>
<td>175</td>
<td>0.72</td>
<td>0.053</td>
<td>-0.6001</td>
<td>1.989</td>
</tr>
</tbody>
</table>

Fig. 8. On-state forward voltage drop versus collector or forward current at \( T_j = 150 \) °C. (a) for switches with \( V_{(BR)CES} = 1200 \) V and (b) for bi-directional switches, cf. Fig. 2, with \( V_{(BR)CES} = 600 \) V.

IV. Comparison of T-type converters with and without RB-IGBTs

A. IGBT/FWD modules suitable for comparison

Different types of IGBTs are considered for the bi-directional switch, including devices optimized with respect to low conduction losses or low switching losses, in order to allow for a meaningful comparison of the losses obtained with conventional IGBTs and RB-IGBTs. Tab. III lists the considered devices:

- IGBT1: 1200 V IGBT + FWD for T1, T2, D1 and D2 .
- IGBT2: 600 V RB-IGBT for T3 and T4 .
- SBD1: 1200 V SiC SBD for D1 and D2 .
- SBD2: 600 V SiC SBD for T3 and T4 .

Two parallel connected components IGBT1 are considered in order to achieve reduced conduction losses and, thus, the total maximum forward currents of D1 and D2 are 60 A. In order to save costs, the rated currents of the selected SiC SBDs (SBD1 and SBD2) are approximately two thirds of the rated currents of the Si FWDs. With this, the diode currents are still well below the rated diode currents, however, considerably increased conduction losses result.

B. Parameterization of the conduction loss models

The conduction loss model is parameterized with data sheet values based on least mean square approximation, the obtained coefficients are listed in Tab. IV. There, IGBT(T) denotes the IGBT and IGBT(D) the FWD if a single package contains both, IGBT and FWD. Fig. 8 depicts the forward characteristics of the considered devices.

C. Switching losses measurement results

During switching, a device with a breakdown voltage of 1200 V and a second device with \( V_{(BR)CES} = 600 \) V are operated together,
TABLE III. Considered semiconductor devices for loss comparison; \( V_{BR(CES)} \): maximum collector-emitter voltage of IGBTs; \( V_{RHM} \): repetitive peak reverse voltage of FWDs; \( I_{F} \): maximum dc collector current of IGBTs; \( I_{p} \): average forward current of FWDs; \( N_{p} \): the number of paralleled modules.

<table>
<thead>
<tr>
<th>Name</th>
<th>Device type</th>
<th>( V_{RHM} )</th>
<th>( I_{F} )</th>
<th>( \text{R}_{th,j(on)} )</th>
<th>( \text{R}_{th,j(off)} )</th>
<th>( N_{p} )</th>
<th>Model</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>IGBT1</td>
<td>Si IGBT and FWD</td>
<td>1200</td>
<td>40/30</td>
<td>0.45/0.7/0.7</td>
<td>2</td>
<td>FGW40NN120HD</td>
<td>Fuji Electric</td>
<td></td>
</tr>
<tr>
<td>IGBT2</td>
<td>Si RB-IGBT</td>
<td>600</td>
<td>85</td>
<td>0.208</td>
<td>1</td>
<td>FGW85N60RB</td>
<td>Fuji Electric</td>
<td></td>
</tr>
<tr>
<td>IGBT3</td>
<td>Si IGBT and FWD</td>
<td>600</td>
<td>75/30</td>
<td>0.21/0.9/1</td>
<td>1</td>
<td>IXTH75N60C3D1</td>
<td>IXYS</td>
<td></td>
</tr>
<tr>
<td>IGBT4</td>
<td>Si IGBT and FWD</td>
<td>600</td>
<td>75/30</td>
<td>0.21/0.9/1</td>
<td>1</td>
<td>IXTH75N60B3D1</td>
<td>IXYS</td>
<td></td>
</tr>
<tr>
<td>SBD1</td>
<td>SiC SBD</td>
<td>600</td>
<td>20</td>
<td>0.55</td>
<td>1</td>
<td>CID20060D</td>
<td>Cree</td>
<td></td>
</tr>
</tbody>
</table>

TABLE V. Combination of switching devices for comparison.

<table>
<thead>
<tr>
<th>Label</th>
<th>Device type</th>
<th>( V_{RHM} )</th>
<th>( I_{F} )</th>
<th>( \text{R}_{th,j(on)} )</th>
<th>( \text{R}_{th,j(off)} )</th>
<th>( N_{p} )</th>
<th>Model</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>Si IGBT (IGBT1(T))</td>
<td>1200</td>
<td>25</td>
<td>0.25/0.5/0.5</td>
<td>2</td>
<td>FGW125N120HD</td>
<td>Fuji Electric</td>
<td></td>
</tr>
<tr>
<td>B1</td>
<td>Si IGBT (IGBT1(T))</td>
<td>1200</td>
<td>25</td>
<td>0.25/0.5/0.5</td>
<td>2</td>
<td>FGW125N120HD</td>
<td>Fuji Electric</td>
<td></td>
</tr>
<tr>
<td>C1</td>
<td>Si IGBT (IGBT1(T))</td>
<td>1200</td>
<td>25</td>
<td>0.25/0.5/0.5</td>
<td>2</td>
<td>FGW125N120HD</td>
<td>Fuji Electric</td>
<td></td>
</tr>
<tr>
<td>A2</td>
<td>Si IGBT (IGBT1(T))</td>
<td>1200</td>
<td>25</td>
<td>0.25/0.5/0.5</td>
<td>2</td>
<td>FGW125N120HD</td>
<td>Fuji Electric</td>
<td></td>
</tr>
<tr>
<td>B2</td>
<td>Si IGBT (IGBT1(T))</td>
<td>1200</td>
<td>25</td>
<td>0.25/0.5/0.5</td>
<td>2</td>
<td>FGW125N120HD</td>
<td>Fuji Electric</td>
<td></td>
</tr>
<tr>
<td>C2</td>
<td>Si IGBT (IGBT1(T))</td>
<td>1200</td>
<td>25</td>
<td>0.25/0.5/0.5</td>
<td>2</td>
<td>FGW125N120HD</td>
<td>Fuji Electric</td>
<td></td>
</tr>
<tr>
<td>A3</td>
<td>Si IGBT (IGBT1(T))</td>
<td>1200</td>
<td>25</td>
<td>0.25/0.5/0.5</td>
<td>2</td>
<td>FGW125N120HD</td>
<td>Fuji Electric</td>
<td></td>
</tr>
<tr>
<td>B3</td>
<td>Si IGBT (IGBT1(T))</td>
<td>1200</td>
<td>25</td>
<td>0.25/0.5/0.5</td>
<td>2</td>
<td>FGW125N120HD</td>
<td>Fuji Electric</td>
<td></td>
</tr>
<tr>
<td>C3</td>
<td>Si IGBT (IGBT1(T))</td>
<td>1200</td>
<td>25</td>
<td>0.25/0.5/0.5</td>
<td>2</td>
<td>FGW125N120HD</td>
<td>Fuji Electric</td>
<td></td>
</tr>
</tbody>
</table>

Fig. 9. The switching loss measurement setup.

cf. Section III, and, according to Tab.II, the resulting switching losses depend on the used combination of switches. With the considered IGBTs and SiC SBDs the eight different combinations of devices listed in Tab.V are feasible. The switching losses resulting from the first six combinations, A1, B1, C1, A2, B2 and C2, are measured with the switching loss measurement setup depicted in Fig.9 and for the conditions listed below.

- Employed dc link voltage: \( V_{dc} = 720 \) V.
- Junction temperatures: \( T_{j1} = 30 \) °C, \( T_{j2} = 150 \) °C.
- Gate resistance: \( R_{G} = 5 \) Ω.
- On- and off-state gate voltages: \( V_{GE,on} = 16 \) V, \( V_{GE,off} = -6 \) V.

The switching losses obtained for the remaining combinations B3 and C3 are estimated with (35).

The resulting switching losses are shown in Fig.10 for all considered device combinations. The extracted parameters of the switching loss model are listed in Tab.VI.

1) Rectifier mode of operation: The turn-on losses of \( T_3 \) and \( T_4, E_{on,T34} \), and the reverse recovery losses of the FWDs of \( D_1 \) and \( D_2, E_{rr,D12} \), largely depend on the reverse recovery behavior of the FWDs of \( D_1 \) and \( D_2 \). Therefore, as shown in Fig.10(b) and (c), \( E_{on,T34} \) and \( E_{rr,D12} \) are similar for the device combinations A1, B1, and C1 and can be considerably reduced with SiC SBDs (combinations A2, B2, C2, A3, and B3), i.e. the type of IGBT used for \( T_1 \) and \( T_2 \) has only little influence on the achieved turn-on losses. The IGBT selected for \( T_3 \) and \( T_4 \) mainly determines the obtained turn-off losses, cf. Fig.10(a): it is seen that the IGBT optimized for speed yields minimum switching losses (e.g. B1), maximum switching losses result with the IGBT optimized for low conduction losses (e.g. C1), and the losses obtained with the considered RB-IGBT are in between (e.g. A1).

2) Inverter mode of operation: The turn-on losses of \( T_1 \) and \( T_2, E_{on,T12} \), and the reverse recovery losses of \( T_1 \) and \( T_4 \) (or the FWDs of \( T_3 \) and \( T_4 \) in case of conventional IGBTs being used), \( E_{rr,T12} \) and \( E_{rr,T34} \), are considerably higher for the configurations A1 and A2 than for the configurations using conventional IGBT/FWD modules (B1, B2, B3, C2, and C3), since the use of faster and smaller chips allows for a reduction of the reverse recovery charge of the employed FWDs. The turn-off losses of \( T_1 \) and \( T_2, E_{off,T12} \) are to a large part caused by the tail currents of \( T_1 \) and \( T_2 \) and are nearly independent of the type of IGBT selected for \( T_3 \) and \( T_4 \).

D. Loss comparison results and discussion

The total semiconductor losses of three-phase 3LTC with and without the RB-IGBT are analyzed. In Fig.11(a) and (b), total semiconductor losses of the 3LTC are presented for operation in the switching frequency range of 5 kHz to 35 kHz for rectifier and inverter mode of operations, respectively.

Fig. 10. Switching losses measured (A1, A2, A3) or estimated (B1, B2, B3, C2, C3) for the different considered device combinations, different switch currents \( I_{sw} \), \( V_{dc} = 720 \) V, and \( T_{j1} = 150 \) °C (a), (b) and (c) denote the switching losses for rectifier mode of operation and (d), (e) and (f) the switching losses for inverter mode of operation.
### Table VI. Parameter Values of the Switching Loss Models for the Different Considered Device Combinations Being Determined for $V_{dc0} = 720 \text{ V}$ and $T_{ij} = 150^\circ \text{C}$.

<table>
<thead>
<tr>
<th></th>
<th>$E_{on} \text{[mA]}$</th>
<th>$E_{off _const} \text{[mJ]}$</th>
<th>$k_{off}$</th>
<th>$E_{on _const} \text{[mA]}$</th>
<th>$E_{off _const} \text{[mJ]}$</th>
<th>$k_{off}$</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>600 V RGT</strong> ($T_1$ and $T_2$)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A1</td>
<td>0.02</td>
<td>0.239</td>
<td>2.123</td>
<td>0.038</td>
<td>0.234</td>
<td>1.259</td>
</tr>
<tr>
<td>B1</td>
<td>0.014</td>
<td>0.139</td>
<td>1.192</td>
<td>0.036</td>
<td>0.235</td>
<td>1.331</td>
</tr>
<tr>
<td>C1</td>
<td>0.03</td>
<td>0.417</td>
<td>1.066</td>
<td>0.036</td>
<td>0.235</td>
<td>1.331</td>
</tr>
<tr>
<td>A2</td>
<td>0.016</td>
<td>0.237</td>
<td>2.498</td>
<td>0.031</td>
<td>-0.081</td>
<td>-0.028</td>
</tr>
<tr>
<td>B2</td>
<td>0.014</td>
<td>0.149</td>
<td>1.191</td>
<td>0.016</td>
<td>-0.092</td>
<td>-0.423</td>
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<tr>
<td>C2</td>
<td>0.029</td>
<td>0.424</td>
<td>1.013</td>
<td>0.017</td>
<td>-0.094</td>
<td>0.146</td>
</tr>
<tr>
<td>A3</td>
<td>Same as A1</td>
<td>Same as A1</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>B3</td>
<td>Same as A1</td>
<td>Same as A1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C3</td>
<td>Same as A1</td>
<td>Same as A1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>1200 V FWD</strong> ($D_1$ and $D_2$)</td>
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<td></td>
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<tr>
<td>A1</td>
<td>0.019</td>
<td>0.357</td>
<td>3.573</td>
<td>0.024</td>
<td>0.581</td>
<td>3.434</td>
</tr>
<tr>
<td>B1</td>
<td>0.013</td>
<td>0.559</td>
<td>3.139</td>
<td>0.024</td>
<td>0.581</td>
<td>3.434</td>
</tr>
<tr>
<td>C1</td>
<td>0.046</td>
<td>0.376</td>
<td>0.929</td>
<td>0.007</td>
<td>0.085</td>
<td>0.024</td>
</tr>
<tr>
<td>A2</td>
<td>0.044</td>
<td>0.376</td>
<td>0.929</td>
<td>0.007</td>
<td>0.085</td>
<td>0.024</td>
</tr>
<tr>
<td>B2</td>
<td>0.045</td>
<td>0.383</td>
<td>0.929</td>
<td>0.022</td>
<td>0.121</td>
<td>1.946</td>
</tr>
<tr>
<td>C2</td>
<td>0.039</td>
<td>0.376</td>
<td>0.929</td>
<td>0.007</td>
<td>0.085</td>
<td>0.024</td>
</tr>
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<td>A3</td>
<td>Same as A1</td>
<td>Same as A1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B3</td>
<td>Same as A1</td>
<td>Same as A1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C3</td>
<td>Same as A1</td>
<td>Same as A1</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

Fig. 11. Total loss comparison of three phase 3LTTCs for the eight different device combinations listed in Tab. V operation with unity power factor. $V = 325 \text{ V}$ and $I = 41 \text{ A}$. (a) rectifier mode of operation (Fig. 10(e) and (f)) for different losses regarding $A_1$ and $B_1$ (or $A_1$ and $C_1$). $f_{cross1}$ is the crossover frequency for total losses. $f_{cross2}$ is the crossover frequency for total losses regarding $A_1$ and $B_1$ (or $A_1$ and $C_1$). $f_{cross2}$ is the crossover frequency of $A_1$ and $B_3$ (or $A_1$ and $C_3$).

In rectifier mode of operation, configuration A1 allows for lower total losses than configurations B1 and C1 for switching frequencies up to $13 \text{ kHz}$. In inverter mode of operation, the assumed total semiconductor losses and for the different configurations. In rectifier mode of operation, configuration A1 allows for lower total losses than configurations B1 and C1, cf. Fig. 10(e) and (f). In inverter mode of operation, with unity power factor, the diodes $D_1$ and $D_2$ do not contribute to the switching losses and, therefore, the losses calculated for the configurations A2, B2, and C2, i.e. $D_1$ and $D_2$ are realized with $S_{ICD}$, B3, and C3 (SiC SBDs used for the FDW). Further total loss reduction are achieved for configurations B3 and C3 (SiC SBDs used for the FDWs) for switching frequencies greater than $8 \text{ kHz}$ due to zero reverse recovery charge from these SiC SBDs.
Inverter mode of operation, Fig. 12(b), configuration A1 shows lower total conduction losses than configurations B1 and C1, however, due to considerably higher switching losses, the lowest operating switching frequency results for configuration A1. The losses calculated for the configurations A2, B2, and C2 are identical to the losses calculated for the configurations A1, B1, and C1 because in inverter mode of operation with unity power factor, the converter configuration with the bi-directional switch being realized with an anti-series connection of standard IGBT/SiC SBD modules shows lowest total losses for switching frequencies greater than 8 kHz and is, therefore, considered most suitable. Still, further improvements of the RB-IGBT, in particular with respect to reverse recovery effects in order to reduce switching losses, e.g. by applying the latest generation’s internal structure with life time control techniques, would change the results obtained in this comparison and may render the RB-IGBT better suitable for inverters based on the 3LTTTC topology, too.

V. CONCLUSION

In this paper, the total semiconductor losses of three-level T-type rectifier and inverter of a 20 kVA UPS system, are determined for different realizations of the bi-directional switches, i.e. with and without RB-IGBTs. In addition, the improvements feasible with SiC SBDs being used instead of Si diodes are analyzed and evaluated for 3LTTTC topologies.

Comparison results show that the rectifier preferably employs RB-IGBTs for the bi-directional switch (low conduction losses) and SiC SBDs for the rectifier diodes (low switching losses). With this, switching frequencies up to 32.5 kHz are feasible for total semiconductor losses of the rectifier of 250 W. In inverter mode of operation with unity power factor, the converter configuration with the bi-directional switch being realized with an anti-series connection of standard IGBT/SiC SBD modules shows lowest total losses for switching frequencies greater than 8 kHz and is, therefore, considered most suitable. Still, further improvements of the RB-IGBT, in particular with respect to reverse recovery effects in order to reduce switching losses, e.g. by applying the latest generation’s internal structure with life time control techniques, would change the results obtained in this comparison and may render the RB-IGBT better suitable for inverters based on the 3LTTTC topology, too.

REFERENCES