



Power Electronic Systems  
Laboratory

© 2013 IEEE

Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE USA 2013), Denver, Colorado, USA,  
September 15-19, 2013

## Novel High Voltage Conversion Ratio „Rainstick“ DC/DC Converters

M. Kasper,  
D. Bortis,  
J. W. Kolar

This material is published in order to provide access to research results of the Power Electronic Systems Laboratory / D-ITET / ETH Zurich. Internal or personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution must be obtained from the copyright holder. By choosing to view this document, you agree to all provisions of the copyright laws protecting it.



Eidgenössische Technische Hochschule Zürich  
Swiss Federal Institute of Technology Zurich

# Novel High Voltage Conversion Ratio “Rainstick” DC/DC Converters

Matthias Kasper, Dominik Bortis and Johann W. Kolar  
Power Electronic Systems Laboratory  
ETH Zurich, Physikstrasse 3  
Zurich, 8092, Switzerland  
kasper@lem.ee.ethz.ch

**Abstract**—Voltage conversions with high step-down ratios are required in many medium voltage applications for supplying auxiliary electronics. In this paper a new topology for high conversion ratios with low voltage stresses of components, modular structure and simple control is presented. The operation principles are described together with analytical descriptions of the average value of the inductor currents and RMS values of the switches. In addition, the influence of the efficiency of the individual modules on the total converter efficiency is provided. Possible modifications of the “Rainstick” converter with benefits for different applications are shown. Furthermore, the measurement results of a prototype with an input voltage range of up to 2.4 kV and 30 W output power are shown.

## I. INTRODUCTION

State-of-the-art power electronic systems comprise not only power electronic components but also auxiliary electronics such as digital signal processors, measurement electronics required for the control of the whole system and gate drives to name just a few. These parts of the system usually require a low DC supply voltage (e.g. 3.3 V for a DSP) and their combined power consumption often lies in the low double-digit Watts range. Generally, it is preferable to generate this auxiliary supply voltage from the input voltage of the power electronic system to avoid further connections to an external supply. However, in high power systems e.g. traction converters, the input voltage is in the medium voltage range and/or up to some tens of kVs and thus a voltage conversion with a high step-down ratio is needed.

A high step-down ratio can be reached in several different ways. The most straight forward option is to use buck converters which are cascaded in order to avoid too small duty cycles. Another option would be to use a flyback or forward converter. The aforementioned possibilities, however, share a common drawback: the employed switches have to be rated for the full input voltage of the system. Due to that, those switches will mainly be IGBT switches, if available for the voltage rating, or a series connection of such. This will lead to an increased size of the passive components, since they operate at a lower switching frequency than MOSFETs. Furthermore, as the auxiliary supply draws only a small current, the conduction losses will be increased if IGBTs have to be used instead of MOSFETs.

The Input Series Output Parallel (ISOP) converter (**Fig. 1(a)**) is another type of converter that has been presented in literature

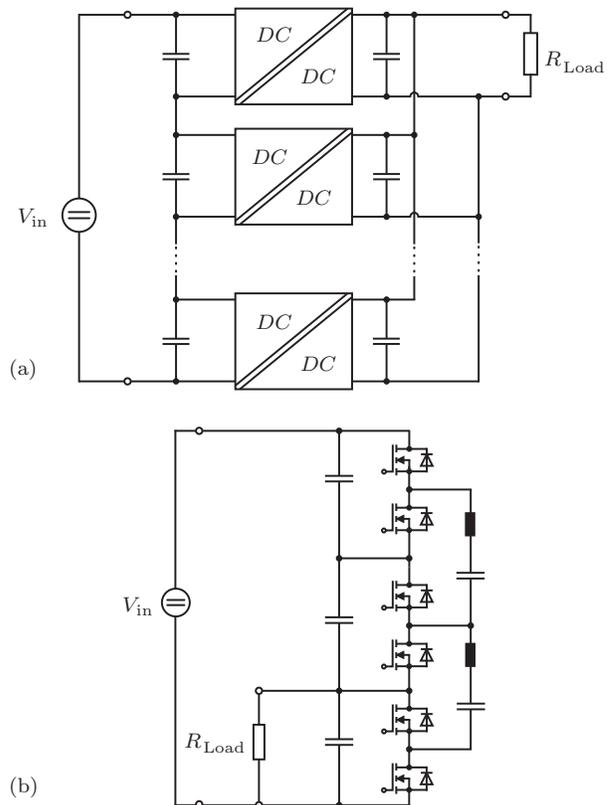


Fig. 1: Converter concepts for high step-down ratios presented in literature: (a) ISOP (Input Series Output Parallel) converter and (b) switched capacitor converter (resonant version).

[1],[2] to facilitate the voltage conversion with a high step-down ratio. Here, the input terminals of several isolated DC-DC converters are connected in series in order to divide the input voltage by the number of converters and to limit the voltage stress of the employed switches of each converter. The converter output terminals are connected in parallel to each other. Additionally, control methods have been published to accomplish an equal sharing of the input voltage as in [3]. One disadvantage is that the employment of transformers is necessary and the isolation between the primary and secondary side needs to withstand voltages as high as the total input voltage.

Another concept to obtain a high step-down conversion ratio is

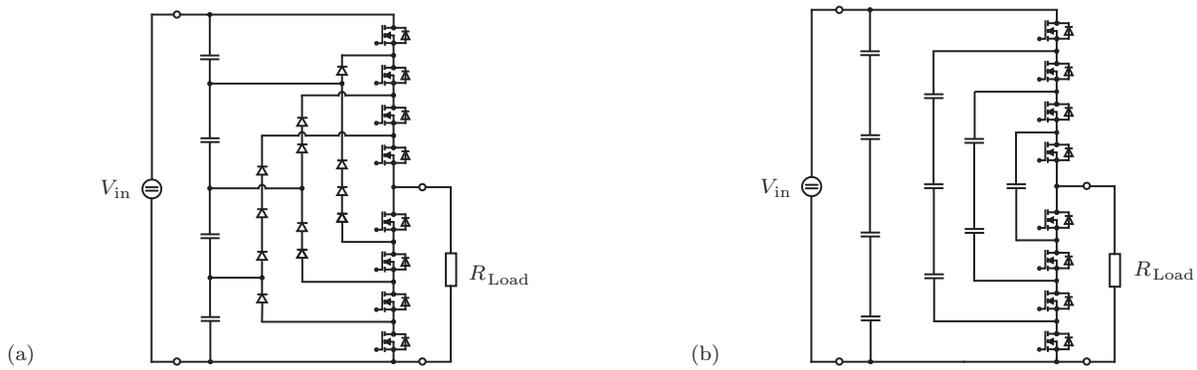


Fig. 2: Multilevel converter concepts: (a) diode-clamped topology and (b) flying capacitor topology.

by using switched capacitor converters (**Fig. 1(b)**) [4],[5]. The circuits consist of a capacitive voltage divider where the load is attached to one or more capacitors. A voltage balancing circuit is attached in order to still ensure an equal voltage distribution among the capacitors despite the asymmetric load connection. Such balancing circuits are known from battery management systems [6],[7]. Capacitors of the balancing circuit are alternately connected in parallel to adjacent capacitors of the voltage divider. As a modification, the topology can also be implemented as a resonant circuit where additional inductors are connected in series to each capacitor of the balancing circuit [8]. A main drawback is that the switches of the balancing circuit have to be controlled synchronously for proper operation of the system. Accordingly, a central control stage and a distribution of the gate drive signals with high isolation voltage has to be provided.

The multilevel converter concept has also been proposed for high step down voltage conversion [9],[10]. The most basic structure does not comprise inductive components and thus features a high power density. Common types of multilevel converters are the diode-clamped topology (**Fig. 2(a)**) and the flying capacitor topology (**Fig. 2(b)**). The former category exhibits high voltage stresses on the diodes and hence requires a large number of series connected diodes which leads

to increased conduction losses. The latter category exhibits high voltage stresses on the capacitors, thus requiring many capacitors to be connected in a series connection. Since the total capacitance of series connected capacitors is smaller than that of a single capacitor, multiple capacitor cascades need to be paralleled. Furthermore, only the flying capacitor topology can actively balance the input voltages of the DC-DC converters equally by means of redundant switching states [11]. The diode-clamped topology, however, requires an additional balancing circuit [12].

The problem of high conversion ratios, although with reversed power flow direction, can also be found in photovoltaic (PV) architectures. A DC-bus voltage which is much larger than the individual PV panel voltages has to be supplied for feeding power into the grid. Among the suitable converter concepts for that application, the parallel connected partial-power converter (P-PPC) [13] equalizes the PV panel voltages of in series connected PV panels. Thus it ensures the operation of all panels in or close to their Maximum Power Point [14], [15], [16], [17], [18]. These P-PPC topologies, many of them known from battery charge equalization circuits [6],[7], can also be applied to vertically stacked voltage domains such as proposed for multi-core microprocessor power supplies [19], [20]. They allow regulating the operating voltage of each

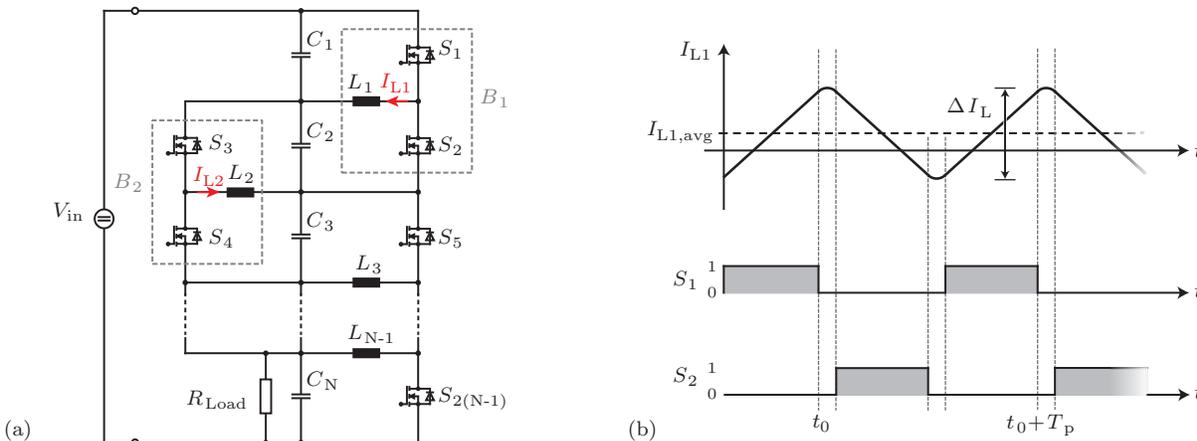


Fig. 3: New Rainstick (RSTC) converter topology: (a) circuit diagram showing capacitive voltage divider ( $C_1 \dots C_N$ ) and balancing modules highlighted ( $B_1, B_2$ ) and (b) characteristic current waveform and gate signals of one balancing module.

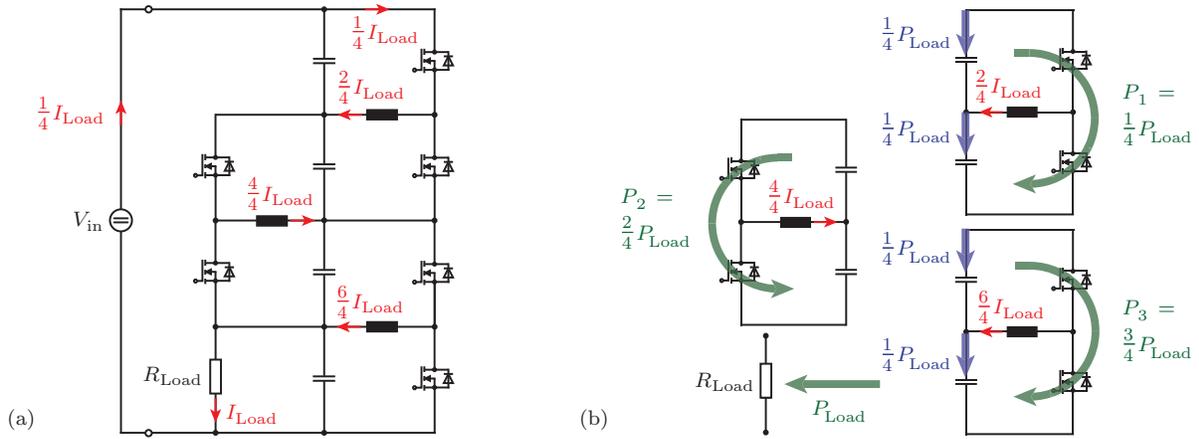


Fig. 4: Steady state analysis of RSTC converter: (a) current distribution in converter and (b) different representation of the converter with multiple buck-boost converters for an easier understanding of power flows. The power is not at once directly transferred from the source to the load but through a cascade of different converter stages, comparable to the pebbles falling down in a rainstick.

in series connected load from a fixed DC-bus. Thus, as the loads are no longer connected in parallel, the load current is decreased, which leads to a higher system efficiency.

This paper introduces a new type of high step-down converters, based on the P-PPC concept. Due to its operating principle, this new converter is denominated as Rainstick (RSTC) converter. The converter features low voltage stresses of the employed components and a simple control scheme. First, the fundamental principle of operation is explained in Sec. II. Subsequently, an analysis of the average current values in the inductors and RMS current values in the switches along with the conversion efficiency is presented in Sec. III. In addition, the topology and the working principle of an on-board auxiliary power supply are detailed in Sec. IV. Furthermore, different alternative converter realizations of the Rainstick converter principle are described in Sec. V. The optimization and realization of a RSTC prototype are shown in Sec. VI and the measurement results are depicted in Sec. VII.

## II. OPERATING PRINCIPLE

In this section the structure of the RSTC converter and the fundamental operating principle are described.

The converter, as depicted in **Fig. 3(a)**, has a modular structure which is based on a capacitive voltage divider ( $C_1 \dots C_N$ ) with buck-boost DC-DC converters as balancing modules (e.g.  $B_1$ ). These balancing modules are connected around two adjacent capacitors. This means, that a RSTC converter consisting of  $N$  capacitors contains  $(N - 1)$  balancing modules i.e.  $(2(N - 1))$  switches and  $(N - 1)$  inductive components in total. A load can be attached to one or more capacitors of the voltage divider. The converter output voltage at the load  $R_{Load}$  is a fixed divider of the input voltage  $V_{in}$ , determined by the number  $N$  of capacitors. For the sake of simplicity, the load is depicted as a single resistor whereas in reality it would usually consist of an additional DC-DC converter in order to provide a variable voltage conversion of the RSTC output voltage to the voltage level of the load.

The switches of each buck-boost converter can be controlled

by a simple PWM signal with a fixed duty cycle of (slightly less than) 50% and a  $180^\circ$  phase shift at a fixed switching frequency. There is no communication or synchronization needed between the different balancing modules which allows them to operate independently from each other.

The waveform of the gate signals and the resulting inductor current and its average value are shown for one balancing module in **Fig. 3(b)**. The system can operate with zero voltage switching (ZVS) as the direction of the inductor current reverses during each half period. Thus, in combination with the parasitic drain-source capacitances of the MOSFETs, ZVS can be provided. The converter can operate in ZVS over the whole range of input voltages by linearly increasing the switching frequency with increasing input voltage, which yields a constant peak-to-peak current ripple  $\Delta I_L$  of the inductor current  $I_L$ .

In this paper, the main focus is on the step-down operation but the converter structure is bidirectional and thus equally well suited for step-up operation, too. For that kind of operation the source would be connected to one or more capacitors and the load would be attached across the whole stack of capacitors.

## III. ANALYTICAL DESCRIPTION

In case of no load operation, the inductor currents yield no DC value. However, if a load is connected to the system, the currents in the inductors exhibit a DC value with superimposed switching ripple as shown in **Fig. 3(b)**. The average current value in the inductors ( $I_{L,avg}$ ) can be calculated for a given load current  $I_{Load}$ . The highest average current is obtained when the load is connected across only one capacitor and at the same time one terminal of the load is either connected to the highest or lowest potential of the system, i.e. the capacitor is connected around the first or last capacitor in the stack of capacitors. Then, for a system with  $N$  capacitors, the average current values in the inductors 1 to  $N - 1$  are given by

$$|I_{L,avg}|_i = \frac{2 \cdot i}{N} I_{Load}, \quad i \in \{1, 2, \dots, N - 1\} \quad (1)$$

where each of those values appears only in one inductor. So, in a converter with e.g.  $N = 5$  capacitors, the average current

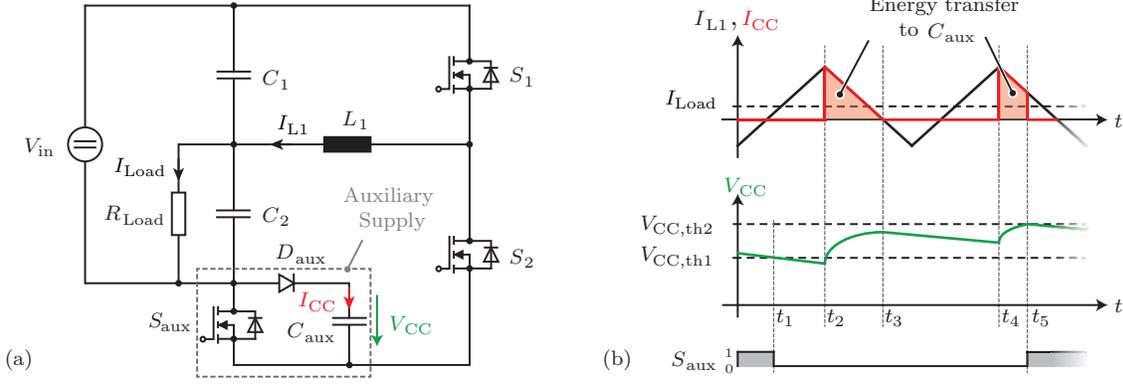


Fig. 5: Structure and analysis of on-board auxiliary power supply unit: (a) balancing module with auxiliary power supply unit comprising switch  $S_{aux}$ , diode  $D_{aux}$  and capacitor  $C_{aux}$ ; (b) characteristic waveforms of inductor current  $I_{L1}$ , charging current  $I_{CC}$  of auxiliary capacitor  $C_{aux}$ , auxiliary voltage  $V_{CC}$  and gate signal of auxiliary switch  $S_{aux}$ .

values in the inductors are  $\frac{2}{5}$ ,  $\frac{4}{5}$ ,  $\frac{6}{5}$  and  $\frac{8}{5}$  of the load current. The largest value occurs in the inductor closest to the load. For  $N \rightarrow \infty$  the maximum average current value approaches  $2 \cdot I_{Load}$ .

The main sources of losses in the RSTC converter are winding and core losses in the inductors and conduction losses of the switches. The RMS values of the currents in the switches of a balancing module depend on the average value  $I_{L,avg}$  and the peak-to-peak amplitude  $\Delta I_L$  of the inductor current ripple in that module, by

$$I_{sw,rms} = \frac{1}{2} \sqrt{2 \cdot I_{L,avg}^2 + \frac{1}{6} \Delta I_L^2}. \quad (2)$$

For calculations of the system efficiency, the power flow in the converter has to be analyzed. In general, the converter structure can be visualized as a stack of multiple buck-boost converters, as shown in **Fig. 4(b)**, which facilitates the power flow analysis. Similar to the pebbles in a rainstick, the power is not at once transferred from the source to the load but through a cascade of buck-boost stages. As seen in **Fig. 4(b)**, the largest amount of power is transferred in the lowest converter of the chain, i.e. the converter closest to the load. It is interesting to note that none of the balancing converters have to transfer the full amount of load power. Thus, this converter concept can be classified as partial-power converter [21].

For the calculation of the RSTC converter efficiency, it is assumed that each of the balancing modules has a certain conversion efficiency which is a function of the module output power  $P_i$ , i.e.  $\eta_i(P_i)$ . Then the total converter efficiency can be calculated as

$$\eta_{sys,N} = \frac{1 + \sum_{i=1}^{N-1} \left( \prod_{j=i}^{N-1} \eta_j(P_j) \right)}{N}. \quad (3)$$

For the above mentioned example of a RSTC converter with 4 capacitors and 3 balancing modules, this equation yields  $\eta_{sys,4} = 1/4 \cdot (1 + \eta_3(P_3) + \eta_3(P_3) \cdot \eta_2(P_2) + \eta_3(P_3) \cdot \eta_2(P_2) \cdot \eta_1(P_1))$ . However, the conversion efficiency is usually of minor interest, since the main idea of the RSTC concept is a high voltage conversion ratio for low power (e.g. auxiliary)

electronics. Since the power consumption of the auxiliary electronics in a power electronic system is usually very small compared to the rated power of such a system, the impact of the efficiency of the auxiliary power supply on the overall system efficiency is very small. Nevertheless, the RSTC converter efficiency can still be optimized, if the hardware of each buck-boost balancing modules is optimized for their power level. The output power of the individual balancing modules can be found as

$$P_i = \begin{cases} P_{Load} \left( 1 - \frac{1}{N \cdot \eta_{sys,N}} \right), & i = N - 1 \\ \frac{P_{i+1}}{\eta_{i+1}(P_{i+1})} - \frac{P_{Load}}{N \cdot \eta_{sys,N}}, & i \in \{1, 2, \dots, N - 2\} \end{cases}. \quad (4)$$

The values of  $\eta_{sys}$  and  $P_i$  can be calculated in an iterative process as they are dependent on each other. This is due to the fact, that the losses of one balancing module influence the power, that has to be delivered by the balancing modules before that module (in direction of power flow).

#### IV. ON-BOARD AUXILIARY POWER SUPPLY

In order to supply the gate drives and the control electronics on each module with power, an on-board power supply with a low component count and simple controllability is preferable. Thus, each module can operate without an external power supply or external gate signals. The proposed power supply consists of capacitor  $C_{aux}$ , diode  $D_{aux}$  and switch  $S_{aux}$  which are integrated in the existing balancing module, as depicted in **Fig. 5(a)**.

With the switch  $S_{aux}$  being turned on, the balancing module operates as usual. If the voltage  $V_{CC}$  drops below the lower threshold  $V_{CC,th1}$ , however, the switch  $S_{aux}$  is turned off, as shown at time  $t_1$  in **Fig. 5(b)**. At time  $t_2$ , when the switch  $S_2$  conducts the inductor current  $I_{L1}$ , capacitor  $C_{aux}$  is charged via the diode  $D_{aux}$ . This charging interval ends when current  $I_{L1}$  changes its direction, i.e. at  $t_3$ , which is necessary for ZVS operation of the switches  $S_1$  and  $S_2$ . Then, the internal body diode of  $S_{aux}$  (or an external diode placed in parallel to that switch) conducts the current  $I_{L1}$ . The charging continues at time  $t_4$  when switch  $S_2$  is turned on again. The switch  $S_{aux}$  is turned on when the voltage  $V_{CC}$  of capacitor  $C_{aux}$  reaches the

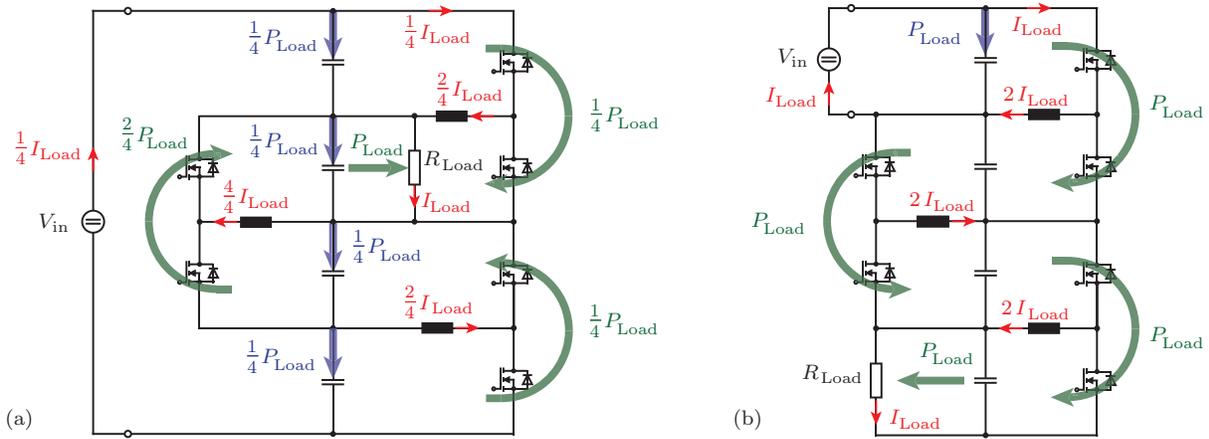


Fig. 6: Possible modifications of the Rainstick converter concept: (a) load connection to a capacitor in the middle of the capacitor stack, yielding lower average current values in the inductors and (b) connection of source to only a fraction of the stacked capacitors.

upper threshold  $V_{CC,th2}$ .

The minimum energy transfer to  $C_{aux}$  during a switching period of  $S_1$  and  $S_2$  can be calculated for the case of an inductor current without an average value (i.e.  $I_{L,avg} = 0$ ), as with increasing load current  $I_{Load}$  the energy transfer is increased (cf. **Fig. 5(b)**). Under the simplification of a narrow band of voltage thresholds (i.e.  $V_{CC} \approx V_{CC,th2} \approx V_{CC,th1}$ ), the transferred energy equals

$$\begin{aligned}
 W_{aux} &= \int_0^{T_p} V_{CC}(t) \cdot I_{CC}(t) dt \\
 &= V_{CC} \int_0^{T_p} I_{CC}(t) dt \\
 &= V_{CC} \cdot \frac{1}{16} \cdot \frac{1}{f_{sw}} \cdot \Delta I_L.
 \end{aligned} \tag{5}$$

Hence, the minimum average power that can be delivered by the auxiliary supply is independent of the switching frequency, as it is given by

$$P_{aux} = W_{aux} \cdot f_{sw} = \frac{V_{CC} \cdot \Delta I}{16}. \tag{6}$$

The proposed power supply unit can also be used in other converter topologies. A drawback of this auxiliary supply unit is, that the voltage, which is applied across inductor  $L_1$ , is altered by the value of  $V_{CC}$  each time the auxiliary switch  $S_{aux}$  is turned on or off.

## V. ALTERNATIVE DESIGNS

The concept of the Rainstick converter can be realized in different ways. In this section a number of possible modifications of the basic circuit from **Fig. 3** are described and examples of their application are given.

### A. Load connection

The load can also be connected to capacitors in the middle of the voltage divider, as shown for example in **Fig. 6(a)**. This offers the advantage to limit the maximum average current value that appears in any inductor to

$$|I_{ind,avg}|_{max} = \begin{cases} I_{Load}, & \text{if } N \text{ is even} \\ \frac{N-1}{N} I_{Load}, & \text{if } N \text{ is odd} \end{cases} \tag{7}$$

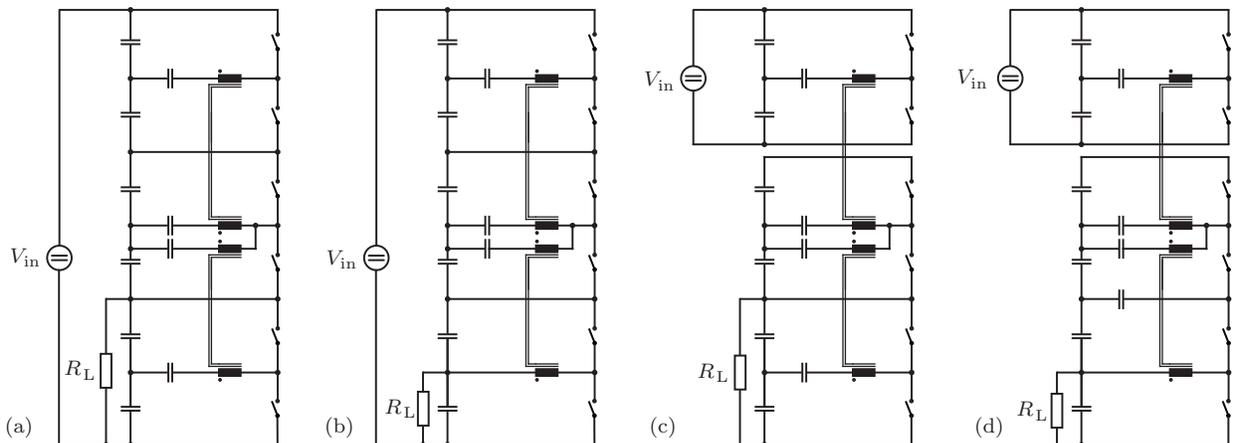


Fig. 7: Possible modifications of the RSTC converter concept with reduced component count by use of coupled inductors: (a, b) resonant version with different load connection and (c, d) isolated output stage.

Hence, inductor losses and conduction losses decrease and the overall system efficiency increases when the load is connected to capacitors closer to the middle of the voltage divider. Moreover, in systems where the load of the RSTC converter is already isolated, the maximum required voltage strength of this isolation can be reduced as not the full DC bus voltage has to be isolated.

### B. Source connection

The RSTC converter operation principle does also apply when the source is only connected to some of the  $N$  capacitors. An example with corresponding power flows is given in **Fig. 6(b)**. In contrast to the original idea of the RSTC converter, those balancing modules that are not connected to the source need to carry the full load power and any losses.

### C. Coupled inductors and isolation

The component count can be reduced by the use of coupled inductors i.e. transformers with voltage ratio 1:1, instead of inductors as depicted in **Fig. 7**. The basic circuit of the RSTC converter can be modified in such way, that for an even number ( $N$ ) of capacitors only  $(N/2 - 1)$  transformers and  $(N)$  switches are needed. With resonant capacitors in series with the transformers the system can still be operated in ZVS. This can be done by adjusting the switching frequency to the resonance frequency of the resonance capacitors and the leakage inductance of the transformer. A disadvantage resulting from the coupling is, that the control of all switches has to be synchronized.

## VI. PROTOTYPE OPTIMIZATION AND REALIZATION

A prototype of the RSTC converter comprising five balancing modules, each with its own on-board power supply unit (cf. Sec. IV), has been assembled and is shown in **Fig. 8**. As five balancing modules are used, the converter output voltage is equal to one sixth of the input voltage. The prototype is designed for a maximum input voltage of  $V_{in,max} = 2.4$  kV

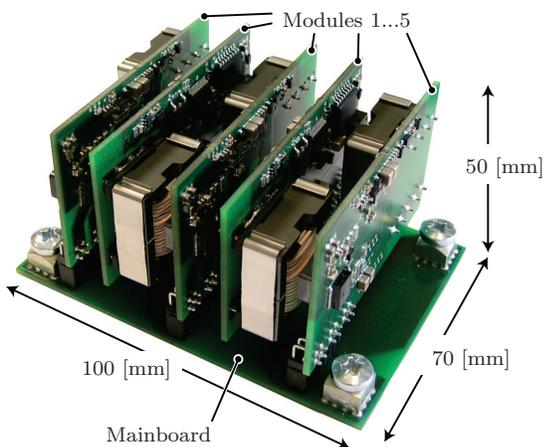


Fig. 8: Raintstick converter prototype with five balancing modules for an input voltage of up to  $V_{in,max} = 2.4$  kV and  $P_{out} = 30$  W.

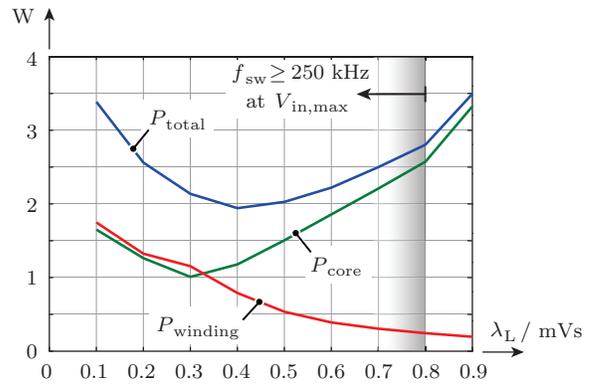


Fig. 9: Calculated inductor losses in dependence of applied volt-second ( $\lambda_L$ ) for an EFD25 N87 core and capacitor voltages of  $V_c = 300$  V. The total inductor losses  $P_{total}$  consist of core losses  $P_{core}$  and winding losses  $P_{winding}$ .

and a rated output power of  $P_{out} = 30$  W (at input voltages between  $V_{in} = 1.6$  kV...2.4 kV). Thus, each balancing capacitor has to be rated for a voltage of at least 400 V and the employed switches have to withstand voltages of up to  $V_{DS,max} = 800$  V. The switching frequency of each balancing module is adjusted by a voltage controlled oscillator (VCO) that senses the voltage across both balancing capacitors. Hence, the switching frequency is linearly increased with increasing converter input voltage, yielding a constant volt-second  $\lambda_L = V_C / (f_{sw} \cdot 2)$  which is applied across the main inductor during all switching periods. As a certain peak-to-peak inductor current ripple  $\Delta I_L$  is required by the auxiliary supply, the inductance of the main inductor  $L_1$  equals

$$L_1 = \frac{\lambda_L}{\Delta I_L} \quad (8)$$

The power consumption of the control electronics was estimated to be less than 400 mW. With a lower voltage threshold level of the auxiliary supply of  $V_{CC,th1} = 8$  V a minimum required peak-to-peak current ripple in the inductor of  $\Delta I_L = 0.8$  A can be calculated. In order to select a suitable value of  $\lambda_L$ , an inductor optimization has been performed. Here, the inductor design with the lowest losses for a given value of  $\lambda_L$  is computed. For this optimization all available EPCOS N87 cores with either ETD or EFD core shape and a selection of Rupalit litz wires have been considered. The results for an EFD25 core are demonstrated in **Fig. 9** for a

Tab. I: List of main components of RSTC prototype. (Note: All quantities are given per balancing module.)

Component	Specifications
2x MOSFETs	STD3NK100Z / ST [ $R_{DS,on} = 5.4 \Omega$ , $V_{DS} = 1000$ V, $I_D = 2.5$ A]
1x Gate driver	Half-bridge gate driver IR2214 / Int. Rectifier
1x Inductor	EFD25/13/7, N87 ferrite / EPCOS [ $L \approx 1$ mH, 60 turns, litz wire (60x71 $\mu$ m), $l_{airgap} = 0.25$ mm]
1x VCO	MCB14046B / ON Semiconductor
2x Capacitors	X7R ceramic capacitors [ $C = 1.05 \mu$ F (7x150 nF), $V_{rated} = 500$ V]

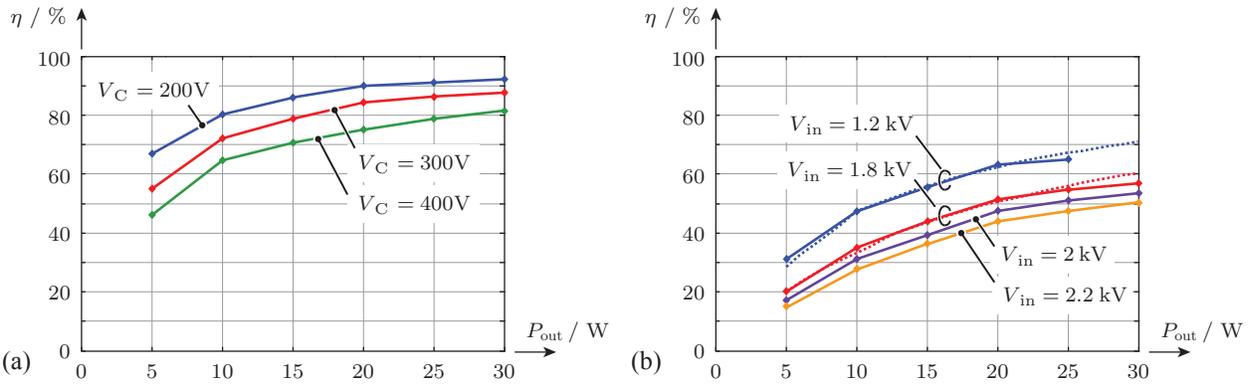


Fig. 10: Efficiency measurement results of the RSTC converter plotted over the output power: (a) single balancing module at two different levels of capacitor voltages  $V_C$  and (b) full system comprising five balancing modules at different levels of input voltage  $V_{in}$ . The dotted lines denote calculated system efficiency values. *Remark:* The measurement for  $V_{in} = 1.2$  kV and  $P_{out} = 30$  W could not be performed as the prototype can only supply the rated output power at input voltages between  $V_{in} = 1.6$  kV...2.4 kV.

capacitor voltage of  $V_C = 300$  V. Even though the lowest inductor losses can be achieved at a volt-second value of  $\lambda_L = 0.4$  mVs, values below 0.8 mVs already yield switching frequencies above  $f_{sw} = 250$  kHz which proved to be unpractical in combination with the selected gate drive due to high gate drive losses. Thus, a value of  $\lambda_L = 0.8$  mVs was selected for the prototype. Furthermore, the employed components of RSTC prototype are listed in **Tab. I**.

## VII. MEASUREMENT RESULTS

The converter efficiency measurements results of a single balancing module at different levels of capacitor voltages are presented in **Fig. 10(a)** in dependence of the output power. The results show, that for higher capacitor voltages and thus higher switching frequencies the efficiency decreases. This is due to the fact, that any increase of the switching frequency results in higher inductor losses since the core losses as well as the winding losses are frequency dependent. Furthermore, the power consumption of the gate-drive is also linearly increasing with the switching frequency. One way to increase the efficiency of the system would be to design

the system with a larger value for  $\lambda_L$  and with a larger core size. Thereby, the switching frequency of the balancing modules could be decreased without increasing the magnetic flux density, both being contributors to core losses. This, however, would decrease the power density of the system and thus has to be considered as a trade-off.

Based on the efficiency measurements of an individual module, the system efficiency has been calculated based on (3) and (4) for different levels of input voltages. The calculated efficiency values are compared to the measured system efficiency in **Fig. 10(b)**. It can be seen that the calculation results correspond well with the measurement results with a maximum error of around 7% at rated power.

The measured waveforms of the inductor current  $I_L$  and the inductor voltage  $U_L$  of the balancing module closest to the load are shown in **Fig. 11** for the operation at an input voltage of  $V_{in} = 1.8$  kV and an output power of  $P_{load} = 20$  W. The small current spikes of the inductor current during the reversal of the inductor voltage is caused by intra-winding capacitances of the inductor.

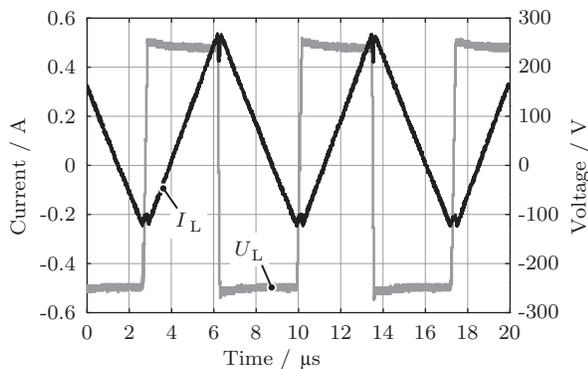


Fig. 11: Measured waveforms of the inductor current  $I_L$  and inductor voltage  $U_L$  of the balancing module closest to the load. The measurements were performed during the operation with an input voltage of  $V_{in} = 1.8$  kV and an output power of  $P_{load} = 20$  W.

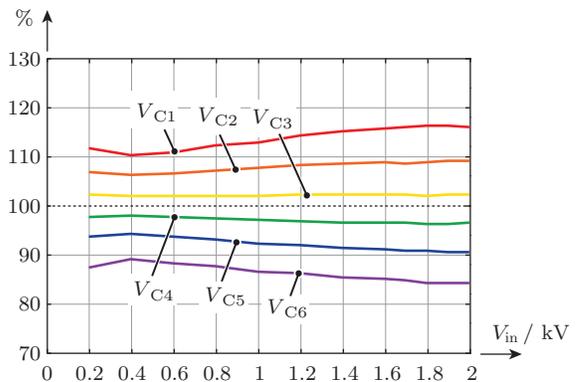


Fig. 12: Distribution of the input voltage  $V_{in}$  among the six capacitors of the RSTC converter prototype in percent of nominal value (i.e.  $V_{in}/6$ ). The capacitors are numbered with  $C_1$  being the uppermost and  $C_6$  the lowest capacitor of the stack. The load is connected in parallel to capacitor  $C_6$ .

The voltage distribution of the input voltage  $V_{in}$  among the six capacitors of the RSTC prototype is shown for no-load operation in **Fig. 12**. It is visible, that the input voltage is not equally divided among the capacitors. Instead, the voltage of the uppermost capacitor is up to around 17% higher than the expected value whereas the voltage of the lowest capacitor is around 16% lower than what is expected if perfect equalization was assumed. This can partly be explained by the fact, that the auxiliary power supply unit is connected in series to the lower capacitor of a balancing module. Thus, each time the auxiliary switch  $S_{aux}$  (cf. **Fig. 5**) is turned off, the voltage of the upper capacitor ( $C_1$ ) is equalized with the voltage of the series connection of the lower capacitor ( $C_2$ ) and the auxiliary capacitor ( $C_{aux}$ ). If a load is connected to the RSTC converter, this unequal voltage distribution tends to become slightly worse, as the superimposed load current causes voltage drops across the MOSFETs and the inductor in each balancing module which influence the voltage equalization. A solution would be to include a controller in each individual balancing module that adapts the duty-cycles of the switches to values slightly different from 50%. This can be implemented e.g. as a feedback loop with the voltage difference of the capacitors as input variable for a PI controller.

### VIII. CONCLUSION

A novel modular converter structure, named the Rainstick converter, has been presented. The converter allows for bidirectional power flow with a fixed voltage conversion ratio, which, due to its modular structure, can be easily adapted for high conversion ratios. Based on the current and power flow analysis, this converter structure can be classified as partial power converter as none of the employed modules needs to transfer the full amount load power. Furthermore, it is shown, that the basic concept can be modified with coupled inductors in order to isolate the converter output, if required. In addition to the converter structure, a self-controlled on-board power supply unit with a low part count has been presented. The proposed RSTC converter concept has been optimized for input voltages up to  $V_{in} = 2.4\text{ kV}$  and an output power up to  $P_{Load} = 30\text{ W}$ . The measurement results show that the converter can be operated over a wide range of input voltages beginning from  $V_{in} = 200\text{ V}$ . In future work, a prototype of the modified RSTC converter with isolated output is going to be optimized and experimentally verified.

### REFERENCES

[1] R. Giri, V. Choudhary, R. Ayyanar, and N. Mohan, "Common-Duty-Ratio Control of Input-Series Connected Modular DC-DC Converters with Active Input Voltage and Load-Current Sharing," *IEEE Trans. Ind. Appl.*, vol. 42, no. 4, pp. 1101–1111, 2006.

[2] W. Chen, K. Zhuang, and X. Ruan, "A Input-Series- and Output-Parallel-Connected Inverter System for High-Input-Voltage Applications," *IEEE Trans. Power Electron.*, vol. 24, no. 9, pp. 2127–2137, 2009.

[3] J.-W. Kim, J.-S. Yon, and B. H. Cho, "Modeling, Control, and Design of Input-Series-Output-Parallel-Connected Converter for High-Speed-Train Power System," *IEEE Trans. Ind. Electron.*, vol. 48, no. 3, pp. 536–544, 2001.

[4] M. D. Seeman and S. R. Sanders, "Analysis and Optimization of Switched-Capacitor DC–DC Converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, 2008.

[5] F. H. Khan and L. M. Tolbert, "A Multilevel Modular Capacitor Clamped DC-DC Converter," in *Proc. 41st IAS Annual Meeting Industry Applications Conf. Conf. Record of the 2006 IEEE*, vol. 2, pp. 966–973, 2006.

[6] N. H. Kutkut, "A Modular Nondissipative Current Diverter for EV Battery Charge Equalization," in *Proc. of Thirteenth Annual Applied Power Electronics Conf and Exposition (APEC)*, vol. 2, pp. 686–690, 1998.

[7] Schmidt and C. Siedle, "The Charge Equalizer - A New System to Extend Battery Lifetime in Photovoltaic Systems, UPS and Electric Vehicles," in *Proc. of 15th International Telecommunications Energy Conference (INTELEC)*, vol. 2, pp. 146–151, 1993.

[8] K. Sano and H. Fujita, "Voltage-Balancing Circuit Based on a Resonant Switched-Capacitor Converter for Multilevel Inverters," *IEEE Trans. Ind. Appl.*, vol. 44, no. 6, pp. 1768–1776, 2008.

[9] H. D. Torresan, D. G. Holmes, and I. Shraga, "Auxiliary Power Supplies for High Voltage Converter Systems," in *Proc. IEEE 35th Annual Power Electronics Specialists Conf. PESC 04*, vol. 1, pp. 645–651, 2004.

[10] F. Z. Peng, W. Qian, and D. Cao, "Recent Advances in Multilevel Converter/Inverter Topologies and Applications," in *Proc. Int. Power Electronics Conf. (IPEC)*, pp. 492–501, 2010.

[11] H. D. Torresan and D. G. Holmes, "A High Voltage Converter for Auxiliary Supply Applications using a Reduced Flying Capacitor Topology," in *Proc. IEEE 36th Power Electronics Specialists Conf. PESC '05*, pp. 1220–1226, 2005.

[12] F. Z. Peng, "A Generalized Multilevel Inverter Topology with Self Voltage Balancing," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 611–618, 2001.

[13] M. Kasper, D. Bortis, T. Friedli, and J. W. Kolar, "Classification and Comparative Evaluation of PV Panel Integrated DC-DC Converter Concepts," in *Power Electronics and Motion Control Conference (EPE/PEMC), 2012 15th International*, 2012.

[14] H. J. Bergveld, D. Büthker, C. Castello, T. Doorn, A. de Jong, R. van Otten, and K. de Waal, "Module-Level DC/DC Conversion for Photovoltaic Systems: The Delta-Conversion Concept," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 2005–2013, 2013.

[15] P. S. Shenoy, K. A. Kim, B. B. Johnson, and P. T. Krein, "Differential Power Processing for Increased Energy Production and Reliability of Photovoltaic Systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2968–2979, 2013.

[16] Kadri, J.-P. Gaubert, and G. Champenois, "Nondissipative String Current Diverter for Solving the Cascaded DC–DC Converter Connection Problem in Photovoltaic Power Generation System," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1249–1258, 2012.

[17] C. Schaef, K. Kesarwani, and J. T. Stauth, "A Coupled-Inductor Multi-Level Ladder Converter For Sub-Module PV Power Management," in *Proc. Twenty-Eighth Annual IEEE Applied Power Electronics Conf. and Exposition (APEC)*, pp. 732–737, 2013.

[18] J. T. Stauth, M. D. Seeman, and K. Kesarwani, "Resonant Switched-Capacitor Converters for Sub-module Distributed Photovoltaic Power Management," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1189–1198, 2013.

[19] P. S. Shenoy and P. T. Krein, "Differential Power Processing for DC Systems," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1795–1806, 2013.

[20] K. Kesarwani, C. Schaef, C. R. Sullivan, and J. T. Stauth, "A Multi-Level Ladder Converter Supporting Vertically Stacked Digital Voltage Domains," in *Proc. Twenty-Eighth Annual IEEE Applied Power Electronics Conf. and Exposition (APEC)*, pp. 429–434, 2013.

[21] J. W. Kolar, F. Krismer, Y. Lobsiger, J. Muhlethaler, T. Nussbaumer, and J. Minibock, "Extreme Efficiency Power Electronics," in *Proc. 7th Int Integrated Power Electronics Systems (CIPS) Conf*, pp. 1–22, 2012.