

# A Comprehensive Design Approach for a Three-Phase High-Frequency Single-Switch Discontinuous-Mode Boost Power Factor Corrector Based on Analytically Derived Normalized Converter Component Ratings

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**Abstract**—In this paper the peak, mean, and rms values of the component currents of a three-phase single-switch discontinuous inductor current mode boost rectifier are calculated analytically. The values are given in rated form in dependency on the output power and on the ratio of output voltage to the amplitude of the mains voltage. Furthermore, the influence of the voltage transfer ratio on the shape of the mains currents and on the power factor of the system is analyzed. The theoretical analysis is verified by digital simulation and a good consistency is achieved. Finally, the approach of the converter dimensioning based on the graphical representation of the calculation results is described and illustrated using a specific example. The correctness of the dimensioning is verified by measurements on a laboratory model.

## I. INTRODUCTION

**B**ASED on the standards (IEC 555-2) and recommendations (IEEE-519) aiming for a reduction of the effects on the mains and on the often given requirement for high-power density of power electronic systems, the development of self-commutated pulse rectifier systems with high operating frequency gains increasing importance [1]–[3].

In [4], which constitutes a major milestone of the development of unidirectional three-phase pulse rectifier systems, a single-switch discontinuous inductor current mode (DICM) boost rectifier (see Fig. 1) is introduced which is characterized by

- approximately sinusoidal input currents,
- resistive fundamental mains behavior, and
- controllability of the output voltage  $u_O$  (being higher than the peak value of the mains line-to-line voltage).

In connection with the very simple structure of the power circuit and the control circuit, this system is of special interest for a hardware realization in the area of electrical drives and for process technology power supplies, e.g., the application of

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this system for feeding the dc voltage link of a PWM inverter makes possible the following:

- the reduction of the filtering effort for limitation of the effects on the mains,
- the control of the dc link voltage to a constant value, independent of the mains voltage and, therefore,
- the maximum utilization of the rated power of the PWM inverter, and
- a matching to different mains voltage nominal values.

This can be achieved with a relatively small additional effort as compared to (uncontrolled) mains-commutated bridge rectification. The simple circuit structure of the proposed converter is paid for, however, by relatively high peak currents and voltages. This makes necessary an exact analysis of the stress on the components for defining the application region of the circuit.

Due to the single-phase equivalent circuit assumed in [4], the analysis of the operating behavior of the system given there is only valid with sufficient accuracy for high output voltage values as compared to the input voltage. Therefore, the guidelines given in [4] cannot be applied for dimensioning the system components and for the calculation of the system costs and the manufacturing costs for the application of the system in the European 380 V-mains (dc output voltage typically < 820 V).

An analytical calculation of the component stresses and of the characteristic system parameters being valid with high accuracy in the entire output voltage region is the topic of this paper. After a short description of the basic operating principle of the circuit (given in Section II), Section III discusses the analysis method which is applied in Section IV and Section V for the calculation of the component stresses in dependency on the output power and on the voltage transformation ratio of the converter. The calculation of the mains current shape and of the mains power factor is given in Section VI. In Section VII, the approach for dimensioning the system is described and illustrated by a numerical example. Finally, in Section VIII, the validity of the theoretical considerations is proven by measurements on a laboratory circuit of the converter which has been built up by using the results of Section VII.

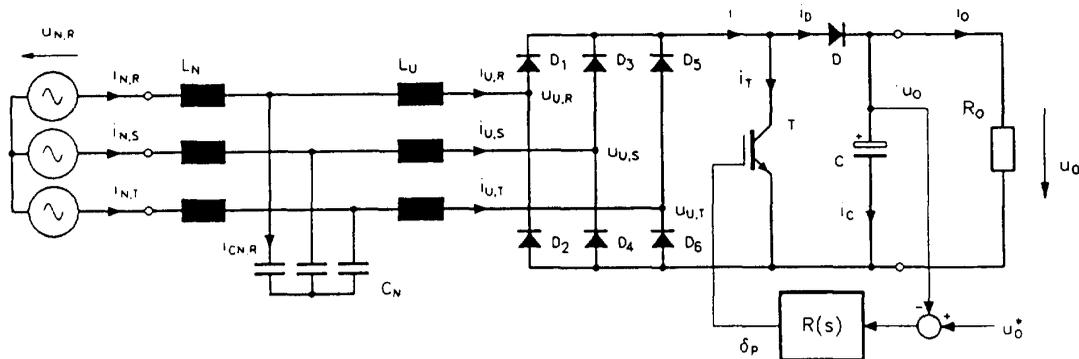


Fig. 1. Structure of the power circuit and the control circuit of a three-phase single-switch discontinuous inductor current mode boost rectifier; filtering of the high-frequency spectral components of the discontinuous input currents  $i_{U,(RST)}$  of the three-phase diode bridge by a mains filter  $L_N, C_N$  (shown simplified as single-stage filter). The feeding mains is replaced by a Y-connection of ideal voltage sources  $u_{N,(RST)}$ ; the control of the power transistor  $T$  is performed with constant pulse frequency  $f_P$  and with a relative on-time (duty-cycle)  $\delta_P$  being constant within the fundamental period and given by an output voltage controller.

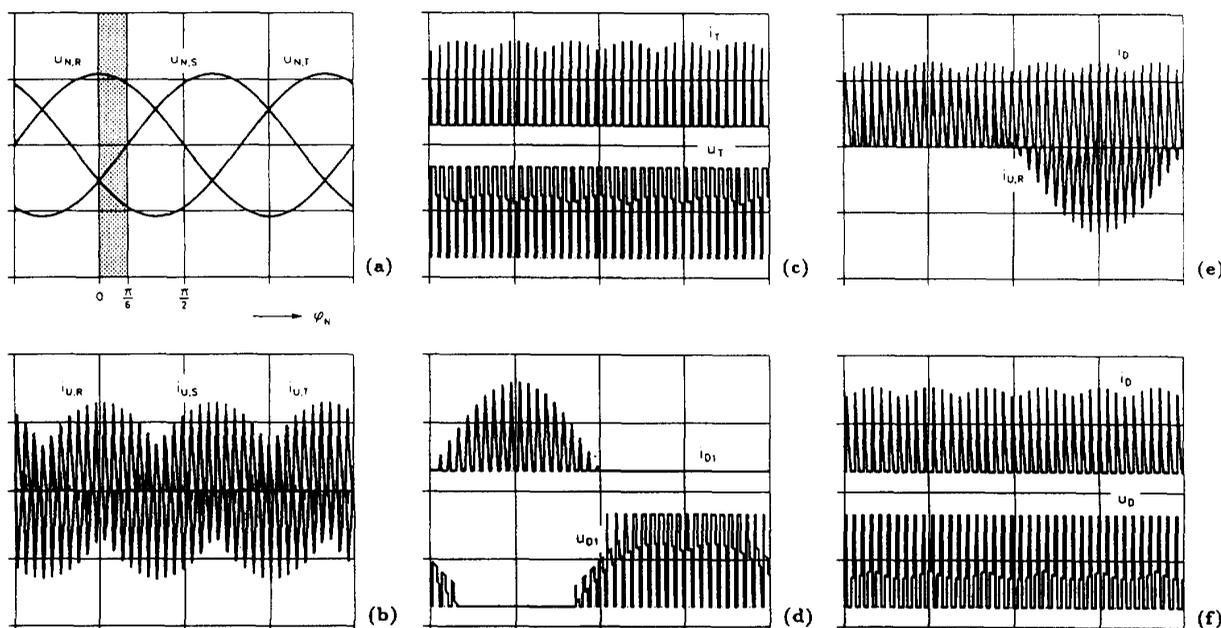


Fig. 2. Digital simulation of a three-phase discontinuous-mode boost rectifier (without mains filter) being operated with constant pulse frequency  $f_P$ . For a clear representation of the system behavior, a low pulse frequency has been assumed; on-time  $t_{\mu,1}$  of  $T$  constant within the fundamental period. (a) Mains phase voltages  $u_{N,(RST)}$  (the angle interval  $\varphi_N \in [0, \pi/6]$  which is considered for the analysis of the system behavior is marked by the dotted area). (b) Input phase currents  $i_{U,(RST)}$ . (c) Transistor current  $i_T$  and transistor voltage  $u_T$ . (d) Current  $i_{D1}$  and blocking voltage  $u_{D1}$  of diode  $D1$  of the three-phase bridge rectifier. (e) Output current  $i$  of the three-phase diode bridge and phase current  $i_{U,R}$ . (f) Diode current  $i_D$  feeding the dc link and diode blocking voltage  $u_D$ . Scaling: (a) 300 V/div; (b)–(f) 25 A/div or 600 V/div, respectively; parameters:  $U_{N,rms} = 230$  V,  $U_O = 820$  V,  $P_O = 5.5$  kW,  $L_U = 1.25$  mH,  $T_N = 20$  ms,  $f_P = 1/T_P = 1.95$  kHz.

## II. PRINCIPLE OF OPERATION

The control of the system shown in Fig. 1 is performed in the stationary case by a pulse frequency  $f_P$  and an on-time of the power transistor  $T$  being constant within the mains fundamental period [4]. A synchronization of  $f_P$  to the mains frequency  $f_N$  can be omitted for  $f_P \gg f_N$ . According to the low-pass characteristic of the mains filter  $L_N, C_N$  the mains voltage can be thought as lying directly at the filter output side. Regarding the mains phase voltages (being approximately constant within the pulse period) we will

assume  $u_{N,R} > 0, u_{N,T} \leq u_{N,S} \leq 0$  in the following. (This is valid within an interval of  $\pi/6$  of the fundamental period. See Fig. 2(a)). Under the assumption of a symmetric, purely sinusoidal three-phase mains voltage, the system behavior within the entire fundamental period is defined, therefore, due to the phase-symmetric converter structure. The dc output voltage  $u_O$  should be sufficiently higher than the peak value of the line-to-line mains voltage. (The output voltage has a lower limit of  $\sqrt{3}\hat{U}_N$ , according to the boost-converter structure).

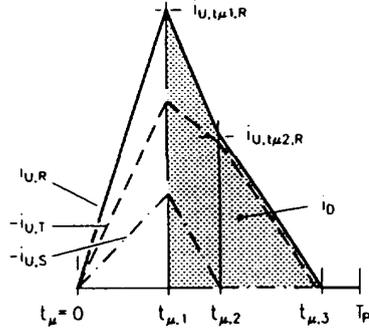


Fig. 3. Time shape of the converter input currents  $i_{U,(RST)}$  and of the output diode current  $i_D$  marked by the dotted area within a pulse period  $t_\mu \in [0, T_P]$  for  $u_{N,R} > 0$ ,  $u_{N,T} \leq u_{N,S} \leq 0$  (valid within the angle interval  $\varphi_N \in [0, \frac{\pi}{6}]$ ). (See Fig. 2(a)).  $t_\mu$  denotes a local time being counted within the pulse period;  $t_\mu = t_{\mu,1}$ : turn-off instant of  $T$ ; the position of the considered pulse interval within the fundamental period is set by the global time  $t$  or by the phase angle  $\varphi_N = \omega_N t$ ; parameter:  $M = 1.5$ .

Before turning on transistor  $T$ , we have  $i_{U,R} = i_{U,S} = i_{U,T} = 0$  (system operating in discontinuous mode).  $T$  is switched on at instant  $t_\mu = 0$ .  $t_\mu$  denotes a *local* time being counted within the considered pulse period. The rate of rise of the phase currents resulting due to the dc-side short circuit of the diode bridge is defined by the magnitudes of the phase voltages and by the inductances  $L_U$ . After turning off  $T$  in  $t_{\mu,1}$  as given by the output voltage controller, the demagnetization of the inductances  $L_U$  via diode  $D$  into the capacitor  $C$  which buffers the output voltage is performed. There, only within the first part  $t_\mu \in [t_{\mu,1}, t_{\mu,2}]$  of the demagnetization interval all three phases conduct current, however (see Fig. 3). At  $t_{\mu,2}$  that phase current becomes 0 which shows the smallest magnitude at  $t_\mu = t_{\mu,1}$  (in the case at hand,  $i_{U,S}$ ). The following second demagnetization interval (demagnetization of the two remaining phases  $R$  and  $T$  which conduct current of equal magnitude, but of opposite direction) is finished at  $t_\mu = t_{\mu,3}$ . Therefore, proper dimensioning has to guarantee  $t_{\mu,3} \leq T_P$  for discontinuous mode.

*Remark:* As the considerations given show clearly, the operating behavior of a three-phase diode bridge which defines the current shape within the demagnetization interval basically *cannot* be described by (decoupled) single-phase bridge circuits. The principle of operation is determined by the line-to-line voltages  $u_{N,RS}, u_{N,ST}, u_{N,TR}$  and not by the phase voltages  $u_{N,R}, u_{N,S}, u_{N,T}$  (which have a phase shift of  $\pi/6$  relative to the line-to-line voltages). If the operating behavior of the system is analyzed using a single-phase equivalent circuit, only the current shape within the turn-on interval of  $T$  is described correctly. Therefore, the calculations given in [4] can only be used as a coarse approximation for the determination of the component stresses in the case of a demagnetization period being short as compared to the on-time of  $T$  or, for  $U_O \gg \sqrt{3}\hat{U}_N$ , respectively.

Fig. 2 shows the current and voltage shapes of a three-phase boost rectifier operated with low pulse frequency, as determined by digital simulation. The discontinuous input phase currents  $i_{U,(RST)}$  follow envelopes which are proportional to the respective phase voltages  $u_{N,(RST)}$ . Via filtering of

the switching frequency spectral components using a mains filter  $L_N, C_N$  connected in series (see Fig. 1) we obtain an approximately resistive loading of the mains as related to the fundamental of the mains currents  $i_{N,(RST)}$ . One has to point out that, due to the on-time of  $T$  being constant within the fundamental period, the current control is performed directly by the mains voltage and not, e.g., by a sinusoidal variation of the duty ratio.

### III. SYSTEM ANALYSIS

#### A. Assumptions

For the analysis of the converter system the following simplifying assumptions are made:

- 1) purely sinusoidal, symmetric mains voltage system  $u_{N,i}$ ,  $i = R, S, T$ ,
- 2) ideal filtering of the pulse-frequency spectral components of the converter input currents  $i_{U,i}$  by a mains filter  $L_N, C_N$ ,
- 3) negligible ripple voltage across the filter capacitors  $C_N$ ,
- 4) amplitudes of the fundamental voltage drops across the filter inductances  $L_N$  are negligible as compared to the amplitude  $\hat{U}_N$  of the phase voltage of the supplying mains (the filter capacitor voltage is assumed as being impressed and set equal to the mains voltage),
- 5) on-time  $t_{\mu,1}$  is constant within the mains fundamental period  $T_N$ ,
- 6) constant output voltage  $U_O$ ,
- 7) constant load current  $I_O$ ,
- 8)  $f_P > 200f_N$  or  $T_P \ll T_N$  (mains phase voltages approximately constant within a pulse period), and
- 9) ideal system components (especially: neglectation of system losses, forward voltage drops, switching times of the power electronic devices, etc.)

The aim of these assumptions and idealizations (which correspond very well to the conditions given for a practical realization of the converter system) is to limit the description of the system behavior to the basic relationships. This shall lead to a compromise between exactness, applicability in a simple manner, and a wide possible validity of the derived dimensioning scheme. From an economical point of view we have to postulate a limitation of the relative error (as caused by the approximations) to values less than  $\pm 10\%$ . This is necessary because an uncertainty in the dimensioning has to be finally compensated by the application of circuit devices which can carry higher stresses in order to guarantee higher operational safety. This also results in a reduction of the utilization of the circuit components.

#### Remarks:

- ad 1): As already mentioned in Section II, we can (based on 1)) limit the analysis of the system behavior to a section of the mains period. This leads to a significant reduction of the calculation effort. For calculating the harmonics content of the mains current of the rectifier system, we possibly have to consider the low-frequency distortions of the voltage shape (see e.g., Fig. 2 in [6]) which occur when the converter is operated from the public

low-voltage mains. For the sake of brevity and clearness we have to omit a more detailed discussion here, however. We only want to point out that (due to the floating mains neutral point; see Fig. 1) voltage harmonics with the order  $\nu = 3n, n = 1, 2, 3$  (for symmetrical phase voltages) have no influence on the current formation.

- ad 2): In order to safely avoid an amplification of low-frequency spectral components of the rectifier input currents  $i_{U,i}$  due to resonances, we have to define the lowest resonance frequency of the mains filter (which, in general, has multiple stages) sufficiently high above the frequency range which is occupied by the low-frequency current harmonics. The low-frequency effects on the mains of the converter can, therefore, be calculated with sufficient accuracy under the assumption of ideal filtering.
- ad 3–6): Regarding the determination of stresses on the circuit devices (as being relevant to the dimensioning) we have to point out that an analytically closed solution of the characteristic parameters is basically linked to the possibility of neglecting the coupling of the state variables and of the coupling of the state variables to the control quantities of the converter system. In our case the feedback of the inverter current to the output voltage of the mains filter (influencing the formation of the input current) is neglected by 3) and 4). Equation (5) gives the neglect of the feedback of the output voltage via the output voltage controller to the control input of the converter system. Furthermore, 6) leads to neglecting the influence of an output voltage deviation (resulting due to low-frequency harmonics of the mains current) to the input current shape. Only this decoupling makes possible an explicit mathematical description or a direct calculation of the device currents without considering a specific dimensioning. (This concerns, e.g., the damping function and the output impedance of the input filter, the output capacitance value, and the design of the output voltage controller.)
- ad 7): Due to the assumption of a constant load current we only consider the contribution of the rectifier system for dimensioning of the stress on the output capacitor. A simple calculation of the capacitor current for the general load case (e.g., for pulsating load currents with variable frequency) is basically not possible. In this case, the output capacitor has to be dimensioned based on a worst-case estimate (cf. Section V, (26)) or based on a digital simulation or on a direct measurement on a laboratory model.
- ad 8): The assumption of a pulse frequency being sufficiently high compared to the mains frequency is of special importance to a simple calculation of the stresses on the circuit devices. The sinusoidal phase voltages  $u_{N,R}, u_{N,S}, u_{N,T}$  with mains frequency can be replaced for  $f_P > 200f_N$  with

a sufficient accuracy within a pulse period by constant values. The shapes of the device currents can be approximated by straight lines and expressed in analytical form directly, i.e., without the solving of transcendental equations. As shown in the following section, this assumption is also the basis for the analytically closed calculation of the average and rms values of the device currents.

- ad 9): A substantial simplification of the mathematical description is obtained by neglecting the system losses. Basically, a direct consideration of the loss contributions of the devices for the dimensioning is not possible in a sensible way because the device stresses and the (exact) device characteristics are not known yet. Based on a value of the efficiency  $\eta$  gained from experience or on an estimate of  $\eta$  we can, therefore, in general, determine the stress on the devices by using a dimensioning scheme valid for  $\eta = 1$  also for  $P = P_O/\eta$ . The efficiency  $\eta$  resulting from calculating the sum of the several loss contributions will be set as new value of  $\eta$ . Then this process is (iteratively) repeated until a sufficient consistency between the assumed and the calculated value is obtained. Alternatively, one can also determine a first approximation of the stresses on the devices for  $\eta < 1$  by dimensioning based on the output power  $P_O$  of the converter and by increasing the calculated stresses on the devices by a factor  $1/\eta$  (cf. Section III in [7]). Dependent on the distribution of the losses in the circuit components we obtain (due to the power flow which decreases between input and output of the circuit) partly too high device stresses and loss contributions. However, considering a typical efficiency lying in the vicinity of  $\eta \approx 0.95$  for the rectifier system, we can omit a more detailed discussion in our case.

Besides the simplified analytical calculation as discussed in this paper, we also can apply digital simulation for analyzing the system behavior and the device stresses. However, in this case the validity of the considerations remains limited basically to a specific application and to specific device values and device characteristics. Therefore, the results do not allow a direct conclusion regarding the dependency of the device stresses on the operating parameters (input voltage, output voltage, output power, pulse frequency, etc.) Therefore, in engineering practice usually an analytical approximation calculation is preferred.

### B. Analysis Method

As a basis for dimensioning of the active and passive components we have to calculate the mean and rms values of the device currents  $i_i$  besides their peak values. There, the determination of the averaged (related to the fundamental period) characteristic parameters of the currents has to be performed via the summation of the contributions of the single pulse intervals and is not possible in analytically closed form, therefore.

As, e.g., shown in [8] and [7], one can replace the summation with sufficient accuracy by an integration

$$I_{i,\text{avg}} = \frac{6}{\pi} \int_0^{\frac{\pi}{6}} \left\{ \frac{1}{T_P} \int_0^{T_P} i_i(\varphi_N, t_\mu) dt_\mu \right\} d\varphi_N \quad (1)$$

$$I_{i,\text{rms}}^2 = \frac{6}{\pi} \int_0^{\frac{\pi}{6}} \left\{ \frac{1}{T_P} \int_0^{T_P} i_i^2(\varphi_N, t_\mu) dt_\mu \right\} d\varphi_N \quad (2)$$

if the pulse frequency is high compared to the mains frequency. With this, the stresses on the devices can be directly calculated *analytically*;  $\varphi_N$  defines the position of a pulse interval within the fundamental period. The relation to the (global) time  $t$  is given by

$$\varphi_N = \omega_N t. \quad (3)$$

As explained in Section II, the consideration of the symmetry relations of a three-phase system allows the limitation of the integration interval to a  $\pi/6$ -wide section of the fundamental period (for  $i_i = i_T$  and  $i_i = i_D$ ).

With this, the characteristic values of the currents can be calculated directly and analytically. One has to point out that contrary to a numerical calculation (whose validity always is restricted to discrete parameter values) the analytical calculation allows an immediate statement concerning the influence of the system parameters (input voltage, output voltage, output power, pulse frequency, etc.) on the dimensioning of the converter.

In connection with a minimization of size and weight of the magnetic components we have to aim in a practical realization, by all means, at a pulse frequency of the converter being much higher than the mains frequency. Due to the discontinuous mode a stress on the transistor  $T$  by reverse recovery currents of the output diode  $D$  is avoided; in this case a pulse frequency  $f_p \geq 500 f_N$  seems to be obtainable. As a check of the calculation by digital simulation (based on the assumptions made in Section III-A) shows, the derivations of the analytically calculated approximations (1), (2) from the exact (simulated) values remain below 2% there for  $f_p \geq 200 f_N$ . Therefore, the calculation results given in Sections IV, V, and VI can be used directly as basis for dimensioning of the components.

### C. Normalization

For a simplification and a wide applicability of the relations derived in this paper, the results are represented in rated form

$$\begin{aligned} t_{\mu,i,r} &= \frac{1}{T_P} t_{\mu,i}, & u_{i,r} &= \frac{1}{U_O} u_i \\ i_{i,r} &= \frac{1}{I_n} i_i, & p_{i,r} &= \frac{1}{P_n} p_i. \end{aligned} \quad (4)$$

Into the base quantities of the normalization

$$I_n = \frac{2}{3} U_O \frac{T_P}{L_U} \quad P_n = \frac{2}{3} U_O^2 \frac{T_P}{L_U} \quad (5)$$

the parameters are included which directly influence the system behavior, namely  $T_P$ ,  $L_U$ , and  $U_O$ . The normalization is

performed related to the dc output voltage, because with this the normalization basis remains unchanged for varying mains voltage conditions (caused by the tolerance band of the mains voltage or different nominal levels of the mains voltage).

### D. Definitions

For characterizing the voltage transfer ratio of the system the ratio between dc output voltage to the peak value of the mains line-to-line voltage is applied

$$M = \frac{U_O}{\sqrt{3}\hat{U}_N} \quad M \geq 1. \quad (6)$$

Due to the boost converter structure the output voltage range has a lower limit given by the peak value  $\sqrt{3}\hat{U}_N$  of the mains line-to-line voltage. For the relative on-time of the transistor  $T$  (duty cycle) we define

$$\delta_P = \frac{t_{\mu,1}}{T_P}. \quad (7)$$

The sum of the on-time  $t_{\mu,1}$  of the power transistor and the *maximum* duration  $T$  of the demagnetization interval (cf. (14)), defining the transition into the continuous mode, is determined via

$$\delta = \frac{t_{\mu,3,\text{max}}}{T_P}. \quad (8)$$

For discontinuous mode we have to guarantee  $\delta \leq 1$ .

## IV. BASIC EQUATIONS

According to (1), (2) the calculation of the current stresses on the components has to be based on the current shape within a pulse period  $t_\mu \in [0, T_P]$ . As can be seen immediately from the description of the operating behavior in Section II and as illustrated in Fig. 3 using the example of the output diode current, the local shape of all device currents can be derived directly from the shape of the converter input currents  $i_{U,(RST)}$ . Furthermore, the mathematical description of the current shape also yields a statement about that maximum on-time of  $T$  or about the maximum output power for which the limit to the discontinuous mode is reached.

The calculation of the input currents is performed for time-constant pulse frequency  $f_P$  and for a local on-time  $t_{\mu,1}$  of  $T$  being constant over the fundamental period. Furthermore, exclusively the discontinuous mode is assumed.

*Remark:* For a partly discontinuous and continuous system operation, a simple analytical formulation is not possible. Due to the occurrence of low-frequency mains current harmonics and a phase shift between mains current and mains voltage fundamentals [9] such modes of operation have no practical significance, however.

As already described in Section II, for the assumption of a symmetric mains voltage system

$$\begin{aligned} u_{N,R} &= \hat{U}_N \cos(\varphi_N) \\ u_{N,S} &= \hat{U}_N \cos\left(\varphi_N - \frac{2\pi}{3}\right) \\ u_{N,T} &= \hat{U}_N \cos\left(\varphi_N + \frac{2\pi}{3}\right) \end{aligned} \quad (9)$$

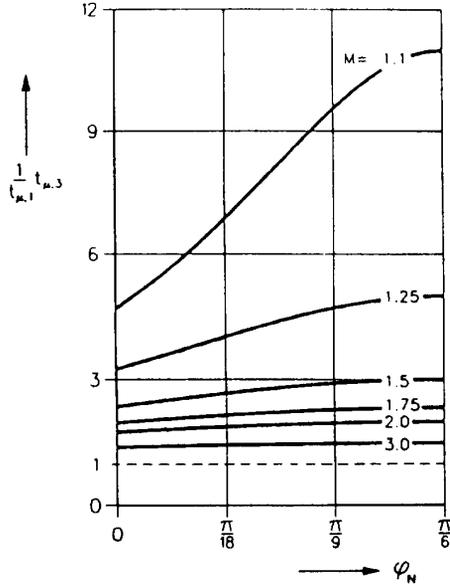


Fig. 4. Local on-time  $t_{\mu,3}$  (see Fig. 3) of the input diode bridge related to the turn-on time  $t_{\mu,1}$  of the power transistor  $T$  in dependency on the position  $\varphi_N$  of the considered pulse interval within the fundamental period (cf. (13)); parameter: voltage transfer ratio  $M$ .

the calculation can be limited to the interval  $\varphi_N \in [0, \frac{\pi}{6}]$  (see Fig. 2). Due to the assumption of phase voltages being constant within a pulse period the phase currents show linear shapes in sections (see Fig. 3); for the current values and time intervals ( $\Delta t_{\mu,ji} = t_{\mu,j} - t_{\mu,i}$ ) defining the time behavior, there follows after a short calculation:

$$\begin{aligned} t_{\mu} &= t_{\mu,1}: i_{U,t\mu 1,R,r} = \frac{\sqrt{3}}{2} \delta_P M^{-1} \cos(\varphi_N) \\ i_{U,t\mu 1,S,r} &= \frac{\sqrt{3}}{2} \delta_P M^{-1} \cos\left(\varphi_N - \frac{2\pi}{3}\right) \\ i_{U,t\mu 1,T,r} &= \frac{\sqrt{3}}{2} \delta_P M^{-1} \cos\left(\varphi_N + \frac{2\pi}{3}\right) \end{aligned} \quad (10)$$

$$\begin{aligned} t_{\mu} &= t_{\mu,2}: i_{U,t\mu 2,R,r} = \frac{3}{2} \delta_P M^{-1} \frac{\sin(\varphi_N)}{1 + \sqrt{3} M^{-1} \sin(\varphi_N - \frac{\pi}{6})} \\ i_{U,t\mu 2,S,r} &= 0 \\ i_{U,t\mu 2,T,r} &= -i_{U,t\mu 2,R,r} \end{aligned} \quad (11)$$

$$\Delta t_{\mu,21,r} = \sqrt{3} \delta_P M^{-1} \frac{\sin(\frac{\pi}{6} - \varphi_N)}{1 + \sqrt{3} M^{-1} \sin(\varphi_N - \frac{\pi}{6})} \quad (12)$$

$$\Delta t_{\mu,32,r} = 2 \delta_P M^{-1} \frac{\sin(\varphi_N)}{(1 + \sqrt{3} M^{-1} \sin(\varphi_N - \frac{\pi}{6}))(1 - M^{-1} \cos(\varphi_N - \frac{\pi}{6}))}$$

Regarding a more detailed derivation of the relations given here, cf. [10]. For the dependency of the local current flow interval of the input bridge rectifier on the position  $\varphi_N$  of the pulse interval and on the voltage transfer ratio  $M$  there follows with (12):

$$t_{\mu,3} = t_{\mu,1} \frac{1}{1 - M^{-1} \cos(\varphi_N - \frac{\pi}{6})} \quad (13)$$

(see Fig. 4). Therefore, the maximum duration of the current flow interval determining the transition into the continuous mode is given by

$$t_{\mu,3,\max} = t_{\mu,3}|_{\varphi_N = \frac{\pi}{6}} = t_{\mu,1} \frac{1}{1 - M^{-1}}. \quad (14)$$

Due to the constant on-time  $t_{\mu,1}$  the maximum conduction interval is determined by the maximum demagnetization interval. One has to point out that the maximum value occurs at the maxima of the line-to-line mains voltages (for  $\varphi_N \in [0, \frac{\pi}{6}]$  we have the maximum of the line-to-line mains voltage  $u_{N,RT} = u_{N,R} - u_{N,T}$  at  $\varphi_N = \frac{\pi}{6}$ ) and not at the maxima of the input currents (for  $\varphi_N \in [0, \frac{\pi}{6}]$  the maximum mains current occurs for  $\varphi_N = 0$  in phase  $R$ ). Under consideration of (7) and (8) we have

$$\delta = \delta_P \frac{M}{M-1}. \quad (15)$$

For  $\delta = 1$  that duty ratio is defined by (15) for a given  $M$  for which the limit to the discontinuous mode is reached. Regarding a system dimensioning one has to raise the question now to which output power this duty ratio corresponds. Due to the constant output voltage the output power is determined directly by the (global) mean value  $I_{D,\text{avg}}$  of the diode current  $i_D$ . This can be seen clearly from the expression

$$P_{O,r} \equiv I_{D,\text{avg},r}. \quad (16)$$

Based on (1), one can calculate the output power directly in analytically closed form, therefore. After an extensive calculation there follows:

$$\begin{aligned} P_{O,r} &= \frac{1}{2} \delta_P^2 \left[ \frac{3}{\pi} \left( \frac{M}{\sqrt{M^2-3}} \left( \tan^{-1} \frac{\sqrt{3}}{\sqrt{M^2-3}} \right. \right. \right. \\ &\quad \left. \left. \left. + \tan^{-1} \frac{\sqrt{3}-1}{\sqrt{3}+1} \frac{M-\sqrt{3}}{\sqrt{M^2-3}} \right) + \frac{3M}{\sqrt{M^2-1}} \tan^{-1} \right. \right. \\ &\quad \left. \left. \times \frac{\sqrt{3}-1}{\sqrt{3}+1} \sqrt{\frac{M+1}{M-1}} - \frac{\sqrt{3}}{2} M^{-1} \right) - 1 \right] \end{aligned} \quad (17)$$

(cf. Fig. 5). By combining (15) and (17) one can now determine the limit of the discontinuous mode in relation to the converter output power. The resulting relation is shown in Fig. 6. The power which can be supplied for  $\delta = 1$  is essentially determined by the value of the voltage transfer ratio. For an input voltage being small as compared to the output voltage (small values of  $M^{-1}$ ) the magnetization interval ( $t_{\mu} \in [0, t_{\mu,1}]$ ) is pronounced in the current shape; for high input voltage ( $M^{-1} \approx 1$ ) due to the low voltage difference the demagnetization interval ( $t_{\mu} \in [t_{\mu,1}, t_{\mu,3}]$ ) is very pronounced. In both cases only relatively low current values  $i_{i,t\mu 1}$  and low output power values are obtained. An optimum utilization of the pulse period and, therefore, high output power is given only for  $M^{-1} \approx \frac{2}{3}$  or  $\sqrt{3} \hat{U}_N \approx \frac{2}{3} U_O$ , respectively.

For the calculation of the fundamental of the mains current which defines the output power of the converter we can use the balance of power

$$P_O = U_O I_O = U_O I_{D,\text{avg}} = \frac{3}{2} \hat{U}_N \hat{I}_{N,(1)} = P_N. \quad (18)$$

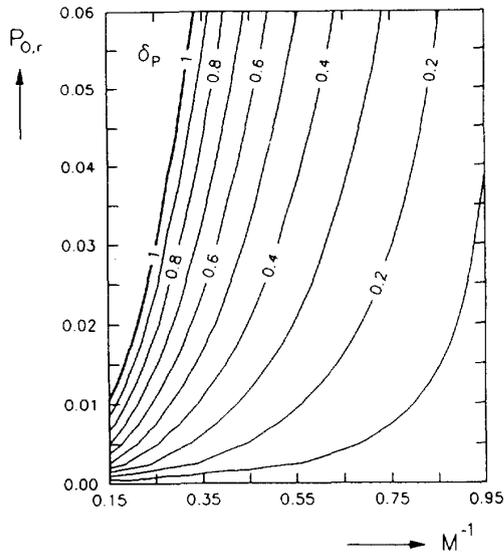


Fig. 5. Dependency of the rated output power  $P_{O,r}$  on the duty cycle  $\delta_P$  of  $T$  and on the voltage transfer ratio  $M$  (cf. (17)).

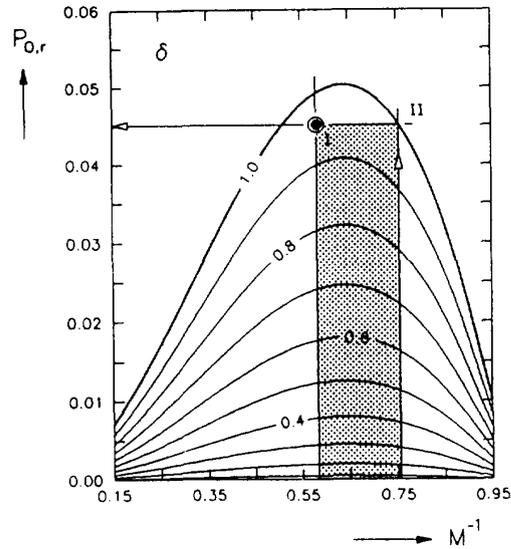


Fig. 6. Dependency of  $P_{O,r}$  on the rated maximum conduction interval  $\delta$  of the diode bridge and on  $M$ ;  $\delta = 1$  defines the limit between continuous and discontinuous mode; validity of the representation limited to discontinuous mode ( $\delta \leq 1$ ) as for all other results given in this paper. The operating region resulting for the dimensioning example given in Section VII-B is marked.

There, loss-free operation is assumed (cf. Section III-A). With Section III-C and with (6) and (16) there follows:

$$\hat{I}_{N,(1),r} = \frac{2}{\sqrt{3}} M P_{O,r}. \quad (19)$$

## V. COMPONENT RATINGS

For a dimensioning of the system especially the current and voltage stresses on the power electronic devices as well as on the passive components are of interest. The same items are of interest for an assessment of the application region of the system.

### A. Blocking Voltage Stress on the Power Semiconductors

As Fig. 2 shows clearly, the ideal maximum blocking voltage stress on all power electronic devices is defined by the output voltage. We have

$$U_{T,\max} = U_{D,\max} = U_{Di,\max} = U_O. \quad (20)$$

### B. Maximum Values, Average Values, and RMS Values of the Device Currents

The (global) mean and rms values of the device currents are calculated based on Section IV by using the defining equations (1), (2), e.g., there follows for the characteristic parameters of the transistor current:

$$I_{T,\text{avg},r} = \frac{3\sqrt{3}}{4\pi} M^{-1} \delta_P^2, \quad (21)$$

$$I_{T,\text{rms},r}^2 = \left( \frac{1}{8} + \frac{3\sqrt{3}}{16\pi} \right) M^{-2} \delta_P^3. \quad (22)$$

For  $t_\mu \leq t_{\mu,1}$  and the angle interval  $\varphi_N \in [0, \frac{\pi}{6}]$  the local shape of the transistor current  $i_T$  is identical to the shape of  $i_{U,r}$ . The global maximum value within the fundamental period therefore is given via (10)

$$I_{T,\max,r} = \frac{\sqrt{3}}{2} M^{-1} \delta_P. \quad (23)$$

The characteristic quantities given can now (with the application of (17)) again be brought into a direct relation to the output power (as shown in Section IV for the example of the quantity  $\delta$ ; see Fig. 6). The resulting dependencies are shown in Fig. 7(a)–(c). There, the limit of the discontinuous mode is shown as a characteristic curve  $\delta = 1$ . The characteristic transistor current quantities being related to a given output power are thereby defined in the entire input and output voltage region (being of interest for a practical realization). Therefore, a fast and simple dimensioning is made possible.

For the sake of brevity, the further discussion is limited to a few basic issues. A description of the relatively involved (analytical) calculation of further component stresses being relevant for dimensioning is omitted. The calculated rms values of the device currents are compiled in Fig. 7(d)–(h). The characteristic values of the currents not shown in Fig. 7 can be determined easily by the relations given in the following.

The maximum current stress on the input inductances  $L_U$ , on the diodes of the three-phase bridge and on the output diode is given (according to the operating principle of the system) by the global maximum value of the transistor current

$$I_{T,\max,r} = I_{D,\max,r} = I_{U,(RST),\max,r} = I_{Di,\max,r}. \quad (24)$$

Therefore, it can be directly read from Fig. 7(c).

Due to the constant output current and due to the average value of the current through the output capacitor being zero one can use the relation

$$I_{C,\text{rms},r}^2 = I_{D,\text{rms},r}^2 - I_{O,r}^2 \quad (25)$$

for determining  $I_{C,\text{rms}}$  (see Fig. 7(d) and (18)). For pulsating (not time constant) output current  $i_O$  we have to use the worst

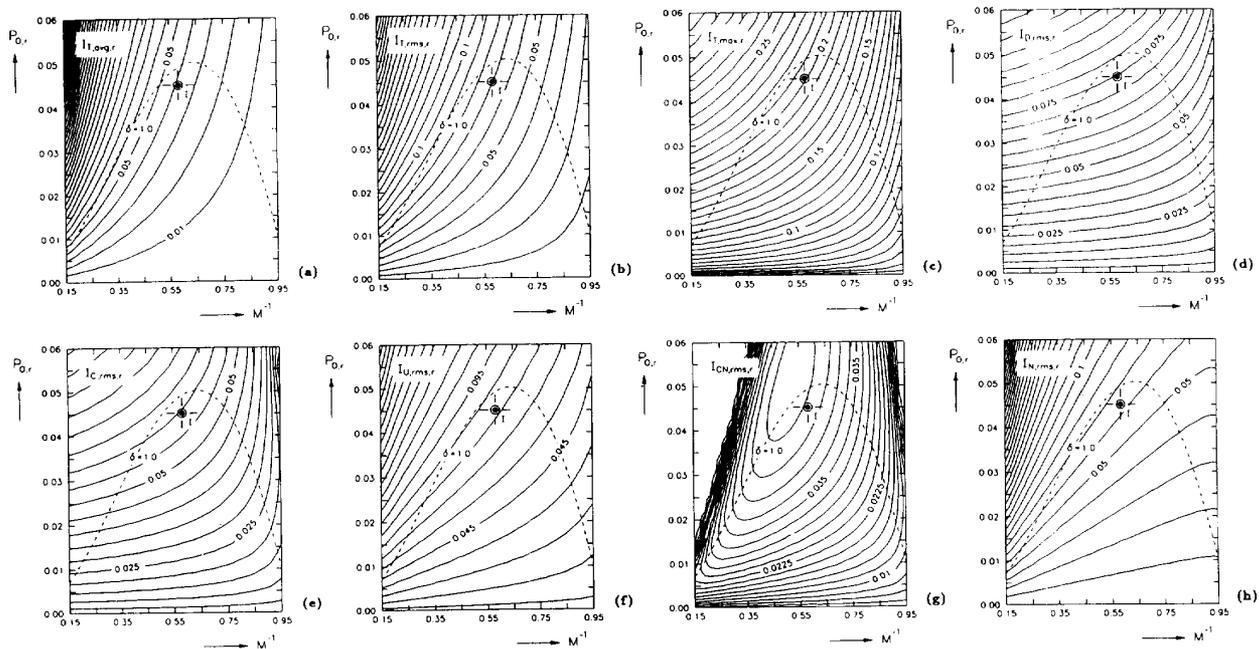


Fig. 7. Dependencies of the rated characteristic current quantities characterizing the component stresses on the rated output power  $P_{O,r}$  and on the voltage transfer ratio  $M$ ; the validity of the diagrams is limited to the discontinuous mode (the limit between continuous and discontinuous mode is shown as characteristic curve  $\delta = 1$  (see Fig. 6)). (a) Average value of the transistor current. (b) RMS value of the transistor current. (c) Peak value of the transistor current. (d) RMS value of the output diode current. (e) RMS value of the output capacitor current. (f) RMS value of the converter input current. (g) RMS value of the mains filter capacitor current. (h) RMS value of the mains current. The operating point  $M_{\max} = 1.71$ ,  $P_{O,r,\delta \leq 1} = 0.045$  (see I in Fig. 6), which is used in Section VII-B for the design example for determining the maximum component stress, is marked.

case estimate

$$I_{C,rms,max,r} = I_{D,ac,rms,r} + I_{O,ac,rms,r} \quad (26)$$

(cf. Appendix or [11]). An estimate of the noise voltage level (with switching frequency) on the output side can be given via the global maximum value

$$I_{C,max,r} = I_{D,max,r} - I_{O,r} \quad (27)$$

and by the ESR of the output capacitor.

Based on the assumption of ideal filtering of the switching frequency spectral components of the converter input currents  $i_{U,(RST)}$  one can set for the ac side converter quantities (in analogy to (25))

$$I_{CN,rms,r}^2 = I_{U,rms,r}^2 - I_{N,rms,r}^2 \quad (28)$$

For multi-stage filtering of the converter currents,  $C_N$  denotes the output capacitor of the mains filter. The low-frequency component of the capacitor current

$$I_{CN,rms,(1)} = \omega_N C_N U_{N,rms} \quad (29)$$

(not being represented in (28)) can be neglected in most cases, as compared to the switching frequency component stress. For the global maximum value of the capacitor current there follows approximately

$$I_{CN,max,r} = I_{U,(RST),max,r} - \hat{I}_{N,(1),r} \quad (30)$$

*Remark:* As discussed in connection with (28), the rms value  $I_{CN,rms}$  is generated by the harmonics (with switching frequency) of an input phase current  $i_{U,i}$ . Therefore,  $I_{CN,rms}$  makes possible (besides the determination of the current stress on the mains filter capacitor) also an estimate of that part of the resistive losses in a phase inductance  $L_U$  which is caused by the current harmonics. There, due to the skin and proximity effects, the dc current resistance of the winding has to be increased by a factor given by the switching frequency and the cross section of the wire (or penetration depth, respectively). For calculating the overall resistive losses one has to add to this loss contribution that loss which is caused by the low-frequency harmonics of  $i_{U,i}$ , which is described via  $I_{N,rms}$  and which is calculated based on the dc resistance [12].

For the characteristic quantities of the diodes  $D_{i=1...6}$  of the three-phase bridge we have (as can be seen directly from the operating principle of the circuit)

$$I_{Di,avg,r} = \frac{1}{3}(I_{T,avg,r} + I_{D,avg,r}), \quad (31)$$

$$I_{Di,rms,r} = \frac{1}{\sqrt{2}} I_{U,rms,r} \quad (32)$$

### C. Conduction and Switching Losses of the Power Semiconductors

The calculation of the conduction losses of the power semiconductors can be performed advantageously by approximating the on-state voltage drop by

$$u_{F,i} = \bar{U}_{F,i} + r_{F,i} i_i \quad (33)$$

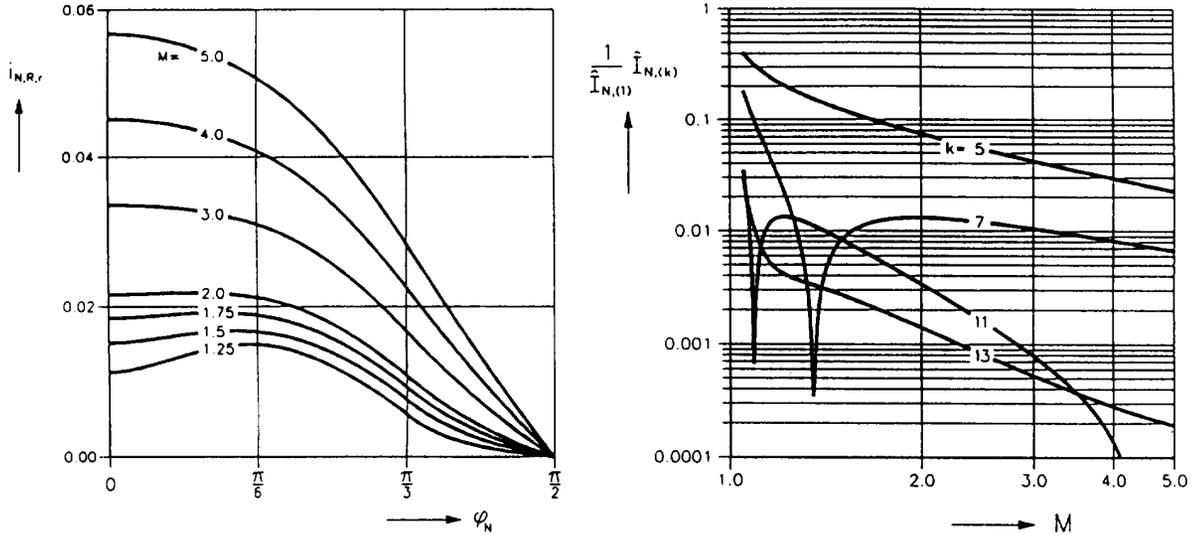


Fig. 8. Representation of the analytically calculated time shapes (shown for a quarter fundamental period) and of the low-frequency mains current harmonics  $\hat{I}_{N,(k)}$  (related to the fundamental  $\hat{I}_{N,(1)}$ ) in dependency on the voltage transfer ratio  $M$ ; constant pulse frequency  $f_P$  and constant on-time  $t_{\mu,1}$  of the power transistor  $T$  within the fundamental period; parameter:  $P_{O,r} = 0.01$ .

(cf., [8]). Therefore, for the conduction losses there follows in general:

$$P_{F,i} = U_{F,i} I_{i,avg} + r_{F,i} I_{i,rms}^2. \quad (34)$$

Concerning the switching losses especially the stress on the power transistor is of importance for dimensioning. As shown in the following, this stress can be also calculated by a simple analytical procedure.

Due to the discontinuous mode of the converter the turn-on losses can be neglected as compared to the turn-off losses. Based on a linear relation (as first approximation) of the power loss occurring during the turn-off process

$$w_{P,T} = k_T i_T \quad (35)$$

a local switching power loss

$$p_{P,T} = \frac{1}{T_P} w_{P,T} \quad (36)$$

is defined by averaging over a pulse period. Averaging of  $p_{P,T}$  within the interval  $\varphi \in [0, \frac{\pi}{6}]$  leads to the switching losses being proportional to the global peak value of the transistor current

$$P_{P,T} = \frac{2}{\pi} \frac{k_T U_O}{L_U} I_{T,max,r}. \quad (37)$$

## VI. MAINS CURRENT

For the calculation of the fundamental component and the low-frequency harmonic components of the mains currents (remaining after filtering of the switching frequency components of the diode bridge input currents) local averaging can be used [10]. Based on symmetry considerations one can extend the description of the phase currents within the fundamental section  $\varphi_N \in [0, \frac{\pi}{6}]$  to the interval  $\varphi_N \in [0, \frac{\pi}{2}]$ . For the shape of the mains current there follows (phase R):

Interval  $[0, \frac{\pi}{6}]$ :

$$i_{N,R,r}(\varphi_N) = \frac{\sqrt{3}}{4} \delta_P^2 M^{-1} \times \frac{\cos(\varphi_N) - 2M^{-1} \cos(\varphi_N) \cos(\varphi_N + \frac{\pi}{6}) + \frac{\sqrt{3}}{2} M^{-1}}{(1 + \sqrt{3} M^{-1} \sin(\varphi_N - \frac{\pi}{6})) (1 - M^{-1} \cos(\varphi_N - \frac{\pi}{6}))}. \quad (38)$$

Interval  $[\frac{\pi}{6}, \frac{\pi}{3}]$ :

$$i_{N,R,r}(\varphi_N) = \frac{\sqrt{3}}{4} \delta_P^2 M^{-1} \times \frac{\cos(\varphi_N) + \frac{1}{2} M^{-1} \cos(2\varphi_N + \frac{\pi}{6})}{(1 - \sqrt{3} M^{-1} \sin(\varphi_N - \frac{\pi}{6})) (1 - M^{-1} \cos(\varphi_N - \frac{\pi}{6}))}. \quad (39)$$

Interval  $[\frac{\pi}{3}, \frac{\pi}{2}]$ :

$$i_{N,R,r}(\varphi_N) = \frac{\sqrt{3}}{4} \delta_P^2 M^{-1} \frac{\cos(\varphi_N)}{1 - \sqrt{3} M^{-1} \cos(\varphi_N)}. \quad (40)$$

Based on the analytical description given here one can now directly calculate the mains current harmonics which are of interest for an assessment of the effects on the mains (see Fig. 8). For calculating the power factor we have to apply

$$\lambda = \frac{I_{N,(1),rms}}{I_{N,rms}} \quad (41)$$

due to the purely sinusoidal, symmetric mains voltage system. There, the current fundamental is assumed as being in phase with the mains voltage. The phase shift between mains voltage and mains current caused by the input filter is not considered due to the assumed essential higher cut-off frequency of the filter as compared to the mains frequency.

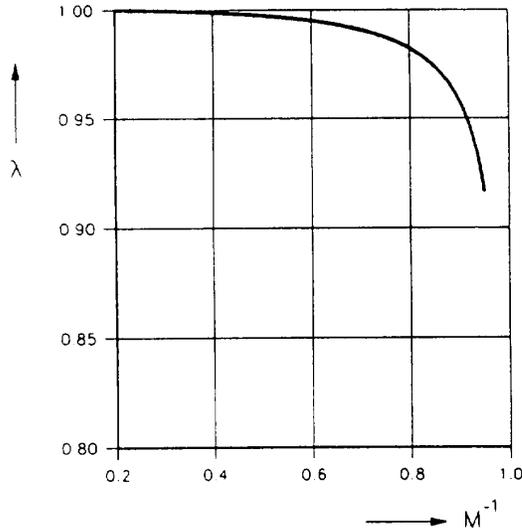


Fig. 9. Mains power factor (cf. (41)) dependency on the voltage transfer ratio  $M$ .

As Fig. 9 shows, the effects on the mains as caused by the converter are influenced essentially in the region  $M < 1.2$  by the voltage transfer ratio. For  $M < 1.09$  the power factor falls to values  $\lambda < 0.95$ , due to the occurrence of low-frequency harmonics in the mains current spectrum. A power factor  $> 0.98$  ( $\hat{I}_{N,(5)} < 0.2\hat{I}_{N,(1)}$ ) is obtained only for  $U_O > 3U_{N,rms}$  ( $M > 1.22$ ). For operating the converter from the European low-voltage mains this means a relatively high output voltage ( $U_O > 760$  V, where the mains voltage tolerance band is considered), considering today's typical maximum allowed blocking voltage (about 1200 V) of high-voltage power transistors.

## VII. CONVERTER DESIGN

As shown in the following, the calculation results being represented in rated form allow a direct and simple dimensioning of the system components.

### A. Design Procedure

The main point of the dimensioning is the calculation of that value of the inductance  $L_U$  which guarantees the discontinuous mode in the entire input voltage and output power region for maximum utilization of the pulse interval (and, therefore, of the rated power of the converter). The maximum output power  $P_{O,max}$ , the controlled output voltage  $U_O$  and the input voltage region  $\hat{U}_N \in [\hat{U}_{N,min}, \hat{U}_{N,max}]$  may be given.

The global maximum value of the rated conduction interval  $\delta$  (which has to be considered for dimensioning) is set, as explained in Section IV, by the voltage transfer ratio and by the rated output power. Using the dependency (shown graphically in Fig. 6) one can now determine that power value

$$P_{O,r,\delta \leq 1} = \min\{P_{O,r}(M^{-1}, \delta)\}_{M^{-1} \in [M_{min}^{-1}, M_{max}^{-1}], \delta=1} \quad (42)$$

for which the system operates in the entire input voltage region in the discontinuous mode ( $\delta \leq 1$ ). By inversion of the normalization equation of the power (cf. (4)) one can calculate the critical (maximum) value of the inductance as

$$L_{U,crit} = \frac{2}{3} U_O^2 T_P \frac{P_{O,r,\delta \leq 1}}{P_{O,max}} \geq L_U. \quad (43)$$

The operating region of the system is described by a rectangle defined by the intervals  $P_{O,r} = [0, P_{O,r,\delta \leq 1}]$ ,  $M^{-1} \in [M_{min}^{-1}, M_{max}^{-1}]$  in the  $P_{O,r}, M^{-1}$ -plane. For determination of the maximum current stress on the devices, one can now assume this rectangle to be inserted into Fig. 7(a)–(h). Then, the maximum occurring component stresses can be seen immediately or can be calculated via (27), (30), (31), and (32).

### B. Design Example

We assume

$$\begin{aligned} U_{N,rms} &= 230 \text{ V}_{-15\%}^{+10\%} \\ P_O &= 7.8 \text{ kW} \\ U_O &= 820 \text{ V} \\ f_P &= 48 \text{ kHz} \quad (T_P = 20.8 \text{ } \mu\text{s}). \end{aligned}$$

The data given here correspond to the values for applying the rectifier system as ac/dc input circuit of a 67 V/100 A telecommunication power supply module (being designed as ac/dc–dc/dc converter system with a rated power of 6.7 kW, cf. e.g., [13] p. 409). Because typically a stationary overload capability of 10% of the rated power is required there, and because an efficiency of  $\eta_{DC/DC} = 0.95$  has to be considered, there follows  $P_O = 7.8$  kW for the maximum output power of the rectifier stage. The dc link voltage is set to  $U_O = 820$  V in order to minimize low-frequency effects on the mains and in consideration of the blocking voltage stress of the power electronic devices. The switching frequency  $f_P = 48$  kHz constitutes a compromise regarding the decreasing size of the mains filter (and therefore of the converter) for increasing  $f_P$  and regarding the system losses which rise with  $f_P$ .

As described in Section III-A (cf. (9)) we have assumed  $\eta = 1$  for deriving the characteristic parameters being relevant for dimensioning (i.e., we have set input and output power equal,  $P_N = P_O$ , cf. (18)). For an inclusion of the efficiency into the dimensioning we have to consider, therefore, in a first approximation a (fictitious) higher output power (or the real input power)  $P_O/\eta$ . There, the efficiency can typically be assumed to be in the region  $\eta_{AC/DC} = 0.94 \dots 0.96$ . For a sufficient dimensioning safety we choose in the case at hand  $\eta_{AC/DC} = 0.94$  and, therefore,  $P_{O,max} = 8.3$  kW as basis for the dimensioning.

For the voltage transfer ratios for minimum and maximum input voltage there follows with (6):

$$\begin{aligned} M_{max} &= 1.71 \quad (U_{N,rms,min} = 195.5 \text{ V}) \\ M_{min} &= 1.32 \quad (U_{N,rms,max} = 253.0 \text{ V}). \end{aligned}$$

For the sake of clearness the consideration of a control margin shall be omitted for the calculation of the inductance  $L_U$ . The dimensioning shall be performed such that for  $P_{O,max}$  the

limit of the discontinuous mode  $\delta = 1$  is reached. In order to guarantee  $\delta \leq 1$  in the entire input voltage region, we have to choose

$$P_{O,r,\delta \leq 1} = 0.045,$$

according to Fig. 6. Here,  $\delta = 1$  is reached for  $M_{\min}$  (cf. II in Fig. 6). If we set  $L_U = L_{U,\text{crit}}$  (cf. (43)), there follows for dimensioning of the input inductances:

$$L_U = 50.6 \mu\text{H}.$$

For the relative on-time of the power transistor for minimum and maximum input voltage there follows with (17) or with Fig. 5:

$$\begin{aligned} \delta_{P,\text{max}} &= 0.39 \\ \delta_{P,\text{min}} &= 0.24. \end{aligned}$$

As discussed in Section V-A, the ideally maximum blocking voltage stress on the power semiconductors

$$U_{T,\text{max}} = U_{D,\text{max}} = U_{Di,\text{max}} = 820 \text{ V}$$

is defined by the output voltage, where for the setting of the blocking voltage capability of the devices transient switching and mains overvoltages have to be considered.

For determining the maximum current stress on the devices we have to transfer the operating point  $I$  (see Fig. 6) as given for minimum input voltage  $\hat{U}_{N,\text{rms},\text{min}}$  (or  $M_{\text{max}}$ , respectively) and for maximum output power  $P_{O,\text{max}}$  (or  $P_{O,r,\delta \leq 1}$ , respectively) into the diagrams of Fig. 7. Then, the maximum component stress can be read directly and/or be calculated via the relations given in Section V.

With the normalization basis for the current values

$$I_n = 225.1 \text{ A}$$

(cf. (5)) there follows:

Power transistor  $T$ :

$$\begin{aligned} \text{Fig. 7(a): } I_{T,\text{avg}} &= 8.6 \text{ A} \quad (9.2 \text{ A}) \\ \text{Fig. 7(b): } I_{T,\text{rms}} &= 16.0 \text{ A} \quad (16.4 \text{ A}) \\ \text{Fig. 7(c): } I_{T,\text{max}} &= 45.5 \text{ A} \quad (45.7 \text{ A}). \end{aligned}$$

Inductance  $L_U$ :

$$\begin{aligned} \text{Fig. 7(f): } I_{U,(RST),\text{rms}} &= 17.5 \text{ A} \quad (17.7 \text{ A}) \\ (24): I_{U,(RST),\text{max}} &= 45.5 \text{ A} \quad (45.7 \text{ A}). \end{aligned}$$

Output diode  $D$ :

$$\begin{aligned} (18): I_{D,\text{avg}} &= 10.1 \text{ A} \quad (9.5 \text{ A}) \\ \text{Fig. 7(d): } I_{D,\text{rms}} &= 16.6 \text{ A} \quad (15.9 \text{ A}) \\ (24): I_{D,\text{max}} &= 45.5 \text{ A} \quad (45.7 \text{ A}). \end{aligned}$$

Diodes  $D_i$  of the three-phase bridge:

$$\begin{aligned} (31): I_{Di,\text{avg}} &= 6.2 \text{ A} \quad (6.2 \text{ A}) \\ (32): I_{Di,\text{rms}} &= 12.5 \text{ A} \quad (12.8 \text{ A}) \\ (24): I_{Di,\text{max}} &= 45.5 \text{ A} \quad (45.7 \text{ A}). \end{aligned}$$

Output capacitor  $C$ :

$$\begin{aligned} \text{Fig. 7(e): } I_{C,\text{rms}} &= 13.2 \text{ A} \quad (12.7 \text{ A}) \\ (27): I_{C,\text{max}} &= 35.4 \text{ A} \quad (36.2 \text{ A}). \end{aligned}$$

Mains filter capacitor  $C_N$ :

$$\begin{aligned} \text{Fig. 7(g): } I_{CN,\text{rms}} &= 10.0 \text{ A} \quad (10.7 \text{ A}) \\ (30): I_{CN,\text{max}} &= 25.5 \text{ A} \quad (27.3 \text{ A}). \end{aligned}$$

*Remark:* According to (5), the reference values  $I_n$  and  $P_n$  of the normalization remain unchanged for proportional change of pulse frequency  $f_P = T_P^{-1}$  and inductivity  $L_U$ . If now  $f_P$  is changed during dimensioning and  $L_U$  is adjusted accordingly, the current stress on the devices is *not* influenced and can be taken directly from the original dimensioning.

For the output diode current there follows with (16) and (18):

$$I_O = 10.1 \text{ A} \quad (10.1 \text{ A}).$$

*Remark:* Because the dimensioning, as mentioned before, is performed based on the input power (or a fictitious higher output power, respectively), a too high value is being calculated for  $I_O$  (as well as for  $I_{D,\text{avg}}$ ). The exact value can be determined via the equation

$$I_O = \frac{P_O}{U_O} = I_{D,\text{avg}} = 9.5 \text{ A}.$$

However, the selection of the output diode is not influenced by this deviation which is small due to the high efficiency. Characteristic values of the mains current

$$(19): \hat{I}_{N,(1)} = 20.0 \text{ A} \quad (19.9 \text{ A})$$

$$\text{Fig. 7(h): } I_{N,\text{rms}} = 14.1 \text{ A} \quad (14.1 \text{ A}).$$

The maximum amplitudes of the low-frequency mains current harmonics can be taken from Fig. 8 for  $M_{\min}$ , the minimum power factor from Fig. 9. The maximum amplitude of the 5th harmonic is of special importance regarding the effects on the mains. There follows:

$$\frac{\hat{I}_{N,(5),\text{max}}}{\hat{I}_{N,(1)}} = 0.16 \quad (0.15).$$

Therefore, for the maximum input voltage a considerable deviation of the mains current from an ideally purely sinusoidal shape occurs. This shows up also in the value of the power factor

$$\lambda_{\min} = 0.985 \quad (0.99).$$

## VIII. EXPERIMENTAL RESULT

The exactness of the calculated results given so far shall finally be verified by measurements on a laboratory model.

According to the assumptions given in Section VII-B the maximum output power of the experimental set-up is set to 7.8 kW (dc link voltage  $U_O = 820 \text{ V}$ , mains rated voltage  $U_N = 230 \text{ V}$ , pulse frequency  $f_P = 48 \text{ kHz}$ ). For measurement of the maximum stress on the devices a phase-voltage-rms value

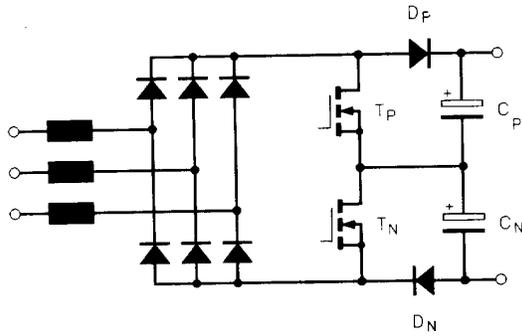


Fig. 10. Realization of the power circuit of the laboratory set-up of the converter system.

of  $U_{N,rms} = 195.5$  V corresponding to  $M_{max} = 1.71$  is set by a three-phase regulating auto-transformer.

The three-phase diode bridge on the converter input side is formed by a combination of single diodes BYT30P-1000 with low reverse-recovery time. Due to high blocking voltage stress on the power transistor  $T$  (regarding the application of power MOSFET's with low on-resistance) the output circuit of the converter is split into two synchronously pulsed partial systems (see Fig. 10). Via inclusion of the output voltage center point a defined blocking voltage distribution is obtained ( $T_P, T_N$ : two power MOSFET's IXFH26N50 connected in parallel for each switch;  $D_P, D_N$ : BYT30P-1000;  $C_P, C_N$ : SIC SAFCO FELSIC85 1500  $\mu$ F/450 V).

*Remark:* During an experimental investigation of, e.g., the industrial applicability of the converter concept (which goes beyond the analysis of basic relationships) we should also consider the realization of  $T$  by an IGBT in connection with a low-loss active turn-off snubber circuit. This could minimize the effort regarding circuit technology, the switching losses and the EMI of the system. Pertinent proposals are given in [14], [15] (zero current switching) and [4], [16], [17] (zero voltage switching). For the sake of brevity, these techniques cannot be discussed in greater detail here.

The series inductance  $L_U$  of each phase is formed by 22 turns of HF-Litz wire (5.54 mm<sup>2</sup> Cu) on an E65/3C85-ferrite core. The mains filter is designed as a single-stage type. It is realized by a star-connection of  $C_F = 10$   $\mu$ F in connection with the inner impedance of the auto-transformer (corner frequency  $f_F \approx 4$  kHz).

Measurements of characteristic shapes of the electrical quantities of the converter system are shown in Fig. 11. In Section VII-B, the average and rms values (being calculated with a Tektronix TDS 544 A digital storage oscilloscope) of the device currents are given in parentheses in connection with the respective results of the theoretical analysis. The deviation of the measurements from the calculated results remains below 7.5%. Also, the measurement of the efficiency  $\eta = 0.945$  (fan losses and power consumption of the control circuitry are not considered) is in good consistency with the assumption of  $\eta = 0.94$  as made in Section VII-B. (A theoretical estimate of the efficiency based on typical data sheet parameters of the used devices leads with the assumption of a heat sink temperature of  $T_s = 85^\circ\text{C}$  to  $\eta \approx 0.95$ .) The good consistency

(as already stated where the results of the analytical calculation have been compared with a digital simulation, cf. Section III-B) of the calculated device stresses which are relevant for dimensioning therefore is also verified by experimental research.

## IX. CONCLUSION

In this paper a procedure is introduced which can be applied in a simple way for determining the component stresses in a three-phase single-switch DICM boost rectifier system. Because the mathematical modeling avoids an application of a single-phase equivalent system, the derived relations show an excellent consistency with the results of a digital simulation also for low values of the voltage transfer ratio (e.g.,  $U_O = 820$  V,  $M \approx 1.5$ , as being of interest for a practical application in the European low-voltage system with a line-to-line voltage  $\sqrt{3}U_{N,rms} = 380$  V). The deviation of the calculated results remains below 2% for pulse frequencies  $f_P \geq 200f_N$ . We have to point out finally that the calculation results can be used also for dimensioning of the devices of the input circuit and for the analysis of the mains behavior of other three-phase single-switch DICM rectifiers with equal structure of the input circuit (see Fig. 4 in [18] or Fig. 19 in [19], respectively). Therefore, the analysis given is valid for a whole class of converter structures. The high accuracy of the calculated results is also verified by measurements on a laboratory model of the converter which has been built up based on the dimensioning guidelines given.

## APPENDIX

The rectifier system is frequently used for supplying a dc/dc converter stage with an input current being pulsed with switching frequency. In this case a direct analytical calculation of the output capacitor current rms value  $I_{C,rms}$  (being similar to the determination of  $I_{C,rms}$  for constant load current) can be performed only if the two converter systems are operated with synchronous switching frequencies (cf. Section 3 in [11] or p. 537, paragraph 8, in [7]). For the general case of not constant switching frequency of the load-side converter or of a stochastically current consumption  $i_O$  (not being linked to a specific pulse pattern) we therefore have to pose the question for the possibility of a simple worst-case estimate.

The output capacitor current is determined by the difference of the output diode current of the rectifier system and the load current

$$i_C = i_D - i_O. \quad (44)$$

Because  $i_D$  and  $i_O$  show the same average value  $I_{D,avg}$  in the stationary case, we can set (when splitting the currents into a dc and an ac part)

$$\begin{aligned} i_D &= I_{D,avg} + i_{D,ac} \\ i_O &= I_{D,avg} + i_{O,ac} \end{aligned} \quad (45)$$

or

$$\begin{aligned} I_{D,ac,rms}^2 &= I_{D,rms}^2 - I_{D,avg}^2 \\ I_{O,ac,rms}^2 &= I_{O,rms}^2 - I_{D,avg}^2, \end{aligned} \quad (46)$$

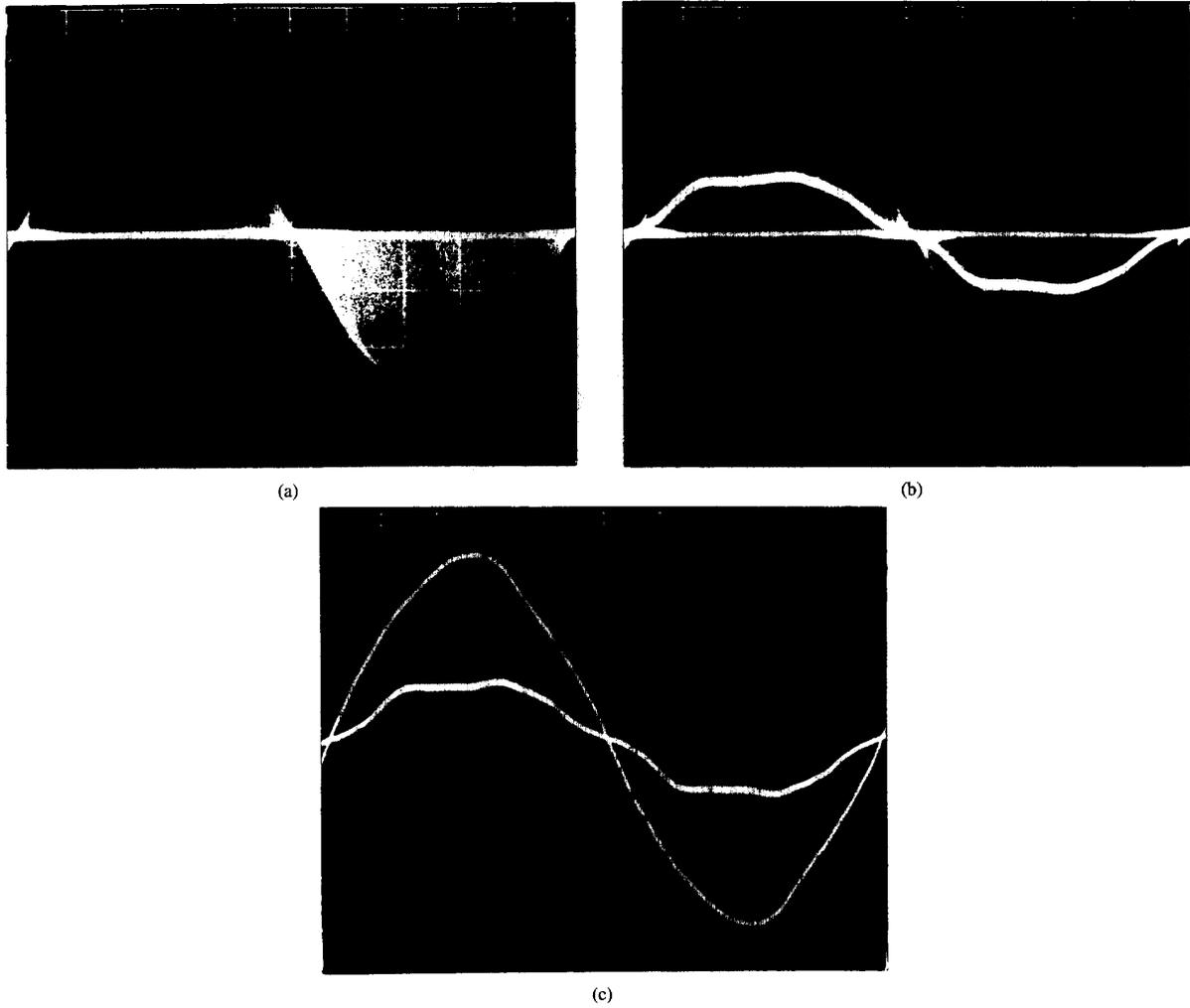


Fig. 11. Results of the measurements on a laboratory set-up of a three-phase single-switch DICM boost-rectifier. Representation of a mains fundamental period (20 ms, 2 ms/div). (a) Mains phase voltage  $u_{N,R}$  (100 V/div) and mains phase current  $i_{N,R}$  (10 A/div). (b)  $i_{N,R}$  and rectifier input current  $i_{U,R}$ . (c)  $i_{U,R}$  and transistor current  $i_T$ . Operating parameters:  $P_O = 5.3$  kW (75% of rated power),  $U_N = 230$  V,  $U_O = 820$  V. Device parameters and types according to the data given in Section VII-B and Section VIII.

respectively. Then, there results for the rms value of the capacitor current there follows:

$$I_{C,rms}^2 = I_{D,ac,rms}^2 + I_{O,ac,rms}^2 - \frac{2}{T} \int_T i_{D,ac} i_{O,ac} dt. \quad (47)$$

$$I_{C,rms}^2 \leq I_{D,ac,rms}^2 + I_{O,ac,rms}^2 + \frac{2}{T} \sqrt{\int_T i_{D,ac}^2 dt} \sqrt{\int_T i_{O,ac}^2 dt}. \quad (49)$$

There, the integration interval  $T$  is defined by the period of the capacitor current. For a not periodic (stochastic) output current the integration has to be performed over a sufficiently large number of fluctuations of the capacitor current.

Because the term  $\int_T i_{D,ac} i_{O,ac} dt$  assumes positive or negative values dependent of the correlation of the ac parts of the currents, there can be given in general only an estimate of the upper limit of the capacitor current rms value. Considering the CAUCHY-SCHWARZ inequality

$$\sqrt{\int_T i_{D,ac}^2 dt} \sqrt{\int_T i_{O,ac}^2 dt} \geq \int_T i_{D,ac} i_{O,ac} dt \quad (48)$$

For dimensioning the output capacitor we have to consider therefore

$$I_{C,rms,max} = I_{D,ac,rms} + I_{O,ac,rms} \quad (50)$$

or

$$I_{C,rms,max} = \sqrt{I_{D,rms}^2 - I_{D,avg}^2} + \sqrt{I_{O,rms}^2 - I_{O,avg}^2}, \quad (51)$$

respectively (cf. Section V-B, (26)).

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