« X-Concepts »
The DNA of Future High-Performance Power Electronic Systems

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The DNA of Future High-Performance Power Electronic Systems

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Power Electronics

Driving Applications
Performance Indicators / Trends
Technology S-Curve
Driving Applications

- Global Megatrends → Industry Automation | Renewable Energy | Sustainable Mobility | Urbanization etc.

- Clean Energy Transition → “All-Electric” Society

Source: Status of Power Electronics Industry 2019 Report

Power Electronic Systems Laboratory

ETH Zürich

IEEE PEAS 2021
The 1st IEEE International Power Electronics and Applications Symposium
Performance Indicators / Trends

- Power Density [kW/dm³]
- Power per Unit Weight [kW/kg]
- Relative Costs [kW/$]
- Relative Losses [%]
- Failure Rate [h⁻¹]
- Manufacturability
- Recyclability / Sustainability
- Networked / IIoT

Environmental Impact...

- [kg\textsubscript{Fe} /kW]
- [kg\textsubscript{Cu} /kW]
- [kg\textsubscript{Al} /kW]
- [cm² /kW]
S-Curve of Power Electronics

- « X-Technologies » / “Moon-Shot” Technologies
- « X-Concepts » → Full Utilization of Basic Scaling Laws & X-Technologies
- Power Electronics 1.0 → Power Electronics 4.0
- 2...5...10x Improvement NOT Only 10% !

Performance

1.0  2.0  3.0  4.0

1958  2015  2025

SCRs / Diodes
Solid-State Devices

Digital Power Modeling & Simulation

Power MOSFETs & IGBTs
Circuit Topologies
Microelectronics
Modulation Concepts
Control Concepts

Super-Junct. Techn. / WBG

Full Utilization of Basic Scaling Laws & X-Technologies

« X-Technologies »
« X-Concepts »

ETH Zürich

IEEE PES 2021
The 1st IEEE International Power Electronics and Applications Symposium
X-Technologies

SiC | GaN
3D-Packaging & Integration
Digital Signal Processing
Energy Storage
Low $R_{DS(on)}$ High-Voltage Devices

- **Higher Critical E-Field of SiC** → Thinner Drift Layer
- **Higher Maximum Junction Temperature $T_{j,max}$**

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>GaAs</th>
<th>4H/6H-SiC</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_g$ (eV)</td>
<td>1.12</td>
<td>1.4</td>
<td>3.0-3.2</td>
<td>3.4</td>
</tr>
<tr>
<td>$E_C$ (MV/cm)</td>
<td>0.25</td>
<td>0.3</td>
<td>2.2-2.5</td>
<td>3</td>
</tr>
<tr>
<td>$\mu_n$ (cm²/Vs)</td>
<td>1350</td>
<td>8500</td>
<td>1000-1000</td>
<td>1000</td>
</tr>
<tr>
<td>$\varepsilon_r$</td>
<td>11.9</td>
<td>13</td>
<td>10</td>
<td>9.5</td>
</tr>
<tr>
<td>$V_{sat}$ (cm/s)</td>
<td>$1\times10^7$</td>
<td>$1\times10^7$</td>
<td>$2\times10^7$</td>
<td>$3\times10^7$</td>
</tr>
<tr>
<td>$\lambda$ (W/cmK)</td>
<td>1.5</td>
<td>0.5</td>
<td>3-5</td>
<td>1.3</td>
</tr>
</tbody>
</table>

$R_{on} = \frac{4V_f^2}{\varepsilon\mu_n E_C^3} \left( \frac{W}{\mu_n} \right) N_0 \left( \frac{cm^2}{cm^2} \right)$

For 1kV:

- Si: 100
- SiC: 10

$R_{on, SiC}^* \approx \frac{1}{300} R_{on, Si}^*$

- **Massive Reduction of Relative On-Resistance** → High Blocking Voltage Unipolar Devices
Low $R_{DS(on)}^*$ High-Voltage Devices

- **SiC MOSFETs / GaN HEMTs (Monolithic AC-Switch)**
- Low Conduction Losses & ZVS
- High Efficiency

\[
R_{on}^* = \frac{4V_B^2}{\varepsilon\mu_n P_C^3} \leq
\]

\[
R_{on,Si}^* \approx \frac{1}{300} R_{on,Si}
\]

- **High-Voltage Unipolar (!) Devices** → **Excellent Switching Performance**
Monolithic 600V GaN Bidirectional/Bipolar Switch

- **POWER AMERICA Program** — Based on Infineon’s CoolGaN™ HEMT Technology
- Dual-Gate Device / Controllability of Both Current Directions
- Bipolar Voltage Blocking Capability | Normally On or Off

**Analysis of 4-Quadrant Operation** of $R_{DS(on)} = 140m\Omega$ | 600V Sample @ ±400V
Example of 3-Level T-Type Inverter

- Utilization of 600V Monolithic Bidirectional GaN Switches
- 2-Gate Structure Provides Full Controllability

- Factor 4 (!) Reduction of Chip Area vs. Discrete Realization
X-Technology

3D-Packaging / Integration
Circuit Parasitics

- Extremely High \( \frac{di}{dt} \)
- Commutation Loop Inductance \( L_s \)
- Allowed \( L_s \) Directly Related to Switching Time \( t_s \)

\[
L_s \leq \frac{\alpha U_i}{I_L} = \alpha t_s \frac{U_i}{I_L} \leq \frac{U_i}{I_L} \cdot \frac{1}{Z}
\]

- Advanced Packaging & Parallel Interleaving for Partitioning of Large Currents (Z-Matching)
3D-Packaging / Heterogeneous Integration

- **System in Package (SiP) Approach**
- **Minim. of Parasitic Inductances / EMI Shielding / Integr. Thermal Management**
- **Very High Power Density** (No Bond Wires / Solder / Thermal Paste)
- **PCBs Embedded Optic Fibres**
- **Automated Manufacturing**

- **Future Application** Up to 100kW (!)
- **New Design Tools & Measurement Systems** (!)
- **University / Industry Technology Partnership** (!)
Remark: Future uP Chip-Stack Packaging

- Slowing Transistor Node Scaling $\rightarrow$ Vertical & Heterogeneous Integr. of ICs for Performance Gains
- Extreme 3D-Integrated Cube-Sized Compute Nodes
- Dual Side & Interlayer Microchannel Cooling

- Interposer Supporting Optical Signaling / Volumetric Heat Removal / Power Conversion
Digital Signal & Data Processing

- **Exponentially Improving uC / Storage Technology (!)**
- Extreme Levels of Density / Processing Speed
- Software Defined Functions / Flexibility
- Continuous Relative Cost Reduction

- Distributed Intelligence
- Fully Digital Control of Complex Systems – Electrical/Optical/Wireless Signal Transfer
- Massive Comp. Power → Fully Automated AI-Based Design / Digital Twins / Industrial IoT (IIoT)

Source: Ostendorf & König / DeGruyter

Source: vario-optics.ch/Electro-Optical PCBs
Automated Design (1)

- Based on Mathematical Model of the Technology Mapping
- Multi-Objective Optimization → Best Utilization of the “Design Space”
- Identifies Absolute Performance Limits → Pareto Front / Surface

- Clarifies Sensitivity $\Delta \dot{p} / \Delta \dot{k}$ to Improvements of Technologies
- Trade-Off Analysis
Automated Design (2)

- **Design Space Diversity**
- **Equal Performance for Largely Different Sets of Design Parameters (!)**

- E.g. Mutual Compensation of Volume or Loss Contributions (e.g. Cond. & Sw. Losses)
- Allows Consideration of Additional Performance Targets (e.g. Costs)
Design Space Diversity — Example

- Design of a Medium-Frequency Transformer
- Power Level & Power Density = const.
- Wdg./Core Loss Ratio, Geometry, n etc. as Design Parameters

Source: T. Guillod / ETH

- Mutual Compensation Core & Winding Losses Changes
- Limits on Part Load Efficiency / Costs / Fixed Geometry → Restricted Diversity

\[
x_{cu} = A_c / A_w, \quad x_c = z_c / 2 t_c, \quad x_w = h_w / d_w
\]
Design Automation Roadmap

- **End-to-End Horizon** — Cradle to Grave/Cradle — Modeling & Simulation
- **Design for Cost / Volume / Efficiency / Manufacturing / Testing / Reliability / Recycling**

**Autonomous Design → Design 4.0**
- Independent Generation of Full Designs for Final Expert Judgement

**Augmented Design**
- Suggestion of Design Details Based on Previous Designs

**Assisted Design**
- Support of the User with Abstracted Database of Former Designs

**State-of-the-Art**
- User Defined Models and Simulation / Fragmented

- **AI-Based Summaries → No Other Way to Survive in a World of Exp. Increasing # of Publications (!)**
X-Concepts

Modularization
Functional Integration
Synergetic Association
Hybridization
Decentralization
Scaling of Multi-Cell/Level Concepts

- Reduced Ripple @ Same (!) Switching Losses
- Lower Overall On-Resistance @ Given Blocking Voltage
- Application of LV Technology to HV

\[ \Delta I_{\text{max},N} = \frac{1}{N^2} \Delta I_{\text{max},N=1} \]

\[ \Delta U_{\text{C, max},N} = \frac{\pi^2 (f_0)^2}{32 f_s} \frac{1}{N^3} \]

- Scalability / Manufacturability / Standardization / Redundancy

Source: R. Pilawa

Integrated Dual-Sided Half-Bridge Flying Capacitor Converter Switching Cell
SiC/GaN Figure-of-Merit

- **Figure-of-Merit (FOM)** Quantifies Conduction & Switching Properties
- **FOM** Determines Max. Achievable Efficiency @ Given Sw. Frequ.

\[
\text{FOM} = \frac{1}{R_{\text{ds,on}} Q_{\text{oss}}}
\]

Advantage of Multi-Level over 2-Level Converter Topologies
X-FOM of ML-Bridge-Legs

- Quantifies Bridge-Leg Performance of N-Level FC Converters

N= # of Levels - 1

\[
P_{\text{semi,min,ML}} \approx \frac{1}{N^{1.2}}
\]

\[
P_{\text{semi,min,2L}}
\]

\[
A_{\text{chip,ML}} \approx N^{1.2} A_{\text{chip,2L}}
\]

- Compared to 2-Level Benchmark @ Same Filter Ind. Volt-Seconds

\[
\frac{U_{\text{dc}}}{N} |_{N=2}
\]
3-Φ Hybrid Multi-Level Inverter

- Realization of a 99%++ Efficient 10kW 3-Φ 400V<sub>rms</sub> Inverter System
- 7-Level Hybrid Active NPC Topology / LV Si-Technology

- 200V Si → 200V GaN Technology Results in 99.5% Efficiency
Quasi-2L & Quasi-3L Inverters (1)

- Operation of N-Level Topology in 2-Level or 3-Level Mode
- Intermediate Voltage Levels Only Used During Sw. Transients

- Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors
- Low Voltage/Low $R_{DS(on)}$/Low $S$ MOSFETs $\rightarrow$ High Efficiency / No Heatsinks / SMD Packages

Source: M. Schweizer

ABB

IEEE CPSS 2021
The 1st IEEE International Power Electronics and Applications Symposium

ETH Zürich
Quasi-2L & Quasi-3L Inverters (2)

- Operation of 5L Bridge-Leg Topology in Quasi-3L Mode
- Intermediate Voltage Levels Only Used During Sw. Transients
- Applicability to All Types of Multi-Level Converters

3.3kW @ 230V_{rms}/50Hz
Equiv. f_{sc} = 48kHz

3.5kW/dm³
Eff. ≈ 99%

- Reduced Average dv/dt → Lower EMI
- Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors
- Low Voltage/Low R_{DS(on)}/Low $ MOSFETs → High Efficiency / No Heatsinks / SMD Packages
Quasi-2L & Quasi-3L Inverters (3)

- Operation of 5L Bridge-Leg Topology in Quasi-3L Mode
- Intermediate Voltage Levels Only Used During Sw. Transients
- Applicability to All Types of Multi-Level Converters

**Operation @ 3.2kW**

- Conv. Output Voltage
- Sw. Stage Output Voltage
- Flying Cap. (FC) Voltage
- Q-FC Voltage (Uncntrl.)
- Output Current
- Conv. Side Current

- Reduced Average dv/dt → Lower EMI
- Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors
- Low Voltage/Low $R_{DS(on)}$/Low $\$$ MOSFETs → High Efficiency / No Heatsinks / SMD Packages
Example of Google Little Box Challenge
Target: 2kW 1-Φ Solar Inverter with Worldwide Highest Power Density
Comparative Analysis of Approaches of the Finalists

3D-Packaging / Integration Highly Crucial for Utilizing Multi-Level Advantages (!)
Remark

2-Level vs. Multi-Level Inverter

- Example of Google Little Box Challenge
- Target: 2kW 1-Φ Solar Inverter with Worldwide Highest Power Density
- Comparative Analysis of Approaches of the Finalists

**ETH zürich**
Little-Box 2.0
240 W/in³
97.4%

**ETH zürich**
Little-Box 2.0
215 W/in³
97.6%

Source: R. Pilawa-Podgurski

- 3D-Packaging / Integration Highly Crucial for Utilizing Multi-Level Advantages (!)
2-Level vs. Multi-Level Inverter

- 400kW Extreme Fast EV Charger
- 3-Φ 13.2kV AC → 1kV DC
- Input Series Output Parallel (ISOP) Solid-State Transformer
- Alternative Low-Frequency Transformer & AC/DC Converter

- 1.2kV SiC MOSFETs Utilized in Both Systems
- 3 x 9 = 27 AC/DC—DC/DC Cells / 3-Level PFC Input Stage & Full-Bridge DC/DC Output Stage
2-Level vs. Multi-Level Inverter

- **400kW Extreme Fast EV Charger**  |  **3-Φ 13.2kV AC → 1kV DC**
- **Input Series Output Parallel (ISOP) Solid-State Transformer**

- **Forced Air Cooling**
- **3 x 9 = 27 AC/DC—DC/DC Cells**
- **98+ % Efficiency**  |  **3000kgs Weight**  |  **3100 x 1300 x 2100 mm Outer Dimensions**

η = 0.98
2-Level vs. Multi-Level Inverter

- 400kVA EcoDry™ High-Efficiency Transformer & AC/DC Converter
- Vacuum Cast Coils → No Fire Hazard
- Amorphous Metal Core → Low No-Load Losses
- High Overvoltage / Overload Capability

- 400kVA → 1400 x 750 x 1500 mm Outer Dimensions
- Utilizing SST SiC MOSFETs in AC/DC Stage → 99++ % Efficiency
- Higher Efficiency / Power Density / Robustness of LFT-Based Concept (!)
X-Concept

Functional Integration
**Buck-Boost 3-Φ Variable Speed Drive Inverter**

- **Generation of AC-Voltages Using Unipolar Bridge-Legs**
- **Utilize Filter Inductor for Boost Operation → Functional Integration**

- **Switch-Mode Operation of Buck OR Boost Stage → Single-Stage Energy Conversion (!)**
- **3-Φ Continuous Sinusoidal Output / Low EMI → No Shielded Cables / No Motor Insul. Stress**
Boost-Operation $u_{an} > U_i$

- **Phase-Module**

- **Motor Phase Voltages**

- **Current-Source-Type Operation**
- **Clamping of Buck-Bridge High-Side Switch** → Quasi Single-Stage Energy Conversion
Buck-Operation $u_{an} < U_i$

- **Phase-Module**

- **Motor Phase Voltages**

- **Voltage-Source-Type Operation**
- **Clamping of Boost-Bridge High-Side Switch → Quasi Single-Stage Energy Conversion**
SiC 3-Φ Buck-Boost Inverter Demonstrator

- DC Voltage Range: 400...750V_{DC}
- Max. Input Current: ± 15A
- Output Voltage: 0...230V_{rms} (Phase)
- Output Frequency: 0...500Hz
- Sw. Frequency: 100kHz

Dimensions → 160 x 110 x 42 mm³  ≈ 245 W/in³
Isolated Matrix-Type 3-Φ PFC Rectifier (1)

- Based on Dual Active Bridge (DAB) Concept
- Integration of 3-Φ PFC Rectifier & DC/DC Converter Stage
- Opt. Modulation ($t_1$…$t_4$) for Min. Transformer RMS Curr. & ZVS or ZCS
- Allows Buck-Boost Operation

- Equivalent Circuit
- Transformer Voltages / Currents
Isolated Matrix-Type 3-Φ PFC Rectifier (2)

- Efficiency $\eta = 99\%$ @ 60% Rated Load (ZVS)
- Mains Current $\text{THD}_I \approx 4\%$ @ Rated Load
- Power Density $\rho \approx 4\text{ kW/dm}^3$

$P_0 = 8\text{ kW}$
$U_{IN} = 400\text{V}_{AC} \rightarrow U_O = 400\text{V}_{DC}$
$f_S = 36\text{kHz}$

- 900V / 10mΩ SiC Power MOSFETs
- Opt. Modulation Based on 3D Look-Up Table
3-Port Resonant GaN DC/DC Converter

- Single Transformer & Decoupled Power Flow Control
- Charge Mode PFC $\rightarrow$ HV (250…500V) SRC DCX / Const. $f_{sw}$, Min. Series Inductance / ZVS
- Drive Mode HV $\rightarrow$ LV (10.5…15V) 2 Interleaved Buck-Converters / Var. $f_{sw}$ / ZVS
- $P = 3.6kW$

- Peak Efficiency of 96.5% in Charge Mode / 95.5% in Drive Mode
- PCB-Based Windings / No Litz Wire Windings $\rightarrow$ Fully Automated Manufacturing

$\approx 16$ kW/dm$^3$
Low-Loss PCB-Winding Inductor

- Conv. PCB Windings & Airgaps → Skin / Proximity / Fringing Field ↓ to PCB → Current Displacement
- Arrangement of Airgaps for Mutual Field Compensation
- Thermal Interfaces for Efficient Cooling

- Optimal Positions & Wdg Distance of Airgaps for Multi-Airgap / Multi-Layer Inductors
- Factor of 3 Red. of Skin & Prox. Losses
X-Concept

Synergetic Association
3-Φ EV-Charger Topology

- Isolated Controlled Output Voltage
- Buck-Boost Functionality & Sinusoidal Input Current
- Applicability of 600V GaN Semiconductor Technology
- High Power Density / Low Costs

→ Conventional / Independent OR “Synergetic Control” of Input & Output Stage
**Synergetic Association**

- **1/3-Modulation** → Significant Red. of Losses of the Power Switches Comp. to 3/3-PWM

- **Conduction Losses of the Switches** ≈ -80%

- **Switching Losses** ≈ -70%

- **Operating Point Dependent Selection of 1/3-PWM OR 3/3-PWM for Min. Overall Losses**
X-Concept Hybridization
Integrated Active Filter (IAF) PFC Rectifier

- Hybrid Combination of Mains- and Forced-Commutated Converter
- 3\textsuperscript{rd} Harmonic Current Injection into Phase with Lowest Voltage
- Phase Selector AC Switches Operated @ Mains Frequency — 3-Φ Unfolder

- Non-Sinusoidal Mains Current

\[ P_o = \text{const. Required} \]

\[ \text{Sinusoidal Mains Current} \]

\[ \text{NO (!) DC Voltage Control} \]
IAF PFC Rectifier & Buck Converter Demonstrator

- **Efficiency** $\eta > 99.1\%$ @ 60% Rated Load
- **Mains Current** $\text{THD}_I \approx 2\%$ @ Rated Load
- **Power Density** $\rho \approx 4\text{kW/dm}^3$

\[
P_0 = 8\text{ kW} \\
U_N = 400\text{V}_{\text{AC}} \rightarrow U_0 = 400\text{V}_{\text{DC}} \\
f_S = 27\text{kHz}
\]

- **SiC Power MOSFETs & Diodes**
- **2 Interleaved Buck Output Stages**
- **Controlled Output Voltage**

\[
P_O = 8\text{ kW} \\
U_N = 400\text{V}_{\text{AC}} \Rightarrow U_0 = 400\text{V}_{\text{DC}}
\]
Partial/Differential Power Processing

\[ U_2 = U_1 - U_c \]

- **Reduced Converter Rating**

\[ p_c = \frac{P_{c,1}}{P_1} = \frac{U_c}{1 + \frac{U_c}{U_2}} \]

- **Low Influence of Converter Efficiency on Overall Efficiency**

\[ \eta = \frac{P_2}{P_1} = \frac{(1 + \frac{U_c}{U_2} \eta_c)}{(1 + \frac{U_c}{U_2})} \]
Pre-Regulated LLC DC-Transformer

- **Aux. Converter Stage for ±10% $V_{in}$ Compensation** | $V_{in} = 340V \ldots 420V$
- **Const. Voltage Transfer Ratio / High Efficiency LLC «DC/DC Transformer» @ Const. Frequency** | $f_{sw} = 100kHz$
- **Const. Output Voltage** | $V_{out} = 48V$

- Rectangular Aux. Voltage Added or Subtracted ($f_{aux} = 600kHz$) from $V_{in}$
- Marginal Impact of Control on Overall Power Density & Efficiency

≈ $140 \text{ W/in}^3$
1-Φ AC/DC—DC/DC Solid-State Transformer

- Bidirectional 3.8 kV \text{rms} 1-Φ AC \rightarrow 400 V DC \text{ @ 25 kW Power Conversion}
- Based on 10 kV SiC MOSFETs
- Full Soft-Switching

- 3.3 kW/dm\(^3\)
- 3.8 kW/dm\(^3\)

- 35...75 kHz iTCM Input Stage
- 48 kHz «DC-Transformer» Output Stage

Isolation Stage
Operating Frequency

Relative voltage

Relative Frequency \(\omega/\omega_0\)
Overall Performance AC/DC — DC/DC

- **Full Soft-Switching**
- **98.1% Overall Efficiency @ 25 kW**
- **1.8 kW/dm$^3$ (30 W/in$^3$)**

- **Significantly Simpler System Structure Compared to Multi-Module (ISOP) SST Approach**
Hybrid EMI-Filter / Leakage Current Reduction

- Future Extension of EMI Limits — 9kHz ... 150kHz
- Earth Leakage Current “Compensation”
- Conducted CM EMI Filter

- Prevents Unintentional Residual Current Device (RCD) Tripping w/o Isolation Transformer
- Attenuation of Cond. EMI Emissions in Wide Frequency Range 30/40/15dB @ 4/10/150kHz
X-Concept  Decentralization
Networking Scaling

- Metcalfe's Law
  - Moving from Hub-Based Concept to Community Concept Increases Potential Network Value Over-Proportional $\rightarrow \sim n(n-1)$ or $\sim n \log(n)$
IIoT in Power Electronics

- **Digital Twin** → Physics-Based “Digital Mirror Image”
- **Digital Thread** → “Weaving” Real/Physical & Virtual World Together

- Requires Proper Interfaces for Models & Automated Design
- Model of System’s Past/Current/Future State → Design Corrections / Predictive Maintenance etc.

Source: www.railwayage.com
IIoT Starts with a Sensor (!)

- **Condition Monitoring of DC Link Capacitors**
- **On-Line Measurement of the ESR in “Frequency Window” (Temp. Compensated)**
- **Data Transfer by Optical Fibre or Near-Field RF Link**

- **Possible Integration into Capacitor Housing or PCB**
- **Additionally features Series Connect. Voltage Balancing**
Smart Inverter Concept

- Utilize High Computing Power and Network Effects in the Cloud

Source: R. Sommer

- On-Line Optimization / Protection / Monitoring on Component | Converter | Drive | Application Level

- Intelligent Gate Drive Unit
  - Semiconductor protection (overcurrent, overvoltage, ...)
  - Collecting and preprocessing of sensor data (current, voltage, temperature, ...)
  - Semiconductor specific condition monitoring functions

- Communication
  - Communication protocol instead of on/off signals

- Drive Controller
  - Observer based condition monitoring functions
  - Predictive maintenance functions
  - Data Processing and data compression
  - Communication to customer automation and/or internet

- Internet / Cloud
  - Service and commissioning tools
  - Algorithms for „Big Data“ analysis
  - Smart documentation (e.g. video to support service)
  - ...
Conclusion
“Moore’s Law” of Power Electronics

- "Moore’s Law" Defines Consecutive Technology Nodes Based on Min. Costs per Integr. Circuit (!)
- Complexity @ Min. Comp. Costs Increases approx. by Factor of 2 / Year

Potential Power Density Improvement — Factor 2 ... 5 Until 2030
Definition of “$\eta_p \cdot \sigma \cdot f_p$— Technology Node” Must Consider Conv. Type / Operating Range etc. (!)
Future Development

- Commoditization / Standardization
- Extreme Cost Pressure (!)

"There is Plenty of Room at the Top" ➔ Medium Voltage/Frequency Solid-State Transformers

100 kW ➔ 10 W
Standard / Integrated Solutions

System Applications

Cost

Power-Supplies on Chip

"There is Plenty of Room at the Bottom"

Key Importance of Technology Partnerships of Academia & Industry
Power Electronics $\rightarrow$ “Energy” Electronics

- **Design Considering Converters as Standardized “Integrated Circuits” (PEBBs)**
- **Extend Analysis to Converter Clusters / Power Supply Chains / etc.**

- “Converter” $\rightarrow$ “Systems” (Microgrid) or “Hybrid Systems” (Automation / Aircraft)
- “Time” $\rightarrow$ “Integral over Time”
- “Power” $\rightarrow$ “Energy”

$$ p(t) \rightarrow \int_{0}^{t} p(t) \, dt $$

- **Power Conversion** $\rightarrow$ **Energy Management / Distribution**
- **Converter Analysis** $\rightarrow$ **System Analysis (incl. Interactions Conv. / Conv. or Load or Mains)**
- **Converter Stability** $\rightarrow$ **System Stability (Autonom. Ctrl of Distributed Converters)**
- **Cap. Filtering** $\rightarrow$ **Energy Storage & Demand Side Management**
- **Costs / Efficiency** $\rightarrow$ **Life Cycle Costs / Mission Efficiency / Supply Chain Efficiency**
- etc.
Energy Electronics Systems
Performance Figures/Trends

- Complete Set of New Performance Indices
  - Power Density [kW/m²]
  - Environmental Impact [kWs/kW]
  - TCO [$/kW]
  - Mission Efficiency [%]
  - Failure Rate [h⁻¹]

Supply Chain & Mission Energy Loss
Manufacturing & Recycling Effort
Total Cost of Ownership
State-of-the-Art
Floorspace Requirement
Future

ETH zürich
Thank you!