A Novel Three-Phase Three-Switch Three-Level High Power Factor SEPIC-Type AC-to-DC Converter

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Abstract. In the paper the topology of a new three-phase three-switch three-level PWM rectifier system is derived based on the basic structure of a DC-to-DC SEPIC converter. The system is characterized by full controllability of the power flow (independent of the level of the output voltage) and by a sinusoidal mains current shape in phase with the mains voltage. The operating principle of the converter is explained based on the conduction states of a bridge leg within a pulse period. The stationary operating behavior is analyzed by digital simulation based on the control of the mains phase currents by independent ramp-comparison controllers. Furthermore, a mathematical description of the operating behavior of the three-phase system including the coupling of the phase current controllers (given due to the floating mains star point) is discussed. Finally, results of an experimental investigation of a laboratory model of the converter are presented.

1 Introduction

In [1] a three-phase three-switch three-level boost-type PWM rectifier system (cf. **Fig.1**) has been proposed which shows especially the advantage of a relatively low blocking voltage stress on the power semiconductors and a low level of mains current harmonics with switching frequency. Further advantages are simple circuit structure, the sinusoidal mains current consumption (being in phase with the mains voltage) and the controllability of the output voltage. However, as being characteristic for boost converters, there is a lower limit of the output voltage region of the system. The possibility of controlling the input current and, therefore, the consumed power is only given (due to the operating principle) for output voltages being sufficiently larger than the peak value of the mains line-to-line voltage. Feeding of a load with rated voltage being lower than the peak value of the line-to-line voltage therefore can only be performed via a series-connected DC-to-DC converter stage. Therefore, this is connected with substantial additional realization effort. (The blocking voltage stress on the power semiconductors of the DC-to-DC converter stage is defined by the boost converter output voltage and not by the (possibly) substantially lower load voltage level.) Furthermore, the limited output voltage region makes necessary an input current limitation which suppresses the occurrence of an input overcurrent at the time of system start-up (output voltage $U_O = 0$). This is realized in the simplest case via series resistances which lie in the mains leads and which are short circuited after the output capacitors are charged up. In connection with this, one has to mention the problem (which exists in general for boost converters) of limiting the current for mains overvoltages and/or for decreasing output voltages due to a load failure or after short interruptions of the mains voltage. This will require further circuit measures.

During the course of developing of new topologies of three-phase PWM rectifier systems one has to ask the question therefore, concerning a converter structure which would allow to control the output voltage in a wide region (i.e., especially also below the peak value of the line-to-line mains voltage). Due to the requirement of high quality of the input current (i.e., a continuous sinusoidal mains current consumption) it is near at hand to consider a three-phase extension of the basic structure of a DC-to-DC SEPIC or DC-to-DC Cuk converter; such as the boost converter these converters have a continuous input current shape being impressed by the input inductances, but in principle no limitation of the voltage transfer ratio. (cf. Fig.2 in [2] and/or p. 184 in [3]).

The derivation of the circuit structure of a

- new three-phase/switch/level SEPIC-type PWM rectifier and of a
- new three-phase/switch/level Cuk-type PWM rectifier

will be shown in **section 2** of this paper. In connection with the circuit of a three-phase/switch/level boost-type PWM (VIENNA) rectifier (as proposed in [4]) a new class of unidirectional three-phase three-switch PWM rectifier systems with impressed input current is formed herewith. A closer analysis of the stationary operating behavior of the new converter is limited (for the sake of brevity) to the SEPIC-type converter which offers advantages concerning practical realization. In **section 3** the conduction states of a bridge leg are analyzed in dependency on the signs of the mains phase currents. Furthermore, a mathematical formulation of the stationary operating behavior of the phase leg is given. There, the input voltage (varying sinusoidally with mains frequency) is assumed to be approximately constant for several pulse periods, i.e., a DC-to-DC equivalent circuit is considered. In **section 4**, the operating behavior and/or the current and voltage shapes characterizing the three-phase system are discussed in relation to the considerations given in section 3. The topic of **section 5** is a mathematical description of the coupling of the phase legs which is given due to the lacking connection between the mains star point and output voltage center point. Furthermore, in this section the current is calculated which is fed into the capacitively formed center point of the output voltage; also, the symmetrization of the partial output voltages is discussed. Finally, in **section 6** the results of the experimental investigation of the converter based on a laboratory model are given.

2 Derivation of the Converter Structure

As mentioned in the beginning of this paper, the derivation of the circuit structures of a three-phase/switch/level AC-to-DC SEPIC and of a three-phase/switch/level AC-to-DC Cuk converter shall be performed based on the related known DC-to-DC basic converter structures and under consideration of the topological characteristica (compiled in the following) of the already known three-phase/switch/level AC-to-DC boost converter (cf. Fig.1).

Structural and topological characteristica of a three-phase three-switch boost-type PWM rectifier (also known as *VIENNA Rectifier*) are:

I. input inductances are situated on the mains side (not on the DC-side)
II. a bidirectional, bipolar switching element exists in each phase

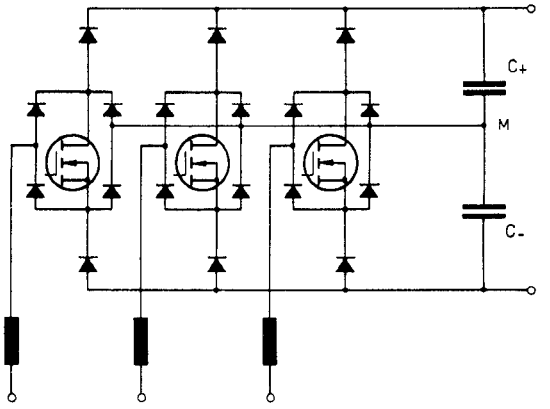

Fig.1: Basic structure of the power circuit of a three-phase three-switch three-level boost-type PWM (VIENNA) rectifier according to [1].

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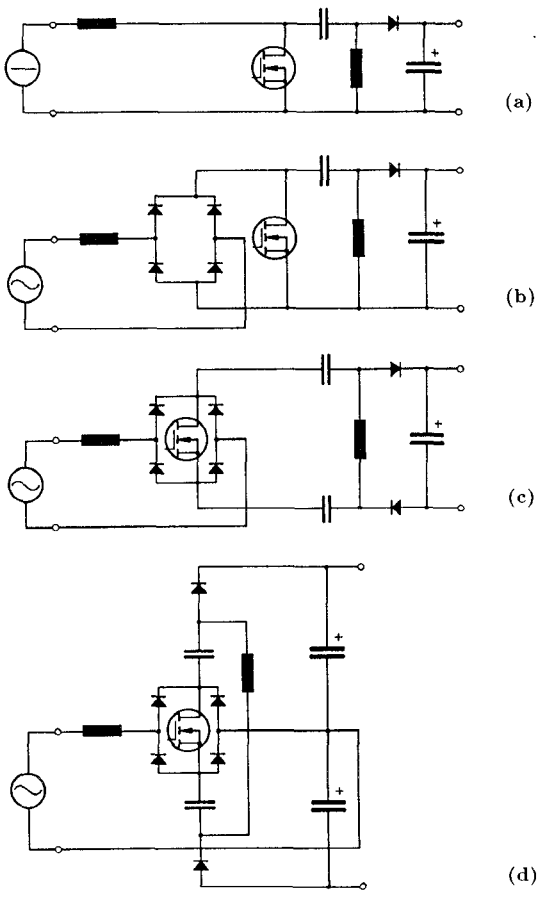

Fig.2: Derivation of the topology of one bridge leg (cf. Fig.2(d)) of a three-phase three-switch three-level AC-to-DC SEPIC converter (cf. Fig.3) based on the basic structure of a DC-to-DC SEPIC converter (cf. Fig.2(a)).

III. symmetrical structure of each phase leg and/or of the negative and positive bridge half

IV. connection of an output of the switching element of each phase with the capacitive center point of the output voltage

V. phase legs have identical structure and are connected in parallel on the DC (output) side.

Remark: In [5], [6], [7] and [8] boost-type three-phase three-switch converters have been proposed which possess structures which differ from the structure of the circuit (cf. Fig.1) on which the compilation given here is based. These systems have no connection of the switching elements to the center point of the output voltage. One also can say that they have a two-level and not a three-level characteristic of the bridge legs. Due to the therefore higher blocking voltage stresses on the power semiconductors and the higher harmonics level of the mains current (for equal switching frequency) these systems are not considered in more detail here.

Based on the consideration of the topological characteristica one can now derive simply step-by-step the converter structure of a phase of a three-phase/switch/level AC-to-DC SEPIC converter. In **Fig.2**(a) the basic structure of a DC-to-DC SEPIC converter is shown which forms the starting point of the considerations. By connecting a single-phase diode bridge in series at the input one obtains an AC-to-DC converter structure which has been proposed for single-phase power factor correction, e.g., in [9] (and also is described, e.g., in [10]). There, the input inductance has to be positioned on the AC side with regard to the three-phase extension according to topological requirement I of the list given (cf. Fig.2(b)). The diode bridge and the turn-off power semiconductor now form a bidirectional, bipolar switching element. With this, also requirement II is fulfilled. With regard to requirement III we have to extend Fig.2(b) in a further step to a symmetrical circuit structure by adding a coupling capacitor and an output diode (cf. Fig.2(c)). Due to the complete isolation of the output circuit by the coupling capacitors one can now freely define the potential relationship between input and output of the resulting circuit. Considering requirement IV the potential of the output

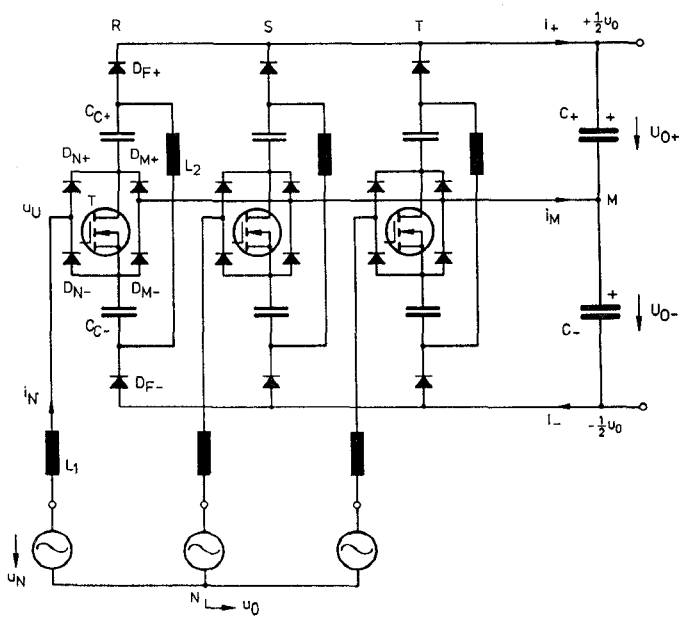

Fig.3: Basic structure of the power circuit of a novel three-phase three-switch three-level AC-to-DC SEPIC-type PWM rectifier system.

circuit is determined by a connecting lead between the capacitive center point of the output voltage (formed by a symmetrical splitting up of the output capacitor and one terminal of the input-side switching element (cf. Fig.2(d)).

With the DC side parallel connection of three phase legs of identical structure and the combination of the output capacitors into C_+ and C_- we finally receive the desired circuit of a three-phase/switch/level AC-to-DC SEPIC converter. (cf. **Fig.3**). There, it is important to point out that with the assumption of a symmetrical three-phase mains current system (which is impressed by an appropriate current control circuit) a connection between the mains star point N and the center point M of the output DC voltage can be omitted. Then we have (as being characteristic in general for three-phase PWM converters) a coupling of the phase legs, i.e., the change of the switching state of one phase influences (due to the thereby changing voltage between N and M) also the current shape in the two other phases. If, e.g., three independent on-off phase current controllers are provided for controlling of the mains current, then always one phase current is controlled by the the controllers of the two other phases and/or one phase is not being switched. (This is described, e.g., in [11] for a bidirectional PWM converter system.) This becomes clearly understandable also under consideration of the sum of the phase currents which is being forced to zero for no star point connection.

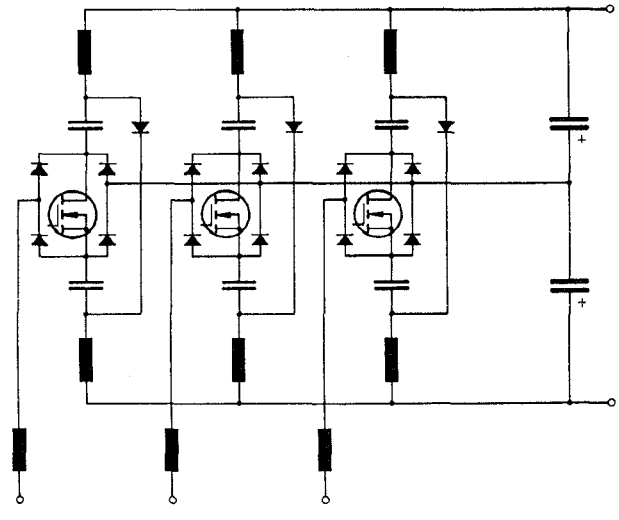

Fig.4: Basic structure of the power circuit of a novel three-phase three-switch three-level AC-to-DC Cuk-type PWM rectifier system.

As opposed to a decoupling of the phases and/or splitting up of the three-phase system into three single-phase systems by connecting points M and N we receive thereby a required harmonic level of the mains current with considerably lower switching frequency. In the same manner an advantage is given for a control of the converter based on a suboscillation method or on a space vector modulation method (cf. section III in [12]). Because a floating mains star point suppresses a current generation by zero sequence components of the phase voltages (of harmonics with ordinal numbers $k = 3, 9, 15 \ldots$) , one can obtain there an essential reduction of the mains current harmonics with switching frequency by addition of zero sequency components to the phase reference values [13] as compared to pure sinusoidal modulation to be provided for decoupling of the phases.

The procedure presented so far (in conncetion with the derivation of the circuit of a three-phase/switch/level SEPIC-type converter) can be transferred in an analogous manner also to a DC-to-DC Cuk converter structure. The circuit of a three-phase/switch/level AC-to-DC Cuk-type converter resulting herefrom is shown in **Fig.4**. As compared to the SEPIC-type converter structure this system has a higher realization effort (three inductive components per phase), however. Therefore, in this paper a more detailed discussion shall be limited to the SEPIC-type system for the sake of brevity.

Remark: For completeness we want to mention here three-phase *single-switch* Cuk- and SEPIC-type converter systems as proposed in [14], [15], [16] and in Figs.4(a)–(c) in [17]. These circuits show (contrary to the circuits according to Figs.3 and 4) a *discontinuous* mains current shape and, therefore, a higher filtering effort for limiting the effects on the mains with switching frequency. Furthermore, the circuits are characterized by a low-frequency deviation of the mains current from the ideal sinusoidal shape and a high stress on the components. On the other hand, these circuits have the advantages of a possible isolation of the output circuit and a very simple control structure.

3 Basic Considerations

As first step for the analysis of the functional principle of the circuit shown in Fig.3 we will consider the conduction states of a bridge leg for positive and negative phase current in the following. Also, the equations describing the operating behavior of the bridge leg are derived. Then, the charging/discharging processes occurring after each zero-crossing of the phase current between positive and negative half of the bridge leg are discussed.

3.1 Conduction States of a Bridge Leg for Positive and Negative Input Current

In the following the bridge leg in a first approximation is considered as DC-to-DC converter with (relative to the switching frequency) slowly varying input voltage $u'_N = u_N + u_{0,\mathrm{avg}}$. This means that the input voltage is approximately constant for one on-off cycle (a pulse period) of the power transistor. Furthermore, a continuous time-behavior of the currents in L_1 ad L_2 is assumed. This corresponds to a typically given operation for practical realization of the system for low effects on the mains and a low stress on the circuit elements.

u_N denotes the mains phase voltage and $u_{0,\mathrm{avg}}$ the local average value (related to a pulse period) of the voltage

$$u_0 = u_N - u_M \tag{1}$$

with switching frequency between the mains star point N and the center point M of the output voltage of the system. u_0 describes the coupling of the phase legs as already mentioned in section 2. As one can see immediately, each switching state change of a phase influences the instantaneous value of u_0. The analytical derivation of $u_{0,\mathrm{avg}}$ will be provided in section 5.

The current paths of the bridge leg being active for positive and negative input current $i_N > 0$ and/or $i_N < 0$ for the on- and off-state of the power transistor T are are shown in **Figs.5**(a) and (b) and/or Figs.5(c) and (d). The switching state of T is denoted by a switching function s in the following for the sake of brevity. There, $s = 1$ stands for power transistor on, $s = 0$ for power transistor off.

Due to the symmetrical structure of the phase leg the following considerations can be limited to $i_N > 0$. According to the desired resistive input behavior of the rectifier system $u'_N > 0$ is assumed there. As Fig.5(a) and (b) clearly show, the current flow through the devices L_1, T, C_{C+} and D_{F+} then corresponds completely to the conditions given for a conventional DC-to-DC SEPIC converter. There, u_{C+} has to be seen as output voltage. The only

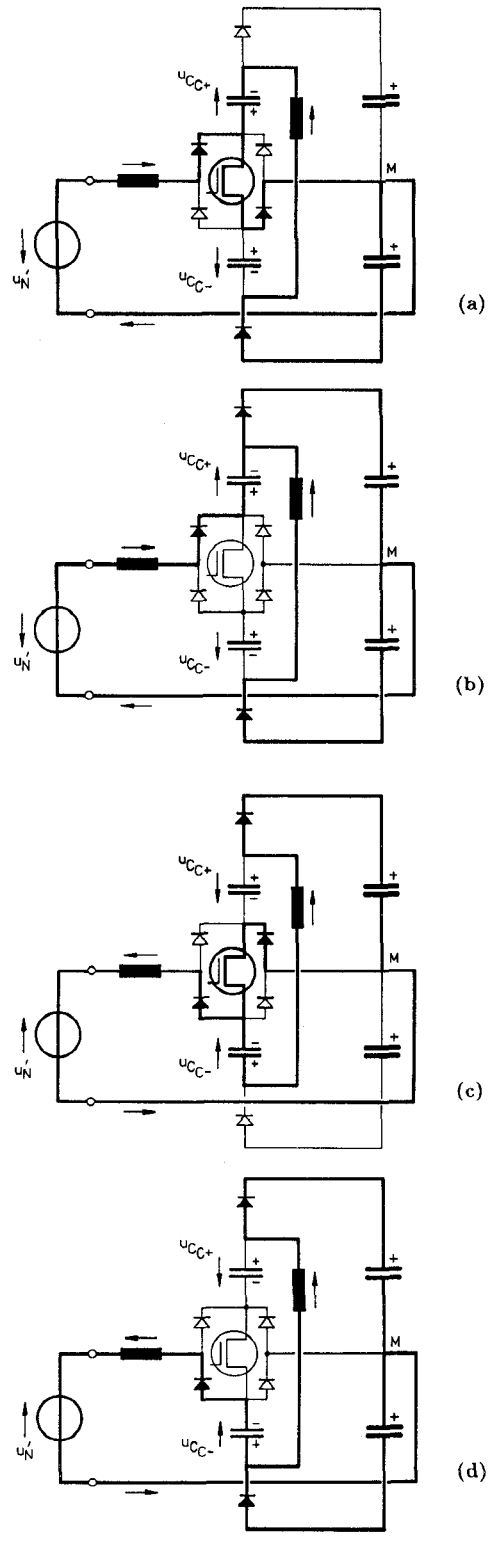

Fig.5: Conduction states of a bridge leg of a three-phase/switch/level SEPIC-type PWM rectifier within a pulse period for positive (cf. **(a)** and **(b)**) and negative (cf. **(c)** and **(d)**) input current i_N (continuous current shape in L_1 and L_2, i.e. continuous inductor current mode, assumed; output current not shown); (a) and (c): power transistor turned on ($s = 1$) , (b) and (d): power transistor turned off ($s = 0$).

speciality of the bridge leg consists in the return path of the current in L_2 leading via the negative output voltage bus and a part U_{O-} of the total output voltage U_O. Theoretically, for $s = 1$ also a return of the current i_{L_2} via C_{C-} would be thinkable (for $u_{C_{C-}} < \frac{1}{2}U_O$). Because for positive input current

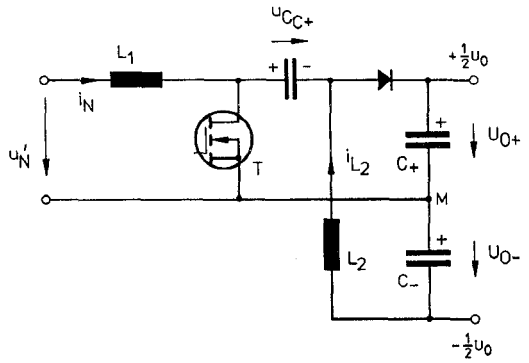

Fig.6: Structure of the power circuit of a DC-to-DC SEPIC converter with shifted negative output voltage potential; the circuit represents the equivalent circuit of a bridge leg of the system shown in Fig .3 for positive phase current $i_N > 0$; the basic structure of the power circuit of a conventional DC-to-DC SEPIC converter is shown in Fig.2(a).

certainly no discharge of C_{C-} takes place, this would mean a steady increase of $u_{C_{C-}}$, however. Then after several pulse periods finally $u_{C_{C-}} = \frac{1}{2}U_O$ would be reached and a further increase of $u_{C_{C-}}$ would be inhibited by D_{F-} which then acts as a clamping device. In the stationary case i_{L_2} then flows through D_{F-} in any case. Therefore, C_{C-} does not participate in the current conduction (for $i_N > 0$) and has a voltage of $u_{C_{C-}} = \frac{1}{2}U_O$. Because in the stationary case no DC voltage component exists across L_2, $C_{C+}$is then connected on one side with the negative output voltage bus. Accordingly, the voltage $u_{C_{C+}}$ is determined not (as for the conventional SEPIC converter) exclusively by the input voltage u'_N but by the sum $u'_N + U_{O-} = u'_N + \frac{1}{2}U_0$.

3.2 Mathematical Description of a Bridge Leg

Based on the previous considerations we can now give directly a mathematical description of the stationary operating behavior and of the current and voltage conditions of a bridge leg of the rectifier system.

The analysis is limited to $i_N > 0$ for the sake of brevity. The equivalent circuit being valid in this case for the phase leg is shown in **Fig.6** (limited to the active current paths). As characteristic system quantities we consider the local average values of the voltages and of the currents as well as the average value of the switching function s, i.e. the duty cycle α. For the sake of clarity we want to omit the special notification of the averaging by an index *avg* for the quantities $u_{C_{C+}}$, $u_{C_{C-}}$, i_N and i_{L_2} which basically show a continuous time behavior.

The stationary operation of the system is, as becomes immediately clear, characterized by

$$u_{L_1,\text{avg}} = 0 \tag{2}$$
$$u_{L_2,\text{avg}} = 0 \tag{3}$$
$$i_{C_{C+},\text{avg}} = 0\ . \tag{4}$$

For the voltage across the coupling capacitor C_{C+} there follows then (by considering Eqs.(2) and (3)), as already treated,

$$u_{C_{C+}} = u'_N + \frac{1}{2}U_O\ . \tag{5}$$

For the voltage transformation there follows with Eq.(2) and/or with $(u_{C_{C+}} - \frac{1}{2}U_O)\alpha = (u_{C_{C+}} + \frac{1}{2}U_O)(1-\alpha)$

$$U_O = \frac{\alpha}{1-\alpha}u'_N\ . \tag{6}$$

There,

$$u'_N = u_N + u_{0,\text{avg}} \tag{7}$$

is the effective mains voltage for the phase leg related to the center point M of the output voltage. Based on this, there follows for the average local duty cycle

$$\alpha = \frac{U_O}{\frac{1}{2}U_O + u_{C_{C+}}} = \frac{U_O}{U_O + u'_N} \tag{8}$$

($u_{0,\text{avg}}$ will be calculated in section 5, cf. Eqs.(26) and (28)). Because according to Eq.(4) no resulting current flow via C_{C+} takes place, we have for the power balance between input and output of the bridge leg

$$u'_N\, i_N = U_O\, i_{L_2}\ . \tag{9}$$

With this there results with Eq.(8)

$$i_{L_2} = \frac{1-\alpha}{\alpha}\, i_N \tag{10}$$

for the relationship between input and/or mains phase current i_N and current i_{L_2} in the output inductance L_2.

Remark: We want to recall here that the previous calculations have been based on $i_N > 0$. Therefore, Eq.(10) must not be misinterpreted as generally valid relation between mains phase current i_N and current i_{L_2}. This would lead to the conclusion that i_{L_2} would be negative for $i_N < 0$. i_{L_2} has (according to the power supply to the output) a positive sign for the positive *and* negative input current half cycle.

Eq.(4) shows clearly that the positive and negative partial output voltages U_{O+} and U_{O-} are fed by the same local current average value

$$i_{+,\text{avg}} = i_{-,\text{avg}} = i_{L_2}\ . \tag{11}$$

For the local average value of the transistor current there follows finally, also by considering Eq.(4)

$$i_{T,\text{avg}} = i_{L_1}\ . \tag{12}$$

In summary we have to point out that the operating behavior of the bridge leg and its current and voltage distribution (with the exception of the voltage across the coupling capacitor) is completely identical to that of a conventional DC-to-DC SPEC converter (cf. Fig.2(a)). This also becomes clear due to the consistency of the blocking voltage and current stresses on the power transistors and on the output diodes of the circuits according to Figs.6 and 2(a) (ripple contributions are not considered).

For the local blocking voltage stress on the power transistor T and on the output diode D_{F+} of the bridge leg we have (as can be derived in a short way)

$$u_{T,\text{max}} = u_{C_{C+}} + \frac{1}{2}U_O = u'_N + U_O\ . \tag{13}$$

The local maximum value of the current in T and D_{F+} follows as

$$i_{T,\text{max}} = i_{D_{F+},\text{max}} = i_N + i_{L_2}\ . \tag{14}$$

Remark: Despite the connection of the power transistor with the center point of the output voltage its blocking voltage stress and the blocking voltage stress on the output diodes (contrary to a three-phase/switch/level boost-type PWM rectifier system; cf. Fig.9 in [1]) is determined by the total value and not only by half the output voltage. This is basically due to the fact that the system has only one inductance L_2 for each bridge leg and not separate partial inductances (connected to M) for the positive and negative bridge half and/or for positive and negative input current. The reduction of the realization effort finally is paid for by an increase of the blocking voltage stress on the valves. Especially for low output voltage levels (as compared to the mains voltage) there does not follow a substantial disadvantage, however.

3.3 Behavior of a Bridge Leg After Zero Crossing of the Input Current

As a comparison of Figs.5(a) and (c) and/or (b) and (d) yields, the coupling capacitors C_{C+} and C_{C-} for $i_N > 0$ and $i_N < 0$ have opposite voltage polarities. There, one has to ask the question regarding the time behavior of the charging process within a bridge leg being required after each zero crossing of the corresponding input phase current (having approximately sinusoidal shape).

In the following we consider the system behavior after a sign change of the current from $i_N > 0$ to $i_N < 0$ in $t = t_0$. The resulting conduction states of a phase leg are shown in **Fig.7**. For the sake of clarity the representation is simplified and an always continuous shape of i_N and i_{L_2} is assumed. In reality this assumption will not be met due to the finite ripple of i_N and i_{L_2} in the immediate vicinity of t_0 (with i_N also i_{L_2} approaches the value 0 according to Eq.(10)). As a closer analysis by digital simulation proves, the basic behavior of a bridge leg is described correctly also for the assumption of continuous current shapes, however.

A basic difficulty of the analysis of the charging process is given by the fact that the change of the voltage across C_{C+} and C_{C-} also has influence on the input voltage part $u_{0,\text{avg}}$. As a digital simulation shows and as is checked by the considerations of section 5, there occurs a sign change of $u_{0,\text{avg}}$ in each zero crossing of a phase current. For the sake of clearness and simplicity this

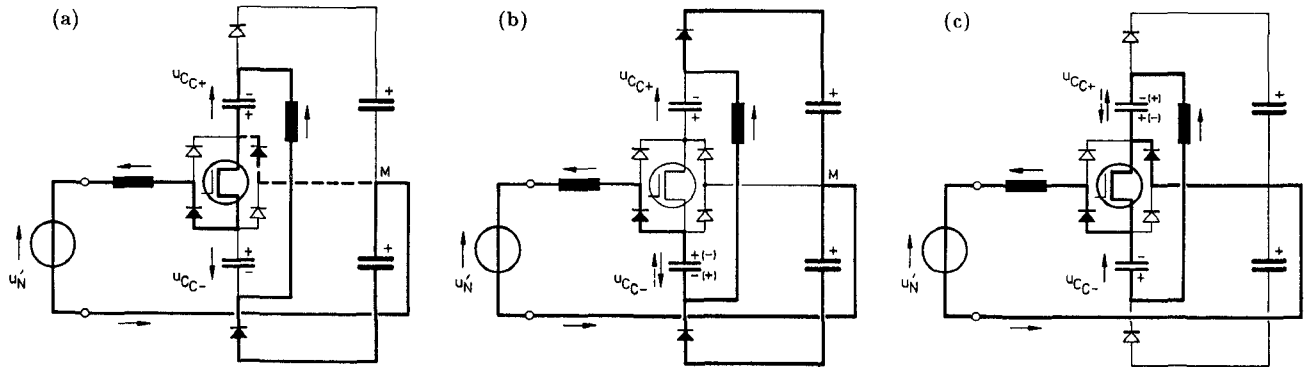

Fig.7: Conduction states of a bridge leg during charging/discharging of the coupling capacitors C_{C+} and C_{C-} after a sign change of the corresponding input current from $i_N > 0$ to $i_N < 0$ in $t = t_0$ (a continuous shape of the currents in L_1 and L_2 is assumed); **(a):** Conduction state after turning-on the power transistor in $t = t_0$, **(b)** and **(c):** $t > t_0$, power transistor off and/or on.

change of $u_{0,avg}$ will not be considered further and $u_{0,avg} \approx 0$ is assumed instead.

As marked in Fig.7(a), C_{C+} and C_{C-} keep the charging status given for $i_N > 0$ and/or $u'_N > 0$ immediately after the zero crossing of i_N.This is due to the fact that with $i_N \to 0$ and $i_{L_2} \to 0$ also $\frac{du_{C_{C+}}}{dt} \to 0$ results; therefore, $u_{C_{C+}}$ cannot follow the input voltage u'_N (cf. Eq.(5)).

Now, if the power transistor is turned on, the already negative mains voltage and/or the voltage across C_{C+} causes an increase of $|i_N|$ and i_{L_2} starting from 0 resulting in the conduction state shown in Fig.7(a) (discharge of C_{C+}). Because the current flow $i_N < 0$ can exist only alternatively via D_{M+} or C_{C+} (and L_2), we have in this case $i_{L_2} \leq i_N$, where D_{M+} does not carry current for $i_{L_2} = i_N$.

Due to the turn-off of T (cf. Fig.7(b)) i_{L_2} commutates into the free-whelling diode D_{F+}. Therefore, the total value of the output voltage results across L_2 giving a relatively fast decrease of i_{L_2}. Contrary to that i_N remains approximately constant and/or is increased in negative direction (the rate of change of i_N is dependent on u_N). The voltage across C_{C-} is decreased starting from $u_{C_{C-}} = \frac{1}{2}U_O$.

With $u_{C_{C-}} < \frac{1}{2}U_O$ the condition for conduction ($u_{C_{C-}} = \frac{1}{2}U_O$ and/or $u_{D_{F-}}$) of D_{F-} is not met any more after turn-on of T. The current flow i_{L_2} driven by $u_{C_{C+}}$ (further discharge of C_{C+}) which is being increased now will cause further (however, only minor) recharging of C_{C-} (cf. Fig.7(c)). i_N is being increased further by u_N.

The steady increase of i_N and the limitation of i_{L_2} to relatively small values (due to the demagnetization of L_2 via U_O) leads after several switching intervals (changing back and forth between Figs.7(b) and (c)) finally to a polarity change of C_{C-}. Therefore, a support for $u_{C_{C+}}$ for the magnetization of L_2 during the turn-off intervals of T is given. Now, i_{L_2} is increased relatively fast, this speeds up the discharge of C_{C+} and leads finally to a polarity change of $u_{C_{C+}}$ and/or $u_{C_{C+}} < 0$.

The charging/discharging process of the bridge leg is finished when the voltage across C_{C+} reaches $u_{C_{C+}} = -\frac{1}{2}U_0$. Then, also for turned-on transistor T the condition for conduction of D_{F+} ($u_{D_{F+}} = 0$) is fulfilled and the (stationary) conditions already shown in Figs.5(c) and (d) are given.

4 Digital Simulation

After explaining the functional principle of a phase leg, we now want to present an overview over the (stationary) operating behavior of the entire system. For this purpose we will show in the following characteristic current and voltage shapes as determined by digital simulation.

4.1 Assumptions

In order to 'stick to the essentials' we want to assume the partial output voltages as being impressed for the simulation of the rectifier system. Therefore, one can disregard an output voltage control circuit. Furthermore, ideal valves (neglection of on-state voltages, switching times, etc.) and ideal passive components are assumed.

For the control of the mains phase currents independent ramp-comparison controllers (cf. **Fig.8**) are employed (cf. Fig.5 in [18] or section III-C in [19]). There, the control errors of the phase currents are being compared to a triangular signal (being equal for all 3 phases) with switching frequency. This comparison yields the switching commands for the power transistors. Thereby, a very simple PWM procedure with direct current impression is realized. Also, the mathematical description of the current control (cf. section 5) is possible with very little effort. The reference values of the phase currents are given in phase to the corresponding mains phase voltages according to the desired resistive mains behavior of the system.

Remark: With regard to an as simple as possible realization of the phase current control also the application of independent tolerance band controllers (hysteresis contollers) would be obvious. As has become clear during the tests of different current control methods by digital simulation, thereby, however, the charging/discharging of the phase legs in the phase current zero crossings is substantially disturbed due to the clamping of one bridge leg in each case in different time intervals (cf. Fig.8 in [11]). This results in a very much irregular time behavior of the currents and voltages (with exception of the impressed phase currents) and in a relatively high switching frequency [20].

The current control by a ramp-comparison current controller is being applied also for switched-mode power supply systems. However, there it is usually called *average current mode control* [21] and the comparison signal shows sawtooth shape. In connection with three-phase systems a sawtooth

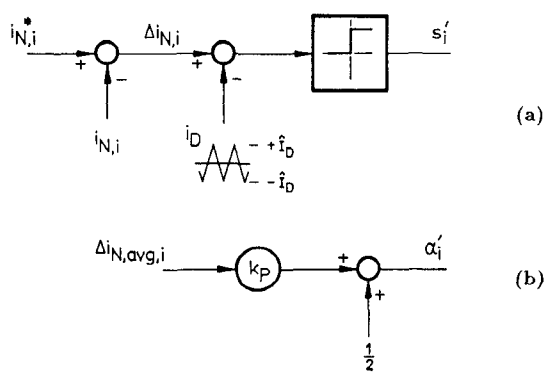

Fig.8: Generation of the control signals s_i for the power transistor T_i of a bridge leg by comparison of the control error $\Delta i_{N,i}$ of the corresponding phase current $i_{N,i}$ with a triangular signal i_D (being equal for all phases) with amplitude $\hat{I}_D$ and frequency f_P (cf. **(a)**, ramp comparison control [18]); because at the input of the rectifier system voltages $u_{U,i}$ of opposite sign are formed for positive and negative phase current $i_{N,i}$, the switching decision s'_i of the current control has to be inverted for $i_{N,i} < 0$ (i.e., $s_i = s'_i$ for $i^*_{N,i} \geq 0$ and s_i =NOTs'_i for $i^*_{N,i} < 0$, cf. Eq.(13) in [1]); **(b)**: equivalent circuit of the phase current control for averaging of the input and output quantities over a pulse period $T_P = f_P^{-1}$; the intersection of $\Delta i_{N,i}$ with i_D as shown in (a) therefore realizes a P-control element with gain $k_P = \frac{1}{2\hat{I}_D}$ and the relative on-time α_i of the power transistor as output variable.

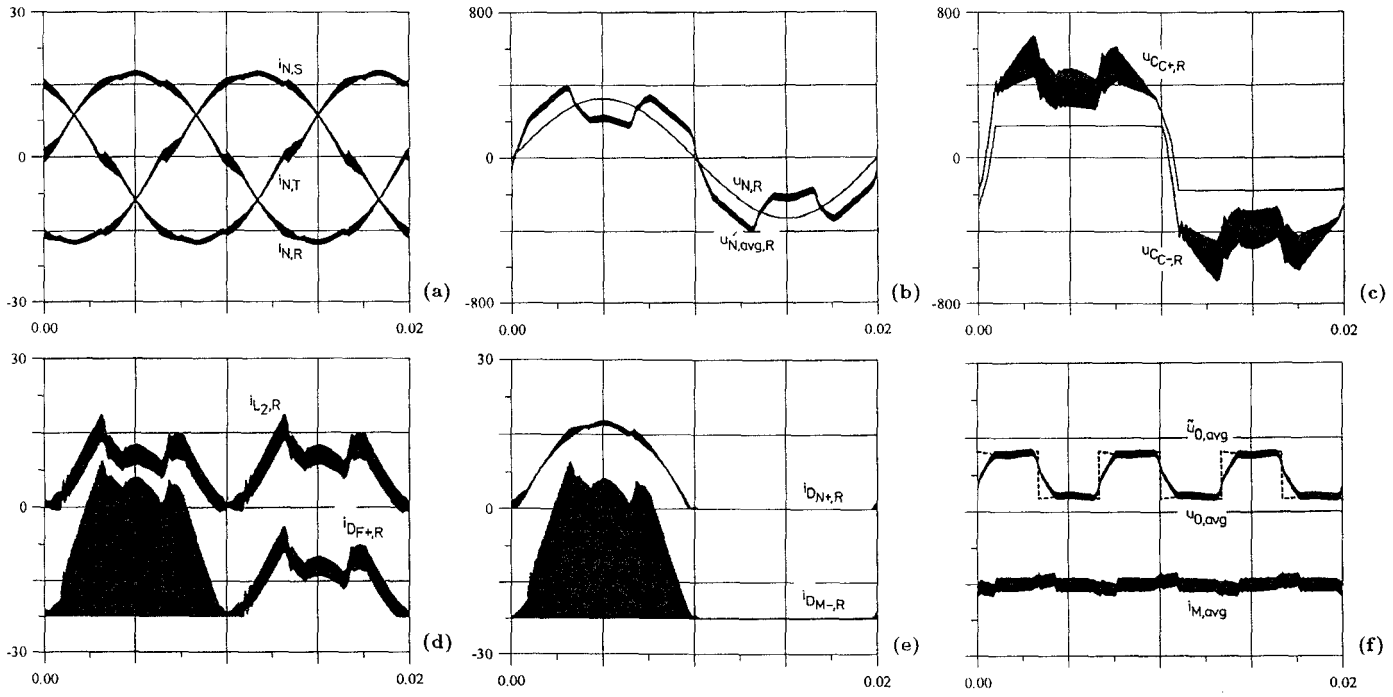

Fig.9: Results of the digital simulation of a three-phase/switch/level SEPIC-type PWM rectifier; representation of the time shapes for a mains period; **(a)**: mains pahse currents $i_{N,i}$, $i = R, S, T$, **(b)**: mains phase voltages $u_{N,R}$ (related to the mains star point N) and locally averaged (by a RC low-pass filter of 1st order with time constant $RC = 100\,\mu s$) *effective* mains voltage $u'_N = u_N + u_{0,avg}$ (cf. Eq.(7) and Fig.5); **(c)**: voltages across the coupling capacitors $C_{C+,R}$ and $C_{C-,R}$; **(d)**: current $i_{L_{2,R}}$ in the inductance $L_{2,R}$ and current $i_{D_{F+,R}}$ through the free-wheeling diode $D_{F+,R}$; scale related to $i_{L_{2,R}}$; **(e)**: current $i_{D_{N+,R}}$ in the input diode $D_{N+,R}$ and current $i_{D_{M-,R}}$ in the center point diode $D_{M-,R}$; scale related to $i_{D_{N+,R}}$; **(f)**: locally averaged (by a RC low-pass filter of 1st order with time constant $RC = 100\,\mu s$) voltage u_O appearing between mains star point N and output voltage center point M as well as local average value $i_{M,avg}$ of the current i_M fed into M; furthermore shown are: the approximation $\tilde{u}_{0,avg}$ of the shape of the voltage $u_{0,avg}$ as calculated in section 5 (where the charging/discharging process within a bridge leg after zero crossing of the associated phase current is not considered); 400 V/div, 20 A/div.

signal (being equal for all phases) would lead to unnecessary synchronous switching actions of the phase legs (caused by the trailing edges). Therefore, a comparison signal consisting of equilateral triangles has to be preferred; it forms a new voltage state (voltage space vector) across the input side of the rectifier system by switching of only one phase in each case.

We choose for the device and operating parameters:

$$\begin{aligned} U_{N,\mathrm{rms}} &= 230\,\mathrm{V} \\ \hat{I}_N^* &= 18\,\mathrm{A} \\ U_O &= 350\,\mathrm{V} \\ L_1 &= 1\,\mathrm{mH} \\ L_2 &= 1\,\mathrm{mH} \\ C_{C\pm} &= 1\,\mu\mathrm{F} \\ f_P &= 32\,\mathrm{kHz} \\ \hat{I}_D &= 2.5\,\mathrm{A} \end{aligned}$$

($U_{N,\mathrm{rms}}$ denotes the rms value of the mains voltage, $\hat{I}_N^*$ the amplitude of the phase current reference values, $\hat{I}_D$ the peak value of the triangular comparison signal of the phase current controllers).

The value of the output voltage U_O has been chosen with respect to a possible application of the system for charging of the batteries of electric vehicles with higher operating voltages.

4.2 Simulation Results

The results of the simulation of the rectifier system (signal shapes within a mains period) are shown in **Fig.9**.

The simulations have been carried out by using the multi-level simulator *CASPOC*™ [22]. This program package, which (1) is especially designed for the simulation of power electronic systems and for the application on PCs has a user interface similar to *SPICE*™. Further advantages are (2) high numerical stability, (3) computation time efficiency, (4) the possibility for direct graphical output of the simulation results during a simulation run as well as for (5) interactive operation during a simulation run.

Considering the simplicity of the current control method used, the mains phase currents $i_{N,i}$, $i = R, S, T$ show a very good sinusoidal shape (cf. **(a)**). The spectrum of a mains phase current is shown in **Fig.10** (where the fundamental is suppressed) for limitation to the low-frequency components which are especially important for the judgement of the effects on the mains. The minor distortions of the phase currents in the zero crossings are caused by the charging/discharging processes in the phase legs (as described in section 3.3. There, the distortion of a phase current also influences the two other phase currents (because the sum is being forced to 0). The amplitudes of the low-frequency harmonics (resulting from the current distortion) remain limited to noncritical values $< 2.5\%$ of the fundamental.

In Fig.7(b) the shape of the phase voltage $u_{N,R}$ (related to the mains star point N) is given as well as the *effective* mains voltage $u'_N = u_N + u_{0avg}$ (related to the outout voltage center point M) being determining for the actual system behavior. For averaging of the discontinuous voltage u_0 (with pulse frequency) a RC low-pass filter of 1st order with time-constant $RC = 100\,\mu s$ has been applied. The resulting shape of the output voltage $u_{0,avg}$ is shown in Fig.7(f) besides the (equally formed) local average value $i_{M,avg}$ of

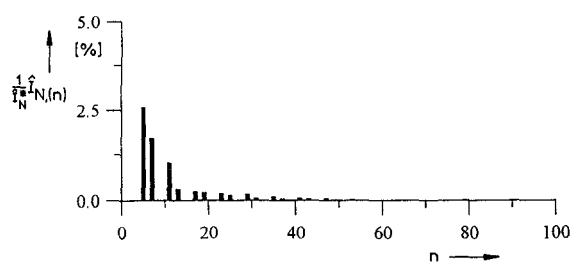

Fig.10: Low frequency harmonics $\hat{I}_{N,(n)}$ of the mains phase current (cf. Fig.9(a)) related to the amplitude $\hat{I}_{N,(1)} \approx \hat{I}_N^*$ of the fundamental; fundamental n = 1 suppressed; n denotes the ordinal number of the harmonics.

the current i_M being fed into M. Furthermore, also the voltage shape $\tilde{u}_{0,\mathrm{avg}}$ resulting from an approximate analytical description of the system behavior (cf. section 5) is given in this figure.

Fig.7(c) shows the voltages across the coupling capacitors $C_{C+,R}$ and $C_{C-,R}$. There, it is interesting to note especially the siganl shape in the regions following the zero crossings of the corresponding phase current $i_{N,R}$. This checks the considerations regarding the charging/discharging processes in the bridge legs (cf. section 3.3)

Finally, in Figs.7(d) and (e) the shape of the current $i_{L_{2,R}}$ in the DC-side inductance $L_{2,R}$, and the current shapes $i_{D_{F+,R}}$, $i_{D_{N+,R}}$ and $i_{M-,R}$ to be associated with the free-wheeling diode $D_{F+,R}$, with the input diode $D_{N+,R}$ and with the center point diode $D_{M-,R}$ are shown. For the sake of brevity we only want to point out the relatively flat rate of rise of $i_{L_{2,R}}$ (flat in comparison to $i_{N,R}$) after the zero crossings of $i_{N,R}$ (cf. Fig.7(a)). This already has been derived in section 3.3.

5 Mathematical Analysis of the Three-Phase System

For the sake of brevity the mathematical analysis of the stationary operating behavior of the rectifier system has to be limited in this paper to the calculation of the voltage $u_{0,\mathrm{avg}}$ which describes the coupling of the phases. As already mentioned $u_{0,\mathrm{avg}}$ denotes the local average value of the voltage u_0 over a pulse period as actually existing between the mains star point N and the center point M of the output voltage.

The selection of $u_{0,\mathrm{avg}}$ is based on the essential importance of this quantity for a further calculation of the system behavior as also becomes clear from the simulation results shown in Fig.9. With the exception of the mains phase currents (being impressed by the current control) all current shapes and the the shapes of the voltages across the coupling capacitors C_{C+} and C_{C-} (and, therefore, also the stresses on the components) are essentially influenced by the shape of $u_{0,\mathrm{avg}}$.

If $u_{0,\mathrm{avg}}$ is known, the bridge legs can be considered separately; then, e.g., the relative on-time α_i of the power transistor T_i as being required for the calculation of the on-state losses, can be determined. The structure of the equivalent circuit one has to apply there already has been shown in in section 3 (cf. Fig.5); there $u_{0,\mathrm{avg}}$ is assumed to be in series to the actual mains phase voltage $u_{N,i}$. This results in an effective overall input voltage $u'_N = u_N + u_{0,\mathrm{avg}}$ (related to M).

5.1 Coupling of the Phases

According to the results of the digital simulation of the system behavior, $u_{0,\mathrm{avg}}$ is essentially influenced by the signs of the phase currents (cf. Fig.7(f)). For the further considerations we assume

$$\begin{array}{l} i_{N,R} > 0 \\ i_{N,S} \leq 0 \\ i_{N,T} \leq 0 \,. \end{array} \tag{15}$$

Due to the mains behavior being assumed as resistive, corresponding relations are valid for the associated mains phase voltages $u_{N,i}$, $i = R, S, T$.

In analogy to Eq.(5) we have for the single bridge legs

$$\begin{aligned} u_{C_{C+},R} &= u_{N,R} + u_{0,\mathrm{avg}} + \frac{U_O}{2} \\ -u_{C_{C-},S} &= u_{N,S} + u_{0,\mathrm{avg}} - \frac{U_O}{2} \\ -u_{C_{C-},T} &= u_{N,T} + u_{0,\mathrm{avg}} - \frac{U_O}{2} \,. \end{aligned} \tag{16}$$

Furthermore, we have with Eq.(8)

$$\begin{aligned} \alpha_R &= \frac{U_O}{\frac{1}{2}U_O + u_{C_{C+},R}} \\ \alpha_S &= \frac{U_O}{\frac{1}{2}U_O + u_{C_{C-},S}} \\ \alpha_T &= \frac{U_O}{\frac{1}{2}U_O + u_{C_{C-},T}} \,. \end{aligned} \tag{17}$$

Remark: We have to point out here that Eqs.(16) and/or Eqs.(17) do not handle the charge/discharge process of $C_{C+,T}$ and $C_{C-,T}$ occurring after the zero crossing of the phase current $i_{N,T}$. Therefore, the relation for $u_{0,\mathrm{avg}}$ derived in the following here will be valid only in a sufficient distance of $i_{N,T} = 0$. A detailed description of the charge/discharge process would lead to rather involved mathematical expressions and shall be omitted in this paper which is oriented towards basic considerations.

For a complete mathematical description of the power circuit of the system we have to introduce now also the relation

$$i_{N,R} + i_{N,S} + i_{N,T} = 0 \tag{18}$$

being valid due to the floating mains star point N. Eq.(18) now has to be combined with the duty cycles α_i. The thought would be obvious here to select the power balance between mains and DC-side

$$p_{O,\mathrm{avg}} = u_{N,R}\, i_{N,R} + u_{N,S}\, i_{N,S} + u_{N,T}\, i_{N,T} = U_O(i_{L_2,R} + i_{L_2,S} + i_{L_2,T}) \tag{19}$$

(which follows immediately under consideration of $i_{C_{C\pm},i,\mathrm{avg}} = 0, i = R, S, T$) as coupling equation. There, for the currents in the DC-side inductances we would have to set (in analogy to Eq.(10))

$$\begin{aligned} i_{L_2,R} &= i_{N,R}\frac{1-\alpha_R}{\alpha_R} \\ i_{L_2,S} &= -i_{N,S}\frac{1-\alpha_S}{\alpha_S} \\ i_{L_2,T} &= -i_{N,T}\frac{1-\alpha_T}{\alpha_T} \,. \end{aligned} \tag{20}$$

This approach fails, however; due to the assumption of negligible average voltages across the inductances and negligible average currents through the coupling capacitor made for the derivation of the equations given before Eq.(19) is already fulfilled implicitely (and/or in linear dependency on the other determining equations). Due to the now too low number of determining equations (10 equations, where Eq.(19) is not considered, and 13 unknowns), the set of equations Eq.(16) - Eq.(20) could not be solved in a unique manner.

The equations still missing for a determination of the system state can only be obtained by the description of the function of the phase current controllers. This becomes immediately clear by inspection because the current controllers define directly the required dependencies of the relative on-times of the power transistors on the phase currents. For the duty ratios we have for ramp-comparison-control

$$\begin{aligned} \alpha_R &= \frac{1}{2} + k_P(i^*_{N,R} - i_{N,R}) \\ \alpha_S &= \frac{1}{2} - k_P(i^*_{N,S} - i_{N,S}) \\ \alpha_T &= \frac{1}{2} - k_P(i^*_{N,T} - i_{N,T}) \,; \end{aligned} \tag{21}$$

there

$$k_\mathrm{P} = \frac{1}{2\hat{I}_D} \tag{22}$$

denotes the gain given in the average over a pulse period for the intersection of the control error with a triangular signal with amplitude $\hat{I}_D$ (k_P corresponds to the gain of a simple pulse-width modulation, cf. Fig. 8(b)). Because for positive and negative phase current $i_{N,i}$ at the input of the rectifier system voltages $u_{U,i}$ of different sign are formed, the switching decision s'_i of the current controllers for $i_{N,i} < 0$ has to be inverted (i.e., $s_i = s'_i$ for $i^*_{N,i} \geq 0$ and s_i =NOTs'_i for $i^*_{N,i} < 0$, cf. Eq.(13) in [1]); this becomes clear in Eq.(22) by the negative signs of the control errors $\Delta i_{N,S}$ and $\Delta i_{N,T}$.

For Eq.(21) there follows for assuming of a symmetrical current reference value system

$$i^*_{N,R} + i^*_{N,S} + i^*_{N,T} = 0 \,; \tag{23}$$

then (if the phase equations Eq.(21) are combined), the relation

$$\alpha_R - \alpha_S - \alpha_T = -\frac{1}{2} \tag{24}$$

can be given. By insertion of Eq.(17) in Eq.(24) and by introducing Eq.(16) there follows after a somewhat lengthy calculation for the determining equation for u_0

$$\begin{aligned} &u^3_{0,\mathrm{avg}} + 5U_O u^2_{0,\mathrm{avg}} - u_{0,\mathrm{avg}}(5U^2_O + 2U_O u_{N,R} - u_{N,R}u_{N,S} + u^2_{N,T}) \\ &-U^3_O - 2U^2_O u_{N,R} - U_O(u^2_{N,R} - 3u_{N,S}u_{N,T}) + u_{N,R}u_{N,S}u_{N,T} = 0 \end{aligned} \tag{25}$$

The value of $u_{0,\mathrm{avg}}$ is, therefore, uniquely defined by the basic circuit function

and not determined by nonidealities or asymmetries as one might assume due to the only capacitive coupling of the phase inputs and the positive and negative output voltage bus (capacitors $C_{C+,i}$ and $C_{C-,i}$).

Now, if $u_{0,\mathrm{avg}}$ is known, the α_i can be determined in a simple way from Eqs.(16) and (17) which in turn makes it possible to calculate the mains current shape from Eq.(21) and the current in the output inductances via Eq.(20).

It is important to note that $u_{0,\mathrm{avg}}$ is influenced according to Eq.(25) only by the relation between mains voltage and output voltage (and by the signs of the phase currents) and not also, e.g., by the selected controller gain k_P, or by the specific device parameters or by the load condition of the system. Due to this invariance of $u_{0,\mathrm{avg}}$ with respect to a specific dimensioning, Eq.(25) gains special importance. If, e.g., during the dimensioning process device parameters are changed, the once calculated shape of $u_{0,\mathrm{avg}}$ can be maintained. As compared to a direct dependency of the voltage coupling the phases on the values still to be obtained by the dimensioning process, this gives a substantial simplification.

The calculation of $u_{0,\mathrm{avg}}$ for other combinations of the signs of the phase currents can be performed in a completely analogous manner. E.g., there follows for

$$\begin{aligned} i_{N,R} &\geq 0 \\ i_{N,S} &\geq 0 \\ i_{N,T} &< 0 \end{aligned} \tag{26}$$

(where one has to assume $i_{N,S}$ to be sufficient larger than 0)

$$\begin{aligned} &u_{0,\mathrm{avg}}^3 - 5U_O u_{0,\mathrm{avg}}^2 + u_{0,\mathrm{avg}}(-5U_O^2 + 2U_O u_{N,T} + u_{N,R}u_{N,S} - u_{N,T}^2) \\ &+U_O^3 - 2U_O^2 u_{N,T} + U_O(u_{N,T}^2 - 3u_{N,R}u_{N,S}) + u_{N,R}u_{N,S}u_{N,T} = 0 \end{aligned} \tag{27}$$

As the analysis of a further combination of signs of the phase currents shows and as is checked by digital simulation, $u_{0,\mathrm{avg}}$ shows approximately a rectangular shape which is periodic in $\frac{2\pi}{3}$ and which is symmetric to the abscissa. The time dependency within an entire fundamental period is therefore, completely defined by Eqs.(25) and (27).

If now, e.g., for a first dimensioning (for gaining an overview) the description of the system function shall be simplified further, then $u_{0,\mathrm{avg}}$ can be replaced in a first approximation by a symmetric rectangular voltage with amplitude

$$\tilde{u}_{0,\mathrm{avg}} = \frac{U_O}{10}\left[\sqrt{\frac{1}{2}\left(\frac{\bar{M}^4}{8} + \bar{M}^3 + 17\bar{M}^2\right) + 15(2\bar{M}+3)} - \left(\frac{\bar{M}^2}{4} + \bar{M} + 5\right)\right] . \tag{28}$$

There,

$$\bar{M} = \frac{\sqrt{3}\hat{U}_N}{U_O} \tag{29}$$

denotes the voltage transformation ratio of the rectifier system.

For the calculation of Eq.(28) the term of 3rd order in Eq.(25) is neglected. The equation of 2nd order now remaining can be solved simply analytically where for Eq.(28) the values of the mains voltages

$$\begin{aligned} u_{N,R} &= \hat{U}_N \cos(\varphi_N) \\ u_{N,S} &= \hat{U}_N \cos\left(\varphi_N - \frac{2\pi}{3}\right) \\ u_{N,T} &= \hat{U}_N \cos\left(\varphi_N + \frac{2\pi}{3}\right) \end{aligned} \tag{30}$$

are used ($\varphi_N = \omega_N t$, ω_N denotes the mains angular frequency) and φ_N is set to $-\frac{\pi}{6}$.

Eq.(28) gives an approximation of the voltage values $u_{0,\mathrm{avg}}$ as resulting in the phase currents zero crossings for neglection the charging/discharging processes in the bridge legs. The error (as compared to the 'exact' solution according to Eq.(25) and/or Eq.(27) where the charging/discharging processes are also neglected) remains limited to $< 5\%$ for the values of the voltage transfer ratio which are typically in the region of $\bar{M} = 0.8 \ldots 2.5$ for practical applications of the system. This deviation is uncritical especially because (as mentioned before) Eqs.(25) and/or Eq.(27) do not exactly describe the really resulting voltage $u_{0,\mathrm{avg}}$ during the charging/discharging of the capacitors $C_{C+,i}$ and $C_{C-,i}$.

5.2 Control of the Center Point Potential

Because the output voltage center point (which is included in the circuit function) is formed only capacitively, i.e., the center point voltage is not impressed, the question regarding stability and/or controllability of the center point potential is of special interest for the operation of the rectifier system. (An asymmetrical distribution of the output voltage leads, e.g., to an increase of the blocking voltage stress on the valves of one bridge half and to the occurrence of even number harmonics in the rectifier input voltage.)

A special advantage of the rectifier system now consists in the fact, however, that contrary to converters of similar structure of the output circuit [1] no control of the average value of the current i_M fed into M and/or no control of the center point potential u_M is required. This becomes clear by the following considerations.

Due to Eq.(12) we have (in the idealized case) in the local average (and, therefore, also in the global average)

$$i_{M,\mathrm{avg}} = i_{T_R,\mathrm{avg}} + i_{T_S,\mathrm{avg}} + i_{T_T,\mathrm{avg}} = i_{N,R} + i_{N,S} + i_{N,T} \equiv 0 . \tag{31}$$

(For an exact treatment , the mains current values $i_{N,i}$ would have to be replaced here by the local average values $i_{N,i,\mathrm{avg}}$ where the ripple contributions are removed.) Eq.(31) becomes clearly understandable if the coupling capacitor currents are seen with no average value according to a consideration of the system as pure DC-to-DC converter with slowly changing input voltage (cf. Eq.(12)). Then the average current flow being fed into the center point via the switches is determined by the sum of the mains phase currents. Therefore, due to the sum of the phase currents being forced to 0 (cf. Eq.(18)) ideally no center point current $i_{M,\mathrm{avg}}$ results.

Eq.(31) is also fulfilled for a asymmetrical distribution of the output voltage. Thereby, no self-balancing system action is given. An asymmetry of the output voltages remains unchanged (as can be verified by digital simulation). For a practical system realization we have, therefore, to provide a passive balancing (e.g., by resistors lying in parallel to the output capacitors C_+ and C_-) for the reduction of an asymmetry of the partial voltages as could be caused, e.g., by a load change.

6 Experimental Results

An experimental analysis of the rectifier system has been performed at the Dept. of Electrical Engineering of the University of Minnesota, Minneapolis, USA.

A detailed description of the laboratory prototype will be the topic of a future paper. Within the scope of this paper we will only show the time behavior of the mains phase current of the prototype and of the related mains phase voltage. (cf. **Fig.11**). As a detailed analysis shows, the system behavior as determined by digital simulation is checked by the experimental results.

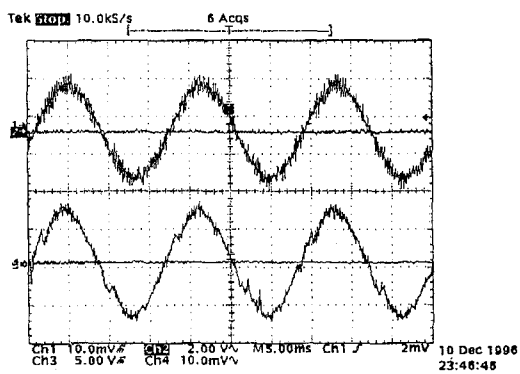

Fig.11: Results of the experimental investigation of a three-phase/switch/level SEPIC-type PWM rectifier; mains phase current $i_{N,R}$ (upper trace) and corresponding mains phase voltage $u_{N,R}$ (lower trace).

7 Conclusions

In this paper the circuit structure of a new three-phase PWM rectifier system (three-phase/switch/level SEPIC-type PWM rectifier) is derived. As compared to a single-phase AC-to-DC SEPIC converter topology only an additional output diode and an additional coupling capacitor per phase leg is required here.

The system is characterized by a sinusiodal shape of the input current and by a highly dynamic controllability of the output voltage. It has (contrary to boost-type PWM rectifier systems) the advantage of a wide output voltage region. The controllability of the power flow which is given independently of the level of the output voltage (inrush und overcurrent limiting capability) is paid for by a relatively high blocking voltage and current stress on the power semiconductors (defined by the sum of the input and output voltages and/or the sum of the input and output currents). For a given output power voltage and current stresses change in opposite directions there regarding the level of the output voltage. For low output voltage a high current stress but low voltage stress on the valves and on the coupling capacitors results and vice versa. A good compromise seems to be given for output voltages in the vicinity of the amlitude of the mains phase voltage; for application of the system in the European low-voltage mains with a rms line-to-line voltage of 400 V, this will be $U_O = 300\,\mathrm{V} \ldots 350\,\mathrm{V}$.

Regarding the realization effort of the control circuit of the rectifier system we want to note that (as shown in section 4) one can apply simple ramp-comparison controllers for the phase current control. Especially no complex control methods (as, e.g., based on space vector calculus) have to be provided. A further control-oriented advantage of the rectifier system is given by the fact that contrary to, e.g., three-level boost-type PWM rectifier systems a control of the potential of the capacitive output voltage center point can be omitted.

The subject of further research now being carried out at the University of Minnesota, USA, and at the Technical University Vienna, Austria, is given by the design of an output voltage control for the system based on a model of reduced order [23]. Further subjects are the analysis of the system behavior during start-up and/or during transient input voltage changes and load changes. Furthermore, the stresses on the power components are being calculated analytically and dimensioning guidelines are worked out. The considerations are verified by using a 2.5 kW laboratory prototype of the system. Furthermore, the research shall be extended to the Cuk-converter structure as shown in Fig.4 of this paper and finally a comparison of the SEPIC- and Cuk-type system to known concepts of PWM rectifier systems [24] with low effects on the mains shall be established.

ACKNOWLEDGEMENT

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